Allwinner R8 Datasheet

Version 1.2

Mar. 07, 2015

REVISION HISTORY

Version	Date	Description
1.0	Dec.17, 2014	Initial release version
1.1	Jan.10, 2015	Correct video engine feature
1.2	Mar.07,2015	Correct Power up/down Specifications

DECLARATION

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TABLE OF CONTENTS

1. OVERVIEW

R8 is designed to provide a low-power capabilities and high performance application processor available in eLQFP176 package, which integrates an ARM Cortex™-A8 that implements the ARM architecture V7-A with supporting numerous popular peripherals.

The processor integrates fully hardware implemented Video Engine, which enables H.264 encoding by 720p@30fps and multi-formats decoding by 1080p@30fps, and Graphic engine, which provides 3-D graphics acceleration, as well as audio codec to reduce the total system cost and to enhance the end-user's experience.

To reduce the BOM costs, the processor is packed with connectivity options including UART, SPI,UART,USB port, CIR,CMOS Sensor Interface and LCD controller etc. Also the R8 interfaces to lower cost memories like nand flash ,DDR2/DRR3 for the optimal performance and supports booting from nand flash or eMMC.

As the brains of Android 4.2,the processor makes multitasking smoother, apps loading more quickly, and anything you touch responds instantly. The processor is an ideal platform to develop a portfolio smart end devices based on hardware design.

Applications:

- Gaming peripherals
- E-book
- Audio playback
- Video boombox
- IoT Module

2. FEATURE

2.1. CPU

- ARM Cortex™-A8 Core
- ARMv7 Instruction set plus Thumb-2 Instruction Set
- 32KB Instruction Cache and 32KB Data Cache
- 256KB L2 Cache
- NEON™ SIMD Coprocessor
- RCT JAVA-Accelerations to optimize just in time(JIT) and dynamitic adaptive compilation(DAC), and reduces memory footprint up to three times

2.2. GPU

- 3D Graphic Engine
- Support Open GL ES 1.1/ 2.0 and open VG 1.1

2.3. Video Engine

Video Decoding
- Support multi-format video decoding, including VP6/8, AVS, H.264, H.263 , MPEG-1/2/4, etc
- Up to 1080p@30fps resolution in all formats

Video Encoding
- Support encoding in H.264 MP format
- Up to 720p@30fps resolution

2.4. Display Subsystem

Display Processing Ability
- Four moveable and size-adjustable layers
- Support multi-format image input
- Support image enhancement processor
- Support Alpha blending /anti-flicker
- Support Hardware cursor
- Support output color correction (luminance / hue / saturation etc)

Display Output Ability
- LCD interface (CPU / Sync RGB)

2.5. Image Subsystem

- Support 8bit CMOS sensor parallel interface
- Support CCIR656 protocol for NTSC and PAL

2.6. Memory Subsystem

SDRAM

- Compatible with JEDEC standard DDR2 /DDR3 SDRAM
- Support clock frequency up to 400MHz
- 16-bits bus width
- Memory capacity up to 512MB

NAND Flash

- Up to 2 chip selects
- 8-bit data bus width
- Up to 64-bit ECC per 1024 bytes
- Support 1024,2048,4096,8192,16K bytes size per page
- Support SLC/MLC/TLC NAND

2.7. System Peripheral

- 8-ch normal DMA and 8-ch dedicated DMA
- Internal 48K SRAM on chip
- 6 asynchronic timers, 2 synchronic timers, 1 watchdog, and 2 AVS counters

2.8. Security System

Crypto Engine

- Support Symmetrical algorithm: AES,DES,TDES
- Support Hash algorithm: MD5,SHA1
- Support 160-bits hardware PRNG with 175-bits seed

Security ID

- Support 128-bits EFUSE for chip ID

2.9. External Peripherals

- One USB 2.0 OTG controller for general application and one USB EHCI/OHCI controller for host application
- Two high-speed memory controllers supporting SD version 3.0 and eMMC version 4.3
- Four UARTs(all with Infrared data Association[IrDA])
- Three SPI controllers(master/slave mode)
- Three Two-Wire Interfaces(TWI)
- IR controller supporting CIR remoter
- 6-bit LRADC for line control
- Internal 4-wire touch panel controller with pressure sensor and 2-point touch
- Internal 24-bit Audio Codec for 2-Ch headphone and 1-Ch microphone
- PWM controller

2.10. Package

- eLQFP176 package

3. BLOCK DIAGRAM

Figure 3-1 shows the block diagram of the R8.

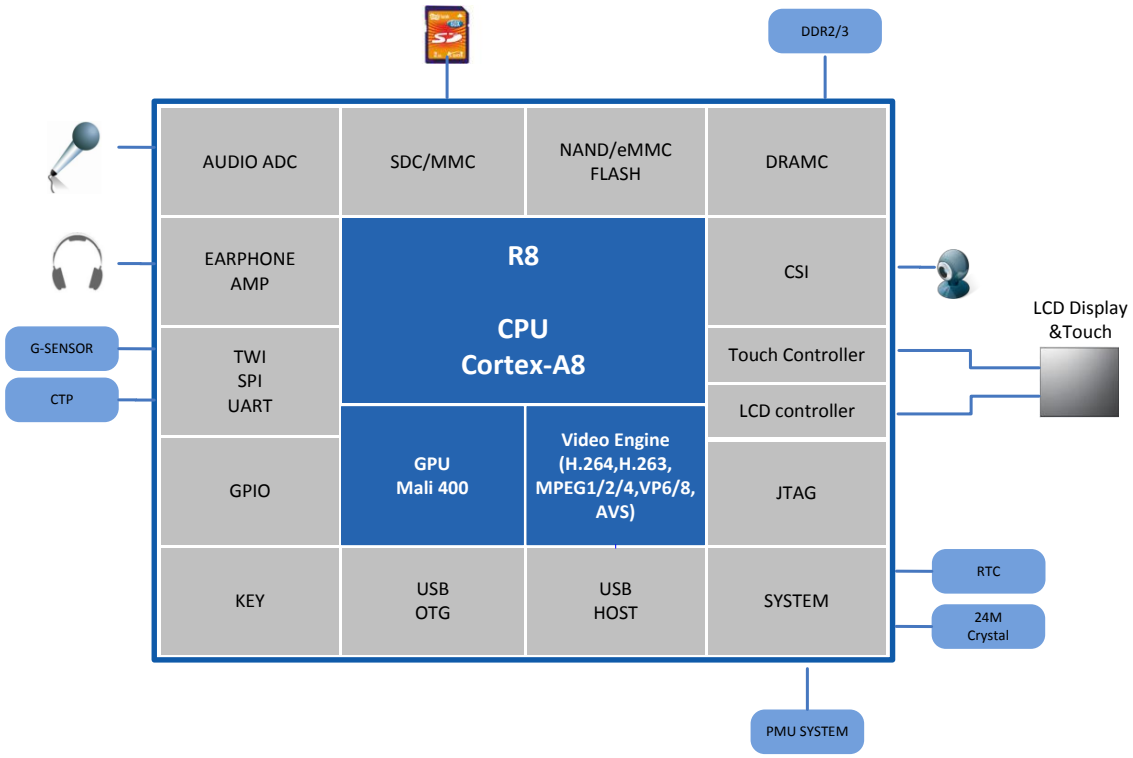


Figure 3-1. R8 Block Diagram

4. PIN DESCRIPTION

4.1. PIN CHARACTERISTICS

Table 4-1 lists the characteristics of R8 Pins from the following aspects: BALL#, Pin Name,Type, Reset State, Default Pull Up/Down, and Buffer Strength.

Table 4-1. Pin Characteristics

No.	Pin Name	Type	Reset State	Pull Up/Down	Buffer Strength
1	NRE	O			
	PC5				
2	NCE0	O		Pull-up	
	PC4				
3	NCE1	O		Pull-up	
	SPI0_CS0				
	PC3				
4	VDD1_CPU	PWR			
5	VCC1	PWR			
6	NCLE	O			
	SPI0_CLK				
	PC2				
7	NALE	O			
	SPI0_MISO				
	PC1				
8	NWE	O			
	SPI0_MOSI				
	PC0				
9	VDD2_CPU	PWR			
10	PB10	I/O			
	EINT24				
11	VDD3_CPU	PWR			
12	PG9	I/O			
	SPI1_CS0				
	UART3_TX				
	EINT9				
13	PG10	I/O			

	SPI1_CLK				
	UART3_RX				
	EINT10				
14	PG11	I/O			
	SPI1_MOSI				
	UART3_CTS				
	EINT11				
15	PG12	I/O			
	SPI1_MISO				
	UART3_RTS				
	EINT12				
16	VDD4_CPU	PWR			
17	DZQ	A			
18	SVREF	P			
19	DDR3_D4	I/O			
20	DDR3_D6	I/O			
21	DDR3_D2	I/O			
22	DDR3_D0	I/O			
23	VCC1_DRAM	PWR			
24	DDR3_D11	I/O			
25	DDR3_D9	I/O			
26	DDR3_D13	I/O			
27	DDR3_D15	I/O			
28	DDR3_DM1	O			
29	DDR3_DM0	O			
30	VCC2_DRAM	PWR			
31	DDR3_DQS0	I/O			
32	DDR3_DQS0_N	I/O			
33	DDR3_DQS1	I/O			
34	DDR3_DQS1_N	I/O			
35	VDD1_INT	PWR			
36	DDR3_D12	I/O			
37	DDR3_D8	I/O			
38	DDR3_D14	I/O			
39	DDR3_D10	I/O			
40	DDR3_D1	I/O			
41	DDR3_D3	I/O			

42	DDR3_D7	I/O			
43	VCC3_DRAM	PWR			
44	DDR3_D5	I/O			
45	DDR3_CK	O			
46	DDR3_CK_N	O			
47	DDR3_CKE	O			
48	DDR3_A10	O			
49	DDR3_BA1	O			
50	DDR3_A12	O			
51	DDR3_A4	O			
52	DDR3_A1	O			
53	VCC4_DRAM	PWR			
54	DDR3_A6	O			
55	DDR3_A8	O			
56	DDR3_A11	O			
57	DDR3_A14	O			
58	DDR3_RAS	O			
59	DDR3_CAS	O			
60	DDR3_WE	O			
61	DDR3_BA2	O			
62	VCC5_DRAM	PWR			
63	DDR3_BA0	O			
64	DDR3_A0	O			
65	DDR3_A3	O			
66	DDR3_A2	O			
67	DDR3_A5	O			
68	DDR3_A13	O			
69	DDR3_A9	O			
70	DDR3_RST	O			
71	DDR3_A7	O			
72	DDR3_ODT	O			
73	VDD2_INT	PWR			
74	HPOUTL	O			
75	HPBP	O			
76	V33_HP	PWR			
77	HPCOM	O			
78	HPOUTR	O			

79	AGND	GND			
80	VRP	A			
81	AVCC	PWR			
82	VRA2	A			
83	VRA1	A			
84	MICIN1	I			
85	VMIC	PWR			
86	LRADC	I			
87	TPX2	I			
88	TPY2	I			
89	TPX1	I			
90	TPY1	I			
91	X24MOUT	AO			
92	X24MIN	AI			
93	UDM0	AIO			
94	UDP0	AIO			
95	UDM1	AIO			
96	UDP1	AIO			
97	V33_USB	PWR			
98	VDD3-INT	PWR			
99	NC				
100	VCC2	PWR			
101	TWI0-SCK	I/O			
	PB0				
102	TWI0-SDA	I/O			
	PB1				
103	PB2/EINT16	I/O			
104	PB4/EINT18	I/O			
105	PB15	I/O			
106	PB16	I/O			
107	SDC0_D1	I/O			
	PF0				
108	SDC0_D0	I/O			
	PF1				
109	VDD4_INT	PWR			
110	SDC0_CLK	O			
	PF2				

111	SDC0_CMD	I/O			
	PF3				
112	SDC0_D3	I/O			
	PF4				
113	SDC0_D2	I/O			
	PF5				
114	CSI_PCLK	I			
	SPI2_CS0				
	EINT14				
	PE0				
115	CSI_MCLK	O			
	SPI2_CLK				
	EINT15				
	PE1				
116	CSI_HSYNC	I			
	SPI2_MOSI				
	PE2				
117	CSI_VSYNC	I			
	SPI2_MISO				
	PE3				
118	CSI_D0	I			
	SDC2_D0				
	PE4				
119	CSI_D1	I			
	SDC2_D1				
	PE5				
120	CSI_D2	I			
	SDC2_D2				
	PE6				
121	CSI_D3	I			
	SDC2_D3				
	PE7				
122	CSI_D4	I			
	SDC2_CMD				
	PE8				
123	CSI_D5	I			
	SDC2_CLK				

	PE9				
124	CSI_D6	I			
	UART1_TX				
	PE10				
125	CSI_D7	I			
	UART1_RX				
	PE11				
126	LCD_VSYNC	I/O			
	PD27				
127	LCD_HSYNC	I/O			
	PD26				
128	LCD_DE	O			
	PD25				
129	LCD_CLK	O			
	PD24				
130	LCD_D23	O			
	PD23				
131	LCD_D22	O			
	PD22				
132	LCD_D21	O			
	PD21				
133	LCD_D20	O			
	PD20				
134	LCD_D19	O			
	PD19				
135	LCD_D18	O			
	PD18				
136	LCD_D15	O			
	PD15				
137	LCD_D14	O			
	PD14				
138	LCD_D13	O			
	PD13				
139	LCD_D12	O			
	PD12				
140	LCD_D11	O			
	PD11				

141	LCD_D10	O			
	PD10				
142	VCC3	PWR			
143	LCD_D7	O			
	PD7				
144	LCD_D6	O			
	PD6				
145	LCD_D5	O			
	PD5				
146	LCD_D4	O			
	PD4				
147	LCD_D3	O			
	PD3				
148	LCD_D2	O			
	PD2				
149	VDD5_INT	PWR			
150	PB3	I/O			
	EINT17				
151	PG4	I/O			
	UART1_RX				
	EINT4				
152	PG3	I/O			
	UART1_TX				
	EINT3				
153	PG2	I/O			
	EINT2				
154	PG1	I/O			
	EINT1				
155	PG0	I/O			
	EINT0				
156	VDD5_CPU	PWR			
157	UBOOT	I		Pull-up	
158	NMI_N	I		No pull	
159	RESET_N	I			
160	PB18	I/O			
161	PB17	I/O			
162	NDQS	I/O			

	PC19				
163	VCC4	PWR			
164	VDD6_CPU	PWR			
165	NDQ7	I/O			
	SDC2_D7				
	PC15				
166	NDQ6	I/O			
	SDC2_D6				
	PC14				
167	NDQ5	I/O			
	SDC2_D5				
	PC13				
168	NDQ4	I/O			
	SDC2_D4				
	PC12				
169	VDD7_CPU	PWR			
170	NDQ3	I/O			
	SDC2_D3				
	PC11				
171	NDQ2	I/O			
	SDC2_D2				
	PC10				
172	NDQ1	I/O			
	SDC2_D1				
	PC9				
173	VDD8_CPU	PWR			
174	NDQ0	I/O			
	SDC2_D0				
	PC8				
175	NRB1	I		Pull-up	
	SDC2_CLK				
	PC7				
176	NRB0	I		Pull-up	
	SDC2_CMD				
	PC6				

Notes:

1) **Pin Number:** Ball numbers on the bottom side associated with each signals on the bottom.
2) **Pin Name**: Names of signals multiplexed on each pin No. (also notice that the name of the pin is the signal name in

function 0);

3) **Type:** signal direction
   I : Input
   O:Output
   I/O: Input/Output
   A:Analog
   AIO: Analog Input/Output
   PWR: Power
   GND: Ground
4) **Pin Reset State:** The state of the terminal at reset (power up)
   0: The buffer drives VOL(pull down/pull up resistor not activated)
   0(PD): The buffer drives VOL with an active pull down resistor.
   1: The buffer drives VOH (pull down/pull up resistor not activated).
   1(PU): The buffer drives V_{OH} with an active pull up resistor.
   Z: High-impedance
   L: High-impedance with an active pull down resistor
   H: High-impedance with an active pull up resistor
5) **Pull Up/Down:** Denotes the presence of an internal pull up or pull down resister
   Pull up and pull down resistor can be enabled or disabled via software
6) **Buffer Strength:** Drive strength of the associated output buffer.
7) Note that the P[B:G] in the following table stands for GPIO [B:G]

4.2. GPIO MULTIPLEXING FUNCTIONS

The following table provides a description of the R8 GPIO multiplexing functions.

Table 4-2. Multiplexing Functions

Port	Multi0	Multi1	Multi2	Multi3	Multi4	Multi5	Multi6
PB0	Input	Output	TWI0_SCK				
PB1	Input	Output	TWI0_SDA				
PB2	Input	Output	PWM				EINT16
PB3	Input	Output	IR_TX				EINT17
PB4	Input	Output	IR_RX				EINT18
PB10	Input	Output	SPI2_CS1				EINT24
PB15	Input	Output	TWI1_SCK				
PB16	Input	Output	TWI1_SDA				
PB17	Input	Output	TWI2_SCK				
PB18	Input	Output	TWI2_SDA				
PC0	Input	Output	NWE	SPI0_MOSI			
PC1	Input	Output	NALE	SPI0_MISO			
PC2	Input	Output	NCLE	SPI0_CLK			
PC3	Input	Output	NCE1	SPI0_CS0			
PC4	Input	Output	NCE0				
PC5	Input	Output	NRE				
PC6	Input	Output	NRB0	SDC2_CMD			

PC7	Input	Output	NRB1	SDC2_CLK			
PC8	Input	Output	NDQ0	SDC2_D0			
PC9	Input	Output	NDQ1	SDC2_D1			
PC10	Input	Output	NDQ2	SDC2_D2			
PC11	Input	Output	NDQ3	SDC2_D3			
PC12	Input	Output	NDQ4	SDC2_D4			
PC13	Input	Output	NDQ5	SDC2_D5			
PC14	Input	Output	NDQ6	SDC2_D6			
PC15	Input	Output	NDQ7	SDC2_D7			
PC19	Input	Output	NDQS				
PD2	Input	Output	LCD_D2	UART2_TX			
PD3	Input	Output	LCD_D3	UART2_RX			
PD4	Input	Output	LCD_D4	UART2_CTS			
PD5	Input	Output	LCD_D5	UART2_RTS			
PD6	Input	Output	LCD_D6	ECRS			
PD7	Input	Output	LCD_D7	ECOL			
PD10	Input	Output	LCD_D10	ERXD0			
PD11	Input	Output	LCD_D11	ERXD1			
PD12	Input	Output	LCD_D12	ERXD2			
PD13	Input	Output	LCD_D13	ERXD3			
PD14	Input	Output	LCD_D14	ERXCK			
PD15	Input	Output	LCD_D15	ERXERR			
PD18	Input	Output	LCD_D18	ERXDV			
PD19	Input	Output	LCD_D19	ETXD0			
PD20	Input	Output	LCD_D20	ETXD1			
PD21	Input	Output	LCD_D21	ETXD2			
PD22	Input	Output	LCD_D22	ETXD3			
PD23	Input	Output	LCD_D23	ETXEN			
PD24	Input	Output	LCD_CLK	ETXCK			
PD25	Input	Output	LCD_DE	ETXERR			
PD26	Input	Output	LCD_HSYNC	EMDC			
PD27	Input	Output	LCD_VSYNC	EMDIO			
PE0	Input		TS_CLK	CSI_PCLK	SPI2_CS0		EINT14
PE1	Input		TS_ERR	CSI_MCLK	SPI2_CLK		EINT15
PE2	Input		TS_SYNC	CSI_HSYNC	SPI2_MOSI		
PE3	Input	Output	TS_DVLD	CSI_VSYNC	SPI2_MISO		

PE4	Input	Output	TS_D0	CSI_D0	SDC2_D0		
PE5	Input	Output	TS_D1	CSI_D1	SDC2_D1		
PE6	Input	Output	TS_D2	CSI_D2	SDC2_D2		
PE7	Input	Output	TS_D3	CSI_D3	SDC2_D3		
PE8	Input	Output	TS_D4	CSI_D4	SDC2_CMD		
PE9	Input	Output	TS_D5	CSI_D5	SDC2_CLK		
PE10	Input	Output	TS_D6	CSI_D6	UART1_TX		
PE11	Input	Output	TS_D7	CSI_D7	UART1_RX		
PF0	Input	Output	SDC0_D1		JTAG_MS1		
PF1	Input	Output	SDC0_D0		JTAG_DI1		
PF2	Input	Output	SDC0_CLK		UART0_TX		
PF3	Input	Output	SDC0_CMD		JTAG_DO1		
PF4	Input	Output	SDC0_D3		UART0_RX		
PF5	Input	Output	SDC0_D2		JTAG_CK1		
PG0	Input		GPS_CLK				EINT0
PG1	Input		GPS_SIGN				EINT1
PG2	Input		GPS_MAG				EINT2
PG3	Input	Output			UART1_TX		EINT3
PG4	Input	Output			UART1_RX		EINT4
PG9	Input	Output	SPI1_CS0	UART3_TX			EINT9
PG10	Input	Output	SPI1_CLK	UART3_RX			EINT10
PG11	Input	Output	SPI1_MOSI	UART3_CTS			EINT11
PG12	Input	Output	SPI1_MISO	UART3_RTS			EINT12

Note:
PE0/PE1/PE2/PG0/PG1/PG2 are for input only.

4.3. POWER AND MISCELLANEOUS SIGNALS

Many signals are available on multiple pins according to the software configuration of the multiplexing options.

1) Signal Name: The signal name
2) Description: Description of the signal
3) Type: Pin type for this specific function:
   I: Input
   O: Output
   Z: High-impedance
   A: Analog
   PWR: Power
   GND: Ground
4) Pin #: Associated ball(s) number

4.3.1. Power Domain Signal Description

Table 4-3. Power Domain Signal Description

Signal Name	Description	Pin Name	Pin No.
Audio DAC Power			
V33_HP	Headphone Power Supply	V33_HP	76
Audio ADC Power			
VMIC	Microphone ADC Power Supply	VMIC	85
USB Power			
V33_USB	USB Power Supply	UVCC	97
IO Power			
VCC	IO Power Supply	VCC(4)	5/100/163/142
CPU Power			
VDD_CPU	CPU Power Supply	VDD2(8)	4/9/11/16/156/164/169/173
System Power			
VDD_INT	System Power Supply	VDD_INT(5)	35/73/98/109/149
DRAM Power			
VCC_DRAM	DRAM Power Supply	VCC(5)	23/30/43/53/62
Analog Power			
AVCC	Analog Power Supply	AVCC	81
AGND	Analog Ground	AGND	79

4.3.2. Miscellaneous Signal Description

Table 4-4. Miscellaneous Signal Description

Signal	Description	Type	Pin Name	Pin No.
Clock				
X24MIN	Main 24MHz crystal Input for internal OSC	AI	X24MIN	92
X24MOUT	Main 24MHz crystal Output for internal OSC	AO	X24MOUT	91
Reset				
RESET_N	System Reset	I	RESET_N	159
FIQ				
NMI_N	External Fast Interrupt Request	I	NMI_N	158
Boot				
UBOOT	Boot Mode	I	BOOT	157

Others				
VRP	Reference voltage	AO	VRP	80
VRA1	Reference voltage	AO	VRA1	83
VRA2	Reference voltage	AO	VRA2	82

5. ELECTRICAL CHARACTERISTICS

5.1. ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage to the device.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter	MIN	Max	Unit
$I_{I/O}$	In/Out current for input and output	-40	40	mA
VCC	Supply Voltage for I/O	-0.3	3.6	V
VDD_INT	Supply Voltage for Internal Digital Logic	-0.3	1.4	V
VDD_CPU	Supply Voltage for CPU	-0.3	1.4	V
AVCC	Supply Voltage for Analog Part	-0.3	3.6	V
VCC_DRAM	Supply Voltage for DRAM Part	-0.3	1.98	V
V33_USB	Supply Voltage for USB PHY	-0.3	3.6	V
V33_HP	Supply Voltage for Headphone	-0.3	3.6	V
T_{STG}	Storage Temperature	-40	125	℃

5.2. RECOMMENDED OPERATING CONDITIONS

All R8 modules are used under the operating Conditions contained in Table 5-2.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	℃
VCC	Supply Voltage for I/O	1.7	1.8~3.3	3.6	V
VDD_INT	Supply Voltage for Internal Digital Logic	1.1	1.2	1.3	V
VDD_CPU	Supply Voltage for CPU	1.1	1.2	1.3	V
AVCC	Supply Voltage for Analog Part	2.7	3.0	3.3	V
VCC_DRAM	Supply Voltage for DDR2	1.7	1.8	1.9	V
	Supply Voltage for DDR3	1.425	1.5	1.575	V
V33_USB	Supply Voltage for USB PHY	3.0	3.3	3.45	V

5.3. DC ELECTRICAL CHARACTERISTICS

Table 5-3 summarizes the DC electrical characteristics of R8.

Table 5-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit

V_{IH}	High-Level Input Voltage	0.7 * VCC	-	VCC + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC	V
R_{PU}	Input pull-up resistance	50	100	150	KΩ
R_{PD}	Input pull-down resistance	50	100	150	KΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC -0.2	-	VCC	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

5.4. OSCILLATOR ELECTRICAL CHARACTERISTICS

R8 contains one 24.000MHz oscillator.

The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks,the clock is provided through X24MIN.Table 5-4 lists the 24.000MHz crystal specifications.

Table 5-4. 24MHz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	–	24.000	–	MHz
t_{ST}	Startup Time	–	–	–	ms
	Frequency Tolerance at 25 °C	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
P_{ON}	Drive level	–	–	300	uW
C_L	Equivalent Load capacitance	12	18	22	pF
R_S	Series Resistance(ESR)	–	25	–	Ω
	Duty Cycle	30	50	70	%
C_M	Motional capacitance	–	–	–	pF
C_{SHUT}	Shunt capacitance	5	6.5	7.5	pF
R_{BIAS}	Internal bias resistor	0.4	0.5	0.6	MΩ

5.5. POWER UP/DOWN AND RESET SPECIFICATIONS

The section provides information about the R8 power up and power down sequence requirements.

5.5.1. Power Up Sequence Requirements

These requirements must be applied to meet the R8 device power-up requirements (system power off to power on).

- Power up all domains simultaneously.

Figure 5-1 shows the power up sequence.

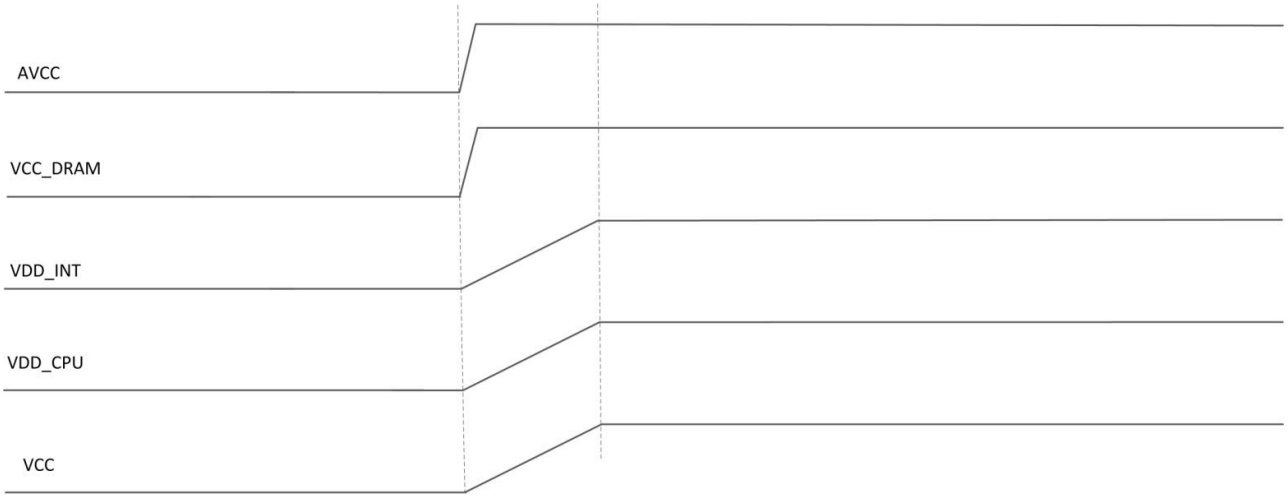


Figure 5-1. Power Up Sequence

5.5.2. Power Up Reset Sequence Requirements

The device has a system reset signal to reset the board. When asserted, the following steps give an example of power up reset sequence supported by the R8 device.

- AVCC ,VDD_CPU and VCC_DRAM can be powered up simultaneously.
- VDD_INT can be powered up after VDD_CPU is powered up, the time difference is T1ms.
- VCC can be powered up after VDD_INT is powered up, the time difference is T2ms.

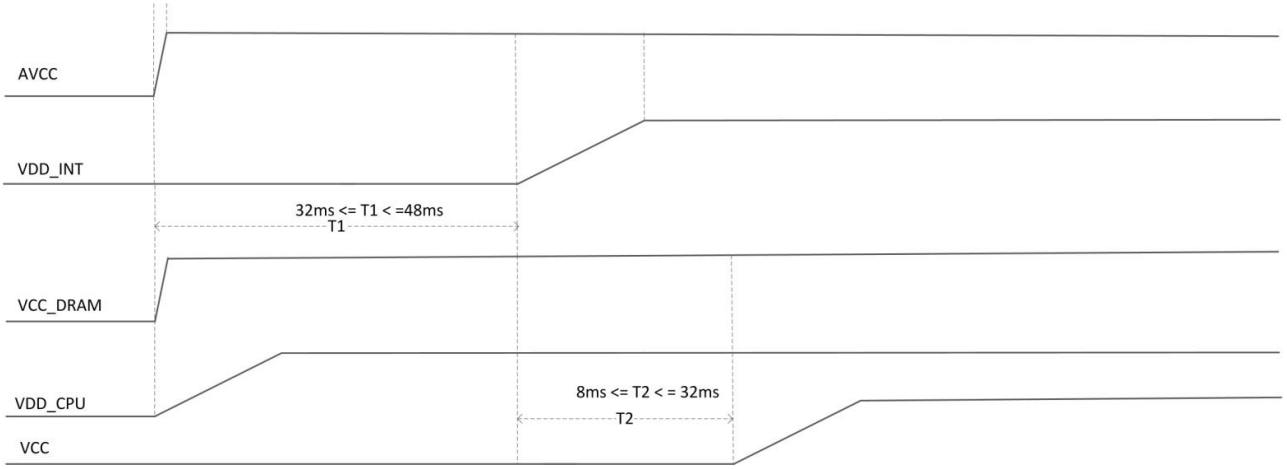


Figure 5-2. Power Up Reset Sequence

5.5.3. Resume Power Up Sequence from Super Standby Mode

To resume a power up sequence when the device is in Super Standby mode:

- VCC_DRAM and AVCC remains powered up always.
- VDD_CPU can be powered up firstly.
- VDD_INT can be powered up after VDD_CPU is powered up, the time difference is T1ms.
- VCC can be powered up after VDD_INT is powered up, the time difference is T2ms.

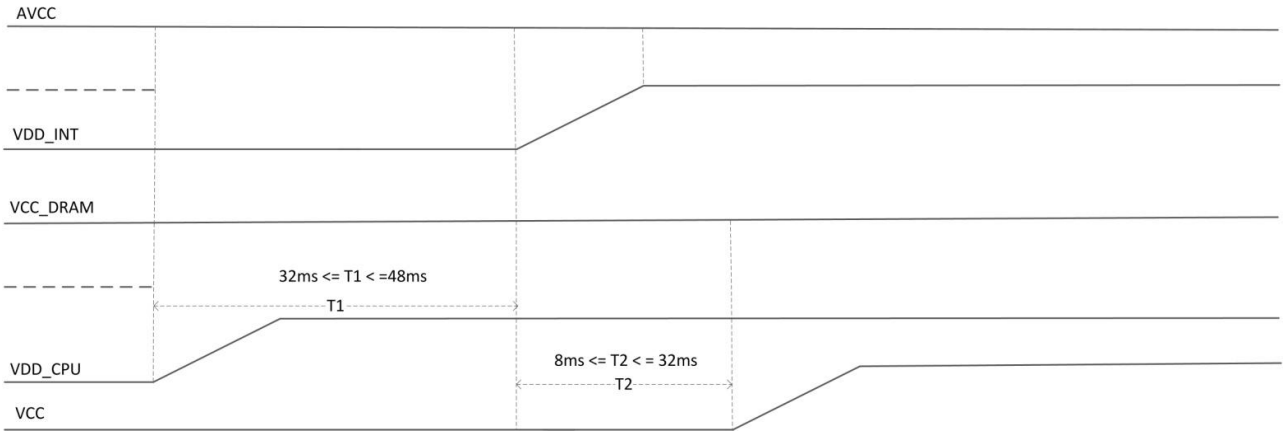


Figure 5-3. Exit Super Standby and Resume Power Up Sequence

5.5.4. Power Down Sequence Requirements

To reduce power consumption,the R8 can be partially powered down.The section lists the power down requirements in each mode.In Super Standby mode,

- VCC_DRAM and AVCC must be kept powered up.
- VDD_CPU,VDD_INT and VCC are powered down simultaneously.
- VCC voltage fall time is more longer than VDD_INT.

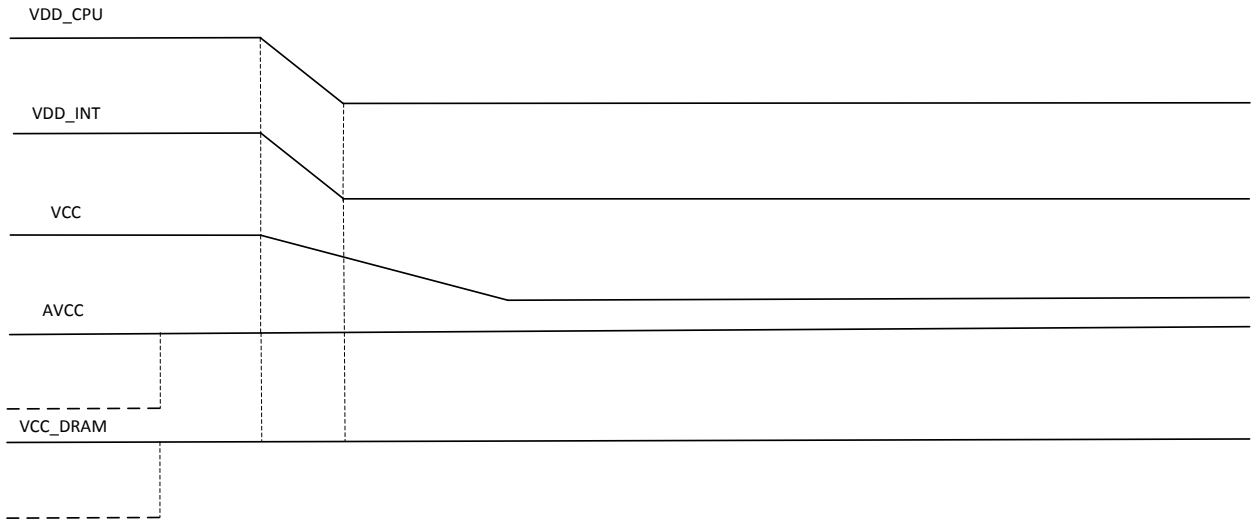


Figure 5-4. Power Down and Enter Super Standby Sequence

Figure 5-5 gives an example of the power-down sequence supported by the R8 device.

- VDD_CPU,VDD_INT and VCC are powered down simultaneously.
- VCC_DRAM and AVCC can be powered down after delay 16ms.
- VCC voltage fall time is more longer than VDD_INT.

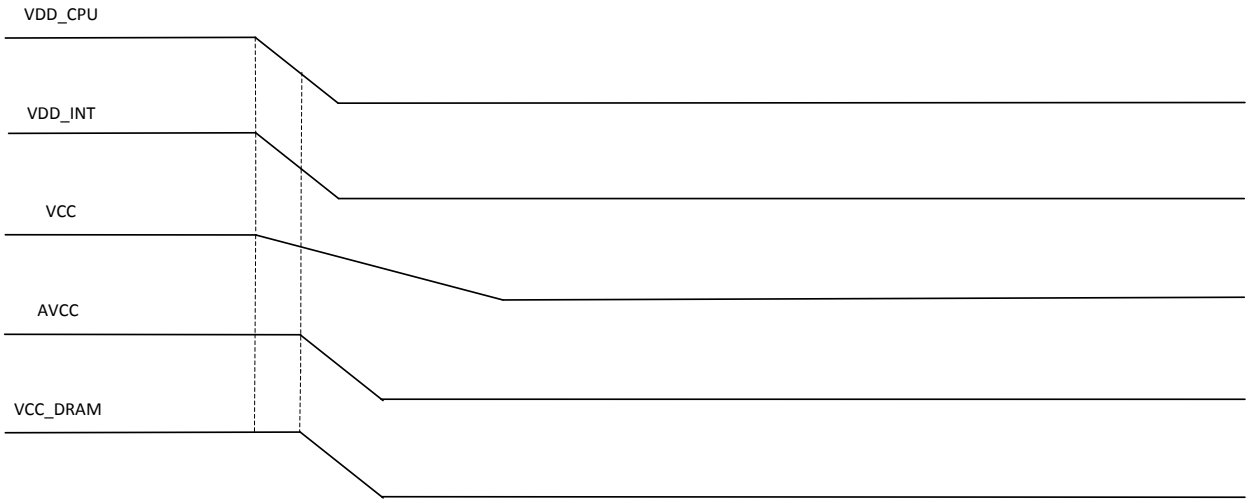
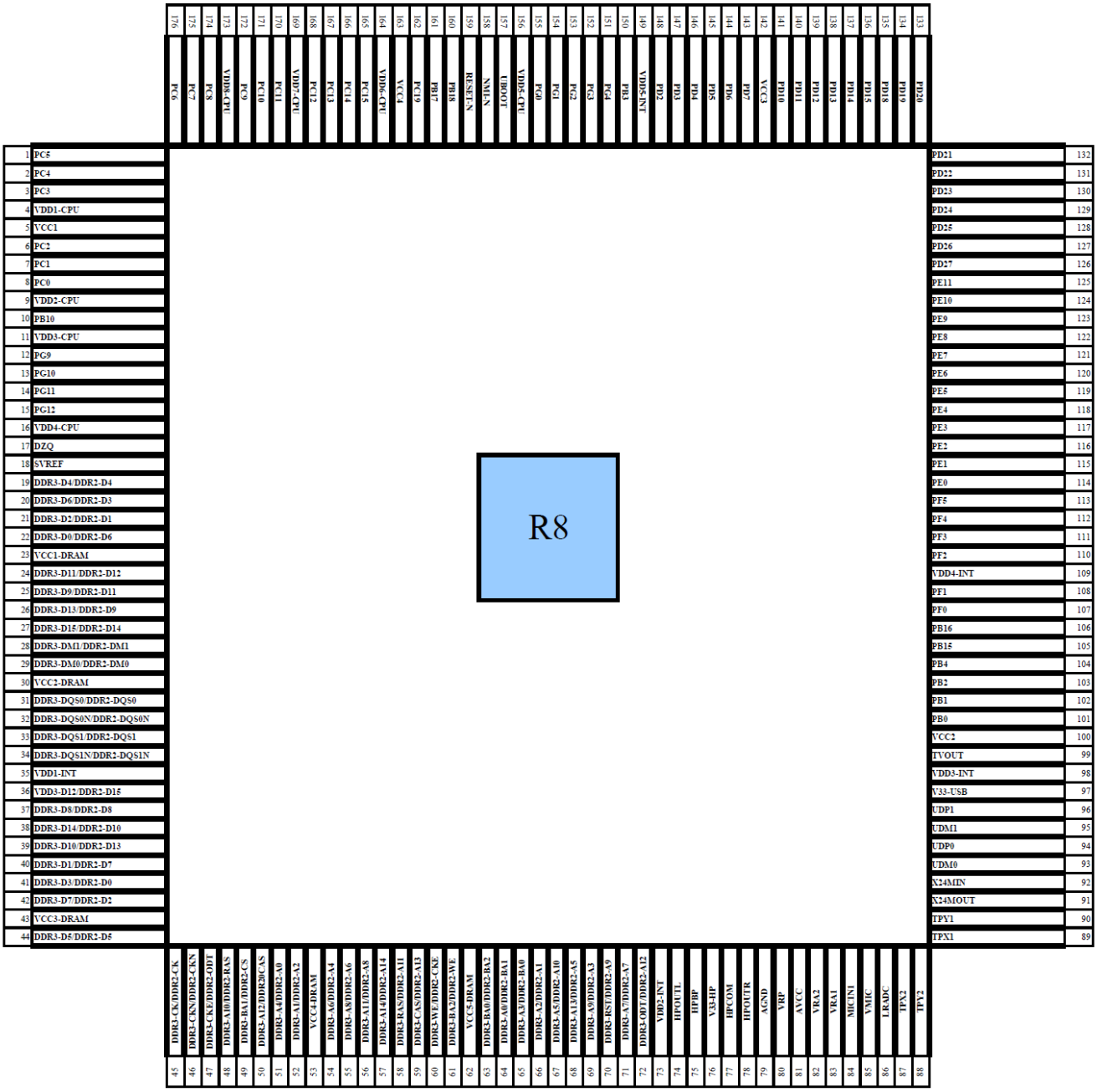


Figure 5-5. Power Down Sequence

6. PIN ASSIGNMENT

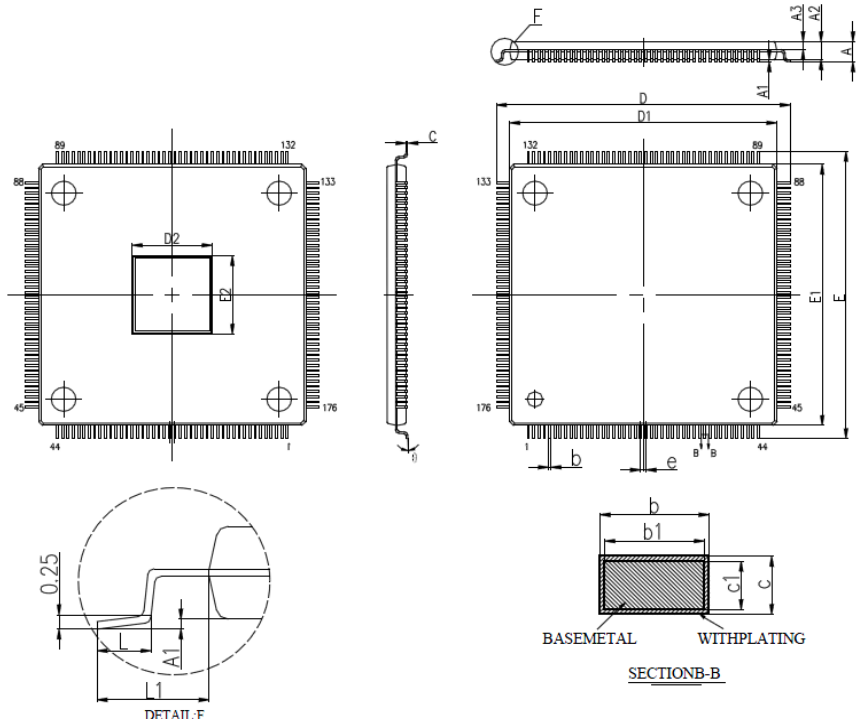
6.1. PIN MAP

The following pin maps show the top views of the 176-pin eLQFP package.



6.2. PACKAGE DIMENSION

The following diagram shows the package dimension of R8.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.14	—	0.23
b1	0.13	0.16	0.18
c	0.13	—	0.18
c1	0.12	0.127	0.14
D	21.80	22.00	22.20
D1	19.80	20.00	20.20
E	21.80	22.00	22.20
E1	19.80	20.00	20.20
e	0.40BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	7°

[illegible]	D2	E2
236*236	6.00REF	6.00REF