Technical Information Manual

PC 300GL (6561 and 6591)

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Note

Before using this information and the product it supports, be sure to read the general information under Appendix E, “Notices and Trademarks” on page 49.

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Preface

This *Technical Information Manual* provides information for the IBM PC 300GL (Models 6561 and 6591). It is intended for developers who want to provide hardware and software products to operate with these IBM computers and provides an in-depth view of how these IBM computers work. Users of this publication should have an understanding of computer architecture and programming concepts.

Related Publications

In addition to this manual, the following IBM publications provide information related to the operation of the PC 300GL (Models 6561 and 6591). To order publications in the U.S. and Puerto Rico, call 1-800-879-2755. In other countries, contact an IBM reseller or an IBM marketing representative.

- *Using Your Personal Computer*
  This publication contains information about configuring, operating, and maintaining the PC 300GL (Models 6561 and 6591). Also, information on diagnosing and solving problems, how to get help and service, and warranty issues is included.
- *Installing Options in Your Personal Computer*
  This publication contains instructions for installing options in the PC 300GL Model 6561 or 6591.
- *Understanding Your Personal Computer*
  This online document includes general information about using computers and detailed information about the features of the PC 300GL (Models 6561 and 6591).
- *PC 300 Systems (6561/6591) Compatibility Report*
  This publication contains information about compatible hardware and software for the PC 300GL (Models 6561 and 6591). This publication is available at http://www.pc.ibm.com/us/cdt.
- *Network Administrator's Guide*
  This publication contains information for network administrators who configure and service local-area networks (LANs). Look for this publication at http://www.pc.ibm.com/us/cdt.

Terminology Usage

Attention! The term *reserved* describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

In this manual, some signals are represented in a small, all-capital-letter format (-ACK). A minus sign in front of the signal indicates that the signal is active low. No sign in front of the signal indicates that the signal is active high.

The use of the term *hex* indicates a hexadecimal number. Also, when numerical modifiers such as “K”, “M” and “G“ are used, they typically indicate powers of 2, not powers of 10. For example, 1 KB equals 1 024 bytes (2^{10}), 1 MB equals 1 048 576 bytes (2^{20}), and 1 GB equals 1 073 741 824 bytes (2^{30}).

When expressing storage capacity, MB equals 1 000 KB (1 024 000). The value is determined by counting the number of sectors and assuming that every two sectors equals 1 KB.

Note: Depending on the operating system and other system requirements, the storage capacity available to the user might vary.

Chapter 1. System Overview

The IBM PC 300GL (Models 6561 and 6591) is a versatile product designed to provide state-of-the-art computing power with room for future growth. Several model variations are available.

Major Features

The major features are:

- Intel® Pentium II® processor with MMX™ Technology
- 512 KB of L2 cache
- Up to 256 MB of system memory
- Integrated AGP Cirrus GD5465 3-D SVGA (super video graphics array) controller
- 2 MB of RDRAM video memory standard
- Industry-standard compatibility
- Network connection
  - Ethernet Wake on LAN adapter (some models only)
  - Token-ring Wake on LAN adapter (some models only)
- ISA/PCI I/O-bus compatibility
- ISA/PCI expansion slots
- Enhanced IDE drives
- Bus master IDE controller, ultra DMA/33 capable
- Two 16550-UART serial ports
- Two USB ports
- One 15-pin monitor port
- One parallel port
- Ports for keyboard and mouse
- Preinstalled 32X Max CD-ROM drive (some models only)
- Preinstalled SoundBlaster-compatible audio adapter (some models only)
- EnergyStar compliant
- Choice of system unit size
  - The PC 300GL Model 6561 has four expansion slots and four drive bays
  - The PC 300GL Model 6591 has six expansion slots and six drive bays

Other Features

The following features are supported by the PC 300GL (Models 6561 and 6591). Optional hardware is required for these features.

Wake on LAN

The power supply of the computer supports the Wake on LAN feature. With the Wake on LAN feature, the computer can be turned on when a specific LAN frame is passed to the PC over the LAN.

To use the Wake on LAN feature, the computer must be equipped with a network subsystem that supports Wake on LAN.

The menu used for setting the Wake on LAN feature is found in the Configuration/Setup Utility Program.

Wake Up on Ring

All models are configurable to turn on the computer after a ring is detected from an external or internal modem. The menu used for setting the Wake Up on Ring feature is found in the Configuration/Setup Utility Program. Two options control this feature:

- **Serial Ring Detect:** Use this option if the computer has an external modem connected to the serial port.
- **Modem Ring Detect:** Use this option if the computer has an internal modem.

Network Enablement

The PC 300GL (Models 6561 and 6591) is enabled to support management over the network. The following is a list of functions that are supported:

- Selectable startup sequence
- Selectable Automatic Power On Startup Sequence
- Update POST/BIOS from network
- Wake on LAN
- CMOS Save/Restore utility program
- CMOS setup over LAN

Chapter 2. System-Board Features

This section includes information about system-board features. For an illustration of the system board, see “System Board, Models 6561 and 6591” on page 12.

Microprocessor

The microprocessor in the PC 300GL (Models 6561 and 6591) is the Intel Pentium II Processor with MMX Technology. The microprocessor features are:

- Optimization for 32-bit software
- Operation at a lower voltage level than previous microprocessors
- 64-bit microprocessor data bus
- 32-bit microprocessor address bus
- Math coprocessor
- MMX technology (boosts the processing of graphic, video, and audio data)
- L2 cache integrated into the microprocessor
  - 4-way set associative
  - Nonblocking
  - 50-percent processor speed
  - Performance increase over placement of L2 cache on the system board

The microprocessor (which has a heat sink attached) plugs directly into a connector on the system board.

For information on replacing a microprocessor or installing an upgrade, refer to *Installing Options in Your Personal Computer*.

Note: More information on the Intel Pentium II microprocessor can be found on the World Wide Web at http://www.intel.com.

Chip Set Control

The Intel 440LX and PIIX4 chip set is the interface between the microprocessor and the following:

- Memory subsystem
- PCI bus
- Busmaster IDE connection
- High-performance, PCI-to-ISA bridge
- USB ports
- SMBus
- AGP bus
- Enhanced DMA controller
- RTC

L2 Cache

The L2 cache is contained within the Pentium II processor. It has 512 KB of cache.

System Memory

The system memory interface is controlled by the 440LX chip set. Synchronous dynamic random access memory (SDRAM) is standard.

The maximum amount of system memory is 256 MB. For memory expansion, the system board provides two dual inline memory module (DIMM) connectors. DIMM sizes of 16MB, 32MB, 64MB, and 128MB with a speed of 60ns are supported. The amount of memory preinstalled varies by model.

The following information applies to system memory:

- SDRAM (synchronous dynamic random access memory), nonparity memory is standard.
- Error correcting code (ECC) nonparity DRAM is also supported.
- The maximum height of memory modules is 3.18 cm (1.25 in.).
- Only industry-standard, gold-lead DIMMs are supported.
- A mix of parity and nonparity types configures as nonparity.

For information on the pin assignments for the memory module connectors, see “System Memory Connector” on page 29.

The following figure shows some possible configurations for the supported DIMMs.

Figure 1 (Page 1 of 2). System Memory Configuration

Total Memory (MB)	MEM 0	MEM 1
16	16	0
32	16	16
32	32	0
48	32	16
64	64	0
64	32	32
80	64	16
96	64	32
128	64	64

Figure 1 (Page 2 of 2). System Memory Configuration		
Total Memory (MB)	**MEM 0**	**MEM 1**
128	128	0
256	128	128

PCI Bus

The fully synchronous 33 MHz PCI bus originates in the chip set. Features of the PCI bus are:

- Integrated arbiter with multi-transaction PCI arbitration acceleration hooks for high performance graphics
- Built-in PCI bus arbiter with support for up to five masters
- Microprocessor-to-PCI memory write posting with 5-Dword-deep buffers
- Converts back-to-back sequential microprocessor-to-PCI memory write to PCI burst write
- PCI-to-DRAM posting 18 Dwords
- PCI-to-DRAM up to 100+ MB/sec bandwidth
- Multitransaction timer to support multiple short PCI transactions within one PCI ARB cycle
- PCI 2.1 compliant
- Delayed transaction
- PCI parity checking and generation support

Bus Master IDE Interface

The system board incorporates a PCI-to-IDE interface that complies with the *AT Attachment Interface with Extensions*. The subsystem that controls direct access storage devices (DASD) is integrated with the IDE interface.

The chip set functions as a *bus master* for the IDE interface. The chip set is PCI 2.1 compliant; it connects directly to the PCI bus and is designed to allow concurrent operations on the PCI bus and IDE bus. The chip set is capable of supporting PIO mode 0–4 devices and IDE DMA mode 0–2 devices, ultra 33 transfers up to 33 Mbytes/sec.

The IDE devices receive their power through a four-position power cable containing +5, +12, and ground voltage. When adding devices to the IDE interface, one device is designated as the master device and another is designated as the slave or subordinate device. These designations are determined by switches or jumpers on each device. There are two IDE ports, one designated 'Primary' and the other 'Secondary', allowing for up to four devices to be attached.

For the IDE interface, no resource assignments are given in the system memory or the direct memory access (DMA) channels. For information on the resource assignments, see “Input/Output Address Map” on page 41 and Figure 48 on page 45 (for IRQ assignments).

Two connectors are provided on the riser for the IDE interface. For information on the connector pin assignments, see “IDE Connectors” on page 31.

PCI-to-ISA Bridge

On the system board, the chip set provides the interface between the peripheral component interface (PCI) and industry standard architecture (ISA) buses. The chip set is used to convert PCI bus cycles to ISA bus cycles; the chip set also includes all the subsystems of the ISA bus, including two cascaded interrupt controllers, two DMA controllers with four 8-bit and three 16-bit channels, three counters equivalent to a programmable interval timer, and power management. The PCI bus operates at 33 MHz

(one-half the microprocessor bus). The ISA bus operates at 8.25 MHz (one-quarter of the PCI bus speed) with a 66 MHz microprocessor bus.

For the ISA bus, no resource assignments are given in the system memory or the DMA channels. For information on resource assignments, see “Input/Output Address Map” on page 41 and Figure 48 on page 45 (for IRQ assignments).

USB Interface

Universal serial bus (USB) technology is a standard feature of the computer. Using the chip set, the system board provides the USB interface with two connectors. A USB-enabled device can attach to each connector, and if that device is a hub, multiple peripherals can attach to the hub and be used by the system. The USB connectors use Plug and Play technology for installed devices. The speed of the USB is up to 12 MB/sec with a maximum of 127 peripherals.

Features provided by USB technology include:

- Support for hot pluggable devices
- Support for concurrent operation of multiple devices
- Suitable for different device bandwidths
- Support for up to five meters length from host to hub or from hub to hub
- Guaranteed bandwidth and low latencies appropriate for specific devices
- Wide range of packet sizes
- Limited power to hubs

For information on the connector pin assignments for the USB interface, see “USB Connectors” on page 32.

Video Subsystem

The video subsystem on the system board includes the Integrated AGP Cirrus GD5465 3-D SVGA (super video graphics array) controller. The system board supports up to two RDRAM memory modules. Each module contains 2 MB of RDRAM memory.

Integrated AGP Cirrus GD5465 3-D SVGA (super video graphics array)

The Integrated AGP Cirrus GD5465 3-D SVGA (super video graphics array) supports all video graphics array (VGA) modes and is compliant with super video graphics array (SVGA) modes, Video Electronics Standards Association (VESA) 1.2. Some enhanced features are:

- Plug and Play support
- 533 MHz RAMBUS DRAM support
- Advanced Power Management support
- Color space conversion
- Hardware scaling

AGP bus and is AGP 1.0 compliant. The CL-GD5465 video subsystem supports the VESA Display Data Channel (DDC) standard 1.1 and uses DDC1 and DDC2B to determine optimal values during automatic monitor detection.

For information on resource assignments, see Appendix B, “System Address Maps” on page 41 and Appendix C, “IRQ and DMA Channel Assignments” on page 45.

The video subsystem provides a 15-pin monitor connector on the system board; For information on connector pin assignments, see “Monitor Connector” on page 32.

Video Memory

The video memory interface is controlled by the GD5465 graphics controller.

The amount of RAMBUS RDRAM shipped with the video subsystem is 2MB.

The video memory module used is a 2MBX9 533MHz RDRAM.

Input/Output Controller

Control of the integrated input/output (I/O) and diskette drive controllers is provided by a single module, the SMC 37C673. This module, which supports Plug and Play, controls the following features:

- Diskette drive support
- Serial port
- Parallel port
- Keyboard and mouse ports
- General purpose I/O ports

Diskette Drive Support

A maximum of two diskette drives and one tape backup drive are supported on the system board. The actual number of diskette drives that can be installed is dependent upon the system unit size (the PC 300GL Model 6561 has four drive bays for installing internal devices and the PC 300GL Model 6591 has six drive bays for installing internal devices). The following is a list of devices that the diskette drive subsystem supports:

- 1.44 MB, 3.5 inch diskette drive
- 2.88 MB, 3.5 inch diskette drive
- 1.2 MB, 5.25 inch diskette drive

One connector is provided on the system board for diskette drive support. For information on the connector pin assignments, see “Diskette Drive Connector” on page 32.

Serial Port

Integrated into the system board are two universal asynchronous receiver/transmitter (UART) serial ports. The serial ports include a 16-byte data, first-in first-out (FIFO) buffer, and have programmable baud rate generators. The serial ports are NS16450 and PC16550A compatible.

For information on the connector pin assignments, see “Serial Port Connectors” on page 33.

Note: Current loop interface is not supported.

The following figure shows the serial port assignments used in configuration.

Figure 2. Serial Port Assignments

Port Assignment	Address Range (hex)	IRQ Level
Serial 1	03F8–03FF	IRQ4
Serial 2	02F8–02FF	IRQ3
Serial 3	03E8–03FF	IRQ4
Serial 4	02E8–02FF	IRQ3

Parallel Port

Integrated in the system board is support for extended capabilities port (ECP), enhanced parallel port (EPP), and standard parallel port (SPP) modes. The modes of operation are selected through the Configuration/Setup Utility program with the default mode set to SPP.

The following figure shows the parallel port assignments used in the configuration.

Figure 3. Parallel Port Assignments

Port Assignment	Address Range (hex)	IRQ Level
Parallel 1	03BC–03BE	IRQ7
Parallel 2	0378–037F	IRQ5
Parallel 3	0278–027F	IRQ5

The system board has one connector for the parallel port. For information on the connector pin assignments, see “Parallel Port Connector” on page 33.

Keyboard and Mouse Ports

The keyboard and mouse subsystem is controlled by a general purpose 8-bit microcontroller; it is compatible with 8042AH. The controller consists of 256 bytes of data memory and 2 KB of read-only memory (ROM).

The controller has two logical devices: one controls the keyboard and the other controls the mouse. The keyboard has two fixed I/O addresses and a fixed IRQ line and can operate without the mouse. The mouse cannot operate without the keyboard because, although it has a fixed IRQ line, the mouse relies on the addresses of the keyboard for operation. For the keyboard and mouse interfaces, no resource assignments are given in the system memory addresses or DMA channels. For information on the resource assignments, see “Input/Output Address Map” on page 41 and Figure 48 on page 45 (for IRQ assignments).

The system board has one connector for the keyboard port and one connector for the mouse port. For information on the connector pin assignments, see “Keyboard and Mouse Port Connectors” on page 35.

Network Connection

Some models are equipped with a Network adapter which supports the Wake on LAN feature.

Features of the Ethernet adapter are:

- Operation in shared 10BASE-T or 100BASE-TX environment
- Transmits and receives data at 10 Mbps or 100 Mbps
- RJ-45 connector for LAN attachment
- Operates in symmetrical multiprocessing (SMP) environments
- Wake on LAN support
- Remote Program Load (RPL) support

Features of the token-ring adapter are:

- Transmits and receives data at 4 Mbps or 16 Mbps
- RJ-45 and D-shell connectors for LAN attachment
- Wake on LAN support
- Remote Program Load (RPL) support

General Purpose I/O Ports

The system board has up to 16 general purpose input/output (GPIO) pins which are implemented through two 8-bit GPIO ports. The use of GPIO pins is dependent upon system design. Features of the GPIO ports are:

- Open-drain outputs with internal pull-ups and transistor-transistor logic (TTL) inputs
- Base address is software configurable
- Direction is programmable
- Occupies 4-byte I/O address

Real-Time Clock and CMOS

The real-time clock is a low-power clock that provides a time-of-day clock and a calendar. The clock settings are maintained by an external battery source of 3 V ac.

The system uses 242 bytes of memory to store complementary metal-oxide semiconductor (CMOS) memory. Moving a jumper on the system board erases CMOS memory.

To locate the battery, see “System Board, Models 6561 and 6591” on page 12.

Flash EEPROM

The system board uses flash electrically-erasable, programmable, read-only memory (EEPROM) to store the basic input/output system (BIOS), video BIOS, IBM logo, Configuration/Setup Utility, and Plug and Play data.

If necessary, the EEPROM can be easily updated using a standalone utility program that is available on a 3.5 inch diskette.

Riser Card

The system board uses a riser card to route PCI and ISA bus signals to the expansion connectors. Each ISA-expansion connector is 16 bits, and each PCI-expansion connector is 32 bits. PCI-expansion connectors support the 32 bit 5, V dc, local-bus signalling environment that is defined in *PCI Local Bus Specification 2.1*. The ISA bus is buffered to provide sufficient drive for the ISA-expansion connectors, assuming two low-power Schottky (LS) loads per slot.

The system board uses one of two riser cards. The two riser cards provide different configurations of PCI and ISA connectors and are representative of the different mechanical sizes. The following figure summarizes the characteristics of the two riser cards.

Figure 4. Riser Card Characteristics

Expansion Slots	4x4 Riser Card	6x6 Riser Card
Shared ISA/PCI	1	0
Dedicated ISA	1	3
Dedicated PCI	2	3

For information on the connector pin assignments, see “ISA Connectors” on page 36 and “PCI Connector” on page 38.

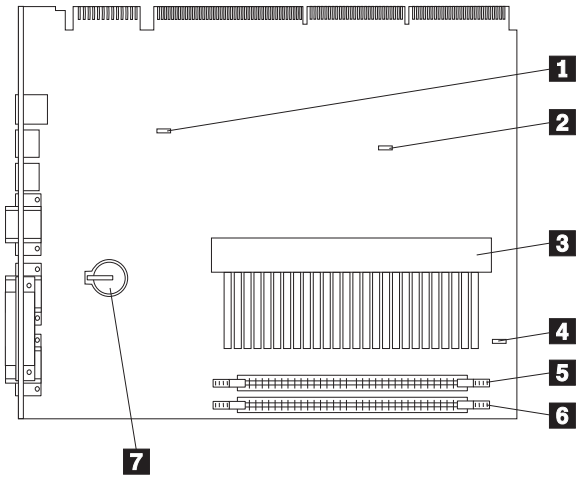
Physical Layout

The system board might look slightly different from the one shown.

Note: A diagram of the system board, including switch and jumper settings, is attached to the underside of the computer cover.

System Board, Models 6561 and 6591

1. Flash recovery jumper
2. CMOS clear (password) jumper
3. Microprocessor
4. Asset Serial EPROM write-protect jumper
5. DIMM Connector 0 (Mem 0)
6. DIMM Connector 1 (Mem 1)
7. Battery



Jumpers

Jumpers on the system board are used for custom configurations. The following figures show the description of pin numbers for specific jumpers. To locate these jumpers, see “System Board, Models 6561 and 6591.”

2

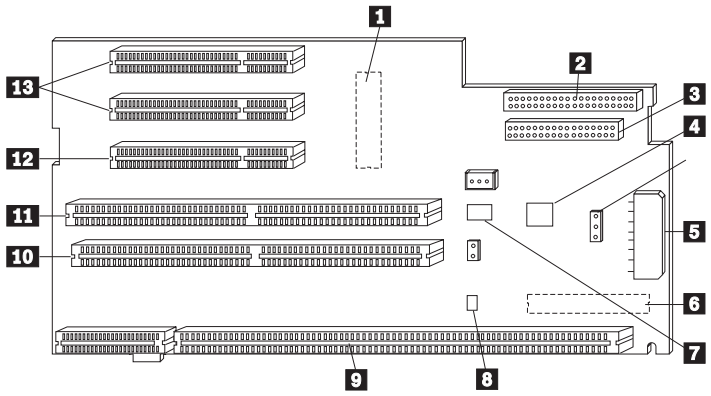
Figure 5. CMOS Clear/Password Jumper	
Pins	**Description**
1 and 2	Normal
2 and 3	Clear CMOS/Password

1

Figure 6. FLASH Recovery Jumper	
Pins	**Description**
1 and 2	Normal
2 and 3	Recovery mode

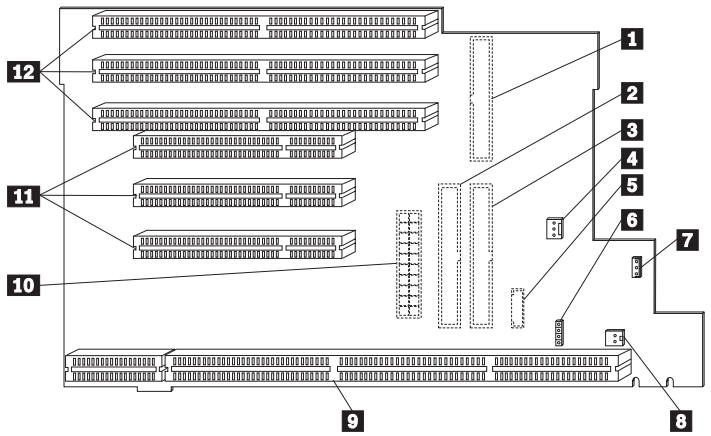
Riser Card, Model 6561

1 Power connector (back side of riser card)
2 Secondary IDE connector
3 Diskette drive connector
4 Fan connector
5 System front panel connector
6 Primary IDE connector (back)
7 Wake on LAN connector
8 Modem wakeup connector
9 340-pin connector
10 ISA connector
11 ISA connector, shared
12 PCI connector, shared
13 PCI connectors



Riser Card, Model 6591

1 Diskette drive connector (back side of riser card)
2 Primary IDE connector (back)
3 Secondary IDE connector (back)
4 Fan connector
5 LED panel (back)
6 SCSI hard disk LED connector
7 Wake on LAN connector
8 Modem wakeup connector (back)
9 340-pin connector
10 Power connector (back)
11 PCI connectors
12 ISA connectors



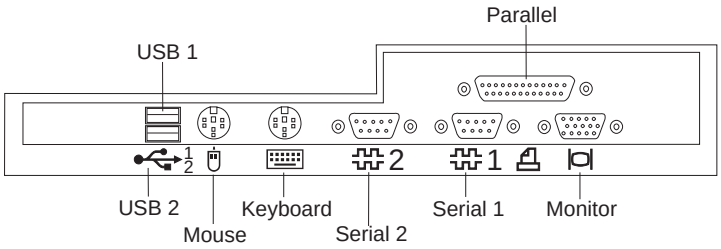
Connectivity

Connections for attaching devices are provided on the back of the computer. The connectors are:

- Network
  - Ethernet integrated with the system board (some models only)
  - Ethernet or token-ring adapter (some models only)
- Keyboard
- Mouse
- Serial (2)
- Parallel
- Monitor
- USB (2)
- Audio (some models only)

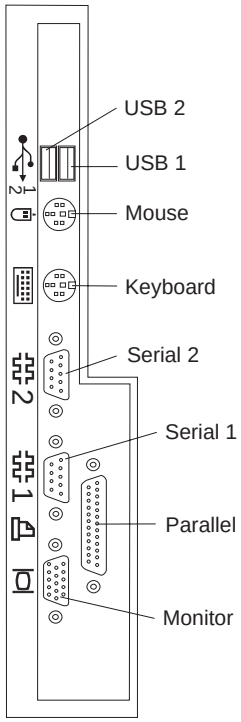
Model 6561 Connector Panel

Connections for features that are integrated into the system board can be identified by a symbol directly above the connector. Connectors provided by an adapter might not have an identifying symbol, as shown in the following illustration.



Model 6591 Connector Panel

Connections for features that are integrated into the system board can be identified by a symbol to the left of the connection. Connectors provided by an adapter might not have an identifying symbol, as shown in the following illustration.



Chapter 3. Physical Specifications

This section lists the physical specifications for the PC 300GL (Models 6561 and 6591). The PC 300GL Model 6561 has four expansion slots and four drive bays, and the PC 300GL Model 6591 has six expansion slots and six drive bays.

Notes:

- The maximum altitude for the PC 300GL (Models 6561 and 6591) is 2133.6 m (7000 ft.). This is the maximum altitude at which the specified air temperatures apply. At higher altitudes, the maximum air temperatures are lower than those specified.
- The PC 300GL (Models 6561 and 6591) computers comply with FCC Class B.

PC 300GL Model 6561

The following figures list the physical attributes for the PC 300GL Model 6561.

Figure 7. Size (PC 300GL Model 6561)

Description	Measurement
Width	450 mm (17.7 in.)
Depth	450 mm (17.7 in.)
Height	128 mm (5.0 in.)

Figure 8. Weight (PC 300GL Model 6561)

Description	Measurement
Minimum configuration	9.9 kg (22 lb)
Maximum configuration (fully populated with typical options)	11.3 kg (25 lb)

Figure 9. Cables (PC 300GL Model 6561)

Description	Measurement
Power cable	1.8 m (72 in)
Keyboard cable	2 m (79 in)

Figure 10. Air Temperature (PC 300GL Model 6561)

Description	Measurement
System on	10.0 to 32.0°C (50 to 90°F)
System off	10.0 to 43.0°C (50 to 110°F)

Figure 11. Humidity (PC 300GL Model 6561)

Description	Measurement
System on	8% to 80%
System off	8% to 80%

Figure 12. Heat Output (PC 300GL Model 6561)

Description	Measurement
Minimum configuration	50 watts (170 Btu per hour)
Maximum configuration (based on 145-watt maximum capacity of the power supply)	204 watts (700 Btu per hour)

Figure 13. Electrical (PC 300GL Model 6561)

Description	Measurement
Low range	90 (min) to 137 (max) V ac
High range	180 (min) to 265 (max) V ac
Frequency	50 ± 3 Hz or 60 ± 3 Hz
Input, minimum configuration	0.11 kVA
Input, maximum configuration	0.52 kVA

PC 300GL Model 6591

The following figures list the physical attributes for the PC 300GL Model 6591.

Figure 14. Size (PC 300GL Model 6591)

Description	Measurement
Width	200 mm (7.9 in)
Depth	445 mm (17.5 in)
Height	492 mm (19.4 in)

Figure 15. Weight (PC 300GL Model 6591)

Description	Measurement
Minimum configuration	15 kg (33 lb)
Maximum configuration (fully populated with typical options)	17.3 kg (38 lb)

Figure 16. Cables (PC 300GL Model 6591)

Description	Measurement
Power cable	1.8 m (72 in)
Keyboard cable	2 m (79 in)

Figure 17. Air Temperature (PC 300GL Model 6591)

Description	Measurement
System on	10.0 to 35.0°C (50 to 95°F)
System off	10.0 to 43.0°C (50 to 110°F)

Figure 18. Humidity (PC 300GL Model 6591)

Description	Measurement
System on	8% to 80%
System off	8% to 80%

Figure 19. Heat Output (PC 300GL Model 6591)

Description	Measurement
Minimum configuration	50 W (170 Btu per hour)
Maximum configuration (based on 200-watt maximum capacity of the power supply)	285 W (969 Btu per hour)

Figure 20. Electrical (PC 300GL Model 6591)

Description	Measurement
Low range	90 (min) to 137 (max) V ac
High range	180 (min) to 265 (max) V ac
Frequency	50 ± 3 Hz or 60 ± 3 Hz
Input, minimum configuration	0.11 kVA
Input, maximum configuration	0.7 kVA

Chapter 4. Power Supply

The power supply requirements are supplied by a 85-watt (PC 300GL Model 6561) or 145-watt (PC 300GL Model 6591) power supply. The power supply converts the ac input voltage into four dc output voltages and provides power for the following:

- System board
- Adapters
- Internal DASD drives
- Keyboard and auxiliary devices

A logic signal on the power connector controls the power supply; the front panel switch is not directly connected to the power supply.

Power Input

The following figure shows the input power specifications. The power supply has a manual switch to select the correct input voltage.

Figure 21. Power Input Requirements

Specification	Measurements
Input voltage, low range	90 (min) to 137 (max) V ac
Input voltage, high range	180 (min) to 265 (max) V ac
Input frequency	50 Hz ± 3 Hz or 60 Hz ± 3 Hz

Power Output

The power supply outputs shown in the following figures include the current supply capability of all the connectors, including system board, DASD, PCI, and auxiliary outputs.

Note: Simultaneous loading of +5 V ac and +3.52 V ac must not exceed 50 watts.

PC 300GL Model 6561

Figure 22. Power Output (145 Watt)

Output Voltage	Regulation	Minimum Current	Maximum Current
+5 volts	+5% to –4%	1.5 A	18.0 A
+12 volts	+5% to –5%	0.2 A	4.2 A
–12 volts	+10% to –9%	0.0 A	0.4 A
–5 volts	+10% to –10%	0.0 A	0.3 A
+3.52 volts	+2% to –2%	0.0 A	10.0 A
+5 volt (auxiliary)	+5% to –10%	0.0 A	.720

PC 300GL Model 6591

Figure 23. Power Output (200 Watt)

Output Voltage	Regulation	Minimum Current	Maximum Current
+5 volts	+5% to –4%	1.5 A	20.0 A *
+12 volts	+5% to –5%	0.2 A	8.0 A
–12 volts	+10% to –9%	0.0 A	0.4 A
–5 volts	+10% to –10%	0.0 A	0.3 A
+3.52 volts	+2% to –2%	0.0 A	20.0 A *
+5 volt (auxiliary)	+5% to –10%	0.005 A	.720 A

* The total combined 3.52 V/5 V power should not exceed 120 watts.

Component Outputs

The power supply provides separate voltage sources for the system board and internal storage devices. The following figures show the approximate power that is provided for specific system components. Many components draw less current than the maximum shown.

Figure 24. System Board

Supply Voltage	Maximum Current	Regulation Limits
+3.52 V dc	3000 mA	+2% to –2.0%
+5.0 V dc	4000 mA	+5.0% to –4.0%
+12.0 V dc	25.0 mA	+5.0% to –5.0%
–12.0 V dc	25.0 mA	+10.0% to –9.0%

Figure 25. Keyboard Port

Supply Voltage	Maximum Current	Regulation Limits
+5.0 V dc	275 mA	+5.0% to –4.0%

Figure 26. Auxiliary Device Port

Supply Voltage	Maximum Current	Regulation Limits
+5.0 V dc	300 mA	+5.0% to –4.0%

Figure 27. ISA-Bus Adapters (Per Slot)

Supply Voltage	Maximum Current	Regulation Limits
+5.0 V dc	4500 mA	+5.0% to –4.0%
–5.0 V dc	200 mA	+5.0% to –5.0%
+12.0 V dc	1500 mA	+5.0% to –5.0%
–12.0 V dc	300 mA	+10.0% to –9.0%

Figure 28. PCI-Bus Adapters (Per Slot)

Supply Voltage	Maximum Current	Regulation Limits
+5.0 V dc	5000 mA	+5.0% to –4.0%
+3.52 V dc	5000 mA	+5.0% to –4.0%

Note: For each PCI connector, the maximum power consumption is rated at 25 watts for +5 V ac and +3.52 V ac combined.

Figure 29. Internal DASD		
Supply Voltage	**Maximum Current**	**Regulation Limits**
+5.0 V dc	1400 mA	+5.0% to –5.0%
+12.0 V dc	1500 mA	+5.0% to –5.0%

Note: Some adapters and hard disk drives draw more current than the recommended limits. These adapters and drives can be installed in the system; however, the power supply will shut down if the total power used exceeds the maximum power that is available.

Output Protection

The power supply protects against output overcurrent, overvoltage, and short circuits. See the power supply specifications on the previous pages for details.

A short circuit that is placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state, with no damage to the power supply. If this shutdown state occurs, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

If an overvoltage fault occurs (in the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of the nominal value of the power supply.

Connector Description

The power supply for the PC 300GL Model 6561 has four 4-pin connectors and the PC 300GL Model 6591 has six 4-pin connectors for internal devices. The total power used by the connectors must not exceed the amount shown in “Component Outputs” on page 20. For information on the pin assignments for the connectors, see Appendix A, “Connector Pin Assignments” on page 28.

Chapter 5. System Software

This section briefly describes some of the system software included with the computer.

BIOS

The computer uses the IBM basic input/output system (BIOS), which is stored in flash electrically erasable programmable read only memory (EEPROM). Some features of the BIOS are:

- PCI support according to PCI BIOS Specification 2.1
- Plug and Play support according to Plug and Play BIOS Specification 1.1
- Advanced Power Management (APM) support according to APM BIOS Interface Specification 1.2
- PCI Bus Master IDE interface with device-specific performance tuning
- IDE Logical Block Addressing (LBA) support
- Cirrus video BIOS for the video graphics controller
- Startable CD-ROM support
- Flash-over-LAN support

Plug and Play

Support for Plug and Play conforms to the following:

- Plug and Play BIOS Specification 1.1 and 1.0
- Plug and Play BIOS Extension Design Guide 1.0
- Plug and Play BIOS Specification, Errata and Clarifications 1.0
- Guide to Integrating the Plug and Play BIOS Extensions with system BIOS 1.2
- Plug and Play Kit for DOS and Windows

POST

IBM power-on self-test (POST) code is used. Also, initialization code is included for the on-board system devices and controllers.

POST error codes include text messages for determining the cause of an error. For more information, see Appendix D, “Error Codes” on page 46.

Configuration/Setup Utility

The Configuration/Setup Utility program provides menus for selecting options for devices, I/O ports, date and time, system security, start options, advanced setup, ISA legacy resources, and power management.

More information on using the Configuration/Setup Utility program is provided in *Using Your Personal Computer*.

Advanced Power Management (APM)

The PC 300GL (Models 6561 and 6591) come with built-in energy-saving capabilities. Advanced Power Management (APM) is a feature that reduces the power consumption of systems when they are not being used. When enabled, APM initiates reduced-power modes for the monitor, microprocessor, and hard disk drive after a specified period of inactivity.

The BIOS supports APM 1.1. This enables the system to enter a power-managed state, which reduces the power drawn from the ac wall outlet. Advanced Power Management is enabled through the Configuration/Setup Utility Program and is controlled by the individual operating system.

For more information on APM, see *Using Your Personal Computer* and *Understanding Your Personal Computer*.

Flash Update Utility Program

The flash update utility program is a standalone program to support flash updates. This utility program updates the BIOS code in flash and the Machine Readable Information (MRI) to different languages.

The flash update utility program is available on a 3.5 inch diskette.

Diagnostic Program

The diagnostic program that comes with this system is provided as a startable *IBM Enhanced Diagnostic* diskette image on your hard disk and on the *Ready-to-Configure Utility Program* CD. It runs independently of the operating system. The user interface for running the diagnostics and utilities is provided by Watergate Software's PC-Doctor. It is also available online and may be downloaded from the following World Wide Web page:

`http://www.pc.ibm.com/support/desktop/desktop_support.html`

For more information on this diagnostic program, see *Using Your Personal Computer*.

Chapter 6. System Compatibility

This chapter discusses some of the hardware, software, and BIOS compatibility issues for the computer. Refer to *PC 300 Systems (6561/6591) Compatibility Report* for a list of compatible hardware and software options.

Hardware Compatibility

This section discusses hardware, software, and BIOS compatibility issues that must be considered when designing application programs.

Many of the interfaces are the same as those used by the IBM Personal Computer AT. In most cases, the command and status organization of these interfaces is maintained.

The functional interfaces are compatible with the following interfaces:

- Intel 8259 interrupt controllers (edge-triggered mode)
- National Semiconductor NS16450 and NS16550A serial communication controllers
- Motorola MC146818 Time of Day Clock command and status (CMOS reorganized)
- Intel 8254 timer, driven from a 1.193 MHz clock (channels 0, 1, and 2)
- Intel 8237 DMA controller, except for the Command and Request registers and the Rotate and Mask functions; the Mode register is partially supported
- Intel 8272 or 82077 diskette drive controllers
- Intel 8042 keyboard controller at addresses hex 0060 and hex 0064
- All video standards using VGA, EGA, CGA, MDA, and Hercules modes
- Parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode

Use the above information to develop application programs. Whenever possible, use the BIOS as an interface to hardware to provide maximum compatibility and portability of applications among systems.

Hardware Interrupts

Hardware interrupts are level sensitive for PCI interrupts and edge sensitive for ISA interrupts. The interrupt controller clears its in-service register bit when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI command is sent regardless of whether the incoming interrupt request to the controller is active or inactive.

The interrupt-in-progress latch is readable at an I/O-address bit position. This latch is read during the interrupt service routine and might be reset by the read operation or it might require an explicit reset.

Note: For performance and latency considerations, designers might want to limit the number of devices sharing an interrupt level.

With level-sensitive interrupts, the interrupt controller requires that the interrupt request be inactive at the time the EOI command is sent; otherwise, a new interrupt request will be detected. To avoid this, a level-sensitive interrupt handler must clear the interrupt condition (usually by a read or write operation to an I/O port on the device causing the interrupt). After processing the interrupt, the interrupt handler:

1. Clears the interrupt
2. Waits one I/O delay
3. Sends the EOI
4. Waits one I/O delay
5. Enables the interrupt through the Set Interrupt Enable Flag command

Hardware interrupt IRQ9 is defined as the replacement interrupt level for the cascade level IRQ2. Program interrupt sharing is implemented on IRQ2, interrupt hex 0A. The following processing occurs to maintain compatibility with the IRQ2 used by IBM Personal Computer products:

1. A device drives the interrupt request active on IRQ2 of the channel.
2. This interrupt request is mapped in hardware to IRQ9 input on the second interrupt controller.
3. When the interrupt occurs, the system microprocessor passes control to the IRQ9 (interrupt hex 71) interrupt handler.
4. This interrupt handler performs an EOI command to the second interrupt controller and passes control to the IRQ2 (interrupt hex 0A) interrupt handler.
5. This IRQ2 interrupt handler, when handling the interrupt, causes the device to reset the interrupt request before performing an EOI command to the master interrupt controller that finishes servicing the IRQ2 request.

Diskette Drives and Controller

The following figures show the reading, writing, and formatting capabilities of each type of diskette drive.

Figure 30. 5.25-Inch Diskette Drive Reading, Writing, and Formatting Capabilities

Diskette Drive Type	250/500 KB Mode	300/500 KB Mode	1 MB Mode
Single sided (48 Tracks Per Inch (TPI))	RWF	—	—
Double sided (48 TPI)	RWF	RWF	—
High capacity (1.2 MB)	RWF	RWF	RWF

Figure 31. 3.5-Inch Diskette Drive Reading, Writing, and Formatting Capabilities

Diskette Drive Type	720 KB Mode	1.44 MB Mode	2.88 MB Mode
1.44 MB drive	RWF	RWF	—
2.88 MB drive	RWF	RWF	RWF

Notes:

1. Do not use either a 250/500 KB or 300/500 KB diskette drive for 5.25-inch diskettes that are designed for the 1.2MB mode.
2. Low-density 5.25-inch diskettes that are written to or formatted by a high-capacity 1.2 MB diskette drive can be reliably read only by another 1.2 MB diskette drive.
3. Do not use in a 1.44MB diskette drive any 3.5-inch diskettes that are designed for the 2.88 MB mode.

Copy Protection

The following methods of copy protection might not work in systems using the 3.5-inch 1.44 MB diskette drive.

- Bypassing BIOS routines
  - Data transfer rate: BIOS selects the proper data transfer rate for the media being used.
  - Diskette parameter table: Copy protection, which creates its own diskette parameter table, might not work in these drives.
- Diskette drive controls
  - Rotational speed: The time between two events in a diskette drive is a function of the controller.
  - Access time: Diskette BIOS routines must set the track-to-track access time for the different types of media that are used in the drives.
  - 'Diskette change' signal: Copy protection might not be able to reset this signal.
- Write-current control: Copy protection that uses write-current control does not work, because the controller selects the proper write current for the media that is being used.

Hard Disk Drives and Controller

Reading from and writing to the hard disk is initiated in the same way as in IBM Personal Computer products; however, new functions are supported.

Software Compatibility

To maintain software compatibility, the interrupt polling mechanism that is used by IBM Personal Computer products is retained. Software that interfaces with the reset port for the IBM Personal Computer positive-edge interrupt sharing (hex address 02F*x* or 06F*x*, where *x* is the interrupt level) does not create interference.

Software Interrupts

With the advent of software interrupt sharing, software interrupt routines must daisy chain interrupts. Each routine must check the function value, and if it is not in the range of function calls for that routine, it must transfer control to the next routine in the chain. Because software interrupts are initially pointed to address 0:0 before daisy chaining, check for this case. If the next routine is pointed to address 0:0 and the function call is out of range, the appropriate action is to set the carry flag and do a RET 2 to indicate an error condition.

Machine-Sensitive Programs

Programs can select machine-specific features, but they must first identify the machine and model type. IBM has defined methods for uniquely determining the specific machine type. The machine model byte can be found through Interrupt 15H, Return System Configuration Parameters function (AH)=C0H).

Appendix A. Connector Pin Assignments

The following figures show the pin assignments for various system board connectors.

System Memory Connector

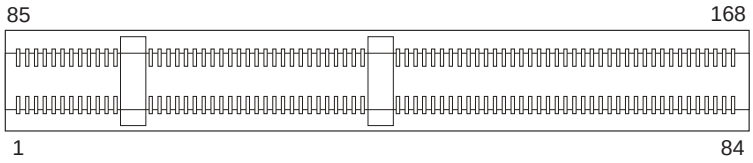


Figure 32 (Page 1 of 3). System Memory Connector Pin Assignments

Pin	x64 Non-Parity	x72 ECC	Pin	x64 Non-Parity	x72 ECC
1	VSS	VSS	85	VSS	VSS
2	DQ0	DQ0	86	DQ32	DQ32
3	DQ1	DQ1	87	DQ33	DQ33
4	DQ2	DQ2	88	DQ34	DQ34
5	DQ3	DQ3	89	DQ35	DQ35
6	VCC	VCC	90	VCC	VCC
7	DQ4	DQ4	91	DQ36	DQ36
8	DQ5	DQ5	92	DQ37	DQ37
9	DQ6	DQ6	93	DQ38	DQ38
10	DQ7	DQ7	94	DQ39	DQ39
11	DQ8	DQ8	95	DQ40	DQ40
12	VSS	VSS	96	VSS	VSS
13	DQ9	DQ9	97	DQ41	DQ41
14	DQ10	DQ10	98	DQ42	DQ42
15	DQ11	DQ11	99	DQ43	DQ43
16	DQ12	DQ12	100	DQ44	DQ44
17	DQ13	DQ13	101	DQ45	DQ45
18	VCC	VCC	102	VCC	VCC
19	DQ14	DQ14	103	DQ46	DQ46
20	DQ15	DQ15	104	DQ47	DQ47
21	NC	CB0	105	NC	CB4
22	NC	CB1	106	NC	CB5
23	VSS	VSS	107	VSS	VSS
24	NC	NC	108	NC	NC
25	NC	NC	109	NC	NC
26	VCC	VCC	110	VCC	VCC
27	/WE	/WE	111	/CAS	/CAS
28	DQMB0	DQMB0	112	DQMB4	DQMB4
29	DQMB1	DQMB1	113	DQMB5	DQMB5
30	/S0	/S0	114	NC	S1
31	DU	DU	115	/RAS	/RAS
32	VSS	VSS	116	VSS	VSS
33	A0	A0	117	A1	A1
34	A2	A2	118	A3	A3
35	A4	A4	119	A5	A5
36	A6	A6	120	A7	A7

Figure 32 (Page 2 of 3). System Memory Connector Pin Assignments

Pin	x64 Non-Parity	x72 ECC	Pin	x64 Non-Parity	x72 ECC
37	A8	A8	121	A9	A9
38	A10/AP	A10/AP	122	BA0	BA0
39	NC	BA1	123	NC	A11
40	VCC	VCC	124	VCC	VCC
41	VCC	VCC	125	CK1	CK1
42	CK0	CK0	126	A12	A12
43	VSS	VSS	127	VSS	VSS
44	DU	DU	128	CKE0	CKE0
45	/S2	/S2	129	NC	/S3
46	DQMB2	DQMB2	130	DQMB6	DQMB6
47	DQMB3	DQMB3	131	DQMB7	DQMB7
48	DU	DU	132	A13	A13
49	VCC	VCC	133	VCC	VCC
50	NC	NC	134	NC	NC
51	NC	NC	135	NC	NC
52	NC	CB2	136	NC	CB6
53	NC	CB3	137	NC	CB7
54	VSS	VSS	138	VSS	VSS
55	DQ16	DQ16	139	DQ48	DQ48
56	DQ17	DQ17	140	DQ49	DQ49
57	DQ18	DQ18	141	DQ50	DQ50
58	DQ19	DQ19	142	DQ51	DQ51
59	VCC	VCC	143	VCC	VCC
60	DQ20	DQ20	144	DQ52	DQ52
61	NC	NC	145	NC	NC
62	NC	Vref,NC	146	NC	Vref,NC
63	NC	CKE1	147	NC	NC
64	VSS	VSS	148	VSS	VSS
65	DQ21	DQ21	149	DQ53	DQ53
66	DQ22	DQ22	150	DQ54	DQ54
67	DQ23	DQ23	151	DQ55	DQ55
68	VSS	VSS	152	VSS	VSS
69	DQ24	DQ24	153	DQ56	DQ56
70	DQ25	DQ25	154	DQ57	DQ57
71	DQ26	DQ26	155	DQ58	DQ58
72	DQ27	DQ27	156	DQ59	DQ59
73	VCC	VCC	157	VCC	VCC
74	DQ28	DQ28	158	DQ60	DQ60
75	DQ29	DQ29	159	DQ61	DQ61
76	DQ30	DQ30	160	DQ62	DQ62
77	DQ31	DQ31	161	DQ63	DQ63
78	VSS	VSS	162	VSS	VSS
79	CK2	CK2	163	CK3	CK3

Figure 32 (Page 3 of 3). System Memory Connector Pin Assignments

Pin	x64 Non-Parity	x72 ECC	Pin	x64 Non-Parity	x72 ECC
80	NC	NC	164	NC	NC
81	NC	NC	165	SA0	SA0
82	SDA	SDA	166	SA1	SA1
83	SCL	SCL	167	SA2	SA2
84	VCC	VCC	168	VCC	VCC

IDE Connectors

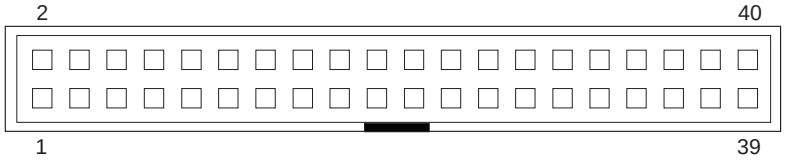


Figure 33. IDE Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	NC	O	21	NC	NA
2	Ground	NA	22	Ground	NA
3	Data bus bit 7	I/O	23	I/O write	O
4	Data bus bit 8	I/O	24	Ground	NA
5	Data bus bit 6	I/O	25	I/O read	O
6	Data bus bit 9	I/O	26	Ground	NA
7	Data bus bit 5	I/O	27	I/O channel ready	I
8	Data bus bit 10	I/O	28	ALE	O
9	Data bus bit 4	I/O	29	NC	NA
10	Data bus bit 11	I/O	30	Ground	NA
11	Data bus bit 3	I/O	31	IRQ	I
12	Data bus bit 12	I/O	32	CS16#	I
13	Data bus bit 2	I/O	33	SA1	O
14	Data bus bit 13	I/O	34	PDIAG#	I
15	Data bus bit 1	I/O	35	SA0	O
16	Data bus bit 14	I/O	36	SA2	O
17	Data bus bit 0	I/O	37	CS0#	O
18	Data bus bit 15	I/O	38	CS1	O
19	Ground	NA	39	Active#	I
20	Key (Reserved)	NA	40	Ground	NA

USB Connectors

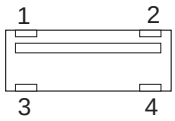


Figure 34. USB Connector Pin Assignments

Pin	Signal
1	VCC
2	-Data
3	+Data
4	Ground

Monitor Connector

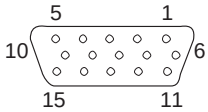


Figure 35. Monitor Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Red	O	2	Green	O
3	Blue	O	4	Monitor ID 2 - Not used	I
5	Ground	NA	6	Red ground	NA
7	Green ground	NA	8	Blue ground	NA
9	+5 V, used by DDC2B	NA	10	Ground	NA
11	Monitor ID 0 - Not used	I	12	DDC2B serial data	I/O
13	Horizontal sync	O	14	Vertical sync	O
15	DDC2B clock	I/O			

Diskette Drive Connector

Figure 36 (Page 1 of 2). Diskette Drive Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Drive 2 installed #	I	2	High density select	O
3	Not connected	NA	4	Not connected	NA
5	Ground	NA	6	Data rate 0	NA
7	Ground	NA	8	Index#	I
9	Reserved	NA	10	Motor enable 0#	O
11	Ground	NA	12	Drive select 1#	O
13	Ground	NA	14	Drive select 0#	O
15	Ground	NA	16	Motor enable 1#	O

Figure 36 (Page 2 of 2). Diskette Drive Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
17	MSEN1	I	18	Direction in#	O
19	Ground	NA	20	Step#	O
21	Ground	NA	22	Write data#	O
23	Ground	NA	24	Write enable#	O
25	Ground	NA	26	Track0#	I
27	MSEN0	I	28	Write protect#	I
29	Ground	NA	30	Read data#	I
31	Ground	NA	32	Head 1 select#	O
33	Data rate 1	NA	34	Diskette change#	I

Serial Port Connectors

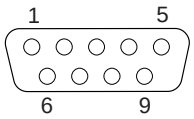


Figure 37. Serial Port Connectors Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Data carrier detect	I	2	Receive data#	I
3	Transmit data#	O	4	Data terminal read	O
5	Ground	NA	6	Data set ready	I
7	Request to send	O	8	Clear to send	I
9	Ring indicator	I			

Parallel Port Connector

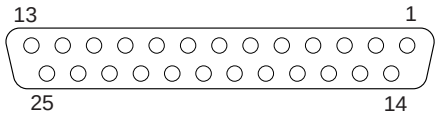


Figure 38 (Page 1 of 2). Parallel Port Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	STROBE#	I/O	2	Data bit 0	I/O
3	Data bit 1	I/O	4	Data bit 2	I/O
5	Data bit 3	I/O	6	Data bit 4	I/O
7	Data bit 5	I/O	8	Data bit 6	I/O
9	Data bit 7	I/O	10	ACK#	I
11	BUSY	I	12	PE	I
13	SLCT	I	14	AUTO FD XT#	O
15	ERROR#	I	16	INIT#	O
17	SLCT IN#	O	18	Ground	NA

Figure 38 (Page 2 of 2). Parallel Port Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
19	Ground	NA	20	Ground	NA
21	Ground	NA	22	Ground	NA
23	Ground	NA	24	Ground	NA
25	Ground	NA			

Keyboard and Mouse Port Connectors

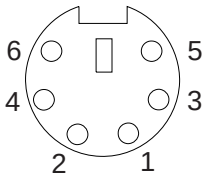
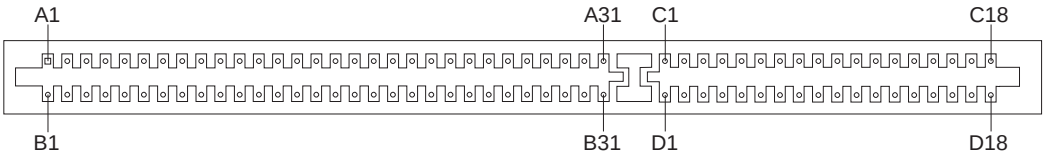


Figure 39. Keyboard and Mouse Connectors Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	Data	I/O	2	Reserved	NA
3	Ground	NA	4	+5 V dc	NA
5	Clock	I/O	6	Reserved	I/O

ISA Connectors



Note: The ISA connectors are part of the riser card.

Figure 40 (Page 1 of 2). ISA Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
B1	Ground	NA	A1	IOCHCK#	I
B2	RESET DRV	O	A2	SD7	I/O
B3	+5 V dc	NA	A3	SD6	I/O
B4	IRQ2	I	A4	SD5	I/O
B5	-5 V dc	NA	A5	SD4	I/O
B6	DRQ2	I	A6	SD3	I/O
B7	-12 V dc	NA	A7	SD2	I/O
B8	OWS#	I	A8	SD1	I/O
B9	+12 V dc	NA	A9	SD0	I/O
B10	Ground	NA	A10	IOCHRDY	I
B11	SMEMW#	O	A11	AEN	O
B12	SMEMR#	O	A12	SA19	I/O
B13	IOW#	I/O	A13	SA18	I/O
B14	IOR#	I/O	A14	SA17	I/O
B15	DACK3#	O	A15	SA16	I/O
B16	DRQ3	I	A16	SA15	I/O
B17	DACK1#	O	A17	SA14	I/O
B18	DRQ1	I	A18	SA13	I/O
B19	REFRESH#	I/O	A19	SA12	I/O
B20	CLK	O	A20	SA11	I/O
B21	IRQ7	I	A21	SA10	I/O
B22	IRQ6	I	A22	SA9	I/O
B23	IRQ5	I	A23	SA8	I/O
B24	IRQ4	I	A24	SA7	I/O
B25	IRQ3	I	A25	SA6	I/O
B26	DACK2#	O	A26	SA5	I/O
B27	TC	O	A27	SA4	I/O
B28	BALE	O	A28	SA3	I/O
B29	+5 V dc	NA	A29	SA2	I/O
B30	OSC	O	A30	SA1	I/O
B31	Ground	NA	A31	SA0	I/O
D1	MEMCS16#	I	C1	SBHE#	I/O
D2	IOCS16#	I	C2	LA23	I/O
D3	IRQ10	I	C3	LA22	I/O

Figure 40 (Page 2 of 2). ISA Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
D4	IRQ11	I	C4	LA21	I/O
D5	IRQ12	I	C5	LA20	I/O
D6	IRQ15	I	C6	LA19	I/O
D7	IRQ14	I	C7	LA18	I/O
D8	DACK0#	O	C8	LA17	I/O
D9	DRQ0	I	C9	MEMR#	I/O
D10	DACK5#	O	C10	MEMW#	I/O
D11	DRQ5	I	C11	SD8	I/O
D12	DACK6#	O	C12	SD9	I/O
D13	DRQ6	I	C13	SD10	I/O
D14	DACK7#	O	C14	SD11	I/O
D15	DRQ7	I	C15	SD12	I/O
D16	+5 V dc	NA	C16	SD13	I/O
D17	MASTER#	I	C17	SD14	I/O
D18	Ground	NA	C18	SD15	I/O

PCI Connector

Note: The PCI connectors are part of the riser card.

Figure 41 (Page 1 of 2). PCI Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
A1	TRST#	O	B1	–12 V dc	NA
A2	+12 V dc	NA	B2	TCK	O
A3	TMS	O	B3	Ground	NA
A4	TDI	O	B4	TDO	I
A5	+5 V dc	NA	B5	+5 V dc	NA
A6	INTA#	I	B6	+5 V dc	NA
A7	INTC#	I	B7	INTB#	I
A8	+5 V dc	NA	B8	INTD#	I
A9	Reserved	NA	B9	PRSNT1#	I
A10	+5 V dc (I/O)	NA	B10	Reserved	NA
A11	Reserved	NA	B11	PRSNT2	I
A12	Ground	NA	B12	Ground	NA
A13	Ground	NA	B13	Ground	NA
A14	Reserved	NA	B14	Reserved	NA
A15	RST#	O	B15	Ground	NA
A16	+5 V dc (I/O)	NA	B16	CLK	O
A17	GNT#	O	B17	Ground	NA
A18	Ground	NA	B18	REQ#	I
A19	Reserved	NA	B19	+5 V dc (I/O)	NA
A20	Address/Data 30	I/O	B20	Address/Data 31	I/O
A21	+3.3 V dc	NA	B21	Address/Data 29	I/O
A22	Address/Data 28	I/O	B22	Ground	NA
A23	Address/Data 26	I/O	B23	Address/Data 27	I/O
A24	Ground	I/O	B24	Address/Data 25	NA
A25	Address/Data 24	I/O	B25	+3.3 V dc	NA
A26	IDSEL	O	B26	C/BE 3#	I/O
A27	+3.3 V dc	NA	B27	Address/Data 23	I/O
A28	Address/Data 22	I/O	B28	Ground	NA
A29	Address/Data 20	I/O	B29	Address/Data 21	I/O
A30	Ground	I/O	B30	Address/Data 19	NA
A31	Address/Data 18	I/O	B31	+3.3 V dc	NA
A32	Address/Data 16	I/O	B32	Address/Data 17	I/O
A33	+3.3 V dc	NA	B33	C/BE 2#	I/O
A34	FRAME#	I/O	B34	Ground	NA
A35	Ground	NA	B35	IRDY#	I/O
A36	TRDY#	I/O	B36	+3.3 V dc	NA
A37	Ground	NA	B37	DEVSEL#	I/O
A38	STOP#	I/O	B38	Ground	NA
A39	+3.3 V dc	NA	B39	LOCK#	I/O

Figure 41 (Page 2 of 2). PCI Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
A40	SDONE	I/O	B40	PERR#	I/O
A41	SBO#	I/O	B41	+3.3 V dc	NA
A42	Ground	NA	B42	SERR#	I/O
A43	+3.3 V dc	NA	B43	+3.3 V dc	NA
A44	C/BE(1)#	I/O	B44	C/BE 1#	I/O
A45	Address/Data 14	I/O	B45	Address/Data 14	I/O
A46	Ground	NA	B46	Ground	NA
A47	Address/Data 12	I/O	B47	Address/Data 12	I/O
A48	Address/Data 10	I/O	B48	Address/Data 10	I/O
A49	Ground	NA	B49	Ground	NA
A50	Key	NA	B50	Key	NA
A51	Key	NA	B51	Key	NA
A52	Address/Data 8	I/O	B52	Address/Data 8	I/O
A53	Address/Data 7	I/O	B53	Address/Data 7	I/O
A54	+3.3 V dc	NA	B54	+3.3 V dc	NA
A55	Address/Data 5	I/O	B55	Address/Data 5	I/O
A56	Address/Data 3	I/O	B56	Address/Data 3	I/O
A57	Ground	NA	B57	Ground	NA
A58	Address/Data 1	I/O	B58	Address/Data 1	I/O
A59	+5 V dc (I/O)	NA	B59	+5 V dc (I/O)	NA
A60	ACK64#	I/O	B60	ACK64#	I/O
A61	+5 V dc	NA	B61	+5 V dc	NA
A62	+5 V dc	NA	B62	+5 V dc	NA

Wake on LAN and Modem/Ring Wake-up Connectors

Figure 42. J27 Modem/Ring

Pin	Description
1	External Wake Up on Ring
2	Ground

Figure 43. J28 Wake on LAN

Pin	Description
1	+5v AUX
2	Ground
3	External Wake on LAN

Power Supply Connectors

Figure 44. Pin Assignments for Power Supply Connectors

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	ON/OFF
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWR GOOD	18	-5 V
9	+5 V AUX	19	+5 V
10	+12 V	20	+5 V

Appendix B. System Address Maps

System Memory Map

The first 640 KB of system board RAM is mapped starting at address hex 0000000. A 256-byte area and a 1 KB area of this RAM are reserved for BIOS data areas. Memory can be mapped differently if POST detects an error.

Figure 45. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
0 K – 512 K	00000–7FFFF	512 KB	Conventional
512 K – 639 K	80000–9FBFF	127 KB	Extended conventional
639 K – 640 K	9FC00–9FFFF	1 KB	Extended BIOS data
640 K – 800 K	A0000–C7FFF	160 KB	Video memory and BIOS
800 K – 896 K	C8000–DFFFF	96 KB	Available high DOS memory
896 K – 928 K	E0000–E7FFF	32 KB	POST BIOS
928 K – 992 K	F0000–FFFFF	64 KB	POST BIOS
1024 K – 262144 K	100000–10000000	255 MB	Extended

Input/Output Address Map

The following figure lists resource assignments for the I/O address map. Any addresses that are not shown are reserved.

Figure 46 (Page 1 of 3). I/O Address Map

Address (Hex)	Size	Description
0000–000F	16 bytes	DMA 1
0020–0021	2 bytes	Interrupt controller 1
002E–002F	2 bytes	I/O controller configuration registers
0040–0043	4 bytes	Counter/timer 1
0048–004B	4 bytes	Counter/timer 2
0060	1 byte	Keyboard controller byte - reset IRQ
0061	1 byte	NMI, speaker control
0064	1 byte	Keyboard controller, CMD/STAT byte
0070, bit 7	1 bit	Enable NMI
0070, bits 6:0	1 bit	Real time clock, address
0071	1 byte	Real time clock, data
0078	1 byte	Reserved - system board configuration
0079	1 byte	Reserved - system board configuration
0080–008F	16 bytes	DMA page registers
00A0–00A1	2 bytes	Interrupt controller 2
00B2–00B3	2 bytes	APM control
00C0–00DE	31 bytes	DMA 2
00F0	1 byte	Reset numeric error

Figure 46 (Page 2 of 3). I/O Address Map

Address (Hex)	Size	Description
0170–0177	8 bytes	Secondary IDE channel
01F0–01F7	8 bytes	Primary IDE channel
0200–0207	8 bytes	Available
0220–022F	16 bytes	Available
0240–024F	16 bytes	Available
0278–027F	8 bytes	LPT2
02E8–02EF	8 bytes	COM4/video
02F8–02FF	8 bytes	COM2
0300–0301	2 bytes	Available
0330–0331	2 bytes	Available
0332–0333	2 bytes	Available
0334–0335	2 bytes	Available
0376	1 byte	Secondary IDE channel command port
0377	1 byte	Diskette channel 2 command
0377, bit 7	1 bit	Diskette change, channel 2
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378–037F	8 bytes	LPT1
0388–038D	6 bytes	Available
03B4–03B5	2 bytes	Video
03BA	1 byte	Video
03BC–03BF	4 bytes	LPT3
03C0–03CA	11 bytes	Video
03CC	1 byte	Video
03CE–03CF	2 bytes	Video
03D4–03D5	2 bytes	Video
03DA	1 byte	Video
03E8–03EF	8 bytes	COM3
03F0–03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F7 (Write)	1 byte	Diskette channel 1 command
03F7, bit 7	1 bit	Diskette disk change channel
03F7, bits 6:0	7 bits	Primary IDE channel status port
03F8–03FF	8 bytes	COM1
04D0–04D1	2 bytes	Edge/level triggered PIC
0530–0537	8 bytes	Windows sound system
0604–060B	8 bytes	Windows sound system (if present)
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + hex 400
0CF8–0CFB	4 bytes	PCI configuration address register
0CF9	1 byte	Turbo and reset control register
0CFC–0CFF	4 bytes	PCI configuration data register
0E80–0E87	8 bytes	Windows sound system (if present)
0F40–0F47	8 bytes	Windows sound system (if present)
0F86–0F87	2 bytes	Available

Figure 46 (Page 3 of 3). I/O Address Map

Address (Hex)	Size	Description
7000–700D	14 bytes	SMBus I/O space registers
8000–8037	56 bytes	Power management I/O space registers
FF00–FF07	8 bytes	IDE bus master register
FFA0–FFA7	8 bytes	Primary bus master IDE registers
FFA8–FFAF	8 bytes	Secondary bus master IDE registers

DMA I/O Address Map

The following figure lists resource assignments for the DMA address map. Any addresses that are not shown are reserved.

Figure 47 (Page 1 of 2). DMA I/O Address Map

Address (Hex)	Description	Bits	Byte Pointer
0000	Channel 0, Memory Address register	00–15	Yes
0001	Channel 0, Transfer Count register	00–15	Yes
0002	Channel 1, Memory Address register	00–15	Yes
0003	Channel 1, Transfer Count register	00–15	Yes
0004	Channel 2, Memory Address register	00–15	Yes
0005	Channel 2, Transfer Count register	00–15	Yes
0006	Channel 3, Memory Address register	00–15	Yes
0007	Channel 3, Transfer Count register	00–15	Yes
0008	Channels 0–3, Read Status/Write Command register	00–07	
0009	Channels 0–3, Write Request register	00–02	
000A	Channels 0–3, Write Single Mask register bits	00–02	
000B	Channels 0–3, Mode register (write)	00–07	
000C	Channels 0–3, Clear byte pointer (write)	N/A	
000D	Channels 0–3, Master clear (write)/temp (read)	00–07	
000E	Channels 0–3, Clear Mask register (write)	00–03	
000F	Channels 0–3, Write All Mask register bits	00–03	
0081	Channel 2, Page Table Address register [1]	00–07	
0082	Channel 3, Page Table Address register [1]	00–07	
0083	Channel 1, Page Table Address register [1]	00–07	
0087	Channel 0, Page Table Address register [1]	00–07	
0089	Channel 6, Page Table Address register [1]	00–07	
008A	Channel 7, Page Table Address register [1]	00–07	
008B	Channel 5, Page Table Address register [1]	00–07	
008F	Channel 4, Page Table Address/Refresh register	00–07	
00C0	Channel 4, Memory Address register	00–15	Yes
00C2	Channel 4, Transfer Count register	00–15	Yes
00C4	Channel 5, Memory Address register	00–15	Yes
00C6	Channel 5, Transfer Count register	00–15	Yes
00C8	Channel 6, Memory Address register	00–15	Yes
00CA	Channel 6, Transfer Count register	00–15	Yes

Figure 47 (Page 2 of 2). DMA I/O Address Map

Address (Hex)	Description	Bits	Byte Pointer
00CC	Channel 7, Memory Address register	00–15	Yes
00CE	Channel 7, Transfer Count register	00–15	Yes
00D0	Channels 4–7, Read Status/Write Command register	00–07	
00D2	Channels 4–7, Write Request register	00–02	
00D4	Channels 4–7, Write Single Mask register bit	00–02	
00D6	Channels 4–7, Mode register (write)	00–07	
00D8	Channels 4–7, Clear byte pointer (write)	N/A	
00DA	Channels 4–7, Master clear (write)/temp (read)	00–07	
00DC	Channels 4–7, Clear Mask register (write)	00–03	
00DE	Channels 4–7, Write All Mask register bits	00–03	
00DF	Channels 5–7, 8- or 16-bit mode select	00–07	

PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 84440LX
00	01	00	Intel 82371AB AGP bus
00	07	00	Intel 82371AB PCI/ISA bus
00	07	01	Intel 82371AB IDE bus master
00	07	02	Intel 82371AB USB
00	07	03	Intel 82371AB power management
01	00	00	Cirrus Logic CL-GD5465 AGP controller

[1] Upper byte of memory address register.

Appendix C. IRQ and DMA Channel Assignments

The following figures list the interrupt request (IRQ) and direct memory access (DMA) channel assignments.

Figure 48. IRQ Channel Assignments

IRQ	System Resource
NMI	I/O channel check
0	Reserved (interval timer)
1	Reserved (keyboard)
2	Reserved (cascade interrupt from slave)
3	COM2 [2]
4	COM1 [2]
5	LPT2/Audio (if present)
6	Diskette controller
7	LPT1 [2]
8	Real-time clock
9	Available to user
10	Available to user
11	Windows sound system (if present)
12	Mouse port
13	Reserved (math coprocessor)
14	Primary IDE (if present)
15	Secondary IDE (if present)

Figure 49. DMA Channel Assignments

DMA Channel	Data Width	System Resource
0	8- or 16- bits	Open
1	8- or 16- bits	Parallel port
2	8- or 16- bits	Diskette drive
3	8- or 16- bits	Parallel port (for ECP or EPP)
4	–	Reserved (cascade channel)
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

[2] Default, can be changed to another IRQ.

Appendix D. Error Codes

The following figures list the POST error codes and beep codes for the computer.

POST Error Codes

POST error messages appear when POST finds problems with the hardware during power-on or when a change in the hardware configuration is found. POST error messages are 3-, 4-, 5-, 8-, or 12-character alphanumeric messages. An *x* in an error message can represent any number.

Figure 50 (Page 1 of 2). POST Error Codes

Code	Description
101	Interrupt failure
102	Timer failure
103	Timer-interrupt failure
104	Protected mode failure
105	Last 8042 command not accepted–keyboard failure
106	System board failure
108	Timer bus failure
109	Low MB chip select test
110	System board parity error 1 (system board parity latch set)
111	I/O parity error 2 (I/O channel check latch set)
112	I/O channel check error
113	I/O channel check error
114	External ROM checksum error
115	DMA error
116	System board post read/write error
120	Microprocessor test error
121	Hardware error
151	Real-time-clock failure
161	Bad CMOS battery
162	CMOS RAM checksum/configuration error
163	Clock not updating
164	CMOS RAM memory size does not match
167	Clock not updating
175	Riser card or system board error
176	System cover has been removed
177	Damaged administrator password
178	Riser card or system board error
183	Administrator password has been set and must be entered
184	Password removed due to checksum error
185	Damaged startup sequence
186	System board or hardware security error
189	More than three password attempts were made to access system
201	Memory data error

Figure 50 (Page 2 of 2). POST Error Codes

Code	Description
202	Memory-address line error 00–15
203	Memory-address line error 16–23
221	ROM-to-RAM remapping error
225	Unsupported memory type installed or memory pair mismatch
301	Keyboard error
302	Keyboard error
303	Keyboard-to-system-board interface error
304	Keyboard clock high
305	No keyboard +5 V dc
601	Diskette drive or controller error
602	Diskette IPL boot record not valid
604	Unsupported diskette drive installed
605	POST cannot unlock diskette drive
662	Diskette drive configuration error
762	Math coprocessor configuration error
11*xx*	Serial port error (*xx* is the serial port number)
1762	Hard disk configuration error
1780	Hard disk 0 failed
1781	Hard disk 1 failed
1782	Hard disk 2 failed
1783	Hard disk 3 failed
1800	PCI adapter has requested an unavailable hardware interrupt
1801	PCI adapter has requested an unavailable memory resource
1802	PCI adapter has requested an unavailable I/O address space, or a defective adapter
1803	PCI adapter has requested an unavailable memory address space, or a defective adapter
1804	PCI adapter has requested unavailable memory addresses
1805	PCI adapter ROM error
1962	Startup sequence error
2401	System board video error
8601	System board or keyboard/pointing device error
8602	Pointing device error
8603	Pointing device or system board error
12092	Level 1 cache error (microprocessor)
12094	Level 2 cache error
I9990301	Hard disk failure
I9990305	No operating system found

Beep Codes

For the following beep codes, the numbers indicate the sequence and number of beeps. For example, a "2-3-2" error symptom (a burst of two beeps, three beeps, and then two beeps) indicates a memory module problem. An *x* in an error message can represent any number.

Figure 51. Beep Codes

Beep	Probable Cause
1-1-3	CMOS write/read failure
1-1-4	BIOS ROM checksum failure
1-2-1	Programmable interval-timer test failure
1-2-2	DMA initialization failure
1-2-3	DMA page register write/read test failure
1-2-4	RAM refresh verification failure
1-3-1	1st 64 K RAM test failure
1-3-2	1st 64 K RAM parity test failure
2-1-1	Slave DMA register test in progress or failure
2-1-2	Master DMA register test in progress or failure
2-1-3	Master interrupt-mask register test failure
2-1-4	Slave interrupt-mask register test failure
2-2-2	Keyboard controller test failure
2-3-2	Screen memory test in progress or failure
2-3-3	Screen retrace tests in progress or failure
3-1-1	Timer-tick-interrupt test failure
3-1-2	Interval timer channel 2 test failure
3-1-4	Time-of-day clock test failure
3-2-4	Comparing CMOS memory size against actual
3-3-1	Memory size mismatch occurred

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