TANDY 4000
TECHNICAL REFERENCE MANUAL
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Tandy 4000 Technical Reference Manual
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Tandy 4000
Technical Reference Manual
Contents

Sections

Main Logic Board
Devices
Power Supplies
Keyboard
Disk Drive
Options
Software

Important Customer Notes:

A gray stripe has been printed along the right edge of the title page of each of the sections to facilitate your finding the begining of the section. Also, a tabbed divider for each section has been provided for insertion at this point.

If you need addtional technical reference information for your 80387 Math Co-processor or other update information, obtain the 700-4108 package from your local Radio Shack Store.

4000 Main Logic Board

Contents

Scope of Document.....4

Introduction.....5

Specifications and Features.....7

Switch Settings And Jumper Pin Configurations.....8

Functional Description.....9

80386 Processor.....9

Weitek Numeric Processor (Optional).....10

Clock Generation.....11

Command and Control Signals.....11

Generation.....11

82C301 Bus Controller.....11

82A306 Control Buffer.....18

Memory Control and Refresh.....20

82C302 Memory Controller.....20

Memory Configurations.....20

Memory Expansion.....31

Address Buffers.....32

82A303 High Address Buffers.....32

82A304 Low Address Buffers.....34

Data Buffers And Conversion Logic.....35

82A305 Data Buffers.....35

I/O Decode.....38
82C206 Integrated Peripherals Controller.....38
DMA Controller.....44
Interrupt Controller.....64
Timer/Counter.....76
Real-Time Clock.....85
Floppy Disk Controller.....93
80287 Numeric Processor (Optional).....120
Serial/Parallel Interface.....120
Keyboard Control.....122
Interface Requirements.....126
System I/O Bus Interface.....126
PC Bus.....127
AT Bus.....131
Memory Expansion Bus.....134

SCOPE OF DOCUMENT

This document provides detailed specifications on the Tandy® 4000.

The Tandy 4000 computer system is composed of four buses:

- **The 80386 Local Bus**--consists of the 80386 CPU, the 82C301 bus controller, and the optional Weitek Numeric Processor.
- **The 32-Bit Memory Bus**--consists of up to four banks of 32-bit access dynamic RAM (DRAM). Two banks are located on the main logic board which also has an expansion slot for an additional two banks. Each bank consists of either four 256Kb x 9 DRAM modules or four 1Mb x 9 DRAM modules with an access time of 100 ns.
- **The System I/O (AT) Bus**--contains the BIOS ROM devices, the floppy disk controller (FDC), and eight expansion slots (two IBM ® PC-compatible and six AT-compatible) for optional devices, and the 80287 co-processor.
- **The Peripheral Bus**--an extension of the system I/O bus; contains the direct memory access (DMA), interrupt, counter/timer, speaker, keyboard, and real-time clock (RTC) operations.

Each bus has different timing characteristics. For example, the 80386 bus operates at a clock rate of 16MHz with either no wait state or one wait state when accessing 32-bit RAM, and the AT bus operates at 8MHz with up to four wait states.

INTRODUCTION

Compatibility. The Tandy® 4000 is designed to be as compatible as possible with the existing Tandy 3000 and the IBM AT®, in terms of both hardware and software.

Most operating systems and application programs that run on the Tandy 3000 will run on the Tandy 4000. The Tandy 3000 BIOS ROMs will not run in the Tandy 4000, however, because of the extra programming information needed to configure the Tandy 4000.

Certain hardware functions from the Tandy 3000 are duplicated on the Tandy 4000. All I/O and memory maps, interrupts, DMA channels, the keyboard interface, and the AT bus have the same configurations and timing parameters. Additional circuitry supports CPU 32-bit data movements to and from the 8- and 16-bit I/O and memory devices.

Although 8- and 16-bit memory cards can be used on the AT bus, performance will be significantly decreased compared to the 32-bit memory options.

Modular Design. The Tandy 4000 is modular in design to allow maximum flexibility in system configuration. The computer consists of a main unit and a detachable keyboard with coiled cable. The main unit is supplied with one internal 3½-inch, 1.44Mb floppy disk drive. The standard types of monitors used with the Tandy 4000 are the monochrome, RGB, and EGA monitors. Because these units are modular, they can be placed on top of the main unit or at any convenient location.

Memory. The Tandy 4000 comes standard with 1 megabyte of 32-bit wide system RAM. This 32-bit wide System memory can be expanded to 2, 4, 8, 10 or 16 megabytes, the maximum RAM allowed by the system memory map.

Additional Features. Other features include a parallel printer port, a serial port, and a speaker for audio feedback.

Main Unit. The main unit is the heart of the Tandy 4000. It houses the main logic assembly, the system power supply, optional hard disk unit, and the floppy disk drive.

The main logic assembly is a large board mounted on the floor of the main unit and connected to the keyboard, power supply, and disk drive by a series of cables.

The power supply is a 192 watt switching regulator type, designed to provide adequate power capacity for a fully configured system using all the option slots.

The floppy disk drive uses 3½-inch, double-sided, double-density diskettes to read or write data. These are soft-sector diskettes. The disk drive assembly is installed in the main unit. The floppy disk stores approximately 1.44 megabytes (formatted) of data. All system programs, with the exception of the system startup sequence, are stored on disk.

Monitors. A monochrome, EGA, or RGB display can be used with the Tandy 4000. The appropriate display adapter must be installed in the main unit.

FEATURES

16MHz, 32-bit 80386 processor with on-chip memory management and protection.

Standard 1Mb, 0-wait state, 32-bit memory.
- Supports up to 8 megabytes of 32-bit wide memory on board
- Bus addressing supports PC (8-bit), AT (16-bit), and 32-bit data widths

Standard 1.44Mb, 3½-inch floppy disk drive.
- Selectable 1.44Mb or 720Kb format allows compatibility with the Tandy 3000, Tandy 1000, IBM AT, or IBM PC
- Channel for additional internal floppy disk drive of 3½-inch or 5¼-inch type

Channel for user-selectable hard disk drive.

Six IBM AT-compatible slots for standard peripherals and additional memory (16-bit) expansion.

Two IBM PC-compatible slots for standard peripherals and additional memory (8 bit) expansion.

One 32-bit memory upgrade slot.
- 2Mb or 8Mb for a total of 16Mb
- 0 wait state (statistical)

True software compatibility with the IBM AT in the single-user MS-DOS® (real) mode or the multi-user (protected) mode. Can support Xenix or a UNIX based operating system and MS-DOS concurrently in the Protected Mode.

Built-in real-time clock with CMOS RAM and battery backup.

Serial/parallel interface adapter included.

Enhanced IBM AT-compatible keyboard.

Support for optional 80287 or Weitek 1167 math co-processor.

192 watt power supply.

PHYSICAL SPECIFICATIONS

Width	19 in.
Height	6 in.
Depth	18 in.
Weight	47 lbs.

SWITCH SETTINGS AND JUMPER PIN CONFIGURATIONS

Jumper	Function	As Shipped
E1-E2	Color/Monochrome Monitor installed = color not installed = monochrome	installed
E3-E4	Not Used	not installed
E5-E6 and E6-E7	Floppy Disk Controller Select E5-E6 installed = primary FDC E6-E7 installed = secondary FDC	 installed not installed
E8-E9	80287 Option installed = option present not installed = option not present	not installed

Table 1. Switch Settings and Jumper Configurations.

FUNCTIONAL DESCRIPTION

The following sections of this document explain in detail the functions of the various devices found in the Tandy® 4000.

80386 PROCESSOR

General Overview

The 80386 processor is an advanced 32-bit microprocessor designed for applications needing very high performance. It is also optimized for multi-tasking operating systems.

The 32-bit registers and data paths support 32-bit addresses and data types. The processor addresses up to four gigabytes of physical memory and 64 terabytes of virtual memory. Even though the processor will access up to four gigabytes of memory the implementation used in the Tandy 4000 only supports up to 16 megabytes.

The integrated memory management and protection architecture includes address translation registers, advanced multi-tasking hardware, and a protection mechanism to support operating systems. The processor also allows the simultaneous running of multiple operating systems.

The 80386 consists of a central processing unit, a memory management unit, and a bus interface.

Central Processing Unit

The central processing unit consists of the execution unit and the instruction unit.

The execution unit contains the eight 32-bit general-purpose registers, which are used for both address calculation and data operations. In addition, it contains a 64-bit barrel shifter, which is used to speedshift, rotate, multiply, and divide data contained in the registers.

The instruction unit decodes the instruction opcodes and stores them in the decoded instruction queue for immediate use by the execution unit.

Memory Management Unit (MMU)

The memory management unit consists of a segmentation unit and a paging unit.

Memory is organized into one or more variable length segments, each up to 4 gigabytes in size. A given region of the linear address space, a segment, has certain attributes associated with it. These attributes include its location, size, type, and protection characteristics. Each task on the 80386 can have a maximum of 16,381 segments of up to 4 gigabytes each, thus, due to the memory management organization of the processor, it provides 64 terabytes of virtual memory to each task. The segmentation unit provides four levels of protection for isolating applications and the operating system from each other. Even though the processor will address up to four gigabytes of memory, the Tandy 4000 only supports up to 16 megabytes.

The 80386 has two modes of operation: Real Address Mode (Real Mode) and Protected Virtual Address Mode (Protected Mode).

In Real Mode, the 80386 operates as a very fast 8086 but with 32-bit extensions if desired. Real Mode is required primarily to set up the processor for Protected Mode operation.

Protected Mode provides access to the sophisticated memory management, paging, and privilege capabilities of the processor. Within Protected Mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each such task behaves with 8086 semantics, thus allowing 8086 software to execute.

Bus Interface

Finally, to facilitate high-performance system hardware designs, the 80386 local bus offers address pipelining, dynamic data bus sizing, and direct byte enable signals for each byte of the data bus. These features are discussed in later sections of the this manual.

WEITEK NUMERIC PROCESSOR WTL1167 (OPTIONAL)

The optional Weitek Numeric Processor Board connects to the 80386 local bus through a 121-pin PGA socket designated U15. This board provides a 32-bit data path to the CPU and performs 32- and 64-bit floating point operations at 4-5 times the speed of other available co-processors. Added modifications are needed for this option on the Rev. A-1 system board. Revision 3002-0044-00 of the Weitek board works with these modifications, however, Radio Shack® does not provide support for the Weitek board. Also note that the 80387 socket on the Weitek board is not supported by this revision of the system board.

CLOCK GENERATION

The 82C301 (U14) provides three major system clocks:

- The processor clock, CLK2
- The BCLK for the AT bus state machine of the 82C301
- The AT bus clock, SYSCLK

The BCLK is a clock internal to the 82C301.

The clock generation circuitry uses two external clocks, CLK2IN and ATCLK1, as selectable clock sources. These are supplied by TTL oscillator (Y3). CLK2IN is a 32MHz input signal and ATCLK1 is a 12MHz input signal.

The clock input to the 80386 processor is CLK2, which is a 32MHz signal. The clock signal provided to the AT bus is ATSCLK and is rated at 8MHz and may be slowed to 6MHz by the speed command in MS-DOS 3.20.3

COMMAND AND CONTROL SIGNALS

GENERATION

The command and control signals necessary for system operation are generated by two devices: the 82C301 bus controller (U14) and the 82C306 control buffer (U13).

82C301 Bus Controller

This 84-pin PLCC device produces and synchronizes the CPU and system clocks and performs interfacing between the 80386 and the rest of the system control lines.

Reset Control

RESET1* is produced at power up/down or when the reset button on the front panel is depressed. When the RESET1* is asserted, the bus controller asserts RESET3 and RESET4 for a system reset. RESET3 is routed to the 80386 CPU and the Weitek co-processor, and RESET4 is sent to the control buffer. For a warm restart not requiring an extensive reset, RESET2* can be asserted to generate RESET3 for resetting only the processor and co-processor. RESET2* is generated by pressing the Ctrl, Alt, and Del keys on the keyboard simultaneously. RESET3 is also asserted when a CPU shutdown is detected. This differentiation is provided so that some register states can be maintained through the reset if so desired.

Bus Arbitration

General

The bus controller performs the synchronization and control required for communication between the local processor bus, the memory subsystem, and the system I/O (AT) bus. It controls all bus activities and handles the HRQ1, HRQ2, and REFREQ signals by generating a HOLD request to the CPU and arbitrating among these requests in a non-preemptive manner.

Upon the CPU assertion of HLDA, the arbitration logic responds by asserting HLDA1 (for HRQ1), or HLDA2 (for HRQ2). The requesting DMA or master device has control of the bus until it de-asserts the Hold Request signal to terminate the HLDA cycle. During the HLDA cycle, the bus controller generates both SMCMD* and AC0 through AC3 to control the buffer enable and directions for the address and data buffers. HRQ2 is disabled in the Tandy 4000. Bus size conversions are not supported by the bus controller for these bus cycles and if necessary should be performed by the requesting device.

All CPU access cycles are started by the bus controller asserting the MALE* signal. The bus controller then samples the AF32* signal one SCLK clock cycle later. If AF32* is active, the cycle is assumed to be a local bus cycle and the bus controller terminates this cycle when it detects the READY* signal active. In response to an MALE*, if AF32* is detected inactive, the control is passed to the AT bus control portion of the bus controller. At the end of the bus access cycle, the AT bus control logic of the bus controller generates READY* to terminate the processor access cycle.

CPU Bus

Interface to the 80386 requires interpretation of the status lines upon assertion of the ADS* signal. It also requires synchronization and generation of a READY* response to the CPU upon completion of the requested operation.

By interpreting the CPU status lines and the ADS* signal, the bus controller generates control signals MALE* and SMCMD*. In response to each ADS* signal generated by the CPU, an MALE* signal is generated by the bus controller to indicate the start of a new CPU access cycle.

In a non-pipelined CPU cycle, MALE* is generated in response to the ADS* signal being asserted by the 80386. In a pipelined cycle, MALE* is generated when the assertion of the READY* signal is detected for the previous CPU cycle.

If the AF32* signal is not active one cycle after MALE* is asserted, control is passed to the AT bus control section of the bus controller. The bus controller then waits for READY* to become active to terminate the access cycle. The READY* signal can also be generated by the 82C302 (U27) page/interleave memory controller, which controls the system memory access.

SMCMD* indicates a memory cycle for both CPU and non-CPU accesses. During CPU cycles, SMCMD* is generated for all memory cycles by decoding the M/(IO)*, D/(C)* and W/(R)* signals. During non-CPU cycles, SMCMD* is active when XMEMR* or XMEMW* signals are active.

Bus Timeout

An optional feature allows generation of a non-maskable interrupt (NMI) if an internal memory cycle does not complete within a certain timeout period. This occurs if AF32* is asserted in response to MALE* and READY* is not returned to the bus controller within 128 CLK2 cycles. A control bit in the 82C301 Bus Controller's Port B register enables this feature and will be explained later in this section.

AT Bus

The bus controller gains control of the AT bus when AF32* is detected inactive. It also performs the necessary synchronization of control and status signals between the AT bus and the processor. The bus controller supports 8-, 16-, or 32-bit transfers between the processor and 8-, 16-, or 32-bit memory or I/O devices located on the I/O bus.

An AT bus cycle is initiated by asserting the ALE signal that is decoded from the CPU status signals and is terminated by asserting READY*. On the trailing edge of ALE, the signals MCS16* and IOCS16* are sampled to determine the bus size conversion required. The bus controller then enters the command cycle. The bus controller provides the sequencing and timing controls for status and command phases of different AT bus cycles. These controls provide timing emulation of lower-speed I/O channels to maintain compatibility with AT or PC/XT I/O adapters and memory cards. The command cycle is terminated by detecting OWS* or IOCHRDY* active.

I/O Channel Speed Control

The bus controller AT bus logic can be programmed to insert wait states in units of ATSCLK and to delay the generation of the XIOR*, XIOW*, XMEMR*, and XMEMW* commands in one-half units of ATSCLK within the selected wait states. The command phase delay can be selectively defined for I/O cycles and for 8-, 16-, or 32-bit wide memory cycles by setting the corresponding fields in the Port B register location 05H. This location controls the I/O channel wait state generation for 8-, 16-, and 32-bit accesses.

Data Conversion

The bus controller performs data conversions for CPU accesses to devices not on the local bus when AF32* is not asserted. AT bus conversions are performed for the following types of transfers:

- 32-bit to 8-/16-bit
- 24-bit to 8-/16-bit
- 16-bit to 8-/16-bit

Larger transfers are broken into smaller AT bus reads or writes and the action codes A0-A3 to the control buffer are generated. Byte Addresses XA0-XA1 are generated to drive the lower two bits of the AT bus.

The bus controller responds to IOCS16*, MCS16*, IOCS32*, and MCS32* to determine what size of data the I/O channel needs. If none of the above signals is asserted, 8-bit transfers are assumed and the request is converted into two, three, or four I/O channel cycles, based on BE0-BE3. For either MCS16* or IOCS16*, the bus controller converts a 32-bit access into two 16-bit AT bus accesses.

The bus controller also supports 32-bit transfers between the processor, memory, and the I/O devices on the I/O channel. IOCS32* and MCS32* inputs allow a device to request a 32-bit transfer. It is assumed that the necessary extensions to the AT bus are made to utilize this feature. IOCS32* and MCS32* override IOCS16* and MCS16*.

In performing these data conversions, the bus controller generates a 4-bit action code AC0-AC3 to control the buffers in the 82A305 data buffer. This is done for the alignment of data path and direction control between the D, MD, and SD data buses. The functional description for these codes is given in the section on "82A305 Data Buffers."

Port B Register

The bus controller contains an AT-compatible configuration register called the Port B register. The following table gives the bit definitions for it:

Port	Bit	Default	Type	Function
61H	7	0	Read Only	System Parity Check
	6	0	Read Only	I/O Channel Check
	5	0	Read Only	Timer 2 Out
	4	0 or 1	Read Only	Refresh Detect
	3	1	Read/Write	Enable I/O Channel Check
	2	1	Read/Write	Enable Parity Check
	1	0	Read/Write	Speaker Data
	0	0	Read/Write	Timer 2 Gate Speaker

Table 2. Bit Definitions for Port B Register.

The bus controller can also be programmed to vary the number of wait states and command delays to the system bus as well as to change the bus clock speed. This is done by writing the address of the Index Register to alter to the Index Register port (22H) and then writing or reading the desired value to or from the Data Register port (23H). Tables 3 - 5 provide the definitions of the Programmable Index Registers:

Note: Use a JMP$+2 instuction between I/O port accesses to allow bus settle time.

Index 04H	Version/Processor Clock Select/NMI Source	
Bit(s)	**Function**	**Default(s)**
7,6	Version (0=initial version)	0,0
5	Reserved	0
4	Processor Clock Select 0 = Use processor oscillator input 1 = Use AT bus state machine clock (SYSCLKx2)	0
3	Enable/Disable power fail NMI 0 = Disable 1 = Enable	0
2	Enable/Disable READY timeout NMI 0 = Disable 1 = Enable	0
1	Enable/Disable power fail warning pin 0 = Disable 1 = Enable	0
0	READY timeout has/has not occurred 0 = Ready timeout has occurred 1 = Ready timeout has not occurred	0

Table 3. Index 04H Bit Definitions.

Index 05H **Command Delay**

The value for each of the command delay fields is as follows:

0 = 0-cycle delay
1 = 1-cycle delay
2 = 2-cycle delay
3 = 3-cycle delay

Bit(s)	Function	Default(s)
7,6	AT bus 32-bit memory command delay	0,0
5,4	AT bus 16-bit memory command delay	0,0
3,2	AT bus 8-bit memory command delay	0,1
1,0	AT bus I/O cycle command delay	0,1

Index 06H	Wait State/Bus Clock Source	
Bit(s)	**Function**	**Default(s)**
7,6	Wait states per 32-bit transfer 0 = 3-cycle delay 1 = 2-cycle delay 2 = 1-cycle delay 3 = 0-cycle delay	0,1
5,4	Wait states per 16-bit transfer 0 = 3-cycle delay 1 = 2-cycle delay 2 = 1-cycle delay 3 = 0-cycle delay	0,1
3,2	Wait states per 8-bit transfer 0 = 5-cycle delay 1 = 4-cycle delay 2 = 3-cycle delay 3 = 2-cycle delay	0,1
1,0	Bus clock source select 0 = Use processor clock/3 for AT bus state machine (5.33MHz) 1 = Use processor clock/2 for AT bus state machine (8 MHz) 2 = Reserved 3 = Use ATCLK input pin for AT bus state machine (6 MHz)	0,1

Table 5. Index 06H Bit Definitions.

82A306 Control Buffer

The control buffer contains the circuitry for decode and generation of the AF32* signal, parity generation, parity checking, byte enable latching of data for the memory cycle, and color reference signal generation.

14MHz Oscillator and Divider

The color reference oscillator is provided by the bus controller IC (U13), thus eliminating the 8284 type device normally used in AT-compatible systems. A divide by 12 counter is also included to generate the OSC/12 (1.19MHz) signal used on the main logic board. The raw clock is supplied by crystal Y2.

AF32* Generation

The AF32* signal generated by the 82A306 is not used in the Tandy® 4000 system.

Byte Enable Latch

The register that holds the byte enables valid during a memory cycle is located in the control buffer. An additional input (FBE*) is provided to force all byte enables active during certain memory operations.

Parity Checking and Generation

The control buffer provides the necessary exclusive OR'ing to generate full (byte) write and read parity from the partial parity bits PPH0-PPH3 and PPL0-PPL3, which are generated on the two (nibble wide) 82A305 data buffers (U23, U24).

For a memory read access, read parity bits PPH0-PPH3 and PPL0-PPL3 are checked against the parity bits MP0-MP3 read from memory. Parity bits PPH0-PPH3, PPL0-PPL3, and MP0-MP3 are latched by CAS* and PCHK* so that they are kept valid during parity checking. The results of the byte-wise comparison are further gated by byte enables to ignore errors for bytes that are not valid. The OR'ed byte-wise parity error is then latched as the output LPAR* if PEN* input is asserted.

During a memory write access, write parity for each byte is generated from PPH0-PPH3 and PPL0-PPL3 and can be gated onto the memory parity bus MP0-MP3 if the control buffer is enabled by the WPE* signal controlling the tri-state drivers.

Bus Drivers

24mA bus drivers are provided for some of the control signals on the I/O channel. These signals include SYSCLK, OSC, OSC/12, RESETDRV, SBHE*, BALE, IOR*, IOW*, MEMR*, MEMW*, SMEMR*, SMEMW*, and OUT1*. The fuctionality for these signals is covered under "I/O Decode" and "Memory Control and Refresh."

MEMORY CONTROL AND REFRESH

82C302 Memory Controller

Memory Configuration

The memory control functions in this system utilize Page Mode Access DRAMs. Memory is organized as 36-bit banks (32 bits for data and 4 bits for parity) using four 9-bit SIMM boards per bank. The system will support up to 16Mb of 32-bit DRAMs using 1Mb x 9 modules.

The minimum configuration is a single bank operating in Non-Interleaved Mode.

The memory controller is designed such that the memory can be upgraded from one to two banks, making it a two-way interleaved organization. Because of the interleaved page operation, the third and fourth banks must be added as a pair. Furthermore, the DRAM types must be identical in each bank of a pair. However, each pair of banks can use different DRAM types. One or both banks of smaller DRAM types can later be upgraded to banks of larger DRAMs.

The following table shows the available configurations:

Number of Banks	Number/Size of SIMMs	Total Memory
1	4 - 256Kb x 9	1 Mb
1	4 - 1Mb x 9	4 Mb
2	8 - 256Kb x 9	2 Mb
2	8 - 1Mb x 9	8 Mb
4	16 - 256Kb x 9	4 Mb
4	8 - 256Kb x 9 8 - 1Mb x 9	10 Mb
4	16 - 1Mb x 9	16 Mb

Table 6. Available Memory Configurations.

Page-Interleaved Operation

The memory controller uses a page-interleaved design that is different from most interleaved memory designs. Normal two-way interleaving uses two banks of DRAMs with even (double word) addresses stored in one bank and odd addresses stored in the other. If accesses are sequential (or at least made to alternating even and odd addresses) the RAS precharge time of one set might overlap the access time of the second set. Typically the hit rate (the fraction of times that the required bank is available) is 50%. This is especially true since operand accesses can be interspersed with instruction fetches.

Page Mode operation available with most DRAMs operates because the access to the row address of the internal DRAM array makes available a large number of bits (512 bits in a 256Kb X 1 DRAM) that are subsequently selected using the column address. Once a row address has been made, higher-speed random access can be made to any bit within the row.

Page Mode access and cycle times are typically half those of the normal access and cycle times. During Page Mode operation any access to the currently active RAS page would occur in the page access rather than the normal access time. Any subsequent access could be to anywhere in the same page without incurring any penalty due to RAS precharge.

When memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving.

Memory Access and Arbitration

The memory controller controls the DRAM memory access from three sources: the CPU, the DMA, and the refresh request. These accesses are arbitrated based on the inputs of HLDA1* and REF*.

CPU Access

The CPU-initiated accesses are decoded according to the memory map defined in the Configuration Registers. These registers are at 08H to 0FH and are covered later in this section. These are the only accesses that use the Page Mode operation of the DRAMs.

The memory controller maintains four page registers, in which it stores the page addresses of the most recently accessed DRAM pages of the two-way interleaved banks. These four registers are called Active Page Registers. Accesses to the active pages are called hits and are faster because the DRAM is operated in the Page Mode with the RAS signal staying asserted.

The memory controller supports memory configurations with either one, two, or four banks. Because one Active Page Register is provided for each bank, the number of active pages varies with the amount of memory installed. In a non-interleaved minimum memory configuration, only one Active Page Register is in use. For each Active Page Register in use, the corresponding RAS* stays asserted after the previous access. If an access does not hit any active pages, a miss cycle, the normal DRAM access cycle is entered by first de-asserting the RAS* associated with the bank accessed.

RAS and CAS Generation

The memory controller is based on 2Kb page-interleaved organization. The following table shows the address lines used for the different organizations:

For Non-Interleaved Operation (One Bank Only)

DRAM Type	Row	Column
256Kb DRAMs	A11-A19	A2-A10
1Mb DRAMs	A12-A21	A2-A11

For Interleaved Memory (Two or Four Banks)

DRAM Type	Row	Column
256Kb DRAMs	A12-A20	A2-A10
1Mb DRAMs	A12-A21	A22, A2-A10

Table 7.
Address Lines for Available Memory Configurations.

In interleaved memory cases, Bit A11 determines which one of the even page banks or odd page banks is accessed. For configurations using only 256Kb DRAMs, A11 and A21 are used to control RAS0*-RAS3*. For those using only 1Mb DRAMs, A11 and A23 are used. For those using both 256Kb and 1Mb DRAMs, the 1Mb DRAMs must occupy the first two banks and the 256Kb DRAMs must occupy the second two banks. This constraint is there to ensure that there will not be a hole in the address space without actual DRAMs.

RAS Timeout

When using DRAM Page Mode, you must observe the maximum RAS pulse width. For most DRAMs, this is 10 microseconds. Using the OSC/12 (1.19MHz) clock generated by the control buffer timers are maintained within the memory controller for each bank to assure data integrity . RAS is de-asserted for each bank when its counter times out at about 10 microsecond intervals. The Memory Configuration Register bit 13H Bit 7 can be programmed to set the desired RAS time-out interval for each bank. See Table 13, later in this section, for details.

Refresh

To reduce power supply noise caused by surges during RAS transitions, RAS pulses to each bank are automatically staggered by one CLK2 cycle. Because all RAS's could be active for Page Mode operation, a refresh cycle requires that all RAS's be first de-asserted then asserted with the correct refresh address.

Direct-Memory Access

Direct-memory accesses are initiated by asserting the signal HLDA1. The XMEMR* and XMEMW* signals determine whether the access is a read or write memory access. The bytes accessed are controlled externally with the BE0*-BE3* signals generated by the bus controller. The memory controller makes one memory access per DMA bus cycle and does not attempt to pack or unpack data transfers to make full 32-bit transfers.

DRAM Access Logic

The DRAM control logic generates the necessary RAS, CAS, and DWE signals for all DRAM accesses. CPU, DMA, and refresh access cycles use DA8-DA9, XDA0-XDA7, and bank select signals BA0-BA1. (Note that in the current version of the memory controller, the signals BA0-BA1 default to zero.) The memory controller control logic provides the signal MDEN* to control the buffer chips. MDEN* enables data buffers for the MD bus for non-refresh DRAM cycles.

NOTE: "Default Configuration" refers to IC power up. The BIOS will reprogram these values.

Memory Mapping Logic

The memory controller Configuration Registers, located at Port 22H Index 08H-13H define what is a valid memory access and what is a ROM memory access, according to the local bus addresses. Registers 08H and 09H determine how ROM areas (as defined by an IBM AT) between the 768Kb to 1Mb address range are accessed.

For valid local memory accesses, the memory controller asserts the AF32* signal to indicate that it has control of the local bus and also asserts the READY* signal at the end of the access cycle. If an access is a ROM access, the memory controller asserts ROMCS* to provide controls for the ROMs. In this case, the READY* signal must be provided to the CPU and memory controller by the bus controller.

Clock, Reset, and Miscellaneous Logic

The RESET4 signal causes all internal registers to be reset to their default values. Configuration Registers not specified with default values are not reinitialized and might not retain their old values. The memory controller control logic generates the PCHK* and PEN* signals to be used for enabling parity error checking.

Configuration/Diagnostic Registers

The memory controller contains Index Registers used to configure the memory. These are accessed like the registers in the bus controller. Write the index address to Port 22H and then the programming value out to the Data Port 23H. XDEN* is asserted for these accesses to control the buffer connecting the XD and XDA buses. The Data Port can also be read.

Memory Configuration Registers

The Configuration Registers 08H to 0FH are used to control how the CPU memory accesses are defined. They define all addresses as ROM accesses, DRAM accesses, other local CPU bus accesses, or I/O channel accesses. These provisions are made because the low 1 megabyte is occupied by both DRAMs and ROMs and also devices on the AT bus. For ROM accesses, the memory controller generates the ROMCS* signal to control the ROM access. For DRAM access, the memory controller generates the necessary DRAM controls to the system memory under its control. It generates AF32* for all other local CPU bus accesses, and it does not control the I/O channel accesses.

The bus controller (U14) provides three 256Kb areas where the ROMs can be located. The functions of these areas are as follows:

Area	Location	Function
Low ROM	Just below the 1 megabyte address	8086-compatible operation
Middle ROM	Below the 16 megabyte address	80286-compatible operation
High ROM	Below the 4 gigabyte address	80386 operation

Table 8. Functions of ROM Areas.

On system reset, the default Configuration Register setting causes accesses to these three ROM areas to generate ROMCS*. The high ROM area is always recognized by the memory controller as BIOS ROM access area. The other two ROM areas can be mapped to be either ROM or RAM access.

After reset, Register 08H Bits 3 and 4, (See Table 9), can be programmed to map the entire middle ROM area to DRAM with write protection if desired.

Register 08H Bit 2 determines whether the bus controller recognizes the addresses generated beyond 16 megabytes as local CPU bus cycles.

Register 08H Bit 1 is used to enable Registers 0AH-0FH, which control the low megabyte DRAM (40000H-FFFFFH) address mapping for 256Kb to 1Mb addresses in 16Kb blocks. This bit defaults upon reset so that only the 0-256Kb areas are accessible. Accesses to the low megabyte DRAM can be made by enabling the mapping after the necessary configuration registers are correctly programmed.

Register 08H Bit 0 defaults to single-bank memory configuration upon reset. Therefore it must be programmed to enable page/interleaved operation.

Register 09H controls the address mapping and write protection for the low ROM area (C0000H-FFFFFH) in 64Kb blocks (See Table 10.) Registers 0AH-0FH define whether each 16Kb address range is a DRAM block in the system memory or on the I/O channel. (See Table 11.)

DRAM Array Configuration and Timing

The Configuration Registers 10H-13H provide the DRAM type definition and starting address for each pair of banks, Banks 0 and 1 and Banks 2 and 3.

Register 10H Bits 6 and 7 and Register 12H Bits 6 and 7 define whether the DRAMs are enabled, and if so, whether the system uses 256Kb DRAMs or 1Mb DRAMs. (See Table 12.) These bits default to 256Kb DRAMs upon reset.

Register 10H Bits 0-5 and Register 12H Bits 0-5 define the Address Bits 20-25 of the starting address of the pairs of banks. (See Table 12.) Some of these banks might not be valid because the memory banks must start at some predefined boundaries. For 256Kb DRAMs, all six bits (20-25) are valid if a only single bank is enabled. The banks starting address can be on any 1 megabyte boundary. Otherwise, only Bits 21-25 are valid starting address bits on 2Mb boundaries. For 1Mb DRAMs, only bits 23-25 are valid, forcing the banks starting address to be on 8Mb boundaries.

Register 11H Bit 7 and Register 13H Bit 7 define the RAS precharge time required when a page miss occurs so that DRAMs of different speeds can be supported for each pair of banks. (See Table 13.)

Register 11H Bit 6 and Register 13H Bit 6 define the wait state to be inserted to meet the DRAM speed. (See Table 13.) These parameters default to the slower timing upon reset so that the system can be powered up with minimal assumptions about the DRAM speed and the memory configuration.

Tables 9-15 describe the functions of the memory controller's programmable registers:

Identification Register (08H)

Bit(s)	Function	Default Value
7	Controller type	0
6-5	Version 0 = initial	0,0
4	Read/Write or Read Only of 256Kb RAM at 16128K 00FC000H 0 = read/write 1 = read only	0
3	Disable/Enable BIOS ROM below 16Mb 0 = disable 1 = enable	0
2	Assert/Do not assert AF32* for addresses above 16Mb 0 = do not assert 1 = assert	0
1	Use/Ignore memory configuration Registers 0AH-0FH 0 = ignore 1 = use	1
0	Disable/Enable interleave 0 = disable (use single bank) 1 = enable	0(*)

* 0 for one bank of 32-bit memory (1 megabyte)
1 for two banks of 32-bit memory (2 megabytes or more)

Table 9. Register 08H.

RAM/ROM Boot Area Configuration Register (09H)

Bit(s)	Function	Default Value
7-4	Disable/Enable writing to RAM located in BIOS 0 = read/write 1 = read only	0
	Bit 7 (RAM at 768K C0000-CFFFF)	0,1*
	Bit 6 (RAM at 832K D0000-DFFFF)	0,1*
	Bit 5 (RAM at 896K E0000-EFFFFH)	0,1*
	Bit 4 (RAM at 960K F0000-FFFFFH)	0,1*
3-0	Disable/Enable substituting BIOS ROM below 1 megabyte with RAM at the same address 0 = disable 1 = enable	1
	Bit 3 (ROM at 768K C0000-CFFFF)	0,0*
	Bit 2 (ROM at 832K C0000-DFFFF)	0,0*
	Bit 1 (ROM at 896K E0000-EFFFFH)	0,0*
	Bit 0 (ROM at 960K F0000-FFFFFH)	1,0*

* Default values change after ROM is initialized (ROM code is moved into DRAM.) The first value is the default before initialization. The second is the default after initialization.

Table 10. Register 09H.

Selective Enabling/Disabling of 16Kb Blocks of RAM (Registers 0AH,0BH, 0CH, 0DH, 0EH, and 0FH)

0 = System board controls address
1 = Address is on the I/O channel

Register	Block (Address Map)	Default Value
0AH	040000-05FFFFH	00H
0BH	060000-07FFFFH	00H
0CH	080000-08FFFFH	00H
0DH	0A0000-0BFFFFH	FFH*
0EH	0C0000-0DFFFFH	FFH*
0FH	0E0000-0FFFFFH	FFH*

* Default depends on options in I/O channel and use of expansion memory.

Table 11. Registers 0AH-0FH.

Bank Type/Starting Address
(10H for Banks 0/1, 12H for Banks 2/3)

Bit(s)	Function	Default Value
7-6	Bank enabled/disabled 0 = bank disabled 1 = bank enabled with 256Kb words (default) 2 = bank enabled with 1Mb words 3 = reserved	40H for 10H; varies for 12H*
5-0	Starting address bits 25-20 256Kb DRAMs 1Mb per bank (first bank only) 25-21 256Kb DRAMs 1Mb per bank (two banks required) 25-23 1Mb DRAMs 4Mb per bank (two banks required)	

* Index 12H default equals 00 if there are no Banks 2/3. It equals 42H for Banks 2/3 if 256Kb DRAMs are used.

Table 12. Registers 10H and 12H.

Bank Timing
(11H for Banks 0/1, 13H for Banks 2/3)

Bit(s)	Function	Default Value
		00H, 00H
7	RAS precharge time for a page miss 0 = 3 CLK2 times (93 ns) 1 = 5 CLK2 times (155 ns)	
6	Access wait states 0 = 0 wait states 1 = 1 wait state	
5-0	Reserved	

Table 13. Registers 11H and 13H.

Error Source/Address (MSBs)
(Register 28H)

Bit(s)	Function	Default Value
7	Enable/Disable parity check 0 = enable 1 = disable	0
6-2	Not Used	
1-0	High parity address bits (25,24) (read only)	

Table 14. Register 28H.

Parity Error Address (LSBs)
(Register 29H)

Bit(s)	Function	Default Value
7-0	Error address bits (23-16) (read only)	

Table 15. Register 29H.

Memory Expansion

The main logic board contains sockets for eight SIMM boards (Banks 0 and 1) of DRAMs. Using 1Mb x 9 SIMMs, this gives 8 megabytes of on-board memory. If more memory is desired, a 32-bit memory expansion card is available that contains eight more SIMM boards (Banks 2 and 3). Because of the interleaved nature of the memory, both Banks 2 and 3 must be used with this card. Using this option can expand the total system memory to a total of 16 megabytes. This card is plugged in the Number 1 expansion slot. It is incompatible with standard AT-type option cards.

ADDRESS BUFFERS

82A303 High Address Buffer (U20)

Address Decode

The address decode circuit provides as outputs the signals LIOCS*, LMEGCS*, L64MEG*, and HIROM*. These signals are active if the address accesses satisfy the conditions defined in Table 16. The signal decodes for LIOCS* and LMEGCS* are controlled by HLDA1 and are latched onto the trailing edge of MALE*. The L64MEG* and HIROM* signals are simply decoded from the address signals.

Signal	Decode Condition
LIOCS*	A12-A15 = 00H
LMEGCS*	A20-A31 = 00H
L64MEG*	A26-A31 = 00H
HIROM*	A26-A31 = 3FH

Table 16. Address Access Conditions.

Address Bus Interfaces

The 82A303 interconnects the local X and system address buses. Bidirectional drivers connect each bus and the internal buses. These drivers have 24 mA current drivers for direct connection to the system address bus. Table 17 shows how the drivers are configured between the buses for each type of active bus request. Note that the default configuration is set up so that the CPU address bus drives the memory address bus for local memory CPU access cycles.

For all CPU-sourced accesses, the addresses are latched on the trailing edge of MALE*.

Active Signal	Source Bus	Target Bus
HLDA1	XA	SA, A, MA
MASTER*	SA	XA, A, MA
REF*	--	SA driven low
ATEN	A	XA, SA, MA
default	A	MA

Table 17. Bus Direction Request Types.

27-Bit Extensions

The standard AT implementation supports only 24-bit addresses. The system architecture allows for address extension on the SA and XA buses to 27 bits (128Mb). This is done by grounding the enable pin XBHE for the XA bus and the enable pin SBHE for the SA bus. Internal pullups are provided so that if the enable pins are left unconnected Bits 24-27 of the respective bus are forced low.

82A304 LOW ADDRESS BUFFER (U21)

Address Decode

The signals IO2XCS*, 8042CS*, PORTBCS*, NMICS*, 287CS*, and AS provide the lower address decodes for the corresponding devices after being qualified by the LIOCS* signal generated by the high address buffer decoder. The resulting decode is as defined by the IBM PC AT I/O addresses and is shown in Table 18. For applications that require these devices to be relocated, the EXDEC signal can be tied low to ignore the LIOCS* qualification and the MA10-MA11 address bits.

Signal	Address Decoded
IO2XCS*	022H, 023H
8042CS*	060H, 064H
PORTBCS*	061H
NMICS*	070H
287CS*	0E0H to 0FFH

Table 18. Address Decode.

Address Bus Interfaces

The 82A304 interfaces between bits 00 to 11 of A, SA, XA, and MA address buses. The buffers and multiplexers are controlled by the HLDA1, MASTER*, REF*, and ATEN* signals to drive the signals from the source to the target buses as defined in Table 19 for each active signal. When REF* is asserted, the refresh counter is gated to the SA bus as the refresh row address and is incremented. When none of the listed signals is active, the default configuration is such that the A bus drives the MA bus for memory accesses by the CPU.

The SA00-SA11 signals are 24mA address buffers for direct interface to the AT bus.

Active Signal	Source Bus	Target Bus
HLDA1	XA	SA, MA, A
MASTER*	SA	XA, MA, A
REF*	Counter	SA
ATEN*	A2-A11	SA2-SA11, XA2-XA11, MA4-MA11
	XA0-XA1	SA0-SA1
default	A	MA

Table 19. Bus Direction Request Types.

DATA BUFFERS AND CONVERSION LOGIC

82A305 Data Buffers (U23, U24)

The data buffers interface between the local, memory, and system (I/O channel) data buses and provide data alignment and size conversion for AT I/O channel operations. It is designed as a nibble slice to reduce pin count. Two of the devices are incorporated into the system design and are used to interface all buses.

Bus Controls

The data buffers control the bus buffers according to the signals HLDA1, ATEN*, MDEN*, LDEN*, SDIR, MRD*, and AC0-AC3. The first group of signals (HLDA1, ATEN*, MDEN*, and LDEN*) determine which buses are connected, and the second group of signals (SDIR, MRD*, and AC0-AC3) determines the direction of the buffers' drivers.

All drivers are active for the active buses, and external bus controls are required if selected data bits need to be controlled. For the DRAM interface, the LBE0*-LBE3* signals must be used to ensure that only the valid data bytes are written to the DRAMs during a write cycle. Table 20 outlines bus connections for different bus cycles.

Bus Cycles	From Bus	To Bus	Direction Control
HLDA1 = 0	D	MD	MRD* = 1
ATEN* = 1	MD	D	MRD* = 0
HLDA1 = 0	D	SD	SDIR = 1
ATEN* = 0	SD	D	SDIR = 0
HLDA1 = 1	SD	MD,D	SDIR = 0
			MRD* = 1
	MD	SD	SDIR = 1
			MRD* = 0
	D	SD	SDIR = 1
			MRD* = 1
			LDEN* = 0

Table 20. Bus Control Definitions.

Data Conversion

The data buffers provide the data bus connections so that data conversions are done correctly for CPU accesses to the AT bus. The action code signals AC0-AC3 are used to control how the bus bits are connected between the I/O channel SD bus and the CPU local Bus D or the system memory MD bus. The action code signals are provided by the 82C301 bus controller for CPU-to-AT bus access cycles and are qualified by the ACEN signal. The meanings of the action code signals are given in Table 21.

AC0-AC3	From Bus	To Bus
0	MD,D Bits 0-15	SD Bits 0-15
1	MD,D Bits 8-15	SD Bits 8-15
		SD Bits 0-7
2	MD,D Bits 16-31	SD Bits 0-15
3	MD,D Bits 24-31	SD Bits 8-15
		SD Bits 0-7
4	MD,D Bits 0-31	SD Bits 0-31
5	SD Bits 0-7	MD,D Bits 0-7
6	SD Bits 0-7	MD,D Bits 8-15
7	SD Bits 0-7	MD,D Bits 16-23
8	SD Bits 0-7	MD,D Bits 24-31
9	SD Bits 0-15	MD,D Bits 0-15
A	SD Bits 0-15	MD,D Bits 16-31
B	Reserved	
C	SD Bits 0-31	MD,D Bits 0-31
D	Reserved	
E	Reserved	
F	Reserved	

Table 21. Action Code Definitions.

System I/O (AT) Bus

The Tandy 4000's system I/O (AT) bus is 100% compatible with the IBM AT bus. It has an open-bus structure that allows multiple microprocessors to share system resources. A total of eight expansion slots are available (six AT- and two PC type). Some features of this bus are:

- 24-bit memory addressing
- 8- or 16-bit data accesses
- I/O addressing range of 100 to 3FF hex
- Interrupt and DMA support
- I/O wait state generation

ROM Subsystem

The on-board ROM consists of two EPROM modules, each capable of holding up to 32 kilobytes of data, or 64 kilobytes total. One module contains the even address BIOS code. The other contains the odd address code.

I/O DECODE

82C206 INTEGRATED PERIPHERALS CONTROLLER (IPC)

The 82C206 (U8) is an LSI implementation of the standard peripherals required to implement an IBM AT system board. This device contains the equivalent of:

- Two 8237A DMA controllers
- A 74LS612 mapper
- Two 8259A interrupt controllers
- An 8254 counter/timer
- An MC146818 real-time clock with RAM

The IPC provides all the standard peripherals required for a system board implementation, except the keyboard interface controller.

DMA Controllers. The two DMA controllers are connected in such a way as to provide four channels of DMA (DMA1) for 8-bit transfers and three channels of DMA (DMA2) for 16-bit transfers. (The first 16-bit DMA channel is used for cascading.) The BIOS programs the DMA controllers at power up as follows:

Master Clear issued to both controllers
All eight channels are first set to -
    Single mode select
    Verify transfer
    Autoinitialization disabled
    Address increment select
Then channel 4 is set to cascade mode and enabled.

Mapper. Included as part of the DMA subsystem is the Page Register (DMAPAGE) device, which is used to supplement the DMA and drive the upper address lines when required.

Interrupt Controllers. The IPC provides 16 channels of interrupt, partitioned into two cascaded controllers (INTC1 and INTC2) with eight inputs each. Three of the sixteen channels are connected internally to various devices. The remaining 13 interrupt channels are user-definable. The BIOS programs the interrupt controllers at power up as follows:

Slave Controller - First Interrupt at 70h
Call address interval = 4 bytes
Slave ID = 2
8086/8088 Mode
Normal EOI
Non-buffered mode
Not special fully nested mode
Cascade mode
Edge triggered mode

Master Controller - First interrupt at 08h
Call address interval = 4 bytes
Slave on IRQ2
8086/8088 mode
Normal EOI
Non-buffered mode
Not special fully nested mode
Cascade mode
Edge triggered mode

The Pre-unmasked IRQs at boot time are:

IRQ0 Timer Tick Clock
IRQ1 Keyboard
IRQ2 Cascade for Slave
IRQ6 Floppy Disk
IRQ9 Software redirected to INT 0Ah for old IRQ2
IRQ14 Hard Disk (If Present)

The three internally connected channels are:

- Channel 0 - Counter/Timer Counter 0 Interrupt
- Channel 2 - Cascade to INTC2 (Slave Interrupt Controller)
- Channel 8 - Real-Time Clock Interrupt

Counter/Timer. The counter/timer (CTC) subsystem contains three independent counters: Counters 0, 1, and 2. All three counters are driven from a clock input pin (TMRCLK) that is independent from the other clock inputs to the device.

Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as timekeeping and task-switching.

Counter 1 can be programmed to generate pulses or square waves for use by external devices.

Counter 2 is a full-function counter/timer that has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or a gated rate/pulse generator.

Real-Time Clock. The real-time clock (RTC) subsystem contains a clock/calendar to maintain the real time and date. In addition, it contains 114 bytes of RAM. To keep the clock/calendar and RAM active when the system is turned off, you must connect the device to an external battery. The Tandy 4000 uses a lithium battery attached to the drive tower for this purpose.

Control of Subsystems

Interconnection and control of all the major subsystems is accomplished via a top-level control section. For discussion purposes, this control section is divided into two subsections:

- **Clock and Wait State Control Section**--controls the generation of DMA wait states and the negation of IOCHRDY (if programmed to do so) during CPU access of the device.

- **Top-Level Decoder**--accommodates the 200-plus registers in the IPC and maintains I/O decode compatibility with the IBM AT. The top-level decoder generates enables to the various subsystems. This subsystem also handles control and direction of the XD0-XD7 data buffers.

Top-Level Decoder

The IPC top-level decoder provides eight separate enables to various internal subsystems of the device. The following is a truth table for the top-level decoder:

ACK*	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	Address Range	Selected Device
1	0	0	0	0	0	0	X	X	X	X	000-00F	DMA1
1	0	0	0	0	1	0	0	0	0	X	020-021	INTC1
1	0	0	0	0	1	0	0	0	1	X	022-023	CONFIG
1	0	0	0	1	0	0	0	0	X	X	040-043	CTC
1	0	0	0	1	1	1	0	0	0	1	071	RTC
1	0	0	1	0	0	0	X	X	X	X	080-08F	DMAPAGE
1	0	0	1	0	1	0	0	0	0	X	0A0-0A1	INTC2
1	0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA2
0	X	X	X	X	X	X	X	X	X	X	Disabled	
X	1	X	X	X	X	X	X	X	X	X	Disabled	
X	X	1	X	X	X	X	X	X	X	X	Disabled	

Table 22. Truth Table for Top-Level Decoder.

The enabling of the IPC XD0-XD7 output buffers is also controlled by the top level decoder. The output buffers are enabled whenever an enable is generated to an internal subsystem and the XIOR* signal is asserted.

The decoder is enabled by three signals: ACK*, XA9, and XA8. To enable any internal device, ACK* must be "1" and both XA8 and XA9 must be "0."

The decode scheme employed in the IPC is designed to comply with the IBM AT requirements. If you wish to take advantage of the areas that are unused by inserting additional peripherals in the I/O map, you can do so. The IPC does not respond to the unused address spaces established by the top-level decoder. The extra peripherals can be tied directly to the XD0-XD7 data lines because the IPC output buffers are not enabled unless an internal subsystem is enabled.

Clock and Wait State Control

The clock and wait state control subsystem performs three functions: control of the DMA command length, control of the CPU read or write cycle length, and selection of the DMA clock rate. All these functions are user-selectable by writing to the Configuration Register located at Address 23H.

Writing and reading this register is accomplished by first writing a 01H to Location 22H to select the IPC Configuration Register and then performing either a read or write to Location 23H. The following is a layout of Configuration Register 23H Index 01H. Explanation of the individual bits follows.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
RW1	RW0	16W1	16W0	8W1	8W0	EMR	CLK

RW1-RW0 - When the higher-speed CPUs are accessing the IPC, the cycle can be extended by programming up to four wait states into the Configuration Register. This causes the IPC to assert a not ready condition (LOW) on the signal IOCHRDY whenever a valid decode from the top-level decoder is detected and either signal XIOR* or signal XIOW* is asserted. IOCHRDY will remain low for the number of wait states programmed into Bits 6 and 7 of the Configuration Register.

RW1	RW0	Read/Write Cycle Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Table 23.
Configuration Register Bits 7 and 6.

Wait states are in increments of one SCLK cycle and are not affected by the DMA clock divider.

16W1-16W0 - Wait states can be independently controlled for both 8-bit and 16-bit DMA cycles, using Bits 4 and 5. This allows you to tailor the DMA cycle more closely to the application.

16W1	16W0	16-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Table 24.
Configuration Register Bits 5 and 4.

8W1-8W0 - Wait states can be inserted in 8-bit DMA cycles by programming Bits 2 and 3 in the Configuration Register.

8W1	8W0	8-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Table 25.
Configuration Register Bits 3 and 2.

Further control of the cycle length is available through the use of the IOCHRDY pin on the IPC. During DMA, this pin is used as an input to the wait state generation logic to extend the cycle if necessary. To extend the cycle, the peripheral drives the input low (0). The cycle can then be completed by releasing IOCHRDY and allowing it to return high (1).

EMR - The EMR bit, Bit 1, enables the extended DMA read function. Normally the assertion of DMAMEMR* is delayed one clock cycle later than XIOR*, (I/O bus read), in the IBM AT implementation. This might not be desirable in some systems. Proramming a "1" into Bit 1 starts DMAMEMR* at the same time as XIOR*.

CLK - The CLK bit, Bit 0, allows you to insert a divider between the DMA controller subsystems and the SCLK input pin or to connect the two directly. When Bit 0 contains a "0," the SCLK input is divided by two and is used to drive both the 8-bit and 16-bit DMA subsystems. A "1" in Bit 0 bypasses the divider and causes the IPC to use the SCLK input directly. Whenever the state of Bit 0 is changed, an internal synchronizer controls the actual switching of the clock to prevent a short clock pulse from causing a DMA malfunction.

Configuration Register Defaults

The Configuration Register contents are pre-loaded by reset to an initial value of 0C0H. This value establishes a default that is IBM AT-compatible. The BIOS then programs a value of 040H upon initialization and corresponds to:

Read/Write Cycles	2 wait states
16-Bit DMA Transfers	1 wait state
8-Bit DMA Transfers	1 wait state

DMAMEMR* is delayed one clock cycle later than XIOR*. DMA clock is equal to SCLK/2.

Description of DMA Controller Functions

As previously stated, the equivalent of two 8237A DMA controllers is implemented in the IPC. Each controller is a four-channel DMA device that generates the memory addresses and control signal necessary to transfer information between a peripheral device and memory directly. This allows high-speed information transfer with little CPU intervention.

The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection of the two DMA devices, thereby maintaining IBM AT compatibility.

DMA cycle length control is provided internally in the IPC, allowing independent control for both 8-bit and 16-bit cycles. This is done through the programmable registers, which can extend command signals or insert wait states.

Each DMA channel has a pair of 16-bit counters and a reload register for each counter. The 16-bit counters allow the DMA subsystem to transfer blocks of as many as 65536 words. The register associated with each counter allows the channel to reinitialize without re-programming.

From this point on, the description of the DMA subsystem pertains to both DMA1 and DMA2 unless otherwise specified.

DMA Operation

During normal operation of the IPC, the DMA subsystem will be in one of three conditions:

- Idle
- Program
- Active

In the idle condition, the DMA controller will be executing cycles of only one state. The idle state S1 is the default condition, and the DMA controller remains in this condition unless the device is initialized and one of the DMA requests becomes active or the CPU attempts to access one of the internal registers.

When a DMA request becomes active, the device enters the active condition and issues a hold request to the system. Once in the active condition, the IPC generates the necessary memory addresses and command signals to accomplish a memory-to-I/O, I/O-to-memory, or memory-to-memory transfer.

I/O-to-memory and memory-to-I/O transfers take place in one cycle. Memory-to-memory transfers require two cycles.

During transfers between memory and I/O, data is presented on the system bus by either memory or the requesting device so the transfer is completed in one cycle. Memory-to-memory transfers, on the other hand, require the DMA subsystem to store data from the read operation in an internal register. The contents of this register are then written to memory on the subsequent cycle.

During transfers between memory and I/O, two commands are activated during the same cycle. In a memory-to-I/O transfer, the IPC asserts both DMAMEMR* (DMA memory read) and XIOW* (I/O bus write), allowing data to be transferred directly to the requesting device from memory. Note that the IPC does not latch data from nor drive data out on this type of cycle.

The number of clock cycles required to transfer a word of data can be varied by programming the DMA subsystem or, optionally extended by the peripheral device. During an active cycle, the DMA subsystem will sequence through a series of states. Each state is one DMA clock cycle long, and the number of states in a cycle varies depending on how the device is programmed and what type of cycle is being performed. The states are labeled S0-S4. (See "Active Condition," later in this section, for further explanation of these states.)

Idle Condition

When no device is requesting service, the DMA subsystem is in an idle condition. During this time, the IPC will sample the DREQ input pins every clock cycle. The internal select from the top-level decoder and HLDA are also sampled at the same time to determine whether the CPU is attempting to access the internal registers. When either of the above situations occurs, the DMA subsystem exits the idle condition. Note that the program condition has priority over the active condition because a CPU cycle has already started.

Program Condition

The program condition is entered whenever HLDA is inactive and an internal select is active. The internal select is derived from the top-level decoder described previously. During this time, Address Lines XA0-XA3 become inputs if DMA1 is selected. If DMA2 is selected, XA1-XA4 become inputs. Note that when DMA2 is selected XA0 is ignored. The XA0-XA4 inputs are used to select the DMA controller registers that are to be read or written. The DMA controller register assignments are shown in Tables 26 and 27.

Because of the large number of internal registers in the DMA subsystem, an internal flip-flop is used to supplement the addressing of the Count and Address Registers. This bit is used to select between the high and low bytes of these registers. The flip-flop will toggle each time a read or write occurs to any of the Word Count or Address Registers in the DMA subsystem. This internal flip-flop is cleared by a reset or a Master Clear command and can be set or cleared by the CPU issuing the appropriate command.

DMA Controller #1

Add.	XIOR*	XIOW*	Flip-Flop	Operation
000h	0	1	0	Read CH0 Current Address low byte
000h	0	1	1	Read CH0 Current Address high byte
000h	1	0	0	Write CH0 Base & Current Address low byte
000h	1	0	1	Write CH0 Base & Current Address high byte
001h	0	1	0	Read CH0 Current Word Count low byte
001h	0	1	1	Read CH0 Current Word Count high byte
001h	1	0	0	Write CH0 Base & Current Word Count low byte
001h	1	0	1	Write CH0 Base & Current Word Count high byte
002h	0	1	0	Read CH1 Current Address low byte
002h	0	1	1	Read CH1 Current Address high byte
002h	1	0	0	Write CH1 Base & Current Address low byte
002h	1	0	1	Write CH1 Base & Current Address high byte
003h	0	1	0	Read CH1 Current Word Count low byte
003h	0	1	1	Read CH1 Current Word Count high byte
003h	1	0	0	Write CH1 Base & Current Word Count low byte
003h	1	0	1	Write CH1 Base & Current Word Count high byte
004h	0	1	0	Read CH2 Current Address low byte
004h	0	1	1	Read CH2 Current Address high byte
004h	1	0	0	Write CH2 Base & Current Address low byte
004h	1	0	1	Write CH2 Base & Current Address high byte
005h	0	1	0	Read CH2 Current Word Count low byte
005h	0	1	1	Read CH2 Current Word Count high byte
005h	1	0	0	Write CH2 Base & Current Word count low byte
005h	1	0	1	Write CH2 Base & Current Word count high byte
006h	0	1	0	Read CH3 Current Address low byte
006h	0	1	1	Read CH3 Current Address high byte
006h	1	0	0	Write CH3 Base & Current Address low byte
006h	1	0	1	Write CH3 Base & Current Address high byte
007h	0	1	0	Read CH3 Current Word Count low byte
007h	0	1	1	Read CH3 Current Word Count high byte
007h	1	0	0	Write CH3 Base & Current Word Count low byte
007h	1	0	1	Write CH3 Base & Current Word Count high byte

DMA Controller #1 Continued

Add.	XIOR*	XIOW*	Flip-Flop	Operation
008h	0	1	X	Read Status Register
008h	1	0	X	Write Command Register
009h	0	1	X	Read DMA Request Register
009h	1	0	X	Write DMA Request Register
00Ah	0	1	X	Read Command Register
00Ah	1	0	X	Write single-bit DMA Request Mask Register
00Bh	0	1	X	Read Mode Register
00Bh	1	0	X	Write Mode Register
00Ch	0	1	X	Set byte pointer flip-flop
00Ch	1	0	X	Clear byte pointer flip-flop
00Dh	0	1	X	Read Temporary Register
00Dh	1	0	X	Master clear
00Eh	0	1	X	Clear Mode Register counter
00Eh	1	0	X	Clear all DMA Request Mask Register bits
00Fh	0	1	X	Read all DMA Request Mask Register bits
00Fh	1	0	X	Write all DMA Request Mask Register bits

Table 26. DMA Controller #1 Register Assignments.

DMA Controller #2

Add.	XIOR*	XIOW*	Flip-Flop	Operation
0C0h	0	1	0	Read CH4 Current Address low byte
0C0h	0	1	1	Read CH4 Current Address high byte
0C0h	1	0	0	Write CH4 Base & Current Address low byte
0C0h	1	0	1	Write CH4 Base & Current Address high byte
0C2h	0	1	0	Read CH4 Current Word Count low byte
0C2h	0	1	1	Read CH4 Current Word Count high byte
0C2h	1	0	0	Write CH4 Base & Current Word Count low byte
0C2h	1	0	1	Write CH4 Base & Current Word Count high byte
0C4h	0	1	0	Read CH5 Current Address low byte
0C4h	0	1	1	Read CH5 Current Address high byte
0C4h	1	0	0	Write CH5 Base & Current Address low byte
0C4h	1	0	1	Write CH5 Base & Current Address high byte
0C6h	0	1	0	Read CH5 Current Word Count low byte
0C6h	0	1	1	Read CH5 Current Word Count high byte
0C6h	1	0	0	Write CH5 Base & Current Word Count low byte
0C6h	1	0	1	Write CH5 Base & Current Word Count high byte
0C8h	0	1	0	Read CH6 Current Address low byte
0C8h	0	1	1	Read CH6 Current Address high byte
0C8h	1	0	0	Write CH6 Base & Current Address low byte
0C8h	1	0	1	Write CH6 Base & Current Address high byte
0CAh	0	1	0	Read CH6 Current Word Count low byte
0CAh	0	1	1	Read CH6 Current Word Count high byte
0CAh	1	0	0	Write CH6 Base & Current Word Count low byte
0CAh	1	0	1	Write CH6 Base & Current Word Count high byte

DMA Controller #2 Continued

Add.	XIOR*	XIOW*	Flip-Flop	Operation
0CCh	0	1	0	Read CH7 Current Address low byte
0CCh	0	1	1	Read CH7 Current Address high byte
0CCh	1	0	0	Write CH7 Base & Current Address low byte
0CCh	1	0	1	Write CH7 Base & Current Address high byte
0CEh	0	1	0	Read CH7 Current Word Count low byte
0CEh	0	1	1	Read CH7 Current Word Count high byte
0CEh	1	0	0	Write CH7 Base & Current Word Count low byte
0CEh	1	0	1	Write CH7 Base & Current Word Count high byte
0D0h	0	1	X	Read Status Register
0D0h	1	0	X	Write Command Register
0D2h	0	1	X	Read DMA Request Register
0D2h	1	0	X	Write DMA Request Register
0D4h	0	1	X	Read Command Register
0D4h	1	0	X	Write single-bit DMA Request Mask Register
0D6h	0	1	X	Read Mode Register
0D6h	1	0	X	Write Mode Register
0D8h	0	1	X	Set byte pointer flip-flop
0D8h	1	0	X	Clear byte pointer flip-flop
0DAh	0	1	X	Read Temporary Register
0DAh	1	0	X	Master clear
0DCh	0	1	X	Clear Mode Register counter
0DCh	1	0	X	Clear all DMA Request Mask Register bits
0DEh	0	1	X	Read all DMA Request Mask Register bits
0DEh	1	0	X	Write all DMA Request Mask Register bits

Table 27. DMA Controller #2 Register Assignments.

In the program condition, the DMA subsystem supports several special commands for controlling the device. These commands do not make use of the data bus but are derived from a set of addresses, the internal select, and XIOW* or XIOR* signals. The special commands are: Master Clear, Clear Mask Register, Clear Mode Register Counter, and Set and Clear Byte Pointer Flip-Flop.

The IPC will enable programming whenever HLDA has been inactive for one DMA clock cycle. It is the responsibility of the system to ensure that programming and the HLDA signal are mutually exclusive. Erratic operation of the IPC can occur if a request for service occurs on an unmasked channel that is being programmed. To prevent the IPC from attempting to service a device with a channel that is partially programmed, the channel should be masked or the DMA subsystem disabled.

Active Condition

The IPC DMA subsystem enters the active condition whenever a software request occurs or whenever a DMA request on an unmasked channel occurs. In either case the device must not be in the program condition. The IPC then begins a DMA transfer cycle.

In a read cycle, for example, after receiving a DREQ signal, the IPC issues an HRQ signal to the system. Until an HLDA signal is returned, the DMA subsystem remains in an idle condition. On the next clock cycle, the DMA subsystem exits the idle condition and enters state S0.

During S0, the device resolves priority and issues the DACK signal on the highest-priority channel requesting service. The DMA subsystem then proceeds to state S1 where the multiplexed addresses are output and latched.

State S2 is then entered, at which time the IPC asserts DMAMEMR*. The device then moves into S3, where the XIOW* command signal is asserted. The DMA subsystem remains in S3 until the wait state counter decrements to zero and the IOCHRDY signal is true. Note that at least one additional S3 occurs unless compressed timing is selected.

Once a ready condition is detected, the DMA subsystem enters S4, where both signals are de-asserted. In Burst Mode and Demand Mode, discussed later, subsequent cycles begin in S2 unless the intermediate addresses require updating. In these subsequent cycles, the lower addresses are changed in S2.

The DMA subsystem can be programmed on a channel-by-channel basis to operate in one of four modes:

- Single Transfer Mode
- Block Transfer Mode
- Demand Transfer Mode
- Cascade Mode

Single Transfer Mode

Single Transfer Mode directs the DMA subsystem to execute only one transfer cycle at a time. The DREQ signal must be held active until the DACK signal becomes active. If the DREQ signal is held active throughout the cycle, the IPC de-asserts the HRQ signal and releases the bus once the transfer is complete. After the HLDA signal becomes inactive, the IPC again asserts the HRQ signal and executes another cycle on the same channel unless a request from a higher-priority channel has been received. In the Single Transfer Mode, the CPU is assured of being allowed to execute at least one bus cycle between transfers.

Following each transfer, the word count is decremented and the address is incremented or decremented. When the word count decrements from 0000h to FFFFh, the terminal count bit in the Status Register is set and a T/C (Terminal Count) signal is generated. If the autoinitialization option has been enabled, the channel reinitializes itself. If not, the DMA subsystem sets the DMA request bit mask and suspends transferring on the channel.

Block Transfer Mode

When Block Transfer Mode is selected, the IPC begins transfers in response to either a DREQ signal or a software request and continues until the terminal count (FFFFh) is reached. At that time, the T/C signal is pulsed and the Status Register terminal count bit is set. In Block Transfer Mode, the DREQ signal need only be held active until the DACK signal is asserted. Autoinitialization is optional in this mode also.

Demand Transfer Mode

In Demand Transfer Mode, the DMA subsystem begins transfers in response to the assertion of the DREQ signal and continues until either the terminal count is reached or the DREQ signal becomes inactive.

Demand Transfer Mode is normally used for peripherals that have limited buffering ability. The peripheral can initiate a transfer and continue until its buffer capacity is exhausted. Then, the peripheral can re-establish service by again asserting the DREQ signal. During idle periods between transfers, the CPU is released to operate and can monitor the operation by reading intermediate values from the Base Address, Current Address, Base Word Count, and Current Word Count Registers. Once the DREQ signal is de-asserted, higher-priority channels are allowed to intervene. Reaching terminal count will result in the generation of a T/C signal pulse, the setting of a terminal count bit in the Status Register, and autoinitialization (if enabled).

Cascade Mode

Cascade Mode is used to interconnect multiple DMA controllers, thus extending the number of DMA channels while preserving the priority chain.

In Cascade Mode, the master DMA controller does not generate address or control signals. The DREQ and DACK signals of the master are used to interface the HRQ and HLDA signals of the slave DMA devices. Once the master receives an HLDA signal from the CPU in response to a DREQ signal caused by the HRQ signal from a slave DMA controller, the master DMA controller ignores all inputs except the HLDA signal from the CPU and the DREQ signal on the active channel. This prevents conflicts between the DMA devices.

Channel 0 of DMA2 is internally connected to DMA1 for Cascade Mode. Additional devices can be cascaded to the available channels in either DMA1 or DMA2 since cascading is not limited to two levels of DMA controllers.

When programming cascaded controllers, begin with the device that is actually generating the HRQ signal to the system. (This is normally the first-level device.) Then, proceed to the second-level devices. Reset causes the DACK signal outputs to become active low and places them in the inactive state.

To allow the internal cascade between DMA1 and DMA2 to function correctly, do not modify the active low state of the DACK signal. The IPC has an inverter between the DACK0 signal of DMA2 and the HLDA signal of DMA1, and the first-level device's DMA request mask bits will prevent second-level cascaded devices from generating unwanted hold requests during the initialization process.

DMA Transfers

Four types of transfers are provided in the IPC DMA subsystem:

- **Read Transfers**--move data from memory to an I/O device by generating the memory address and asserting the DMAMEMR* and XIOW* signals during the same cycle.

- **Write Transfers**--move data from an I/O device to memory by generating the memory address and asserting DMAMEMW* and XIOR* signals.

- **Memory to Memory Transfers**--move block of memory from one location to another. DMA channels 0 and 1 may be used as memory to memory channels by setting bit 0 in the Command register. Once programmed the process can be started by either a software or external request to channel 0 of the DMA controller. Channel 0 provides the source block address during the read portion of the cycle and channel 1 provides the address for the write portion of the cycle. During the read cycle, a byte of data is latched into the internal temporary register of the IPC. The contents are then output to the XD0 - XD7 data lones during the write portion of the cycle and written to memory. Channel 0 may also be programmed to maintain the same source address on every cycle by setting bit 1 in the Command register.

- **Verify Transfers**--useful for diagnostics. In these pseudo-transfers, the DMA subsystem will operate as if it is performing a read or write transfer by generating the HRQ signal, addresses, and the DACK signal but will do so without asserting a command signal. Because no transfer actually takes place, the IOCHRDY signal is ignored during verify transfer cycles.

Autoinitialization

Each of the four DMA channel Mode Registers contains a bit that causes the channel to reinitialize after reaching terminal count. During this process, referred to as autoinitialization, the Base Address and Base Word Count Registers, which were originally written by the CPU, are relocated into the Current Address and Current Word Count Registers. Both the Base and Current Registers are loaded during a CPU write cycle.

The Base Registers remain unchanged during DMA active cycles and can only be changed by the CPU. If the channel has been programmed to autoinitialize, the Request Mask bit will not be set upon reaching terminal count. This allows the DMA to continue operation without CPU intervention.

During memory-to-memory transfers, the Word Count Registers of both Channels 0 and 1 must be programmed with the same starting value for full autoinitialization. If Channel 0 reaches terminal count before Channel 1, then Channel 0 reloads the starting address and word count and continues transferring data from the beginning of the source block. If Channel 1 reaches terminal count first, it reloads the current registers, and Channel 0 remains uninitialized.

DREQ Priority

The IPC supports three schemes for establishing DREQ priority. These are fixed priority, specific rotation, and automatic rotation. The default is fixed priority, which assigns priority based on channel position. In this method, Channel 0 is assigned the highest priority. Priority assignment then progresses downward through the channels, in order, with Channel 3 receiving the lowest priority.

When multiple requests occur at the same time, the IPC issues an HRQ signal but does not freeze the priority logic until the HLDA signal is returned. Once the HLDA signal becomes active, the priority logic is frozen and the DACK signal is asserted on the highest requesting channel. Priority is not re-evaluated until the HLDA signal is deactivated.

Address Generation

Eight intermediate bits of the address are multiplexed onto the data lines during active cycles of the DMA. This reduces the number of pins required by the DMA subsystem. During state S1, the intermediate addresses are output on Data Lines XD0-XD7. These addresses are externally latched by U2 and U3, (74ALS373), and used to drive the system address bus.

Because DMA1 is used to transfer 8-bit data and DMA2 is used to transfer 16-bit data, a 1-bit skew occurs in the intermediate address fields. DMA1 will therefore output Addresses A8-A15 on the data bus at this time, whereas DMA2 will output A9-A16. A separate set of latch and enable signals are provided for both DMA1 and DMA2 to accommodate the address skew.

Eight-Bit Cycles. During 8-bit DMA cycles, in which DMA1 is active, the IPC outputs the lower 8 bits of address on XA0-XA7. The intermediate 8 bits of address are output on XD0-XD7, and the ADSTB8 signal is asserted for one DMA clock cycle. The falling edge of the ADSTB8 signal is used to latch the intermediate addresses A8-A15. An enable signal, AEN8, is used to control the output drivers of the external latch (U2). A16-A23 are also generated at this time from a DMA Page Register in the IPC. Note that A16 is output on the XA16 pin of the device.

Sixteen-Bit Cycles. During 16-bit cycles, in which DMA2 is active, the IPC must output the lower 8 bits of the addresses on XA1-XA8. The intermediate addresses (A9-A16) are output on XD0-XD7. Control for a separate latch (U3) is provided by signals ADSTB16 and AEN16. The DMA Page Register now generates A17-A23. During 16-bit DMA transfers, XA0 and XA16 remain inactive.

DMA Page Register. The DMA Page Register is a set of sixteen 8-bit registers in the IPC that are used to generate the high order addresses during DMA cycles. Only eight of the registers are actually used. The remaining eight are included to maintain IBM AT compatibility. With the exception of Channel 0 of DMA2 (which is used for internal cascading to DMA1), each DMA channel has a register associated with it. Assignment of each register is shown in the following table, along with the register's read/write addresses.

Address	Register Function
080h	Unused
081h	8-bit DMA Channel 2 (DACK2)
082h	8-bit DMA Channel 3 (DACK3)
083h	8-bit DMA Channel 1 (DACK1)
084h	Unused
085h	Unused
086h	Unused
087h	8-bit DMA Channel 0 (DACK 0)
088h	Unused
089h	16-bit DMA Channel 2 (DACK6)
08Ah	16-bit DMA Channel 3 (DACK7)
08Bh	16-bit DMA Channel 1 (DACK5)
08Ch	Unused
08Dh	Unused
08Eh	Unused
08Fh	Refresh Cycle

Table 28. DMA Address Extension Register Map.

During demand and block transfers, the IPC generates multiple sequential transfers. For most of these transfers, the information in the external address latches remains the same, eliminating the need to be relatched. Because the need to update the latches occurs only when a carry or borrow from the lower 8 bits of the address counter exists, the IPC updates the latch contents only when necessary. Therefore, the IPC executes S1 cycles only when necessary, resulting in an overall through-put improvement.

Compressed Timing

The DMA subsystem in the IPC can be programmed to transfer a word in as few as three DMA clock cycles. The normal DMA cycle consists of three states: S2, S3, and S4. (This assumes Demand or Block Transfer Mode.) Normal transfers require four DMA clock cycles because S3 is executed twice because of the one wait state insertion.

In systems capable of supporting higher through-put, the IPC can be programmed to omit one S3 and assert both commands in S2. S2 begins the cycle by generating the address and asserting both commands. One S3 cycle is executed, and the cycle terminates in S4. If compressed timing is selected, the T/C signal will be output in S2, and S1 cycles will be executed as necessary to update the address latch.

Compressed timing is not allowed for memory-to-memory transfers.

Description of Registers

Current Address Register

Each DMA channel has a 16-bit Current Address Register that holds the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes. If autoinitialization is selected, the register is reloaded from the Base Address Register upon reaching terminal count in the Current Word Count Register. Channel 0 can be prevented from incrementing or decrementing by setting the Address Hold bit in the Command Register.

Current Word Count Register

Each DMA channel also has a Current Word Count Register, which determines the number of transfers to perform. The actual number of transfers performed is one greater than the value programmed into the register. The register is decremented after each transfer until it goes from zero to FFFFh. When this roll-over occurs, the IPC generates the T/C signal. Then, it either suspends operation on that channel and sets the appropriate Request Mask bit or it autoinitializes and continues.

Base Address Register

Associated with each Current Address Register is a Base Address Register. This is a write-only register that is loaded by the CPU when writing to the Current Address Register.

The purpose of the Base Address Register is to store the initial value of the Current Address Register for autoinitialization. The contents of the Base Address Register are loaded into the Current Address Register whenever terminal count is reached and the Autoinitiaization bit is set.

Base Word Count Register

The Base Word Count Register preserves the initial value of the Current Word Count Register. It is also a write-only register that is loaded by writing to the Current Word Count Register. The Base Word Count Register is loaded into the Current Word Count Register during autoinitialization.

Command Register

The Command Register controls the overall operation of the DMA subsystem. This register can be read or written by the CPU and is cleared by either a reset or a Master Clear command. The format and explanation of this register are as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
DAK	DRQ	EW	RP	CT	CD	AH	M-M

DAK - Bit 7 determines the DACK signal level. Programming a 1 in this bit position makes the DACK signal an active high signal.

DRQ - Bit 6 determines the DREQ signal active level. Writing a 1 in this bit position causes the DREQ signal to become active low.

EW - Extended write is enabled by writing a 1 to Bit 5, causing the write commands to be asserted one DMA cycle earlier during a transfer. The read and write commands both begin in state S2 when enabled.

RP - Writing a 1 to Bit 4 causes the IPC to use a rotating priority scheme for honoring DMA requests. The default condition (0) is fixed priority.

CT - Writing a 1 to Bit 3 enables compressed timing. The default (0) condition causes the DMA to operate with normal timing.

CD - Bit 2 is the master disable for the DMA controller. Writing a 1 to this location disables the DMA subsystem (DMA1 or DMA2). Disabling is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles from occurring.

AH - Writing a 1 to Bit 1 enables the address hold feature in Channel 0 when performing memory-to-memory transfers.

M-M - Writing a 1 in Bit 0 enables Channels 0 and 1 to be used for memory-to-memory transfers.

Mode Register

Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address.

Bits 0 and 1 of the Write Mode Register determine which channel's Mode Register is written. The remaining six bits control the mode of the selected channel.

Each channel's Mode Register can be read by sequentially reading the Mode Register location. A Clear Mode Register Counter command is provided to allow the CPU to restart the mode read process at a known point. During mode read operations, Bits 0 and 1 will both be a logical 1. The definitions of the Mode Register bits are as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
M1	M0	DEC	AI	TT1	TT0	CS1	CS0

M1-M0 - Mode selection for each channel is accomplished by Bits 6 and 7. The following table shows the definitions.

M1	M0	Mode
0	0	Demand Mode
0	1	Single Cycle Mode
1	0	Block Mode
1	1	Cascade Mode

Table 29. Definition of Mode Selection Bits.

DEC - Determines the direction of the address counter. A 1 in Bit 5 decrements the address after each transfer.

AI - Writing a 1 in Bit 4 enables the autoinitialization function.

TT1-TT0 - Bits 2 and 3 control the type of transfer which is to be performed. The following table gives the definitions:

TT1	TT0	Type
0	0	Verify transfer
0	1	Write transfer
1	0	Read transfer
1	1	Illegal

Table 30. Mode Register Bits 2 and 3 (Transfer Type).

CS1-CS0 - Bits 0 and 1 are the Channel Select bits. They determine which channel's Mode Register will be written. Read back of a Mode Register will result in Bits 0 and 1 being 1's. The following table explains the configuration of Bits 0 and 1.

CS1	CS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Table 31. Mode Register Bits 0 and 1 (Channel Select).

Request Register

The Request Register is a 4-bit register used to generate software requests. (DMA service can be requested either externally or under software control.)

Request Register bits can be set or reset independently by the CPU. The request mask has no effect on software-generated requests. All four bits are read in one operation and appear in the lower four bits of the byte. Bits 4-7 are read as 1's. All four request bits are cleared to zero by reset. The following table gives an explanation of the Request Register:

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
X	X	X	X	X	RB	RSl	RS0

RB - Writing a 1 to Bit 2 sets the Request bit. Bits 0 and 1 select the bit (channel) to be manipulated.

RSl-RS0 - Bits 0 and 1 determine which channel's Mode Register will be written. Read back of the Mode Register will result in Bits 0 and 1 both being 1's. The following is a table of channel selection:

RSl	RS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Table 32.
Request Register Write Operations.

The format for a Request Register read operation is as follows.

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
1	1	1	1	RC3	RC2	RCl	RC0

RC3-RC0 - During a Request Register read, the state of the Request bit associated with each channel is returned in Bits 0-3 of the byte. The bit position corresponds to the channel number.

Request Mask Register

The Request Mask Register is a set of four bits that are used to inhibit external DMA requests from generating transfer cycles. This register can be programmed in two ways. Each channel can be independently masked by writing to the Write Single Mask Bit location. The data format for this operation is as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
X	X	X	X	X	MB	MSl	MS0

MB - Bit 2 sets or resets the Request Mask bit for the channel selected by Bits 0 and 1 (MS0 and MSl). Writing a 1 to Bit 2 sets the mask, inhibiting external requests.

MSl-MS0 - Bits 0 and 1 select the specific mask bit to be set or reset. The following table explains the bit configurations:

MSl	MS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Table 33. Request Mask Register Bits 0 and 1 (Mask Bit Selection).

Alternatively, all four mask bits (Bits 0-3) can be programmed in one operation by writing to the Write All Mask Bits address. Data format for this and the Read All Mask Bits function is shown below.

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
X	X	X	X	MB3	MB2	MBl	MB0

MB3-MB0 - Each bit position in the field represents the mask bit of a channel. The mask bit number corresponds to the channel number associated with the mask bit.

All four mask bits are set following a reset or a Master Clear command. Individual channel mask bits will be set as a result of terminal count being reached if autoinitialize is disabled. The entire register can be cleared, enabling all four channels, by performing a Clear Mask Register operation.

Status Register

The status of all four channels can be determined by reading the Status Register. Information is available to determine whether a channel has reached terminal count and whether an external service request is pending.

Bits 0-3 of this register are cleared by a reset, a Master Clear command, or each time a status read takes place. Bits 4-7 are cleared by a reset, a Master Clear command, or the pending request being de-asserted. Bits 4-7 are not affected by the state of the Mask Register bits. The channel number corresponds to the bit position.

The Status Register is a read-only register. It conforms to the following format:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
DRQ3	DRQ2	DRQ1	DRQ0	TC3	TC2	TC1	TC0

Special Commands

Five special commands are provided to make the task of programming the device easier.

These commands are activated as a result of a specific address and assertion of an XIOR* or XIOW* signal. Information on the data lines is ignored by the IPC whenever an XIOW* signal activated command is issued; thus, data returned on XIOR* signal activated commands is invalid.

Clear Byte Pointer Flip-Flop--initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence. This command is normally executed prior to reading or writing an Address or Word Count Register.

Set Byte Pointer Flip-Flop--allows the CPU to adjust the pointer to the high byte of an Address or Word Count Register.

Master Clear--has the same effect as a hardware reset (clears the Command Register, Status Register, Request Register, Temporary Register, Mode Register counter, and byte pointer flip-flop; sets the Request Mask Register). Immediately following a Master Clear or a reset, the DMA will be in the idle condition.

Clear Request Mask Register--enables all four DMA channels to accept requests by clearing the mask bits in the register.

Clear Mode Register Counter--clears the additional counter, which is used to allow access to the four Mode Registers while only using one address. After clearing the counter, you can read all four Mode Registers by doing successive reads to the Read Mode Register address. The registers are read in order from Channel 0 to Channel 3.

Interrupt Controller

Overview

Two interrupt controllers, INTC1 and INTC2, are included in the IPC. Each of the controllers is equivalent to an 8259A device operating in iAPX86 Mode.

The two devices are connected and must be programmed to operate in Cascade Mode for proper operation of all 16 interrupt channels.

INTC1 is located at Addresses 020h-021h and is configured for master operation in Cascade Mode. INTC2 is a slave device and is located at Addresses 0A0h-0A1h.

The interrupt request output signal from INTC2 (INT) is internally connected to the Interrupt Request Input Channel 2 (IR2) of INTC1. The address decoding and cascade interconnection matches that of the IBM AT.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of Timer 0 in the counter/timer subsystem is connected to Channel 0 (IR0) of INTC1. Interrupt request from the real-time clock is connected to Channel 0 (IR0) of INTC2.

Unless otherwise noted, the following descriptions of the interrupt subsystems pertain to both INTC1 and INTC2. Wherever register addresses are used, the address for the INTC1 register is listed first and the address for the INTC2 register follows, in parentheses. Example: 020h (0A0h).

Controller Operation

The Interrupt Request Register (IRR) is used to store requests from all the channels that are requesting service. The IRR bits are labeled using the channel names IR7-IR0.

The In-Service Register (ISR) contains all the channels that are currently being serviced. The ISR bits are labeled IS7-IS0, corresponding to IR7-IR0.

The Interrupt Mask Register (IMR) allows the CPU to disable any or all of the interrupt channels.

The interrupt controller's priority resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the In-Service Register.

During interrupt acknowledge (INTA) cycles, a master controller outputs a code to the slave device. This code is compared in the cascade buffer/comparator with a 3-bit ID code previously written. If a match occurs in the slave controller, the controller generates an interrupt vector. The contents of the Vector Register are used to provide the CPU with an interrupt vector during INTA cycles.

Interrupt Sequence

The IPC allows the CPU to perform an indirect jump to a service routine in response to a interrupt request for service from a peripheral device. The indirect jump is based on a vector provided by the IPC on the second of two CPU-generated INTA cycles. (The first INTA cycle is used for resolving priority, and the second cycle is for transferring the vector to the CPU.)

The following events occur during an interrupt sequence:

1. One or more of the interrupt requests (IR7-IR0) becomes active, setting the corresponding Interrupt Request Register bit(s).

2. The interrupt controller resolves priority (based on the state of the IRR, IMR, and ISR registers) and asserts the INTR signal (if appropriate).

3. The CPU accepts the interrupt and responds with the INTA cycle.

4. During the first INTA cycle, the highest-priority ISR bit is set and the corresponding IRR bit is reset. The internal cascade address is generated, and the XD7-XD0 outputs remain tri-stated.

5. The CPU executes a second INTA cycle, during which the IPC drives an 8-bit vector onto the data pins XD7-XD0, which is in turn latched by the CPU. The format of this vector is:

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	V7	V6	V5	V4	V3	1	1	1
IR6	V7	V6	V5	V4	V3	1	1	0
IR5	V7	V6	V5	V4	V3	1	0	1
IR4	V7	V6	V5	V4	V3	1	0	0
IR3	V7	V6	V5	V4	V3	0	1	1
IR2	V7	V6	V5	V4	V3	0	1	0
IR1	V7	V6	V5	V4	V3	0	0	1
IR0	V7	V6	V5	V4	V3	0	0	0

Table 34. Interrupt Vector Byte.

Note that V7-V3 are programmable by writing to Initialization Control Word 2. This will be covered later in the section.

6. At the end of the second INTA cycle, the ISR bit will be cleared if the Automatic End of Interrupt Mode is selected. (This mode is covered later in this section.) Otherwise, the ISR must be cleared by an End Of Interrupt (EOI) command from the CPU at the end of the interrupt service routine.

If there is no interrupt request at the beginning of the first INTA cycle, INTCl issues an interrupt level 7 during the second INTA cycle.

The following table defines the interrupt request sources:

Controller	Channel No.	Interrupt Request Source
INTC1	IR0	IRQ0 - Counter/Timer Out0
INTC1	IR1	IRQ1 - Keyboard
INTC1	IR2	IRQ2 - INTC2 Cascade Interrupt
INTC1	IR3	IRQ3 - Serial Port 2
INTC1	IR4	IRQ4 - Serial Port 1
INTC1	IR5	IRQ5 - Parallel Port 2
INTC1	IR6	IRQ6 - Diskette Controller
INTC1	IR7	IRQ7 - Parallel Port 1
INTC2	IR0	IRQ8 - Real-Time Clock IRQ
INTC2	IR1	IRQ9 - Software Redirected to IRQ2
INTC2	IR2	IRQ10 - Reserved
INTC2	IR3	IRQ11 - Reserved
INTC2	IR4	IRQ12 - Reserved
INTC2	IR5	IRQ13 - Co-Processor Interrupt
INTC2	IR6	IRQ14 - Hard Disk Controller
INTC2	IR7	IRQ15 - Reserved

Table 35. Interrupt Request Sources.

End Of Interrupt

An EOI is defined as a condition that causes an In Service Register bit to be reset. To define the ISR bit to reset, you can either use a CPU command (for a specific EOI) or you can instruct the priority resolver to clear the highest-priority ISR bit (for a non-specific EOI).

In modes that do not alter the fully nested structure, a non-specific EOI is sufficient. The IPC can determine the correct ISR bit to reset because the highest-priority ISR bit is necessarily the last level acknowledged and serviced.

In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine.

An ISR bit that is masked, in Special Mask Mode by an Interrupt Mask Register bit, will not be cleared by a non-specific EOI command. The interrupt controller can optionally generate an Automatic End Of Interrupt (AEOI) on the trailing edge of the second INTA cycle.

Priority Assignment

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 the lowest, and priority assignment is fixed (Fixed Priority Mode).

Priority assignment can be rotated either manually (Specific Rotation Mode) or automatically (Automatic Rotation Mode) by programming the Operational Command Word 2 (OCW2) Register.

Fixed Priority Mode

Fixed Priority Mode is the default condition. It exists unless rotation, either manual or automatic, is enabled or the controller is programmed for Polled Mode. In Fixed Priority Mode, interrupts are fully nested with priority assigned as shown below:

Priority:	Lowest						Highest
Interrupt:	7	6	5	4	3	2	1	0

Nesting allows interrupts of a higher priority to generate interrupt requests prior to the completion of the interrupt in service. When an interrupt is acknowledged, the following events occur:

1. Priority is resolved.

2. The vector of the highest-priority request is placed on the bus.

3. The In Service Register bit for that channel is set. This ISR bit remains set until an EOI is issued to that channel.

As long as the ISR bit is set, all interrupts of equal or lower priority are inhibited. A higher-priority interrupt that occurs during an interrupt service routine will be acknowledged only if the CPU has internally re-enabled interrupts.

Specific Rotation Mode

Specific rotation allows the system software to re-assign priority levels by issuing a command that redefines the highest-priority channel. The following is an example of specific rotation when a command is issued with Channel 5 selected.

Before Rotation

Priority:	Lowest						Highest	
Interrupt:	7	6	5	4	3	2	1	0

After Rotation

Priority:	Lowest						Highest	
Interrupt:	5	4	3	2	1	0	7	6

Automatic Rotation Mode

In applications in which a number of equal-priority peripherals are requesting interrupts, you can use automatic rotation to equalize the priority assignment. In Automatic Rotation Mode, a peripheral, after being serviced, is assigned the lowest priority. All peripherals connected to the controller are serviced at least once in eight interrupt requests to the CPU from the controller.

Automatic rotation will occur, if enabled, as a result of an EOI (automatic or CPU-generated). The following is an example of automatic rotation in which IR4 is the highest-priority request being serviced.

Before Rotation

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	1	0	0	0	0

Priority:	Lowest						Highest	
Interrupt:	7	6	5	4	3	2	1	0

After Rotation (IR4 Service Completed)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	0	0	0	0	0

Priority:	Lowest						Highest	
Interrupt:	4	3	2	1	0	7	6	5

Programming the Interrupt Controller

Two types of commands are used to control the IPC interrupt controllers: initialization command words (ICWs) and operational command words (OCWs).

Initialization Command Words

The initialization process consists of writing a sequence of four bytes to each interrupt controller. The initialization sequence is started by writing the first initialization command word (ICW1) to Address 020h (0A0h) with a 1 on Bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1. Resets the Initialization Command Word Counter to 0.
2. Latches ICW1 to the device.
3. Selects Fixed Priority Mode.
4. Assigns IR7 the highest priority.
5. Clears the Interrupt Mask Register.
6. Sets the Slave Mode address to 7.
7. Disables Special Mask Mode.
8. Selects the Interrupt Request Register for status read operations.

The next three I/O writes to Address 021h (0A1h) will load ICW2-ICW4. (All four bytes must be written for the controller to be properly initialized.) The initialization sequence can be terminated at any point by writing to Address 020h (0A0h) with a 0 in Data Bit 4. Note that this will allow OCW2 or OCW3 to be written.

Registers ICW1-ICW4 are write-only registers in the following formats:

ICW1 - Address 020h (0A0h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	SI	LTM	X	SM	X

SI - Bit 4 indicates to the interrupt controller that an initialization sequence is starting. This bit must be a 1 to write ICW1.

LTM - Bit 3 selects level or edge-triggered inputs to the IRR. If a 1 is written to LTM, a high level on the IRR input will generate an interrupt request. To generate the proper interrupt vector, the interrupt request must be active until the first INTA cycle is started. (An IR7 vector is generated if the IRR input is de-asserted early.) The interrupt request must be removed prior to EOI to prevent a second interrupt from occurring.

SM - Bit 1 selects between Single Mode and Cascade Mode. Single Mode is used when only one interrupt controller (INTC1) is used. Therefore, it is not recommended for use with the 82C206.

Cascade Mode allows the two interrupt controllers to be connected through IR2 of INTC1. INTC1 allows INTC2 to generate its own interrupt vectors if Cascade Mode is selected and the highest-priority interrupt request pending is from an INTC2 input. INTC1 and INTC2 must be programmed for Cascade Mode for both controllers to operate.

ICW2 - Address 021h (0A1h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
V7	V6	V5	V4	V3	X	X	X

V7-V3 - These bits are the upper five bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the priority resolver during INTA. (See Table 34, earlier in the section.) INTC1 and INTC2 need not be programmed with the same value in ICW2.

ICW3 Format for INTC1 - Address 021h

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
S7	S6	S5	S4	S3	S2	S1	S0

S7-S0 - These bits determine which interrupt requests have Slave Mode controllers connected. ICW3 in INTC1 must be written with a 04h for INTC2 to function.

ICW3 Format for INTC2 - Address 0A1h

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
0	0	0	0	0	ID2	ID1	ID0

ID2-ID0 - These bits determine which Slave Mode address the controller will respond to during the cascaded INTA sequence. ICW3 in INTC2 should be written with a 02h for Cascade Mode operation. Note that Bits 3-7 should be 0.

ICW4 - Address 021h (0A1h)

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
X	X	X	EMI	X	X	AEOI	X

EMI- Bit 4 will enable multiple interrupts from the same channel in Fixed Priority Mode. This allows INTC2 to fully nest interrupts when Cascade Mode and Fixed Priority Mode are both selected, without INTC2 being blocked by INTCl. Correct handling of this mode requires the CPU to issue a non-specific EOI command to INTC2 and to check its In-Service Register for zero when exiting an interrupt service routine. If a zero value exists, a non-specific EOI command should be sent to INTCl. If not, no command is issued.

AEOI - Auto EOI (AEOI) is enabled when ICW4 is written with a 0 in Bit 1. The interrupt controller performs a non-specific EOI on the trailing edge of the second INTA cycle. Do not use AEOI in a device with fully nested interrupts unless the device is a cascade master.

Operational Command Words

Operational command words (OCWs) allow the IPC interrupt controllers to be controlled or reconfigured at any time while operating. Each interrupt has three operational command words that can be programmed to affect the proper operating configuration and a Status Register to monitor controller operation.

Operational Command Word 1 (OCW1) is located at Address 021h (0A1h). It can be written any time the controller is not in Initialization Mode. OCW2 and OCW3 are located at Address 020h (0A0h). Writing to Address 020h (0A0h) with a 0 in Bit 4 places the controller in Operational Mode and loads OCW2 (if Data Bit 3 = 0) or OCW3 (if Data Bit 3 = 1). The following format descriptions are for OCW1-OCW3. These registers are read/write registers.

OCW1 - Address 021h (0A1h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
M7	M6	M5	M4	M3	M2	M1	M0

M7-M0 - Bits 0-7 control the state of the Interrupt Mask Register. Each interrupt request can be masked by writing a 1 in the appropriate bit position. (M0 controls IR0, M1 controls IR1, M2 controls IR2, and so on.) Setting an IMR bit has no affect on lower-priority requests. All IMR bits are cleared by writing ICW1.

OCW2 - Address 020h (0A0h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
R	SL	EOI	SI	2/3	L2	L1	L0

R - Bit 7, in conjunction with Bits 5 (EOI) and 6 (SL), selects operational function. Writing a 1 in Bit 7 selects one of the rotation functions. The following table shows the R selections:

R	SL	EOI	Function
1	0	0	Rotate on Auto EOI enable*
1	0	1	Rotate on non-specific EOI
1	1	0	Specific Rotate Command
1	1	1	Rotate on Specific EOI

* **This function is disabled by writing a 0 to all three bit positions.**

Table 36. R Selections.

SL - Bit 6, in conjunction with Bits 7 and Bit 5, selects operational function. Writing a 1 in Bit 6 causes a specific or immediate function to occur. All specific commands require Bits 2-0 (L2-L0) to be valid except for no operation. The following table shows the SL selections:

R	SL	EOI	Function
0	1	0	No operation
0	1	1	Specific EOI command
1	1	0	Specific rotate command
1	1	1	Rotate on specific EOI

Table 37. SL Selections.

EOI - Bit 5, in conjunction with Bits 6 and 7, selects operational function. Writing a 1 in Bit 5 causes a function related to EOI to occur. The following table shows the EOI selections.

R	SL	EOI	Function
0	0	1	Non-specific EOI command
0	1	1	Specific EOI command
1	0	1	Rotate on non-specific EOI
1	1	1	Rotate on Specific EOI

Table 38. EOI Selections.

SI - Writing a 0 in Bit 4 takes the interrupt controller out of Initialization Mode and allows OCW2 and OCW3 to be written.

2/3 - If the I/O write places a 0 in Bit 4 (SI), writing a 0 in Bit 3 (2/3) selects OCW2. Writing a 1 selects OCW3.

L2-L0 - These three bits are internally decoded to select the interrupt channel to be affected by the specific command. L2-L0 must be valid during three of the four specific cycles shown in Table 37. Following is a table that defines the L2-L0 selections:

L2	L1	L0	Interrupt
0	0	0	IR0
0	0	1	IR1
0	1	0	IR2
0	1	1	IR3
1	0	0	IR4
1	0	1	IR5
1	1	0	IR6
1	1	1	IR7

L2-L0 Definitions

OCW3 - Address 020h (0A0h)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	ESMM	SMM	SI	2/3	PM	RR	RIS

ESMM - Writing a 1 in Bit 6 enables the Set/Reset Special Mask Mode function, controlled by Bit 5 (SMM). ESMM allows the other functions on OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

SMM - Writing a 1 to both Bits 5 and 6 enables the Special Mask Mode. Writing a 1 to Bit 6 and a 0 to Bit 5 disables Special Mask Mode. During Special Mask Mode, writing a 1 to any bit position inhibits interrupts. Writing a 0 enables interrupts on the associated channel by causing the priority resolver to ignore the condition of the ISR.

SI - Same as for OCW2.

2/3 - Same as for OCW2.

PM - Writing a 1 to Bit 2 of OCW3 enables Polled Mode, causing the IPC to perform the equivalent of an INTA cycle during the next I/O read operation to the controller. The byte read during this cycle has Bit 7 set if an interrupt is pending. If Bit 7 of the byte is set, the level of the highest pending request is encoded on Bits 2-0. The Interrupt Request Register remains frozen until the read cycle is completed, at which time the PM bit is reset.

RR - When Bit 1 is 1, reading the status port at Address 020h (0A0h) causes the contents of the Interrupt Request Register or In Service Register (determined by Bit 0) to be placed on XD0-XD7. Asserting Bit 2 (PM) forces RR reset.

RIS - Bit 0 selects between the IRR and the ISR registers during status read operations if Bit 1 (RR) is 1.

Timer/Counter

The counter/timer circuit (CTC) in the IPC contains three 16-bit counters (Counters 0-3) that can be programmed to count in binary or binary coded decimal (BCD.) Each counter operates independently of the others and can be programmed as a timer or a counter.

All three counters are driven from a common set of control logic. The control logic decodes control information written to the CTC and provides the control necessary to load, read, configure, and control each counter.

Counter 2 can be operated in any of the following six modes:

Mode 0 - Interrupt on Terminal Count
Mode 1 - Hardware-Retriggerable One-Shot
Mode 2 - Rate Generator
Mode 3 - Square Wave Generator
Mode 4 - Software-Triggered Strobe
Mode 5 - Hardware-Retriggerable Strobe

Counters 0 and 1 can be programmed for all six modes. However, the usefulness of Modes 1 and 5 is limited because of the lack of an external hardware trigger signal.

All three counters are driven from a common clock input pin (TMRCLK) that is independent from other clock inputs to the IPC. Counter 0's output (Out0) is connected to IR0 of INTC1 and can be used as an interrupt to the system for keeping time and task switching. Counter 1 can be programmed to generate pulses or square waves for use by external devices. Counter 2 is a full-function counter/timer. It can be used as an interval timer, a counter, or a gated rate/pulse generator.

Counter Description

Each counter contains the following:

- A Control Register.
- A Status Register.
- A 16-bit counting element (CE).
- A pair of 8-bit counter input latches (CIL,CIH).
- A pair of 8-bit counter output latches (COL,COH).
- A clock input for loading and decrementing the CE.
- A mode-defined GATE input for controlling the counter. (Only Gate 2 is accessible.)
- An OUT signal. (OUT0 is not externally accessible.)

The OUT signal's state and function is controlled by the Counter Mode and the condition of the CE. (See "Mode Definitions," at the end of this section.)

The Control Register stores the mode and command information used to control the counter. This register can be loaded by writing a byte, containing a pointer to the desired counter, to the Write Control Word address (043h). The remaining bits in the byte contain the mode, the type of command, and the count format information.

The Status Register allows the software to monitor counter condition and read back the contents of the Control Register.

The CE is a loadable 16-bit synchronous down counter. It is loaded or decremented on the falling edge of the TMRCLK signal. It contains the maximum count when a 0 is loaded, which is equivalent to 65536 in binary operation or 10000 in BCD. The CE does not stop when it reaches 0. In Modes 2 and 3, the CE will be reloaded when it reaches 0. In all other modes, it will wrap around to FFFF in binary operation or 9999 in BCD.

The CE is indirectly loaded by writing one or two bytes (optional) to the counter input latches. The latches are in turn loaded into the CE. This allows the CE to be loaded or reloaded in one TMRCLK cycle.

The CE is also read indirectly by reading the contents of the counter output latches. COL and COH are transparent latches that can be read while transparent or latched. (See "Latch Counter Command," later in this section.)

Programming the CTC

After power-up, the condition of the CTC Control Registers, the Counter Registers, the CE, and the output of all counters is undefined. Each counter must be programmed before it can be used. This is either done by the BIOS or by the software application.

Counters are programmed by writing a control word and then an initial count. The Control Register of a counter is written by writing to the Control Word address. The Control Register is a write-only location. The following table shows the addresses and format of the control words and the Control Word Register.

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
F3	F2	Fl	F0	M2	Ml	M0	BCD

Address	Function
040h	Counter 0 Read/Write
041h	Counter 1 Read/Write
042h	Counter 2 Read/Write
043h	Control Register Write Only

Table 39. Control Word Addresses.

Control Word (043h)

F3-F0 - Bits 7-4 determine the command to be performed. The following table lists the available commands.

F3	F2	F1	F0	Command
0	0	0	0	Latch Counter 0 (See "Counter Latch Command")
0	0	0	1	Read/Write Counter 0 LSB Only
0	0	1	0	Read/Write Counter 0 MSB Only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1 (See "Counter Latch Command")
0	1	0	1	Read/Write Counter 1 LSB Only
0	1	1	0	Read/Write Counter 1 MSB Only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2 (See "Counter Latch Command")
1	0	0	1	Read/Write Counter 2 LSB Only
1	0	1	0	Read/Write Counter 2 MSB Only
1	0	1	1	Read/Write Counter 2 LSB then MSB
1	1	X	X	Read Back Command (See "Read Back Command")

Table 40. Counter Commands.

M2-M0-Bits 3-1 determine the counter's mode during a Read/Write Counter command or select the counter during a Read Back command. (See the specific commands, later in this section.) Bits 3-1 become "don't care" during Latch Counter commands.

BCD - Bit 0 selects the binary coded decimal counting format during Read/Write Counter commands. During a a Read Back command, this bit must be a 0.

Read/Write Counter Command

When writing to a counter, observe the following conventions:

- Write each counter's control word before writing the initial count.
- When writing the initial count, follow the format specified in the control word (for example, least significant byte only or least significant byte, then most significant byte).

Providing the programming format is observed, a new initial count can be written into the counter at any time after programming without rewriting the control word.

During Read/Write Counter commands, M2-M0 are defined as follows:

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
X	1	0	Select Mode 2
X	1	1	Select Mode 3
1	1	0	Select Mode 4
1	1	1	Select Mode 5

Table 41. Mode Select.

Latch Counter Command

When a Latch Counter command is issued, the counter's output latches (COL,COH) latch the current state of the CE. COL and COH remain latched until read by the CPU or until the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition, the latches are enabled and the contents of the CE can be read directly.

It is possible to issue Latch Counter commands to multiple counters before reading the first counter to which a command was issued. However, multiple Latch Counter commands issued to the same counter without reading the counter will cause all but the first command to be ignored.

Read Back Command

The Read Back command allows you to check the count value, mode, and state of the OUT signal, and the Null Count Flag of the selected counter(s). The format for the Read Back command is as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
1	1	LC	LS	C2	Cl	C0	0

LC - Writing a 0 in Bit 5 causes the selected counter(s) to latch the state of the CE in COL and COH.

LS - Writing a 0 in Bit 4 causes the selected counter(s) to latch the current condition of its Control Register, null count, and output into the Status Register. The next read of the counter causes the contents of the Status Register to be read. (See "Status Read," later in the section.)

C2-C0 - Writing a 1 in Bit 3 causes Counter 3 to latch one or both of the registers specified by LC and LS. The same is true for Bits 2 and 1, except that they enable Counters 1 and 0, respectively.

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed.

If LS=LC=0, status is returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter cause the count to be returned.

Status Byte

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
OUT	NC	Fl	F0	M2	Ml	M0	BCD

OUT - Bit 7 contains the state of the counter's OUT signal.

NC - Bit 6 contains the condition of the Null Count Flag. This flag is used to indicate that the contents of the CE are valid. NC will be set to a 1 during a write to the Control Register or the counter. NC is cleared to a 0 whenever the counter is loaded from the Counter Input Registers.

Fl-F0 - Bits 5 and 4 contain the Fl and F0 command bits that were written to the Command Register of the counter during initialization. This information is useful in determining whether the high byte, the low byte, or both must be transferred during counter read/write operations.

M2-M1 - Bits 2 amd 1 reflect the mode of the counter and are interpreted in the same manner as in Write Command operations.

BCD - Bit 0 indicates that the CE is operating in BCD format.

Counter Operation

Because of the previously stated restrictions in Counter 0 and Counter 1, Counter 2 will be used as the example in describing counter operation. However, the descriptions of Modes 0, 2, 3 and 4 are relevant to all three counters.

The following terms are defined for describing CTC operation:

- **TMRCLK Pulse**--A rising edge followed by a falling edge of the IPC TMRCLK input.
- **Trigger**--The rising edge of the GATE2 input signal.
- **Counter Load**--The transfer of the 16-bit value in CIL and CIH to the CE.
- **Initialized**--A control word is written and the counter input latches are loaded.

Counter 2 operates in one of the modes that are described in the following sections.

Mode 0: Interrupt on Terminal Count

Writing the control word causes the OUT2 signal to go low and to remain low until the CE reaches 0. At that time, the signal goes back high and remains high until a new count or control word is written. Counting is enabled when the GATE2 signal is at a logical "1". Disabling the count has no effect on the OUT2 signal.

The CE is loaded with the first TMRCLK pulse after the control word and initial count are loaded. When both CIL and CIH are written, the CE is loaded after CIH is written. This TMRCLK pulse does not decrement the count. Therefore, for an initial count of n, the OUT2 signal does not go high until n + 1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the CE on the next TMRCLK pulse and causes counting to continue from the new count.

If an initial count is written with the GATE2 signal equal to 0, the CE is still loaded on the next TMRCLK pulse. In this case, however, counting does not begin until the GATE2 signal equals 1. The OUT2 signal, therefore, goes high n TMRCLK pulses after the GATE2 signal equals 1.

Mode 1: Hardware-Retriggerable One-Shot

Writing the control word causes the OUT2 signal to go high initially. Once initialized, the counter is armed and a trigger causes the OUT2 signal to go low on the next TMRCLK pulse. The OUT2 signal then remains low until the counter reaches 0. An initial count of n results in a one-shot pulse that is n TMRCLK cycles long.

Any subsequent triggers that occur while the OUT2 signal is low cause the CE to be reloaded, extending the length of the pulse. Writing a new count to CIL and CIH does not affect the current one-shot unless the counter is retriggered.

Mode 2: Rate Generator

Mode 2 functions as a divide-by-n counter, with OUT2 as the carry. Writing the control word during initialization sets the OUT2 signal high.

When the initial count decrements to 1, the OUT2 signal goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high and reloads the CE. Then, the process is repeated. In Mode 2, the counter continues counting (if the GATE2 signal equals 1) and generates an OUT2 pulse every n TMRCLK cycles. A count of 1 is illegal in Mode 2.

When the GATE2 signal goes to 0, it disables counting and forces OUT2 high immediately. A trigger reloads the CE on the next TMRCLK pulse. Thus, GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not affect counter operation unless a trigger is received. Otherwise, the new count is loaded at the end of the current counting cycle.

Mode 3: Square Wave Generator

Mode 3 is similar to Mode 2 in every respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an event count, the duty cycle of OUT2 will be 50%. For odd count values, OUT2 is high one TMRCLK cycle longer than it is low.

Mode 4: Software-Triggered Strobe

Writing the control word causes the OUT2 signal to go high initially. Expiration of the initial count causes the OUT2 signal to go low for one TMRCLK cycle. GATE2=0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. It begins decrementing one TMRCLK pulse later. OUT2 will go low for one TMRCLK cycle, n + 1 cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be retriggered by software.

Mode 5: Hardware-Triggered Strobe

Writing the control word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2=0 disables counting.

The CE is loaded on the TMRCLK pulse after a trigger. Because loading the CE inhibits decrementing, OUT2 will go low for one TMRCLK cycle, n + 1 TMRCLK cycles after the trigger.

If a new count is loaded during counting, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter retriggerable.

GATE2 Definition

In Modes 0, 2, 3, and 4, GATE2 is level-sensitive and is sampled on the rising edge of TMRCLK. In Modes 1, 2, 3, and 5, the GATE2 input is rising-edge sensitive. This rising edge sets an internal flip-flop, the output of which is sampled on the next rising edge of TMRCLK. The flip-flop resets immediately after being sampled. Note that in Modes 2 and 3 the GATE2 input is both edge- and level-sensitive.

The following table describes each channel's control and output. (Note: Channel 1 is programmed as a rate generator to produce a 15-microsecond period signal used for refresh request.)

Channel	Signal Name	Description
0		System Timer
0	Gate 0	Tied active
0	Clk In 0	1.190 MHz Osc
0	Clk Out 0	IRQ0
1		Refresh Request Generator
1	Gate 1	Tied active
1	Clk In 1	1.190 MHz Osc
1	Clk Out 1	REFREQ
2		Speaker Tone Generation
2	Gate 2	Controlled by Bit 0 of Port 061H
2	Clk In 2	1.190 MHz Osc
2	Clk Out 2	Used to drive speaker

Table 42. Channel Control and Output.

Real-Time Clock

This section of the IPC combines a complete time-of-day clock with alarm, 100-year calendar, programmable period interrupt, and 114 bytes of low power static RAM. This section of the device can operate in a battery-powered mode to protect the contents stored in the SRAM and keep the clock functioning.

Register Access

Reading and writing to the 128 locations in the real-time clock is accomplished by first writing the index address out to 070H and then writing the desired data out to 071H. The index addresses for the real-time clock locations are:

Index	Function
00H	Seconds
01H	Seconds alarm
02H	Minutes
03H	Minutes alarm
04H	Hours
05H	Hours alarm
06H	Day of week
07H	Date of month
08H	Month
09H	Year
0AH	Register A
0BH	Register B
0CH	Register C
0DH	Register D
0EH	Diagnostic status byte
0FH	Shutdown status byte
10H	Diskette drive type byte (Drives A and B)
11H	Reserved
12H	Hard disk type byte (Drives C and D) types 1-14
13H	Reserved
14H	Equipment byte
15H	Low base memory byte
16H	High base memory byte
17H	Low expansion memory byte
18H	High expansion memory byte
19H	Disk C extended byte
1AH	Disk D extended byte
1BH-2BH	Reserved
2CH	Bit 0 = swap disk bit
2DH	Reserved
2EH-2FH	2-byte CMOS checksum
30H	Low expansin memory byte
31H	High expansion memory byte
32H	Date century byte
33H	Information flags (set during power on)
34H-7FH	Reserved

Table 43. Index Addresses for the Real-Time Clock Locations.

Time Calendar and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the real-time clock. Initialization of the time, calendar, and alarm information is accomplished by writing to these locations. Information is stored in these locations in binary-coded decimal format.

Before initialization of the internal registers can be performed, the SET bit in Register B should be set to a 1 to prevent real-time clock updates from occurring. The CPU then initializes the first 10 locations in BCD format. The SET bit should then be cleared to allow updates. Once initialized and enabled, the real-time clock will perform clock/calendar updates at a 1Hz rate.

The 24/12 in Register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initialization, the 24/12 bit cannot be changed without reinitializing the hour locations. In 12-hour format, the high order bit of the hour's byte in both the time and alarm bytes will indicate p.m. when it is a "1."

During updates, which occur once per second, the 10 bytes of time, calendar, and alarm information are unavailable to be read or written by the CPU for 2ms. Information read while the real-time clock is performing an update will be undefined. The "Update Cycle" section shows how to avoid update cycle/CPU contention problems.

The alarm bytes can be programmed to generate an interrupt at a specific time or they can be programmed to generate a periodic interrupt. To generate an interrupt at a specific time, you need only program the time that the interrupt is to occur into the three alarm bytes. Alternately, a periodic interrupt can be generated by setting the high order two bits in an alarm register to a "1," which turns that byte into a "don't care" byte. For instance, an interrupt can be generated every hour by programming C0h into Register 5, or it can be generated once a second by programming the same value into all three alarm registers.

Static RAM

The 114 bytes of RAM from Index Addresses 0Eh-7Fh are not affected by the real-time clock. These bytes are accessible during the update cycle and can be used for anything. In the Tandy 4000, these locations are used for nonvolatile configuration storage and calibration parameters because this device is normally battery-powered when the system is turned off.

Control and Status Registers

The IPC contains four registers (A-D) used to control the operation and monitor the status of the real-time clock. These registers are located at Index Addresses 0Ah-0Dh and are accessible by the CPU at all times.

Register A (0Ah)

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
UIP	DV2	DVl	DV0	RS3	RS2	RSl	RS0

Except for UIP, Register A is a read/write register.

UIP - Bit 7 is the Update In Progress flag. It is a status bit used to indicate that an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP goes active (high) 244us prior to the start of an update cycle and remains active for an additional 2ms while the update is taking place. The UIP bit is read-only and is not affected by reset. Writing a "1" to the SET bit in Register B will clear the UIP status bit.

DV0-DV2 - Bits 4-6 are used to control the divider/prescaler on the real-time clock. While the IPC can operate at frequencies higher than 32.768KHz, this is not recommended for battery-powered operation because of the increased power consumption at these higher frequencies. The following table gives the settings for DV0-DV2:

DV2	DVl	DV0	OSCl Frequency	Mode
0	1	0	32.768 KHz	Operate
1	1	X	Reset Divider	

Table 44. Bits 6, 5, and 4 of Register A.

RS0-RS3 - Bits 0-3 control the periodic interrupt rate. The periodic interrupt is derived from the divider/prescaler in the real-time clock and is separate from the alarm interrupt. Both the alarm and the periodic interrupts, however, do use the same interrupt channel in the interrupt controller. Use of the periodic interrupt allows the generation of interrupts at rates higher than once per second. Below are the interrupt rates for which the real-time clock can be programmed:

Rate Selection				Time Base
RS3	RS2	RS1	RS0	32.768 KHz
0	0	0	0	None
0	0	0	1	3.90526ms
0	0	1	0	7.8125ms
0	0	1	1	122.070us
0	1	0	0	244.141us
0	1	0	1	488.281us
0	1	1	0	976.562us
0	1	1	1	1.935125ms
1	0	0	0	3.90625ms
1	0	0	1	7.8125ms
1	0	1	0	15.625ms
1	0	1	1	31.25ms
1	1	0	0	62.5ms
1	1	0	1	125ms
1	1	1	0	250ms
1	1	1	1	500ms

Table 45. Interrupt Rates for Real-Time Clock.

Register B (0Bh)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	0	DM	24/12	DSE

Register B is a read/write register.

SET - Writing a "0" to Bit 7 enables the update cycle and allows the real-time clock to function normally. When Bit 7 is set to a "1," the update cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by the RESET* input signal.

PIE - Bit 6 is the Periodic Interrupt Enable bit. It controls the generation of interrupts based on the value programmed into the RS0-RS3 bits (Bits 0-3) of Register A. This allows you to disable this function without affecting the programmed rate. Writing a "1" to Bit 6 enables the generation of periodic interrupts. Bit 6 is cleared to "0" by RESET*.

AIE - The generation of alarm interrupts is enabled by setting Bit 5 to a "1". Once this bit is enabled, the real-time clock generates an alarm whenever a match occurs between the programmed alarm and clock information. Programming the "don't care" condition into one or more of the Alarm Registers enables the generation of periodic interrupts at rates of 1 second or greater. Bit 5 is cleared by the RESET* signal.

UIE - This read/write bit is used to update the update-end flag bit in Register C. This causes the proper IRQ to be asserted. The RESET* pin going low or the SET bit going high resets the UIE bit.

DM - This bit determines whether the time and calendar updates are to use binary or BCD format. This bit is written or read by the processor program, but not modified by any internal functions or RESET*. A 1 signifies binary data while a 0 specifies BCD data.

24/12 - The 24/12 control bit, Bit 1, is used to establish the format of both hours and hours alarm bytes. If this bit is a "1," the real-time clock interprets and updates the information in these two bytes using the 24-hour mode. This bit can be read or written by the CPU. It is not affected by RESET*.

DSE - The real-time clock can be instructed to handle daylight-saving time changes by setting Bit 0 to a "1." This enables two exceptions to the normal timekeeping sequence to occur. Setting Bit 1 to a "0" disables the execution of these two exceptions. PSRSTB* has no affect on Bit 1.

Register C (0Ch)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

Register C is a read-only register.

IRQF - Bit 7, the Interrupt Request Flag bit, is set to a "1" when any condition that can cause an interrupt is true and the interrupt enable for that condition is true. The condition that causes this bit to be set also generates an interrupt. The logic expression for this flag is as follows:

```
IRQF = PF & PIE or
       AF & AIE or
       UF & UIE
```

This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB* signal. Writing to this register has no affect on the contents.

PF - Bit 6, the Periodic Interrupt flag, is set to a "1" when a transition, which is selected by RS0 - RS3 (Bits 0-3 of Register A), occurs in the divider chain. Bit 6 will become active, independent of the condition of the PIE control bit. The PF bit then generates an interrupt and sets IRQF if PIE is a "1".

AF - A "1" appears in Bit 5, the AF bit, whenever a match has occurred between the Time Registers and the Alarm Registers during an update cycle. This flag is also independent of its enable (AIE) and generates an interrupt if AIE is true.

UF - See "Update Cycle," later in this section.

Register D (0Dh)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

Register D is a read-only register.

VRT - Bit 7, the Valid RAM and Time bit, indicates the condition of the contents of the real-time clock. This bit is cleared to a "0" whenever the PS input signal is low. This pin is normally derived from the power supply that supplies power (Vcc) to the device. It allows you to determine whether the registers have been initialized since power was applied to the device. PSRSTB* has no affect on this bit. This signal can only be set by reading Register D. All unused register bits are "0" when read. They are not writable.

Update Cycle

During normal operation, the real-time clock will perform an update cycle once every second. The performance of an update cycle depends on the divider bits DV0-DV2 not being cleared and the SET bit in Register B being cleared. The function of the update cycle is to increment the Clock/Calendar Registers and compare them to the Alarm Registers. If a match occurs between the two sets of registers, an alarm is issued and an interrupt is issued if the alarm and interrupt control bits are enabled.

During an update, the lower ten registers are unavailable to the CPU. This is done to prevent the possible corruption of data in the registers or the reading of incorrect data. To avoid contention problems between the real-time clock and the CPU, a flag is provided in Register A to alert you of a pending update cycle.

This Update In Process (UIP) bit, Bit 7, is asserted 244us before the actual start of the cycle and is maintained until the cycle is complete. Once the cycle is complete, the UIP bit is cleared and the Update Flag (UF) bit in Register C is set. CPU access is always allowed to Registers A through D during update cycles.

Two methods of reading and writing to the real-time clock are recommended. Both enable you to avoid contention between the CPU and the real-time clock for access to the time and date information:

- The first method is to read Register A, determine the state of the UIP bit and--if it is "0"--perform the read or write operation. For this method to work successfully, the entire read or write operation including any interrupt service routines that might occur must not require more than 244us to complete (from the beginning of the read of Register A to the completion of the last read or write to the Clock/Calendar Registers).

- The second method of accessing the lower ten registers is to read Register C once, disregard the contents, and then continue reading this register until the UF bit is a "1". The UF bit becomes true immediately after an update is completed. You then have until the start of the next update cycle to complete a read or write operation.

Power-Up/Down

Most applications require the real-time clock to remain active whenever the system power is turned off. To accomplish this, an alternate source of power is provided by connecting a battery to the Vcc supply pin of the device. A circuit is provided to switch from system power to batter power in such a way as to eliminate power drain on the battery when the entire IPC is active.

A pin is provided on the device to protect the contents of the real-time clock and reduce power consumption whenever the system is powered down. This pin (PWRGD) should be low whenever the system power supply is not within specifications for proper system operation. To prevent noise on the inactive pins, the PWRGD signal input disables all unnecessary inputs while the system is powered down. PWRGD remains inactive to allow the remainder of the device to operate properly when power is applied to the system.

One pin (PSRSTB) is provided to initialize the device whenever power is applied to the IPC. The PSRSTB pin does not alter the RAM or clock/calendar contents, but it does initialize the necessary Control Register bits. Assertion of the PSRSTB signal disables the generation of interrupts and sets a flag indicating that the contents of the device might not be valid.

Floppy Disk Controller

General Overview

The floppy disk controller resides on the main logic board and is located on the system data bus (SD0-SD15). It is a Western Digital WD37C65 integrated floppy disk control system. It supports two floppy drives through an internal, daisy-chained flat cable.

The controller supports data rates of 250 Kb/s, 300 Kb/s, or 500 Kb/s. High- and low-capacity 5¼-inch and 720K (and 1.44M) 3½-inch floppy disk drives can be used on the same internal controller. The FDC interface uses the DMA (DRQ2-DACK2*) and interrupt request (IRQ6) controls from the system bus. The on-board controller can be strapped to either the primary (3F2-3F7 hex) or the secondary (372-377 hex) FDC port address. The control signals can be disabled through software, allowing two devices to share the same DMA and IRQ channels.

Host Interface

The host interface is the host microprocessor peripheral bus. This bus is composed of eight control signals and eight data lines. In the either the Special or PC/AT Mode, IRQ and DMA requests are tri-stated and qualified by DMA enable, internally provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LS TTL loads. Inputs, except the data bus, are Schmidt Trigger receivers.

During the command or result phase, the Main Status Register must be read by the CPU before each byte of information is written into or read from the Data Register. After each byte is written into or read from the Data Register, the CPU should wait 12us before reading the Main Status Register.

Bits D6 and D7 in the Main Status Register must be "0" and "1," respectively, before each byte of the command word can be written into the FDC. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the FDC.

During the result phase, Bits D6 and D7 in the Main Status Register must both be "1's" before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the FDC is required only in the command and result phases, not during the execution phase.

During the execution phase, the Main Status Register need not be read. If the FDC is in the Non-DMA Mode, the receipt of each data byte from the FDD is indicated by an interrupt signal on Pin 16 (IRQ). The generation of a read signal (RD*) or write signal (WR*) clears the interrupt and outputs the data onto the data bus. If the CPU cannot handle interrupts quickly enough, it might poll the Main Status Register and Bit D7 (RQM) functions as the interrupt signal. If a write command is in process, the WR* signal performs the reset to the interrupt signal.

Note that in the Non-DMA Mode, it is necessary to examine the Main Status Register to determine the cause of the interrupt. It might be a data interrupt or a command interrupt, either normal or abnormal. If the FDC is in the DMA Mode, no interrupt signals are generated during the execution phase. The FDC generates DMA requests when each byte of data is available. The DMA controller responds to these requests with both the DACK* and RD* signal. When the DACK* signal goes low, the DMA Request (DMA) signal is cleared. If a write command has been issued, a WR* signal appears instead of the RD* signal. After the execution phase has been completed, the terminal count has occurred, or the EOT sector has been read or written, an interrupt occurs (IRQ). This signifies the beginning of the result phase. When the first byte of data is read during the result phase, the interrupt is automatically cleared.

The RD* or WR* signals should be asserted while the DACK* is true. The CS* signal is used in conjunction with the RD* and WR* signals as a gating function during programmed I/O operations. CS* has no effect during DMA operations. It is very important to note that in the result phase all bytes must be read. The Read Data command, for example, has several bytes of data in the result phase. All seven bytes must be read to successfully complete the Read Data command. The FDC will not accept a new command until all seven bytes have been read. Other commands might require fewer bytes to be read during the result phase.

The FDC contains five status registers. The Main Status Register, mentioned previously, can be read by the processor at any time. The other four status registers (ST0, ST1, ST2, and ST3) are available only during a result phase and can be read only after completing a command. The particular command that has been executed determines how many status registers are read.

The bytes of data that are sent to the FDC to form the command phase, and those that are read from the FDC in the result phase, must occur in the order shown in the appropriate table (49-63) in the "Commands" section. The command code must be sent first and the other bytes sent in the prescribed sequence.

No foreshortening of the command or result phases is allowed. After the last byte of data in the command phase is sent to the FDC, the execution phase automatically starts. Similarly, when the last byte of data is read out of the result phase, the command ends automatically and the FDC is ready for a new command.

Control Register (3F7h Primary, 377h Secondary)

The Control Register provides support logic that latches the two lsb's of the data bus upon receiving the Load Control Register (LDCR*) and Write (WR*) signals. These bits are used to select the desired data rate, which in turn controls the internal clock generation.

Clock switchover is internally "deglitched," allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the clock or crystal. The frequency must be 64 times the MFM data rate, up to a maximum frequency of 16MHz. This implies a maximum data rate of 250 Kb/s unless the Control Register is used. Bits 0 and 1 are used to set the transfer rate, bits 3-7 are reserved. Table 46 presents the Control Register.

CR1 Bit 0	CR0 Bit 1	DRV Type	Data Rate	Comments	RPM Out
0	0	X	500 Kb/s	MFM	1
0	0	X	250 Kb/s	FM	1
0	1	0	250 Kb/s	MFM	0
0	1	1	300 Kb/s	MFM	0
1	0	X	250 Kb/s	MFM, RST Default	1
1	0	X	125 Kb/s	FM, RST Default	1
1	1	X	125 Kb/s	FM	0

Table 46. Control Register.

Note: Drive type 0 = dual speed, 1 = single speed. Same for RPM bit returned. 0 = dual speed, 1 = single speed.

Main Status Register (3F4h Primary, 374h Secondary)

The Main Status Register is an 8-bit register that contains the status of the FDC. It can be accessed at any time. Only the Master Status Register can be used to facilitate the transfer of data between the processor and FDC.

Bits 6 (DIO) and Bit 7 (RQM) in the Main Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD* or WR* signal during a command or result phase and DIO and RQM getting set is 12us if the 500 Kb/s MFM data rate is selected. The maximum time from the trailing edge of the last RD* in the result phase to CB (FDC Busy) going low is 12us. The locations and functions of the bits in the Main Status Register are as follows:

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
RQM	DIO	EXM	CB	D3B	D2B	DlB	D0B

RQM - When Bit 7 is "1," the Data Register is ready to send data to or receive data from the processor.

DIO - Bit 6 indicates the direction of data transfer between the FDC and the Data Register. A "1" indicates that the transfer is from the register to the processor. A "0" indicates that the transfer is from the processor to the register.

EXM - Bit 5 is set only during the execution phase of Non-DMA Mode. When this bit goes low, it indicates that the execution phase has ended and the result phase has started.

CB - A "1" in Bit 4 indicates that a read or write command is in progress. The FDC will not accept any other command.

D3B - A "1" in Bit 3 indicates that Drive 3 is in the Seek Mode and the FDC will not accept read or write commands.

D2B - A "1" in Bit 2 indicates that Drive 2 is in the Seek Mode and the FDC will not accept read or write commands.

DlB - A "1" in Bit 1 indicates that Drive 1 is in the Seek Mode and the FDC will not accept read or write commands.

D0B - A "1" in Bit 0 indicates that Drive 0 is in the Seek Mode and the FDC will not accept read or write commands.

Status Register 0

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
IC1	IC2	SE	EC	NR	HS	US1	US0

IC1-IC2 - Bits 6 and 7 are Interrupt Code bits. The following table shows their functions:

IC1	IC2	Meaning
0	0	Normal termination of command
0	1	Abnormal termination of command
1	0	Invalid command issued
1	1	Abnormal termination of command because of FDD ready signal changing state

Table 47. Bits 7 and 6 of Status Register 0.

SE - When the FDC completes the SEEK command, the Seek End bit, Bit 5, is set to a "1."

EC - Bit 4, the Equipment Check bit, is set if a fault signal is received from the FDD or if the Track 0 signal fails to occur after 255 step pulses (Recalibrate command).

NR - Drive ready is always presumed true. Therefore, the Not Ready bit, Bit 3, will always be a "0."

HS - Bit 2, the Head Select bit, is used to indicate the state of the head at interrupt.

US1-US0 - Bits 0 and 1 are the Unit Select bits. They are used to indicate the drive unit number at the time of interrupt.

US0	US1	Drive Number
0	0	0
0	1	1

Unit Select Bit Table

Status Register 1

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
EN	X	DE	OR	X	ND	NW	MA

EN - Bit 7, the End of Cylinder bit, is set when the FDC tries to access a sector beyond the final sector of a cylinder.

b6 - Always 0

DE - The Data Error bit, Bit 5, is set if the FDC detects a CRC error in either the ID field or the data field.

OR - Bit 4, the Overrun bit, is set if the FDC is not serviced by the host system during data transfers within a certain time interval.

b3 - Always 0

ND - Bit 3, the No Data bit, is set:

- During the execution of a Read Data, Write Deleted Data, or Scan command if the FDC cannot find the sector specified in the Internal Data Register (IDR)
- During the execution of a Read ID command if the FDC cannot read the ID field without generating an error
- During a Read a Track command if the starting sector cannot be found

NW - The Not Writable bit, Bit 1, is set if the FDC detects a WP* (Write Protect) signal from the FDD during a Write Data, Write Deleted Data, or Format a Track command.

MA - Bit 0 is the Missing Address Mark bit. It is set if the FDC cannot detect the ID address mark after twice encountering the index hole. At the same time, the MD (Missing Address Mark in Data Field) bit in Status Register 2 is set.

Status Register 2

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	CM	DD	WC	SH	SN	BC	MD

b7 - Not used. Bit 7 is always 0.

CM - Bit 6 is the Control Mark bit. It is set during the execution of the Read Data or Scan command if the FDC encounters a sector that contains a Deleted Data Address Mark.

DD - Bit 5, the Data Error bit, is set if the FDC detects a CRC error in the data field.

WC - Bit 4 is the Wrong Cylinder bit. It is set if the contents of the cylinder on the medium are different from that stored in the IDR.

SH - The Scan Equal bit, Bit 3, is set during execution of the Scan command if the condition Equal is satisfied.

SN - Bit 2, the Scan Not bit, is set during the execution of the Scan command if the FDC cannot find a sector on the cylinder that meets the condition.

BC - Bit 1 is the Bad Cylinder bit. It is set when the contents of the cylinder on the medium are different from those stored in the IDR and the contents of the cylinder are FF.

MD - Bit 0 is the Missing Address Mark in Data Field bit. It is set when data is read from the medium and the FDC cannot find an Data Address Mark or Deleted Data Address Mark.

Status Register 3

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	WP*	RY	T0	WP*	HS	US1	US0

b7 - Not used. Bit 7 is always 0.

WP* - Bit 6, the Write Protect bit, is set when write protect status is received from the FDD.

RY - The Ready bit, Bit 5, is always set to logical "1".

T0 - Bit 4 is the Track 0 bit. It is set when the Track 0 signal is received from the FDD.

WP* - Bit 3, the Write Protect bit, is set when write protect status is received from the FDD.

HS - Bit 2 is used to indicate the status of the side select signal from the FDD.

US1 - Bit 1 is used to indicate the status of the unit select signal from the FDD.

US0 - Bit 0 is used to indicate the status of the unit select signal from the FDD.

Data Register (3F5h Primary, 375h Secondary)

The 8-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read from, or written to, the Data Register to program or obtain the results after a particular command.

Operations Register (3F2h Primary, 372h Secondary)

The Operations Register provides support logic that latches the data bus upon receiving the LDOR* and WR* signals. The Operations Register replaces the typical latched port used in floppy subsystems to control disk drive spindle motors and to select the desired disk drive. The following table represents the Operations Register.

msb							lsb
b7	b6	b5	b4	b3	b2	bl	b0
MS	X	MOEN2	MOEN1	DMAEN	SRST*	X	DSEL

b7 - Bit 7 is the Mode Select bit. During a soft reset condition, this bit can be used to select between Special Mode and AT Mode.

b6 - Not used.

MOEN2 - Bit 5 is the Motor On Enable bit, which is the inverted output of MO2*. This bit is only active in AT Mode.

MOEN1 - Bit 4 is the Motor On Enable bit, which is the inverted output of MO1*. This bit is active only in AT Mode.

DMAEN - Bit 3 is the DMA Enable bit, which is active in both the Special and PC/AT Modes. This bit qualifies the DMA and IRQ outputs as well as the DACK* input.

SRST* - Bit 3 indicates a soft reset when it is low.

bl - Not used.

DSEL - Bit 0 is the Drive Select bit. If it is low and MOEN1="1," then DS1 is active. If it is high and MOEN2="1," then DS2 is active. Bit 0 is only used in AT Mode.

Base, Special, and AT Modes

Base Mode

After a hardware reset, the RST signal active, the FDC will be held in soft reset, SRST* signal active, with the normally driven signals and the DMA request and IRQ request outputs tri-stated. Base Mode can be initiated at this time by a chip access by the host. Although the access can be any read or write, it is strongly suggested that the first access be a read of the Main Status Register.

Once Base Mode is entered, the soft reset is released, and IRQ and DMA are driven. Base Mode prohibits the use of the Operations Register. Therefore, there can be no qualifying by the DMAEN signal and no soft resets. The drive select output signals, DS1 to DS4, offer a 1 of 4 decoding of the unit select bits resident in the command structure. The RWC* signal represents reduced write current and indicates when write precompensation is necessary.

Special Mode

Special Mode allows the use of the Operations Register for the DMAEN signal as a qualifier to do a software driven device reset (SRST*). To enter Special Mode, the Operations Register is loaded with 1 X 0 0 X 0 X X, setting Mode Select to "1," which disables MOEN1 and MOEN2 and also causes SRST* to be active. Then, a read of the Control Register address, LDCR* and RD*, sets the device into Special Mode. The DS1 through DS4 signals, as well as the RWC* signal, are again offered in this mode.

AT Mode

For AT compatibility, users will write to the Operations Register, LDOR* and WR*. This action, performed after a hardware reset, or in the Base Mode, initiates AT Mode.

AT Mode can also be entered from Special Mode by loading the Operations Register with 0 X 0 0 X 0 X X, setting Mode S to a logical "0," disabling MOEN1 and MOEN2, and causing SRST* to be active. Then, a read of the Control Register address sets the device in AT Mode.

The DS* outputs are now replaced with the DSEL and MOEN signals buffered from the Operations Register. The RWC* pin is now RPM* so that users with two-speed drives can reduce spindle speed from a nominal 369 RPM to 300 RPM when active low or reduce write current when a slower data rate is selected for a given drive.

Polling Routine

After any reset, either RST or SRST*, US0 and US1 go into a polling routine. In between commands (and in between step pulses in the SEEK command), the FDC polls all four FDDs, looking for a change in the ready line from any of the drives.

Because the drive is always presumed ready, an interrupt is generated only following a reset. This occurs because a reset forces not ready status, which then promptly becomes ready. In Special or AT Mode, if DMAEN is not valid prior to 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus.

The polling of the ready line by the FDC occurs continuously between commands. Each drive is polled every 1.024ms except during read/write commands.

Device Resets

The FDC supports both hardware reset (RST) pin 19, and software reset (SRST*), through the use of the Operations Register.

The RST pin causes a device reset for the active duration, RST causes a default to Base Mode, and default selects 250Kb/s MFM (or 125Kb/s FM code dependent) as the data rate (16MHz input clock).

SRST* resets the microcontroller as does the RST but does not affect the current data rate selection or the mode.

Both RST and SRST*, when active, disable the high current driver outputs to the FDD.

Data Separator

The data separator, built in the WD37C65 FDC, is a WD92C32 Phase Lock Loop Floppy Disk Data Separator (DPLL). It is designed to address high-performance error rates on floppy disk drives and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance.

Write Precompensation

The FDC maintains the standard first-level algorithm to determine when write precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16MHz clock, CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has a 25% duty cycle and is equal to one-half the WCLK period.

When the PCVAL signal is active, all data is precompensated by + or - 125ns, regardless of track number and data rate. However, this is only for MFM encoding. There is no write precompensation for FM. If the PCVAL signal is not active, and if a track inside number 28 is accessed, then + or - 187ns precompensation is generated. When the non-standard data rate using CLK2 is chosen, the MFM precompensation is always two clock cycles. For 9.6MHz, this is + or - 208ns. In this case, the PCVAL signal is disabled.

Clock Generation

This logical block internal to the WD37C65 FDC provides all the clocks needed by the FDC: the sampling clock (SCLK), the write clock (WCLK), and the master clock (MCLK).

SCLK drives the data separator used during data recovery. This clock frequency is always 32 times the selected data rate.

WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency of 2 times the selected data rate.

MCLK is used by the microsequencer. MCLK and MCLK* clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to 8 times the selected MFM data rate or 16 times the FM data rate. The following table presents the clock data rates:

Data Rate	Code	SCLK	MCLK	WCLK
500 Kb/s	MFM	16 MHz	4.0 MHz	1.0 MHz
250 Kb/s	FM	8 MHz	4.0 MHz	500 KHz
250 Kb/s	MFM	8 MHz	2.0 MHz	500 KHz
125 Kb/s	FM	4 MHz	2.0 MHz	250 KHz
300 Kb/s	MFM	9.6 MHz	2.4 MHz	600 KHz

Table 48. Clock Data Rates.

Commands

The FDC is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The result after the execution of the command can also be a multibyte transfer back to the processor.

Command operation consists of three phases:

- **Command Phase**--The FDC receives all information required to perform a particular operation from the processor.
- **Execution Phase**--The FDC performs the operation as instructed.
- **Result Phase**--After completion of the operation, status and other housekeeping information are made available to the processor.

Tables 49-63 provide details about the FDC commands.

Command Symbol Description

Symbol	Name	Description
A0	Address Line 0	Controls selection of Main Status Register (A0=0) or Data Register (A0=1)
C	Cylinder Number	Current selected cylinder number
D	Data	Data pattern to be written into a sector
D7-D0	Data bus	8 bit data bus D0=lsb, D7=msb
DTL	Data Length	When N is 0, DTL stands for the data length to be written into a sector
EOT	End of Track	Final sector number on a cylinder. During read or write operations the FDC will stop data transfer after it reaches a sector number equal to EOT.
GPL	Gap Length	Gap 3 length. During a format command it determines the size of Gap 3.
H	Head Address	Head number, 0 or 1, as specified in the ID field.
HLT	Head Load Time	Head Load Time of FDD from 2-254ms in increments of 2ms.
HS	Head Select	Selected head number 0 or 1.
HUT	Head Unload Time	Head unload time after a read or write operation from 16-240ms in 16ms increments.
MF	FM or MFM	If low, FM mode is selected, if high, MFM mode is selected.

Command Symbol Legend

Symbol	Name	Description
MT	Multitrack	If MT is high, a multitrack operation is performed.
N	Number	Number of data bytes written in a sector.
NCN	New Cylinder Number	The new cylinder number that will be reached after a seek operation.
ND	Non DMA Mode	The operation is performed in the non-DMA mode.
PCN	Present Cylinder Number	The cylinder number at the end of the Sense Interrupt Status command.
R	Record	Sector number which will be read or written.
R/W	Read/Write	Read or Write signal.
SC	Sector	Number of sectors per cylinder.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	Stepping rate for the FDD 1-16ms in 1ms increments.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Stands for one of the four status registers where information is stored after a command is executed.
STP		During scan operations if STP = 1 then contiguous sectors are compared with the data sent, if STP = 2 then alternate sectors are compared.

Command Symbol Legend

Read Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	0	0	1	1	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		Data length							
Execution										Data transfer between FDD (Floppy Disk Drive) and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 49. Read Data Command.

Read Deleted Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	0	1	1	0	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		Data length							
Execution										Data transfer between FDD and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 50. Read Deleted Data Command.

Write Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	0	0	0	1	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		Data length							
Execution										Data transfer between FDD and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 51. Write Data Command.

Write Deleted Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	0	0	1	0	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution. The four bytes are compared with the header on the floppy disk.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		Data length							
Execution										Data transfer between FDD and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 52. Write Deleted Data Command.

Read a Track

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	MF	SK	0	0	0	1	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		Data length							
Execution										Data transfer between FDD and system. FDD reads all data fields from index hole to EOT.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 53. Read a Track Command.

Read ID

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	MF	0	0	1	0	1	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
Execution										The first correct ID information on the cylinder is stored in the Data Register.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 54. Read ID Command.

Format a Track

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	MF	0	0	1	1	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Number of bytes							Bytes per sector.
	W		Number of sectors							Sectors per track.
	W		Gap length							Gap 3.
	W		DT							Filler byte.
Execution										FDC formats the entire track.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 55. Format a Track Command.

Scan Equal

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	1	0	0	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		STP							1 = compare contiguous sectors; 2 = compare alternate sectors.
Execution										Data compared between FDD and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 56. Scan Equal Command.

Scan Low or Equal

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	1	1	0	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W		Cylinder number							Sector ID information prior to command execution.
	W		Head address							
	W		Sector number							
	W		Number of bytes							
	W		Final sector number							
	W		Gap length							
	W		STP							1 = compare contiguous sectors; 2 = compare alternate sectors.
Execution										Data compared between FDD and system.
Results	R		ST0							Status information after command execution.
	R		ST1							
	R		ST2							
	R		Cylinder number							Sector ID information after command execution.
	R		Head address							
	R		Sector number							
	R		Number of bytes							

Table 57. Scan Low or Equal Command.

Scan High or Equal

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	MT	MF	SK	1	1	1	0	1	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
	W	Cylinder number								Sector ID information prior to command execution.
	W	Head address								
	W	Sector number								
	W	Number of bytes								
	W	Final sector number								
	W	Gap length								
	W	STP								1 = compare contiguous sectors; 2 = compare alternate sectors.
Execution										Data compared between FDD and system.
Results	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	Cylinder number								Sector ID information after command execution.
	R	Head address								
	R	Sector number								
	R	Number of bytes								

Table 58. Scan High or Equal Command.

Recalibrate

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	1	1	1	Command codes.
	W	X	X	X	X	X	0	US1	US0	
Execution										Heads retract to Track 0.

Table 59. Recalibrate Command.

Sense Interrupt Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	1	0	0	0	Command codes.
Results	R		ST0							Status information about the FDC at the end of a SEEK operation.
	R		Present cylinder							

Table 60. Sense Interrupt Status Command.

Specify

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	0	1	1	Command codes.
	W	Step rate time, head unload time								
	W	Head load time, Non-DMA Mode								

Table 61. Specify Command.

Sense Drive Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	1	0	0	Command codes.
	W	X	X	X	X	X	HS	US1	US0	
Results	R	ST3								Status information about FDC.

Table 62. Sense Drive Status Command.

Seek

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	1	1	1	1	Command codes.
	W	X	X	X	X	X	0	US1	US0	
	W	New cylinder number								
Execution										Heads positioned to the proper cylinder.

Table 63. Seek Command.

80287 Numeric Processor

The optional 80287 numeric processor is a 40-pin IC that can be used in the available socket (U25) on the main logic board. The optional 80287 receives its input clock from the oscillator Y5, an 8MHz crystal. Chip select and interrupt control for the Numeric Processor and the Weitek are provided by PAL U22. The numeric processor executes mathematical calculations independently, allowing the CPU to perform other tasks. It runs asynchronously to the 80386 and interfaces through the system bus through IRQ13 of the interrupt controller.

Serial/Parallel Interface

The serial/parallel card (standard) is compatible with the IBM AT. The serial portion of the card supports the EIA RS-232C interface standard through a 9-pin male D-shell connector located on the rear of the unit for external chassis access.

The UART, an National Semiconductor NS16450, used on this card is fully programmable and supports asynchronous communications with 5, 6, 7, or 8 character bits; 1, 1.5, or 2 stop bits; with or without parity. The baud-rate generator supports operation from 50 to 9600 baud. A prioritized interrupt scheme controls transmit, receive, error, line status, and data set interrupts.

The Serial portion of the adapter is accessible through Interrupt IR4 for COM1 and IR3 for COM2. The serial port is addressible through I/O port 3F8h-3FFh for COM1 and 2F8h-2FFh for COM2. For a detailed set of instructions and programming information, refer to the NS16450 in the Devices section.

The parallel portion of the board is accessible through Interrupt IR7 for LPT1 and IR5 for LPT2. The following is a table of addresses that can be used in programming the parallel port. The first address is for the primary port and the second is for the secondary port.

0378h (37Ch) Printer - Data Latch

Bit	Description
0	Bit 0 - LSB
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7 - MSB

0379h (37Dh) Printer - Read Status

Bit	Description
0	Not Used
1	Not Used
2	Not Used
3	"0" = Error
4	"1" = Printer Select
5	"1" = Out of Paper
6	"0" = Acknowledge
7	"0" = Busy

Address	Description
037Ah (037Eh)	Printer - Control Latch

Bit	Description
0	"1" = Strobe
1	"1" = Auto FD XT
2	"0" = Initialize
3	"1" = Select Printer
4	"1" = Enable Interrupt
5	Not Used
6	Not Used
7	Not Used

037Bh	Not Used

Keyboard Control

The keyboard controller (U1) is a single-chip microcomputer (Intel 8042) that is programmed to be IBM AT compatible.

The controller receives serial data from the keyboard, checks the parity of the data, translates scan codes, and presents the data to the system as a byte of data in its output buffer, I/O address 060h. The controller will interrupt the CPU on interrupt line IR1 when data is available to be read.

Data is sent to the keyboard by writing to the controller's input buffer, I/O address 064h for issuing a command, and 060h for data. (Status Register bits inform the CPU of any error encountered in receiving the data.) The byte of data is serialized and sent to the keyboard, with odd parity bits automatically inserted. The keyboard acknowledges all data transmissions, and the acknowledgment separates each byte transmitted.

The keyboard sends serial format data to the controller, using an 11-bit frame. (Data sent is synchronized by a keyboard-supplied clock.) The first bit is a start bit. It is followed by 8 data bits, an odd parity bit, and a stop bit. At the end of a transmission, the controller disables the interface until the system accepts the data byte.

For a received byte of data with a parity error, a resend command is sent to the keyboard.

Whenever the controller is unable to receive the data correctly, FF hex is placed in its output buffer, and the parity bit in the Status Register is set to 1.

The controller will also time a byte of data from the keyboard, and if the byte transmission does not end within 2 milliseconds, FF hex is placed in the controller's output buffer, and the receive time-out bit in the Status Register is set. (No retries will be attempted on a receive time-out error).

For scan codes received from the keyboard, the controller converts these codes to system scan codes before they are put into the controller's output buffer.

Data is sent to the keyboard in the same serial format used to receive data from the keyboard. If the keyboard does not start clocking the data out of the controller within 15 milliseconds, or if it completes that clocking within 2 milliseconds, FE hex is placed in the controller's output buffer, and the transmit time-out error bit is set in the Status Register.

If the response contains a parity error, FE hex is placed in the controller's output buffer, and the transmit time-out and parity error bits are set in the Status Register. The controller is programmed to a set time limit for the keyboard to respond. If 25 milliseconds are exceeded, the controller places FE hex in its output buffer and sets the transmit and receive time-out error bits in the Status Register. (No retry is made by the controller for any transmission error.)

The controller also senses the status of the display type jumper E1-E2.

Status Register Bit Definitions

Bit 0, Output Buffer Full - When this bit is a 0 it indicates that the output buffer is empty. A 1 indicates that there is data in the output buffer but the system has not yet read the data. When the system does read the data this bit is returned to a 0.

Bit 1, Input Buffer Full - A 0 in this position means the input buffer at I/O address 60h or 64h is empty. A 1 indicates that data has been written into the buffer but the controller (8042) has not read it yet. When the data is read by the controller this bit returns to a 0.

Bit 2, System Flag - This bit may be set to 0 or 1 by writing to the flag bit in the controller's command byte. It is set to 0 on power up reset.

Bit 3, Command/Data - The input buffer may be addressed as I/O address 60h or 64h. Address 60h is defined as a data port while address 64h is a command port. Writing to address 64h sets this bit to a 1, and writing to address 60h sets it to 0. The controller uses this bit to determine if the byte in the input buffer is a data or command byte.

Bit 4, Inhibit Switch - This bit is updated when data is placed in the output buffer. It reflects the state of the keyboard inhibit switch. A 0 in this bit means the keyboard is inhibited.

Bit 5, Transmit Time Out - A 1 in this bit indicates that a transmit by the keyboard controller was not properly completed. This bit works in conjunction with bits 6 and 7. If the transmit byte was not clocked out in the specified time limit, this will be the only bit set. If the transmit byte was clocked out and a response was not sent within the specified time limit, this bit and the receive time out bit is set. If the transmit byte was sent and a response was received with a parity error, this bit and the parity error bits are set.

Bit 6, Response Time Out - A 1 indicates that a transmission was started by the keyboard but did not finish within the programmed time limit.

Bit 7, Parity Error - A 0 indicates the last byte received from the keyboard had odd parity. A 1 indicates the last byte received had even parity. The keyboard should send data with odd parity.

Keyboard Controller Command Set (I/O Address 64h)

20 -- Read Keyboard Controller's Command Byte The controller sends the current command byte to the output buffer.

60 -- Write Keyboard Controller's Command Byte The next byte of data written to I/O address 60h is put in the controller's command byte. Bit definitions for the command byte are as follows:

Bit 7 - Reserved. Should be a 0.

Bit 6 - IBM Personal Computer Compatibility Mode.
Writing a 1 to this bit causes the controller to convert the scan codes it receives to those used by the IBM Personal Computer.

Bit 5 - IBM Personal Computer Mode.
Writing a 1 to this bit programs the keyboard to support the IBM Personal Computer keyboard interface. The controller will not check parity or convert scan codes.

Bit 4 - Disable Keyboard.
Writing a 1 to this bit disables the keyboard interface by driving the clock line low. Data is not sent or received.

Bit 3 - Inhibit Override.
A 1 in this bit disables the keyboard inhibit function.

Bit 2 - System Flag.
The value written to this bit is put in the system flag bit of the status register.

Bit 1 - Reserved. Should be written to a 0.

Bit 0 - Enable Output Buffer Full Interrupt.
Writing a 1 to this bit causes the controller to generate an interrupt when it places data into the output buffer.

AA -- Self Test Causes the controller to perform internal diagnostics. 55h is placed in the output buffer if no errors are encountered.

AB -- Interface Test Causes the controller to test the clock and data lines. The result is placed in the output buffer as follows:

00 - No error detected
01 - Clock line stuck low
02 - clock line stuck high
03 - data line stuck low
04 - data lone stuck high

AC -- Diagnostic Dump Sends 16 bytes of the controller's RAM, current state of the input port, current state of the output port, and the controller's program status word to the system. All items are sent in scan code format.

AD -- Disable Keyboard Feature This sets bit 4 of the controller's command byte. This disables keyboard interfacing by driving the clock line low. Data will not be sent or received.

AE -- Enable Keyboard Interface This command clears bit 4 of the command byte. This releases the keyboard interface.

C0 -- Read Input Port Tells the controller to read the input port and place the data in the output buffer. This command should be used only if the output buffer is empty.

D0 -- Read Output Port Causes the controller to read the output port and place the contents in the output buffer. This command should only be used if the output buffer is empty.

D1 -- Write Output Port The next byte of data written to I/O address 60h is placed in the output port. Note that bit 0 of the controller's output port is connected to system reset and should not be written low.

E0 -- Read Test Inputs This causes the controller to read it's T0 and T1 inputs. The data is placed in the output buffer with data bit 0 representing T0 and data bit 1 representing T1.

F0-FF -- Pulse Output Port Bits 0-3 of the controllers output port may be pulsed low for approximately 6usec. Bits 0-3 of this command indicate which bits are to be pulsed. A 0 causes the bit to be pulsed, and a 1 causes the bit not to be pulsed. Note that bit 0 of the controller's output port is connected to system reset and should not be written low.

Interface Requirements

System I/O (AT) Bus

This section identifies the I/O interface requirements for both the PC-compatible and AT-compatible option cards. There are eight expansion slots in the Tandy 4000. Two are PC-type slots. Each of these has a 62-position connector. The other six are AT-type slots, each of which has one 62-position connector and one 36-position connector. The last slot is a for a 32-bit memory expansion option. System board power consumption is rated at 3.5 Amps for the +5V supply and 45 mA for the +12V supply, including the FDC. This allows an effective 16.3A available for the +5V and 6.5A total for the +12V on the system I/O bus and disk drive power connectors.

PC Interface Compatiblity

The following pin assignments are used on the 62-position connector found on both the AT- and the PC-type option slots:

Pin	Signal Name	Pin	Signal Name
A1	IOCHCHK*	B1	Ground
A2	SD7	B2	RESETDRV
A3	SD6	B3	+5 V
A4	SD5	B4	IRQ9
A5	SD4	B5	-5 V
A6	SD3	B6	DRQ2
A7	SD2	B7	-12 V
A8	SD1	B8	0WS*
A9	SD0	B9	+12 V
A10	IOCHRDY	B10	Ground
A11	AEN	B11	SMEMW*
A12	SA19	B12	SMEMR*
A13	SA18	B13	IOW*
A14	SA17	B14	IOR*
A15	SA16	B15	DACK3*
A16	SA15	B16	DRQ3
A17	SA14	B17	DACK1*
A18	SA13	B18	DRQ1
A19	SA12	B19	REFRESH*
A20	SA11	B20	SYSCLK*
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	DACK2*
A27	SA4	B27	T/C
A28	SA3	B28	BALE
A29	SA2	B29	+5 V
A30	SA1	B30	OSC
A31	SA0	B31	Ground

Table 64. Pin Assignments for 62-Position Connector.

PC Bus Pin Definitions

The following signal descriptions for the System I/O Bus are for PC and AT bus-compatible option cards. Note that all signal lines are TTL compatible levels and that I/O adapters should be designed with a maximum of two low power Shottky (LS) loads per line.

CLK (B20). CLK is the System clock. It has a 50% duty cycle and is used only for sychronization with the CPU. It is not intended for uses requiring a fixed frequency. It is an 8 MHz signal.

SA0 through SA19 (A12-A31). These lines are 20 address bits used to address memory and I/O devices within the Tandy 4000. They are gated on the system bus when the BALE signal is high and are latched on the falling edge of the BALE signal. Generation of these signals is accomplished by the CPU or a DMA controller. SA0-SA19 are active high.

BALE (B28). BALE is a Buffered Address Latch Enable generated by the CPU Bus Controller. It is used to latch valid addresses from the CPU, and can be used by an I/O board to indicate a valid CPU address, in conjunction with AEN. BALE is pulled to a high state during DMA cycles, which include Refresh cycles. BALE is active high.

AEN (A11). AEN is an Address Enable signal used to remove the CPU and other devices from the bus to allow DMA transfers to take place. During AEN active, the DMA controller has control of the address bus, the data bus, the READ command lines, and the WRITE command lines. AEN is active high.

SD0 through SD7 (A2-A9). These signals are the data bus bits 0 through 7 from the CPU to memory and I/O devices on the bus. SD0 is the least significant bit (lsb), and SD7 is the most significant bit (msb).

RESETDRV (B2). RESETDRV is used to reset or initialize the expansion logic during power-up time, line voltage outage, or when the Reset switch on the front panel is pressed. RESETDRV is active high.

IOCHCHK* (A1). This signal indicates an uncorrectable system error when active. The IOCHCHK* signal provides the system board with parity information about memory or devices on the bus. IOCHCHK* is active low.

IOCHRDY (A10). This signal is used to lengthen I/O or memory cycles when driven low by the active device. (This signal should not be held low more than 15 microseconds.) Any slow device using this line should drive it low immediately upon detecting its valid address and a READ or WRITE command. See the timing diagram for setup times. IOCHRDY is active high (Ready condition).

IRQ9 and IRQ3 through IRQ7 (B4, B21-B25). These signals are used to tell the CPU that an I/O device needs attention. The Interrupt Requests are prioritized with IRQ9 (software redirected to IRQ2) having the highest priority and IRQ7 the lowest. An Interrupt Request is generated when any IRQ signal is driven high and held high until the CPU acknowledges the interrupt.

IOR* (B14). IOR* is a read signal that instructs an I/O device to drive its data onto the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller. IOR* is active low.

IOW* (B13). IOW* is a write signal that instructs an I/O device to read, or latch, the data from the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller. IOW* is active low.

SMEMR* (B12). SMEMR* is a read signal that instructs a memory device to drive its data onto the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller through the CPU Bus Controller. SMEMR* is active only when the memory address is within the first 1 megabyte range (000000-0FFFFFH). SMEMR* is active low.

SMEMW* (B11). SMEMW* is a write signal that instructs a memory device to read, or latch, the data from the data bus (SD0-SD7). This line can be driven by the CPU Bus Controller or by the DMA controller through the CPU Bus Controller. SMEMW* is active only when the memory address is within the first 1 megabyte range (000000-0FFFFFH). SMEMW* is active low.

DRQ1, DRQ2, and DRQ3 (B18, B6, B16). These lines are asynchronous DMA requests by peripheral devices to gain DMA service. They are prioritized with DRQ1 having the highest priority, DRQ2 next, and DRQ3 lowest. A DMA request is generated by driving a DRQ line active high and holding it until the corresponding DACK (DMA acknowledge) signal goes active. DRQ1, DRQ2, and DRQ3 perform only 8-bit transfers. All DRQ lines are active high.

DACK1*, DACK2*, and DACK3* (B17, B26, B15). These lines are DMA acknowledge signals used to acknowledge DMA requests DRQ1, DRQ2, and DRQ3. All DACK signals are active low.

REFRESH* (B19). This signal is used to indicate a refresh cycle that can be used by a memory board to refresh Dynamic memory. REFRESH* is active low and generated every 15 usec.

T/C (B27). T/C is a signal that provides a pulse when the terminal count for any DMA channel is reached. T/C is active high.

OSC (B30). OSC is an oscillator signal that is a high-speed clock with a 70 nanosecond period (14.31818 megahertz). It has a 50% duty cycle.

AT Interface Compatibility

The following pin assignments are used on the 36-position connector found only on the AT-type slots.

Board Pin No.†	Signal Name	Board Pin No.††	Signal Name
C1†	SBHE	D1††	MEMCS16*
C2	SA23	D2	IOCS16*
C3	SA22	D3	IRQ10
C4	SA21	D4	IRQ11
C5	SA20	D5	IRQ12
C6	SA19	D6	IRQ15
C7	SA18	D7	IRQ14
C8	SA17	D8	DACK0*
C9	MEMR*	D9	DRQ0
C10	MEMW*	D10	DACK5*
C11	SD08	D11	DRQ5
C12	SD09	D12	DACK6*
C13	SD10	D13	DRQ6
C14	SD11	D14	DACK7*
C15	SD12	D15	DRQ7
C16	SD13	D16	+5 V
C17	SD14	D17	MASTER*
C18	SD15	D18	Ground

Table 65. Pin Assignments for 36-Position Connector.

† Note: Pin No.s that begin with a C on the PCB are labeled A on the schematic.

†† Note: Pin No.s that begin with a D on the PCB are labeled B on the schematic.

AT Bus Pin Definitions

SBHE (C1). Bus High Enable indicates a transfer on the upper eight bits of the data bus, SD8-SD15. Sixteen bit devices use this signal to condition the data bus buffers tied to SD8-SD15. SBHE is active high.

SA17-SA23 (C2 through C8). These signals are used to address memory and I/O devices in the system. These signals are valid when BALE is high. These signals are not latched during microprocessor cycles, therefore they do not stay valid for the entire cycle. They generate decodes for 1 wait state memory cycles. These decodes should be latched by the I/O adapters on the falling edge of BALE. These signals may also be driven by other DMA controllers or microprocessors that reside on the bus. SA17-SA23 are active high.

MEMR* (C9). This signal, along with SMEMR*, is used to instruct memory devices to drive data onto the data bus and is active on all memory read cycles. MEMR* may be driven by any DMA controller or microprocessor on the I/O bus. When a microprocessor on the bus wishes to assert MEMR*, it must have address lines valid on the bus for at least one system clock period before asserting MEMR*. MEMR* is active low.

MEMW* (C9). This signal, along with SMEMW*, is used to instruct memory devices to store data present on the data bus and is active on all memory write cycles. MEMW* may be driven by any DMA controller or microprocessor on the I/O bus. When a microprocessor on the bus wishes to assert MEMW*, it must have address lines valid on the bus for at least one system clock period before asserting MEMW*. MEMW* is active low.

SD8-SD15 (C11 through C18). These are the upper eight bus bits for the memory and I/O devices. 16 bit devices will use SD0-SD7 of the PC bus and SD8-SD15 of the AT bus.

MEMCS16* (D1). This signal is used to tell the system board if the present data transfer is a 16-bit N wait state memory cycle where N is determined by the 82C301. The default is 2. It is decoded from the SA17-SA23 lines. MEMCS16* is active low.

IOCS16* (D2). This signal is used to tell the system board if the present data transfer is a 16-bit N wait state I/O cycle where N is determined by the 82C301. The default is 2. IOCS16* is active low.

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IRQ10-IRQ12, IRQ14-IRQ15 (D3 through D7). Interrupt Requests IRQ10-IRQ12,IRQ14-IRQ15 are used to signal the microprocessor that an I/O device needs attention. An interrupt request is generated by raising an IRQ line high. The line must be held high until the microprocessor acknowledges the request. IRQ13 is reserved for the system board.

DRQ0, DRQ5-DRQ7 (D9, D11, D13, D15). DMA request 0 and DMA request 5 through 7 are asynchronous channel requests used by peripheral devices on the I/O bus to gain DMA service. A request is generated by bringing the DRQ line high, and the line must be held high until a DMA Acknowledge line goes active. DRQ0 will perform 8-bit transfers, and DRQ5-DRQ7 will perform 16-bit transfers. These signals are active high.

DACK0*, DACK5* - DACK7* (D8, D10, D12, D14). These lines are used to acknowledge DRQo and DRQ5-DRQ7. These signals are active low.

+5V (D16). Bus connector power.

MASTER* (D17). This signal is used with the DRQ lines to gain control of the system. A processor or DMA controller on the I/O bus can issue a DRQ to a DMA channel and receive a DACK*. In response to the DACK*, the processor or DMA controller can pull the MASTER* signal low, thus allowing it to control the system data, address, and control lines. After MASTER* is low, the I/O device must wait one system clock period before driving the address and data lines, and two clock periods before issuing a read or write command. Warning, if this signal is held low for more than 15 microseconds, system memory may be lost due to lack of refresh.

GROUND (D18). Ground for I/O bus.

Memory Expansion Bus

The memory expansion bus (MEB) is located in Slot #1 of the card cage. It is designed to support one 32-bit memory card with either 2 or 8 megabytes of 100nS DRAM. The memory expansion bus is presented to two 36-pin card edge connectors with the following signal description:

Pin	Signal Name	Pin	Signal Name
A1	+5 V	B1	+5 V
A2	Ground	B2	Ground
A3	MD00	B3	MD01
A4	MD02	B4	MD03
A5	MD04	B5	MD05
A6	MD06	B6	MD07
A7	MD08	B7	MD09
A8	MD10	B8	MD11
A9	MD12	B9	MD13
A10	MD14	B10	MD15
A11	MD16	B11	MD17
A12	MD18	B12	MD19
A13	MD20	B13	MD21
A14	MD22	B14	MD23
A15	MD24	B15	MD25
A16	MD26	B16	MD27
A17	MD28	B17	MD29
A18	MD30	B18	MD31
C1	+5 V	D1	+5 V
C2	Ground	D2	Ground
C3	+5 V	D3	+5 V
C4	Ground	D4	Ground
C5	MA0	D5	MA1
C6	MA2	D6	MA3
C7	MA4	D7	MA5
C8	MA6	D8	MA7
C9	MA8	D9	MA9
C10	Ground	D10	+5 V
C11	+5 V	D11	DWE*
C12	RAS2*	D12	CAS2*
C13	RAS3*	D13	CAS3*
C14	LBE0*	D14	MP0
C15	LBE1*	D15	MP1
C16	LBE2*	D16	MP2
C17	LBE3*	D17	MP3
C18	+5 V	D18	Ground

Table 66. Signal Description for 36-Pin Memory Card Edge.

Tandy 4000 80387 Support Version

Differences in Rev. A and Rev. C Main Logic Boards

1. 80287 Socket U25 has been removed.
2. Oscillator Clock Y5 has been removed.
3. PAL U22 has been removed.
4. PAL U53 has been added for 80387 select and decode.
5. PAL U49 has been added to generate 80386 handshake and control signals.
6. Jumper E3-E4 has been added to select 80387 as installed.

Note: The BIOS for Rev. C is not interchangeable with the BIOS for Rev. A.

80387 Numeric Processor

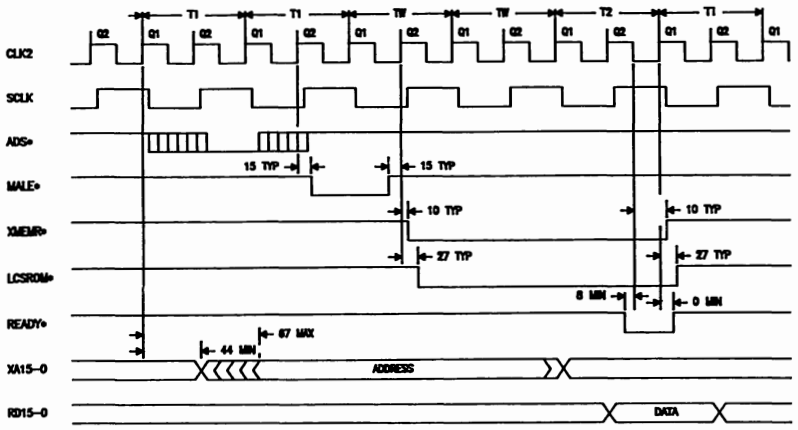
The optional 80387 numeric processor is a 68-pin IC that can be used in the available socket (U15) on the main logic board. Socket U15 is a 121 PGA superset of the 68-pin socket and can also be used for the Weitek 1167 Co-Processor. Chip select and address decoding for the Numeric Processor and the Weitek are provided by PAL U53. PAL U49 is used to generate the READY, BUSY, ERROR, PEREQ, and IRQ13 signals needed to interface the 80387 to the system. The numeric processor executes mathematical calculations independently, allowing the CPU to perform other tasks. It runs synchronously to the 80386, interfaces through the local CPU bus, and uses the same clock. Error reporting is interfaced through IRQ13 via the 82C206 IPC. A detailed description of the 82C206 IPC is provided in the "I/O Decode" and "Devices" sections of this manual. A detailed description of the 80387 can be found in "Appendix A" in this manual.

```
 1:
 2:                PARTNO    U53;
 3:                NAME      U53;
 4:                DATE      12/28/87 ;
 5:                REV       C ;
 6:                DESIGNER  R. THOMPSON ;
 7:                COMPANY   Tandy ;
 8:                ASSEMBLY  XXXX ;
 9:                LOCATION  YYYY ;
10:
11:/*************************************************************************/
12:/*                                                                       */
13:/* This device performs address decoding for the 80387 circuitry        */
14:/* on the TANDY 4000.                                                    */
15:/*                                                                       */
16:/*************************************************************************/
17:/*  Allowable Target Device Types: 16L8B                                 */
18:/*************************************************************************/
19:
20:/**  Inputs  **/
21:
22:PIN 1         = A31       ;       /*                                    */
23:PIN 2         = MALE      ;       /*                                    */
24:PIN 3         = RESET3    ;       /*                                    */
25:PIN 4         = XIOW      ;       /*                                    */
26:PIN 5         = XA04      ;       /*                                    */
27:PIN 6         = XA03      ;       /*                                    */
28:PIN 7         = XA02      ;       /*                                    */
29:PIN 8         = XA01      ;       /*                                    */
30:PIN 9         = XA00      ;       /*                                    */
31:PIN 11        = 287CS     ;       /*                                    */
32:PIN 13        = NPSEL     ;       /*                                    */
33:PIN 18        = MIO       ;       /*                                    */
34:
35:/**  Outputs  **/
36:
37:PIN 14        = !NPCS     ;       /* NUMERIC PROCESSOR SELECT           */
38:PIN 16        = !AE32FF   ;       /* OUTPUT TO AF32 FLIP-FLOP           */
39:
40:/** Declarations and Intermediate Variable Definitions **/
41:
42:
43:/**  Logic Equations  **/
44:
45:NPCS = !XIOW & !287CS &  XA04 & !XA03 & !XA02 & !XA01 ;
46:
47:AF32FF = !MALE & A31 & !MIO & !NPSEL & !RESET3 ;
48:

Jedec Fuse Checksum       (0E8C)
Jedec Transmit Checksum   (6DB1)
```

```
 1:
 2:                PARTNO     U49;
 3:                NAME       U49;
 4:                DATE       11/16/87 ;
 5:                REV        B ;
 6:                DESIGNER   R. THOMPSON ;
 7:                COMPANY    Tandy ;
 8:                ASSEMBLY   XXXX ;
 9:                LOCATION   YYYY ;
10:
11:/*************************************************************************/
12:/*                                                                       */
13:/* This device generates READY, BUSY, ERROR, PEREQ and IRQ13             */
14:/* on the TAND 4000 .                                                    */
15:/*                                                                       */
16:/*************************************************************************/
17:/*  Allowable Target Device Types: 16L8B                                 */
18:/*************************************************************************/
19:
20:/**  Inputs  **/
21:
22:PIN 1         = 387ERROR   ;       /*                                  */
23:PIN 2         = 387BUSY    ;       /*                                  */
24:PIN 3         = 387PERQ    ;       /*                                  */
25:PIN 5         = INTA       ;       /*                                  */
26:PIN 7         = RESET3     ;       /*                                  */
27:PIN 8         = 386RDY     ;       /* 386 SYSTEM READY                 */
28:PIN 9         = NPCS       ;       /* NUMERIC PROCESSOR SELECT         */
29:PIN 11        = INT13FF    ;       /* LATCHED IRQ13 FROM FLIP-FLOP     */
30:
31:/**  Outputs  **/
32:
33:PIN 12        = !386BSY    ;       /* BUSY TO 80386                    */
34:PIN 13        = PEREQ      ;       /* PEREQ TO 80386                   */
35:PIN 15        = !MSKERR    ;       /*                                  */
36:PIN 16        = BUSYFF     ;       /*                                  */
37:PIN 17        = !ERRFF     ;       /*                                  */
38:PIN 18        = !FB13      ;       /*                                  */
39:PIN 19        = !386ERR    ;       /*                                  */
40:
41:/** Declarations and Intermediate Variable Definitions **/
42:
43:/**  Logic Equations  **/
44:
45:386BSY = !387BUSY # INT13FF ;
46:
47:386ERR = !387ERROR & !MSKERR ;
48:
49:BUSYFF = !387BUSY ;
50:
51:PEREQ = 387PERQ # 387BUSY & INT13FF ;
52:
53:MSKERR = !RESET3 # 386RDY & MSKERR ;
54:
55:ERRFF = 387ERROR ;
56:
57:FB13 = !RESET3 # INTA & !NPCS ;
58:
Jedec Fuse Checksum        (462A)
Jedec Transmit Checksum    (D8BA)
```

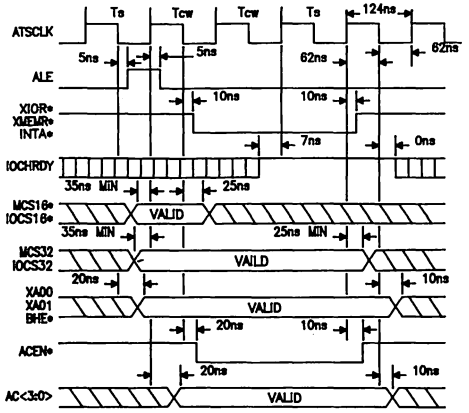
ROM READ CYCLE

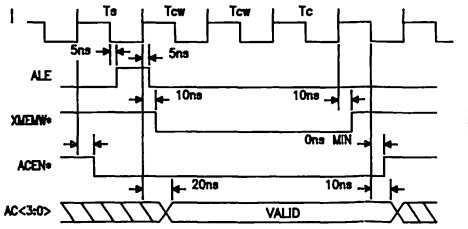


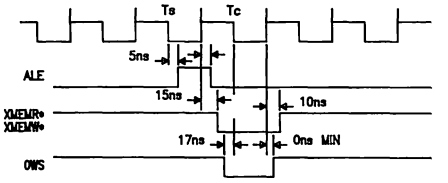
NOTES

1. ALL UNITS IN NANOSECONDS.

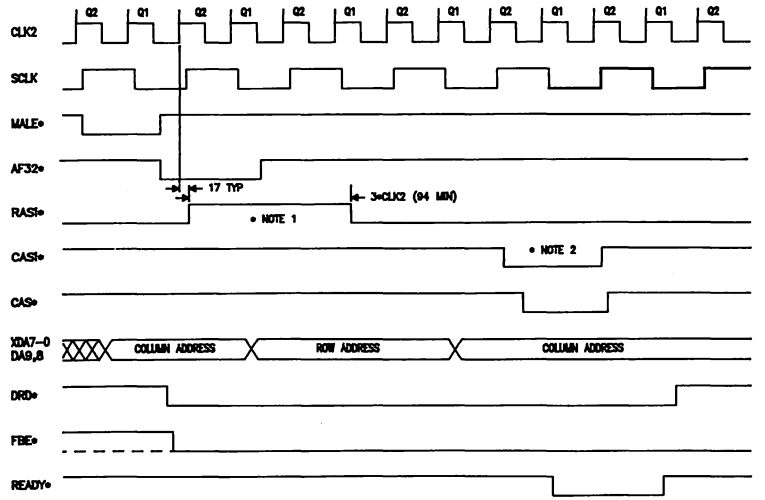
82C301 I/O TIMING DIAGRAMS







82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ MISS CYCLE

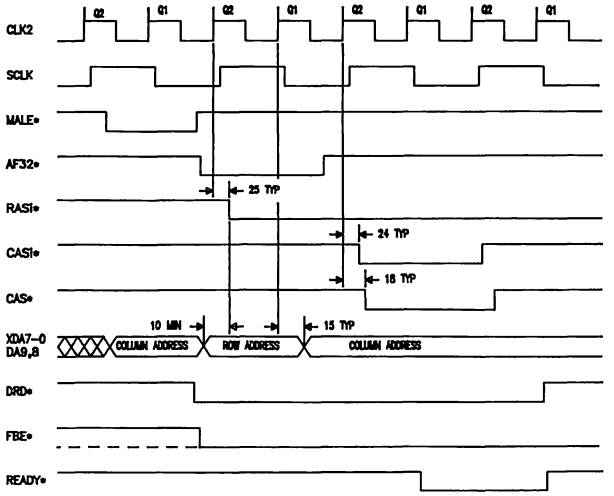


NOTES

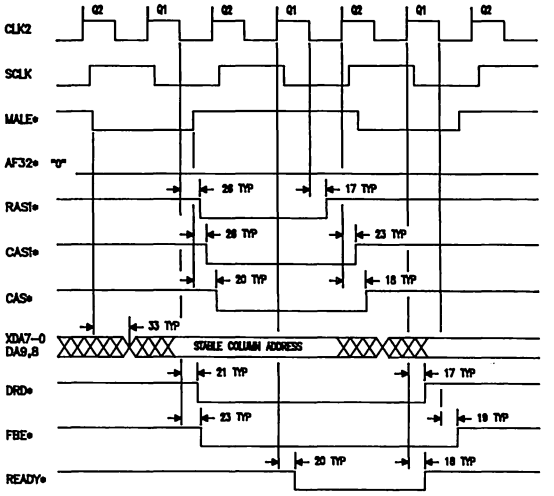
1. RAS• PRECHARGE TIME WILL BE INCREAS BY 2 CLK2 CYCLES IF BIT 7 OF REGISTER 11 (OR 13) IS PROGRAMMED TO "1".
2. CAS• & CAS• PULSE WIDTHS WILL BE INCREASED BY 2 CLK2 CYCLES IF BIT 6 OF REGISTER 11 (OR 13) IS PROGRAMMED TO "1".

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
WRITE MISS CYCLE

82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ CYCLE WITH RAS BEING INACTIVE



82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ HIT, 0 WAIT STATE



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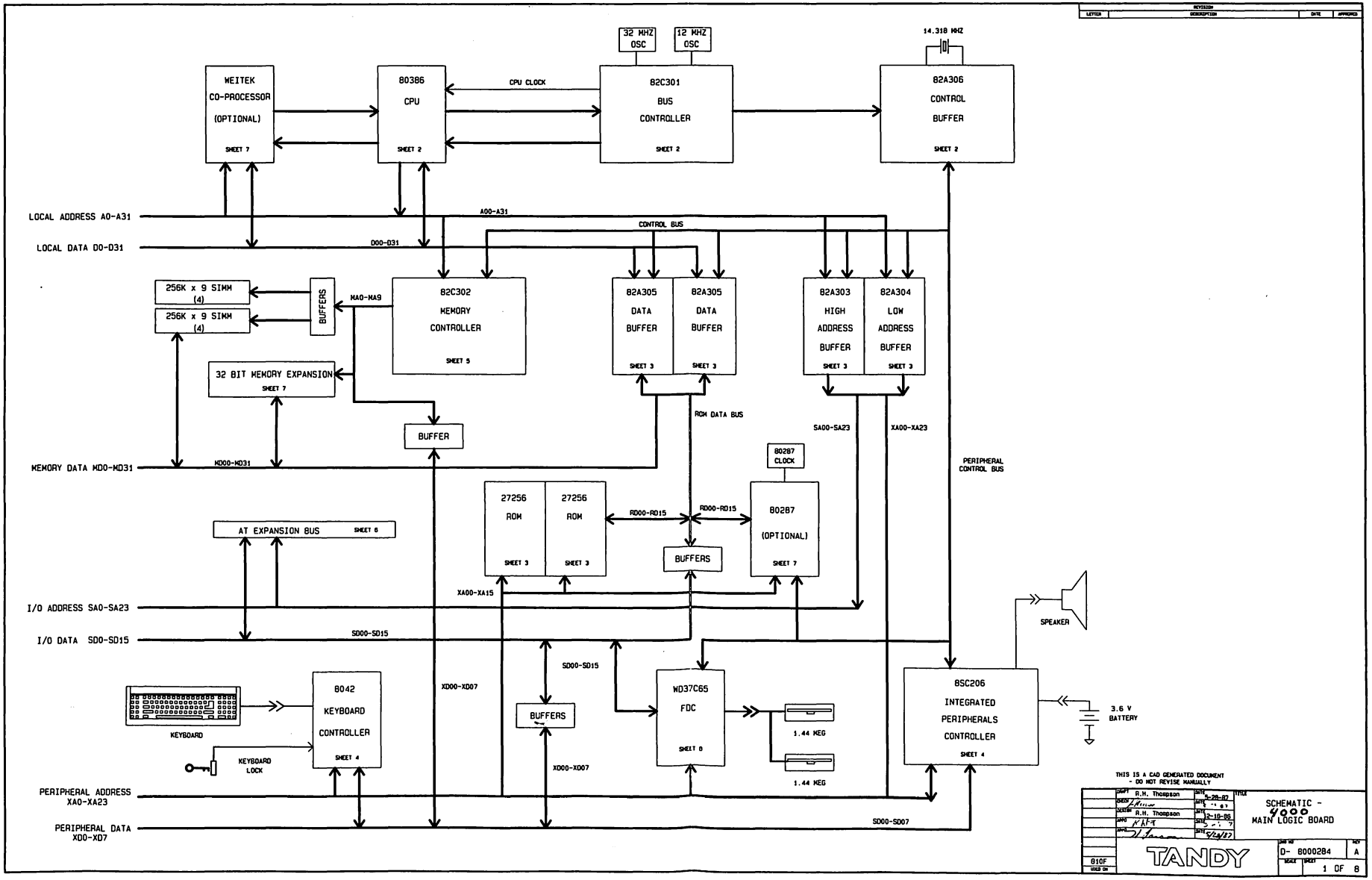
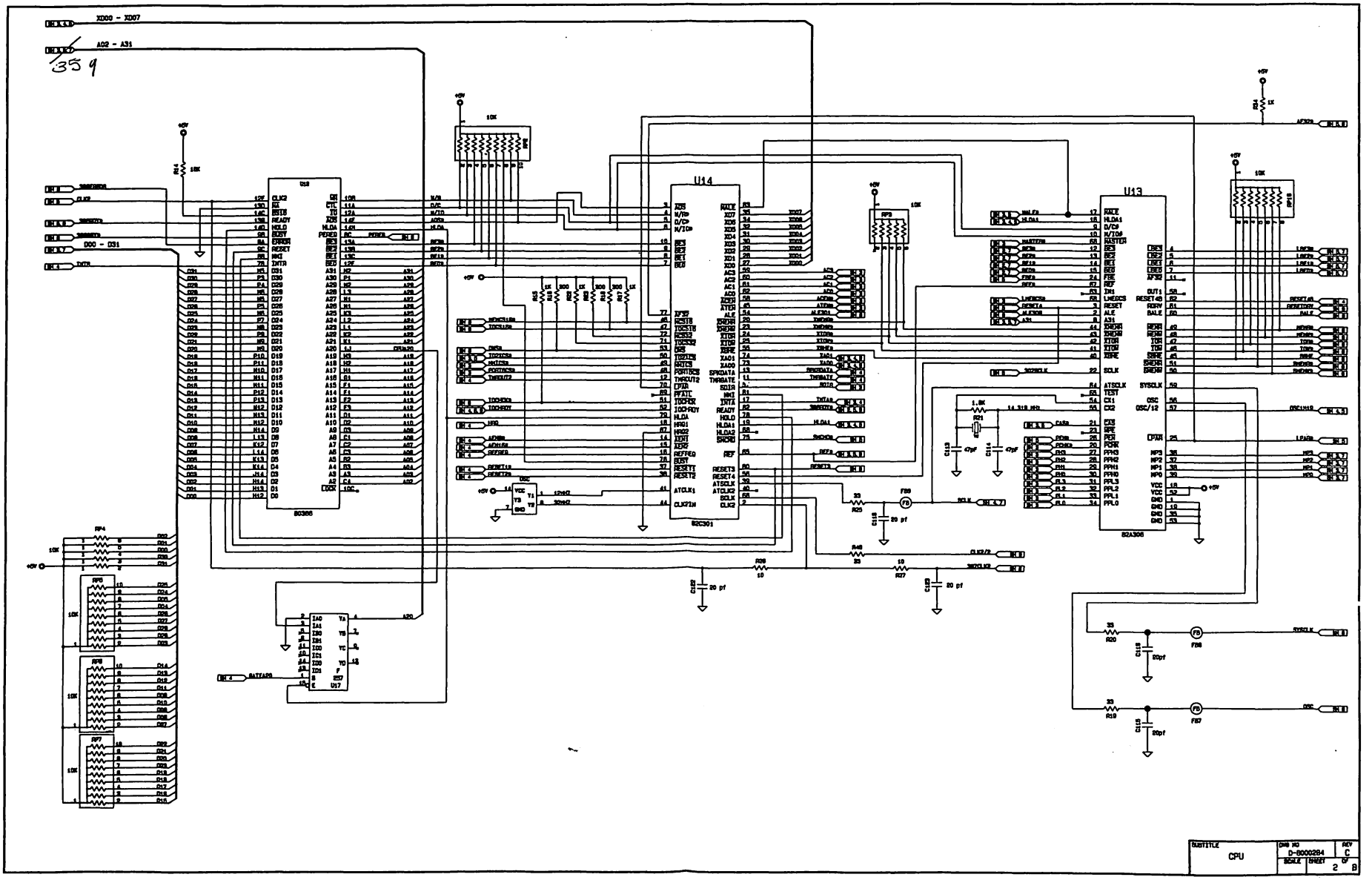
SCHEMATIC –
TANDY V000
TIMING DIAGRAM

TANDY

D–

1 OF


32 MHZ OSC
12 MHZ OSC
14.318 MHZ
WEITEK CO-PROCESSOR (OPTIONAL) SHEET 7
80386 CPU SHEET 2
CPU CLOCK
82C301 BUS CONTROLLER SHEET 2
82A306 CONTROL BUFFER SHEET 2
LOCAL ADDRESS A0-A31
A00-A31
CONTROL BUS
LOCAL DATA D0-D31
D00-D31
256K x 9 SIMM (4)
256K x 9 SIMM (4)
BUFFERS
MA0-MA9
82C302 MEMORY CONTROLLER SHEET 5
82A305 DATA BUFFER SHEET 3
82A305 DATA BUFFER SHEET 3
82A303 HIGH ADDRESS BUFFER SHEET 3
82A304 LOW ADDRESS BUFFER SHEET 3
32 BIT MEMORY EXPANSION SHEET 7
BUFFER
ROM DATA BUS
SA00-SA23
XA00-XA23
80287 CLOCK
MEMORY DATA MD0-MD31
MD00-MD31
PERIPHERAL CONTROL BUS
27256 ROM SHEET 3
27256 ROM SHEET 3
RD00-RD15
RD00-RD15
80287 (OPTIONAL) SHEET 7
AT EXPANSION BUS SHEET 6
BUFFERS
XA00-XA15
I/O ADDRESS SA0-SA23
I/O DATA SD0-SD15
SD00-SD15
SPEAKER
8042 KEYBOARD CONTROLLER SHEET 4
KEYBOARD
KEYBOARD LOCK
XD00-XD07
SD00-SD15
BUFFERS
WD37C65 FDC SHEET 8
1.44 MEG
1.44 MEG
82C206 INTEGRATED PERIPHERALS CONTROLLER SHEET 4
3.6 V BATTERY
XD00-XD07
PERIPHERAL ADDRESS XA0-XA23
PERIPHERAL DATA XD0-XD7
SD00-SD07
THIS IS A CAD GENERATED DOCUMENT - DO NOT REVISE MANUALLY
DRAFT R.H. Thompson 4-25-87
CHECK
DESIGN R.H. Thompson 2-19-88
APP'D
APP'D
SCHEMATIC - 4000 MAIN LOGIC BOARD
TANDY
D- 8000284 A
SHEET 1 OF 8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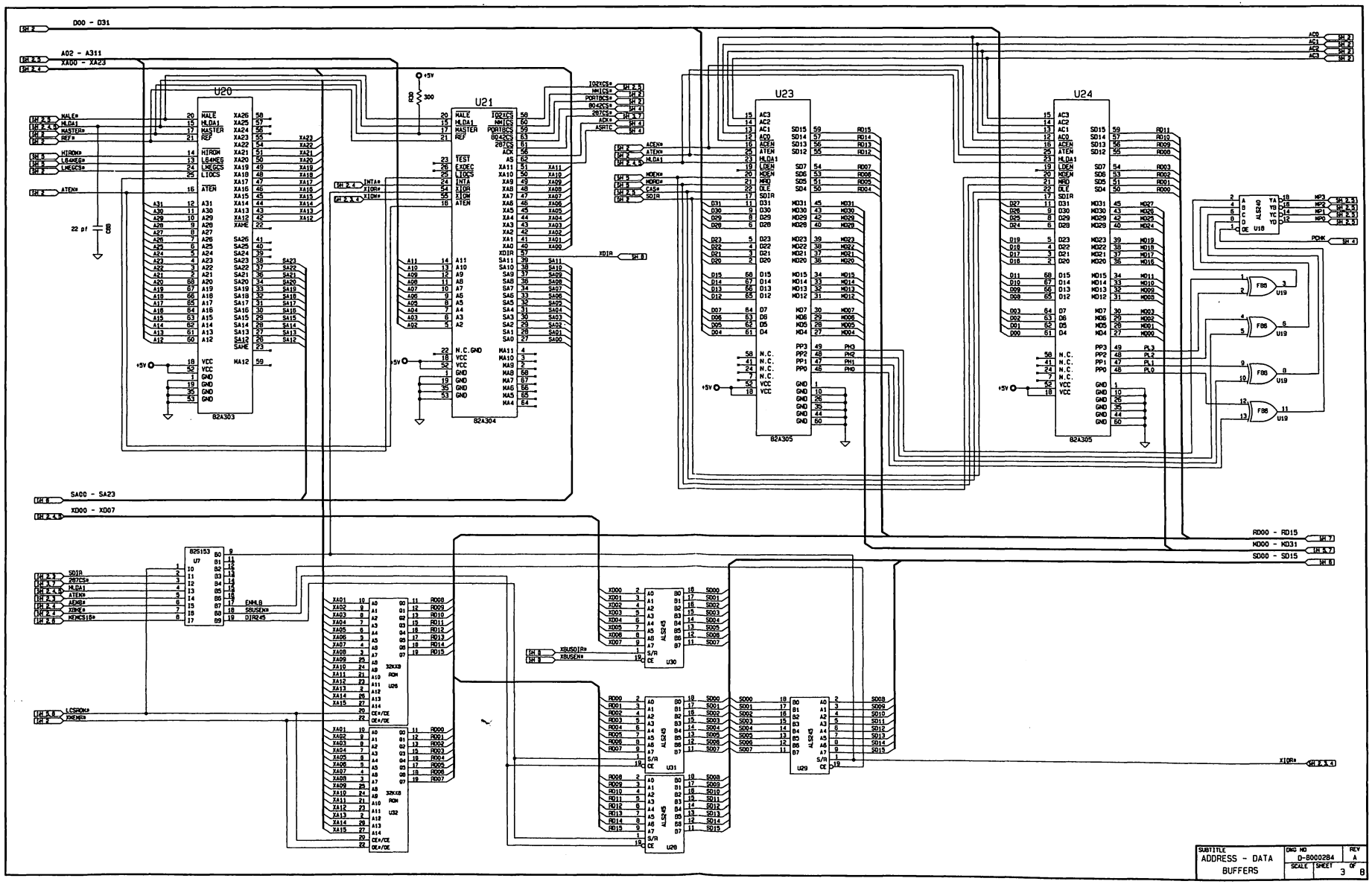

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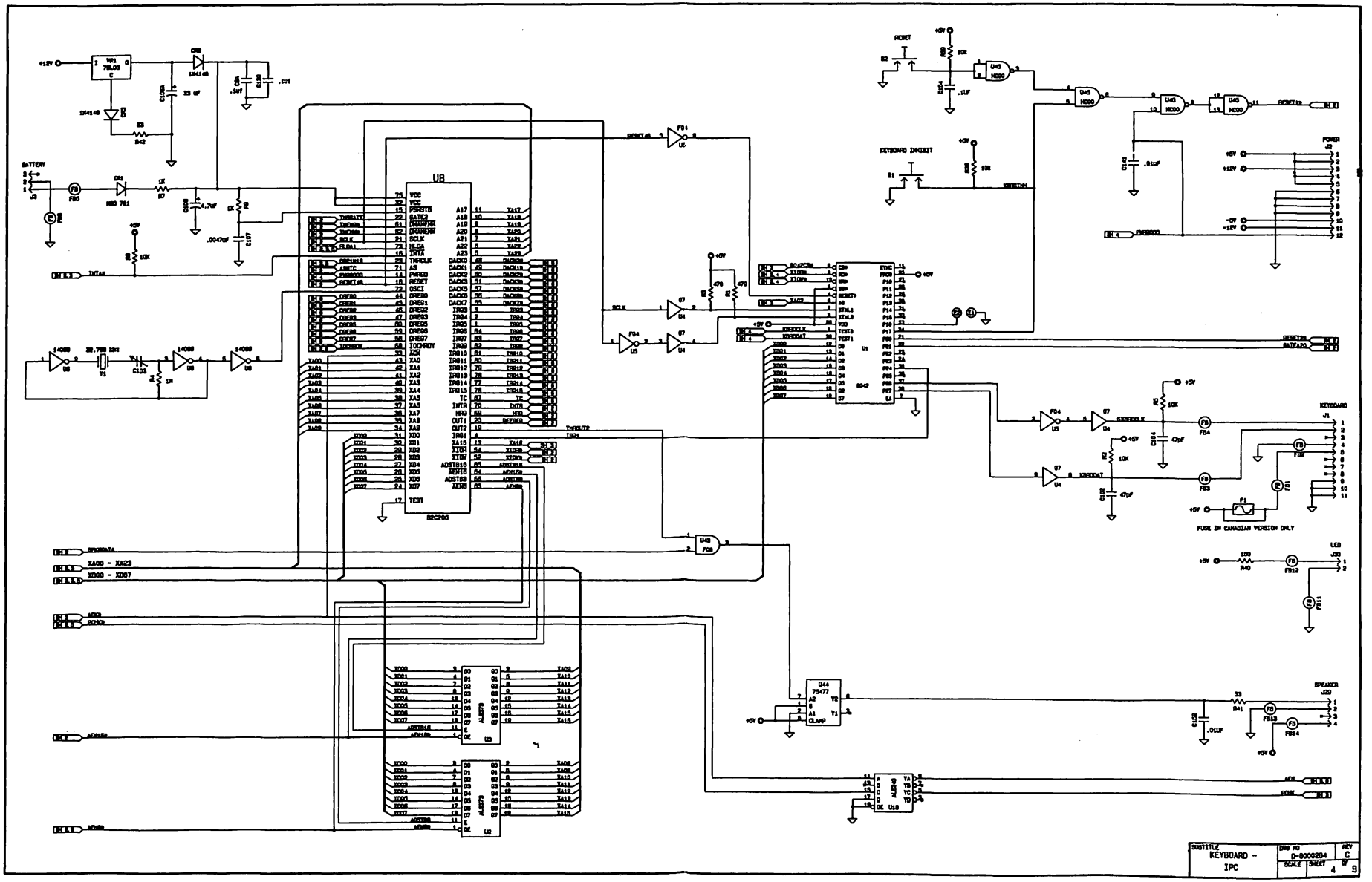
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REV C
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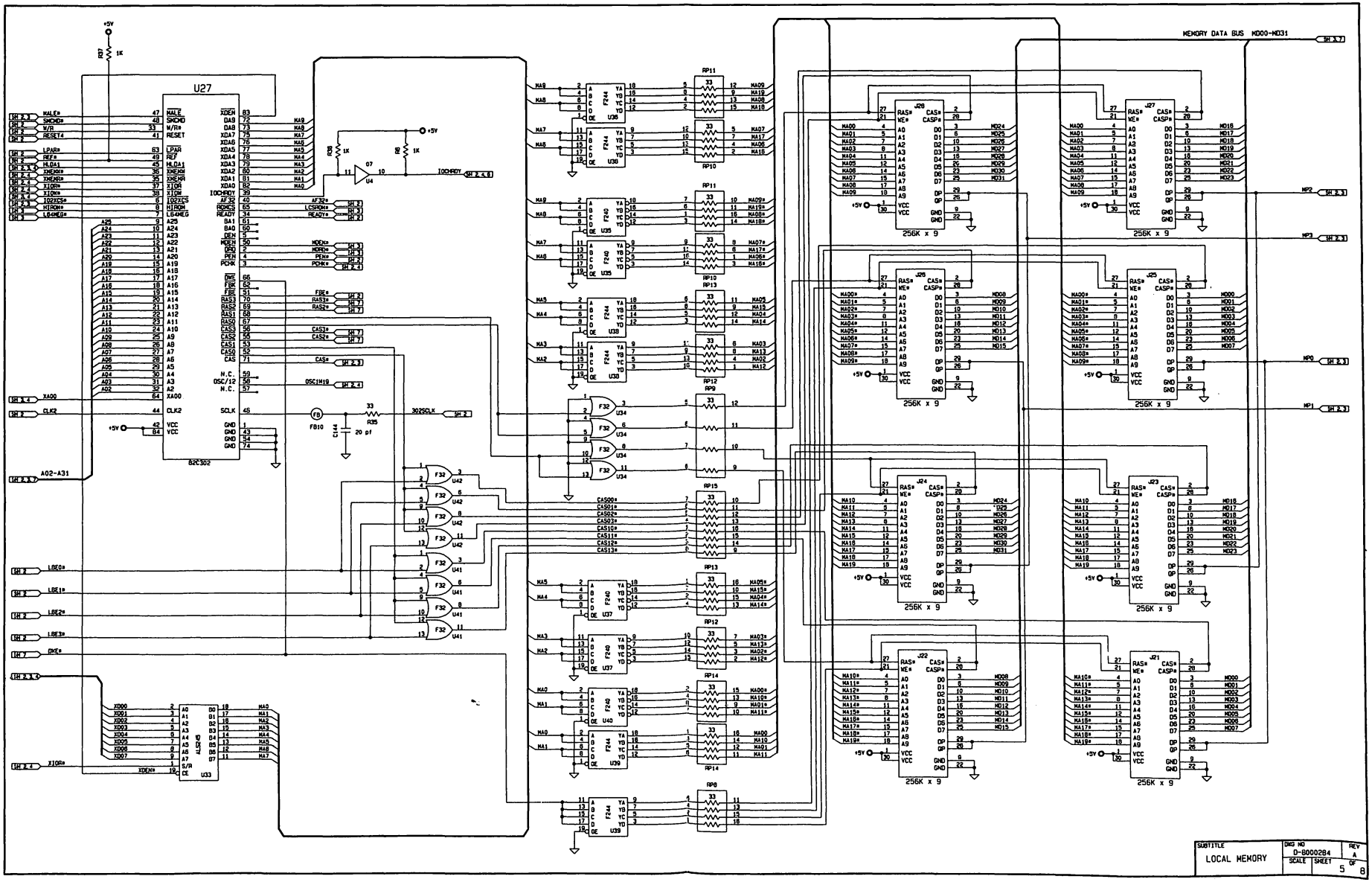
SPEAKER
KEYBOARD
POWER
BATTERY
XA00 - XA23
XD00 - XD07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U33
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DWG NO
D-8000284
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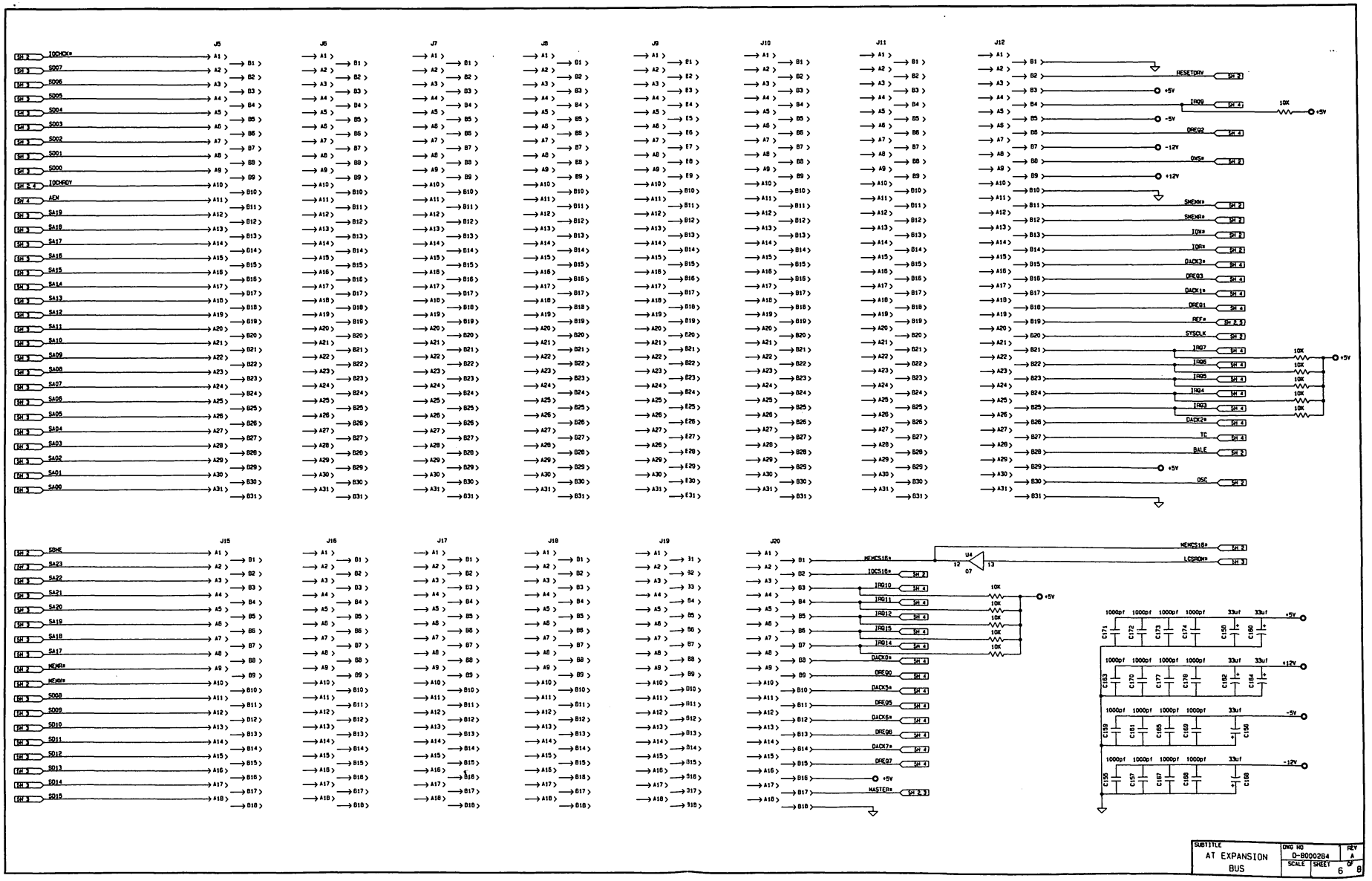
A
SCALE
SHEET
5 OF 8



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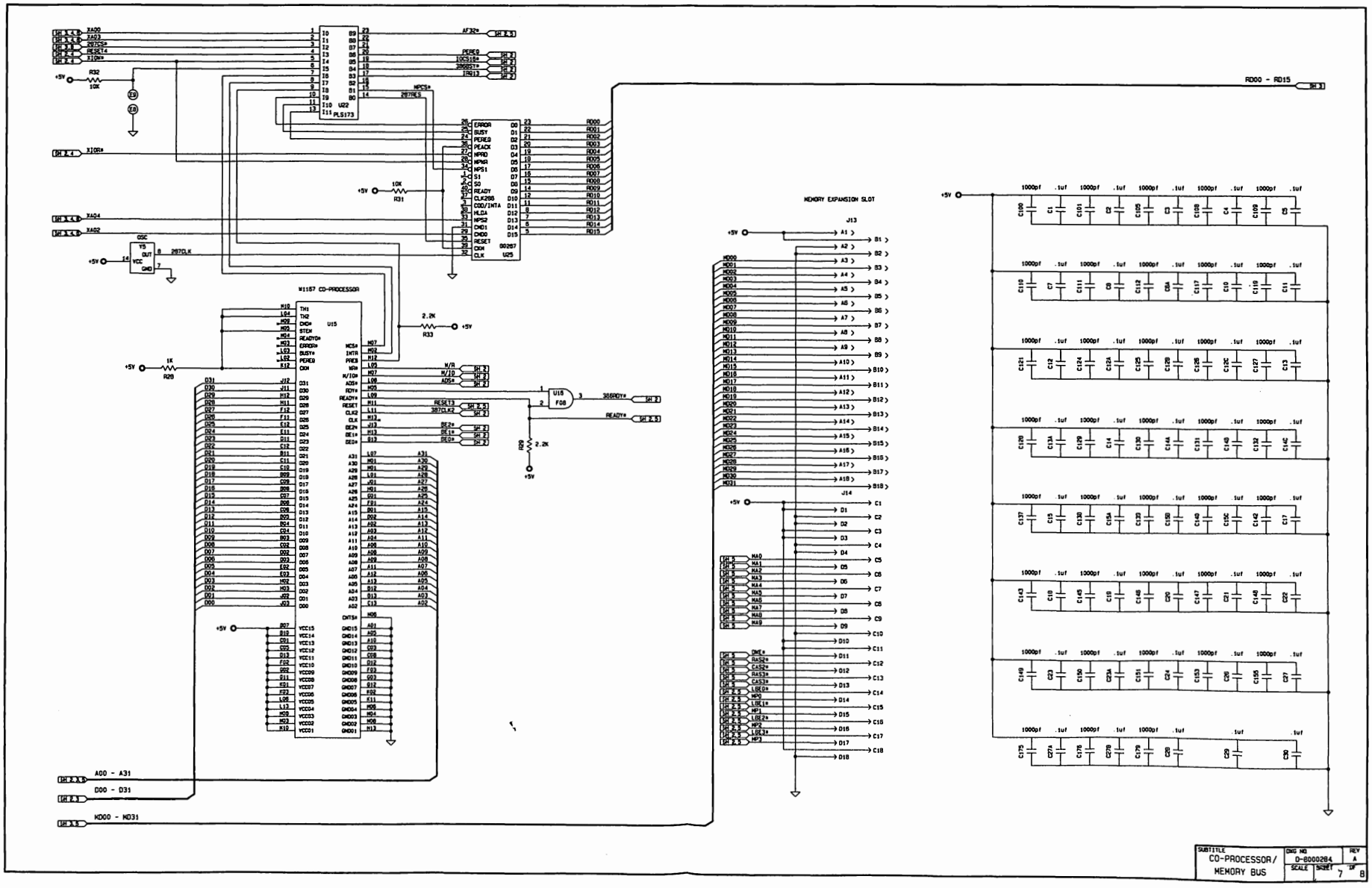
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A00 - A31
D00 - D31
MD00 - MD31
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D-8000284
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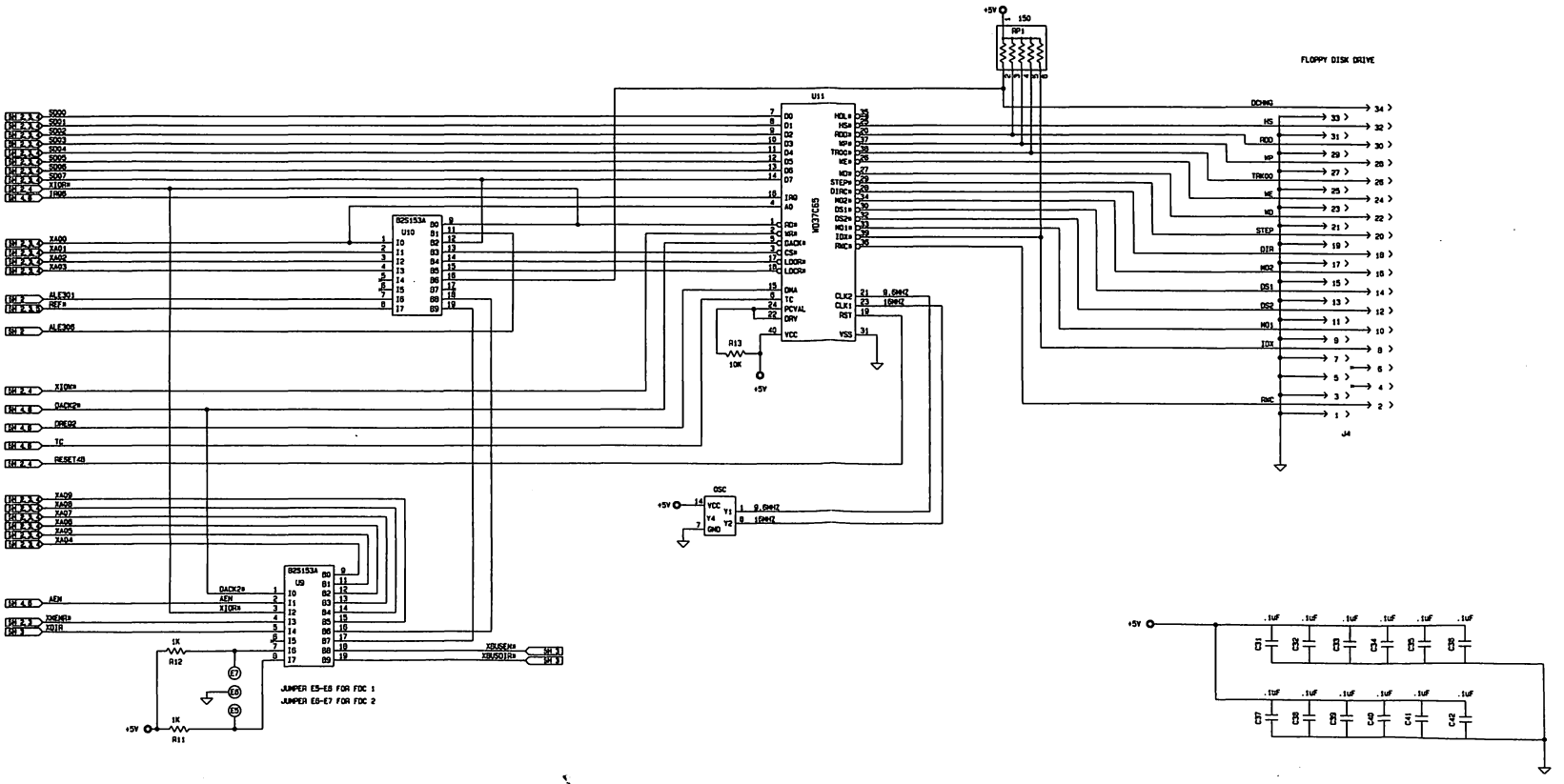
SHEET
7
OF
8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JUMPER E5-E6 FOR FDC 1
JUMPER E6-E7 FOR FDC 2
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D-8000284
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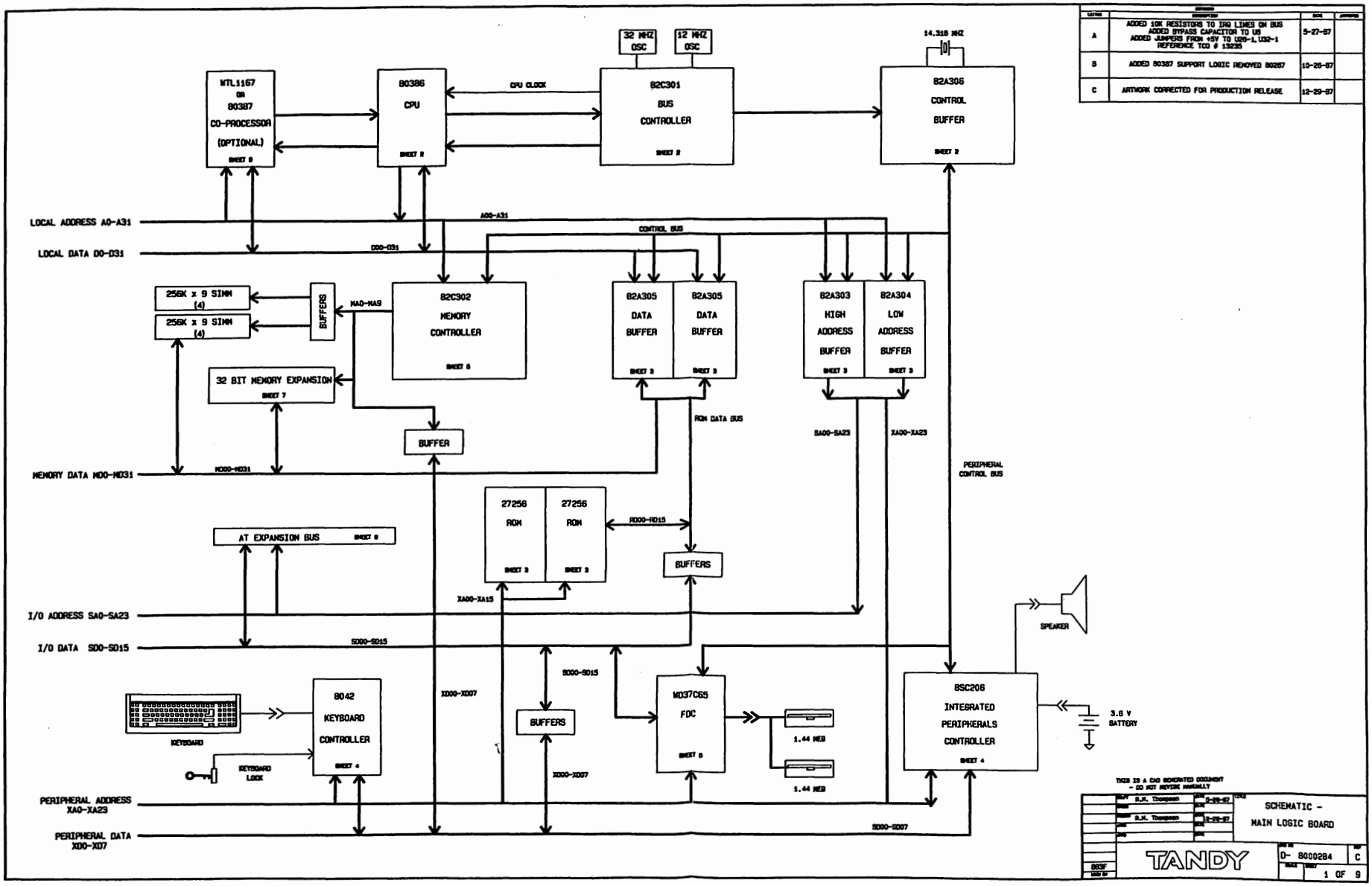
8
OF
8



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A	ADDED 10K RESISTORS TO IRQ LINES ON BUS ADDED BYPASS CAPACITOR TO U8 ADDED JUMPERS FROM +5V TO U20-1, U32-1 REFERENCE TCO # 13235	5-27-87	
B	ADDED 80387 SUPPORT LOGIC REMOVED 80287	10-26-87	
C	ARTWORK CORRECTED FOR PRODUCTION RELEASE	12-29-87	

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- DO NOT REVISE MANUALLY

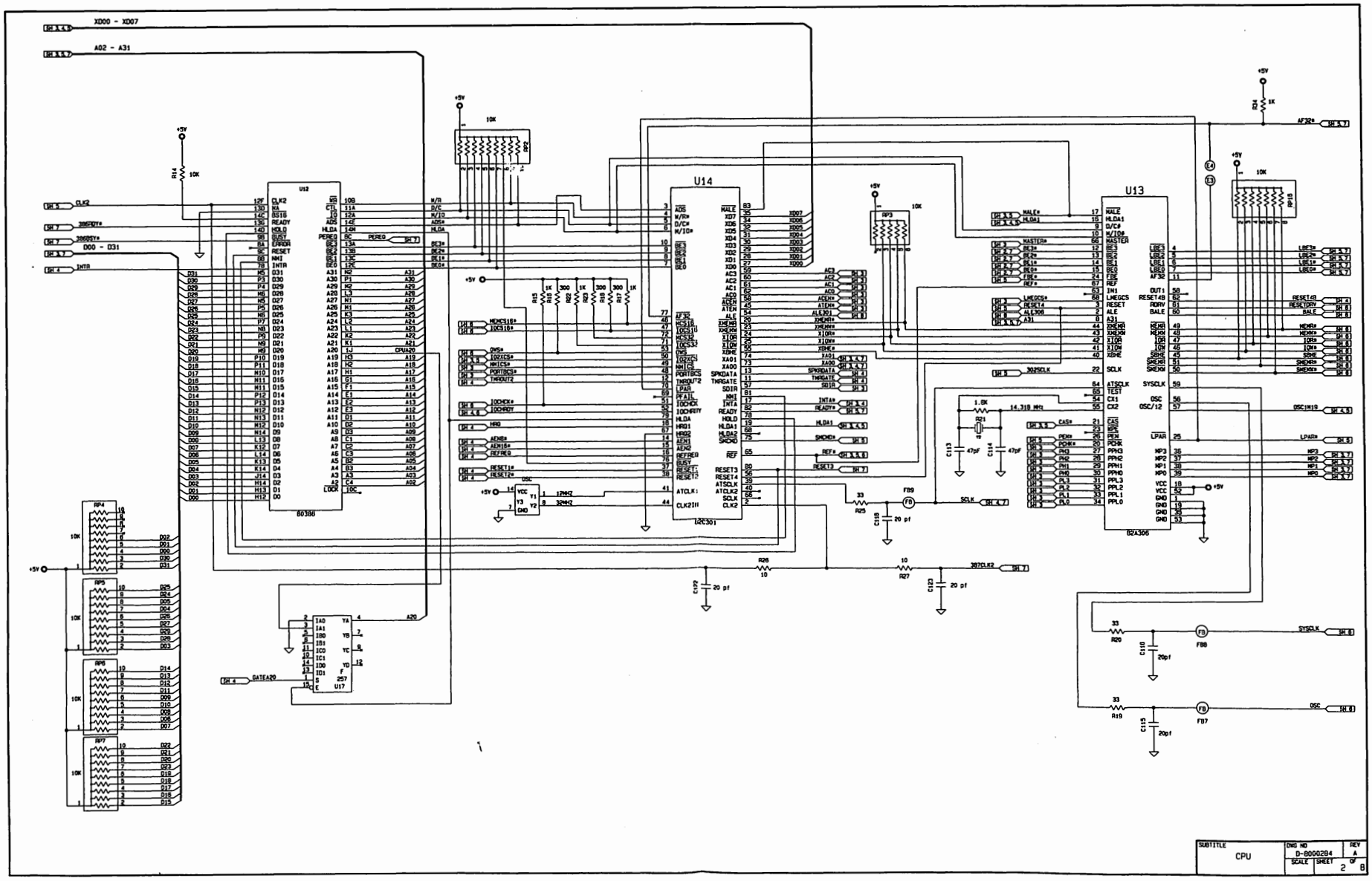
DRAFT	R.H. Thompson	5-26-87	
DESIGN			
ENGR	R.H. Thompson	12-29-87	
APVD			

SCHEMATIC - MAIN LOGIC BOARD

TANDY

D- 8000284 C

1 OF 9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D00 - D31
U12
80386
U14
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U13
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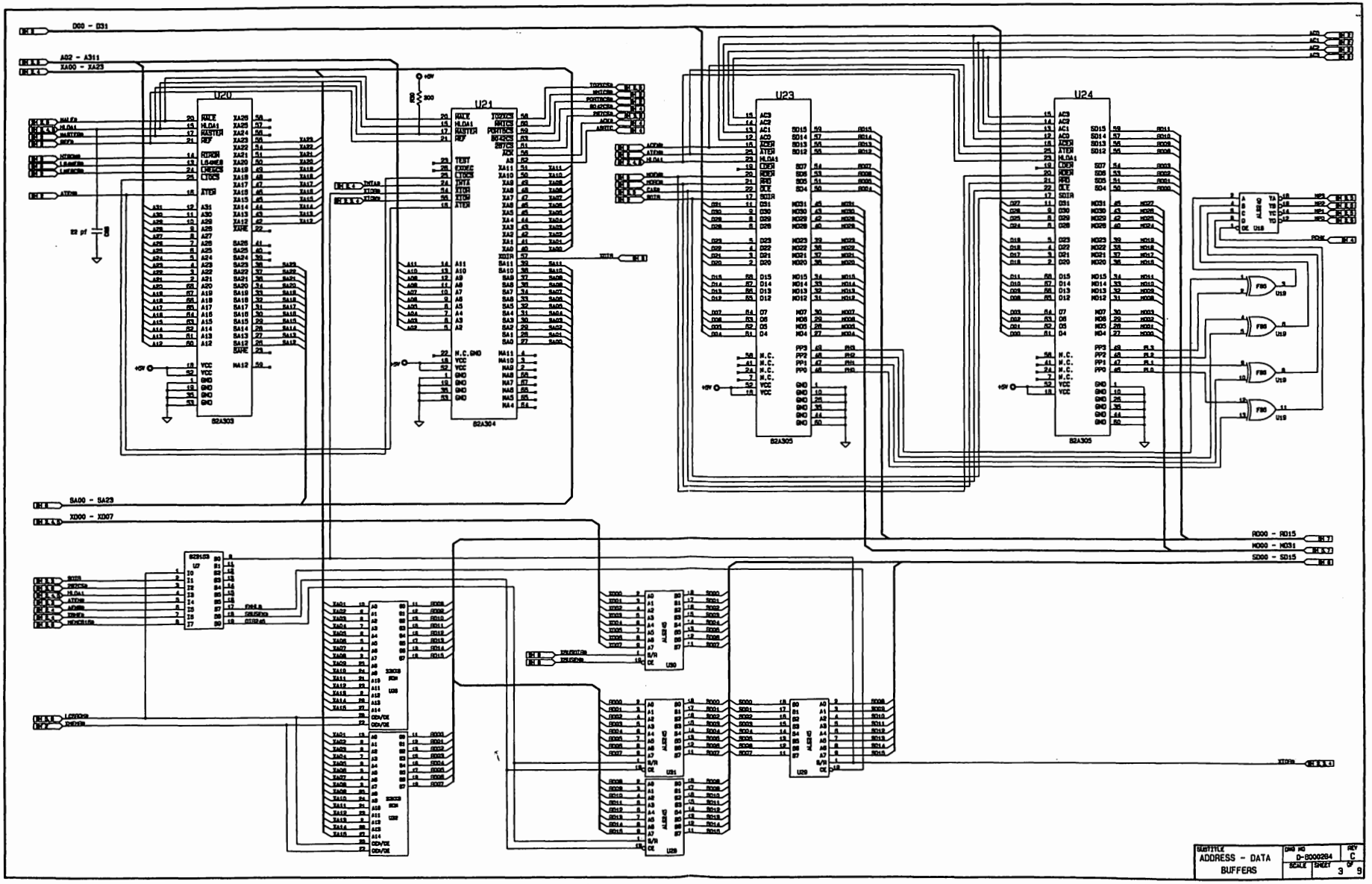
CPU
DWG NO
D-8000284
REV
A
SCALE
SHEET
2 OF 8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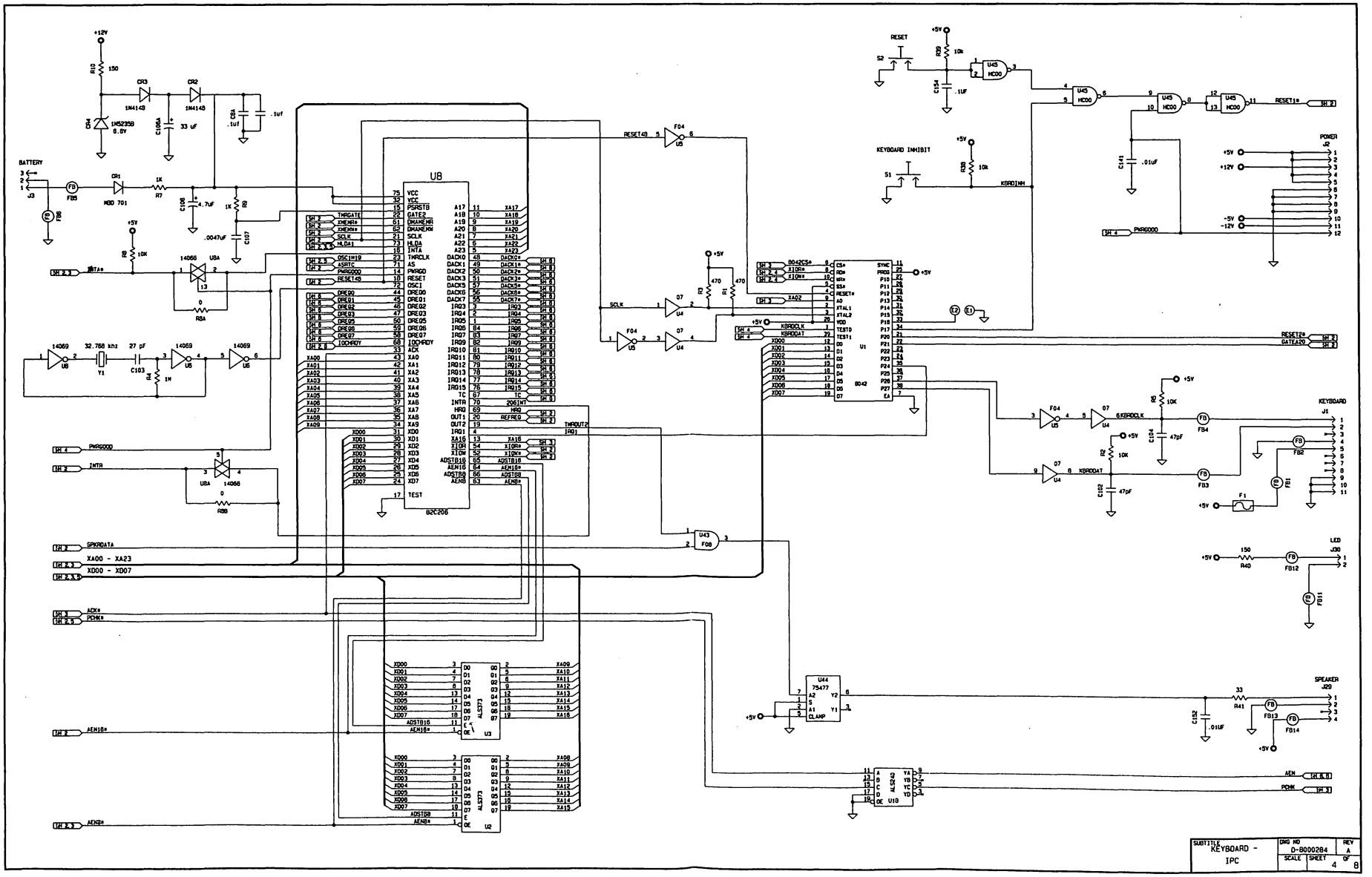
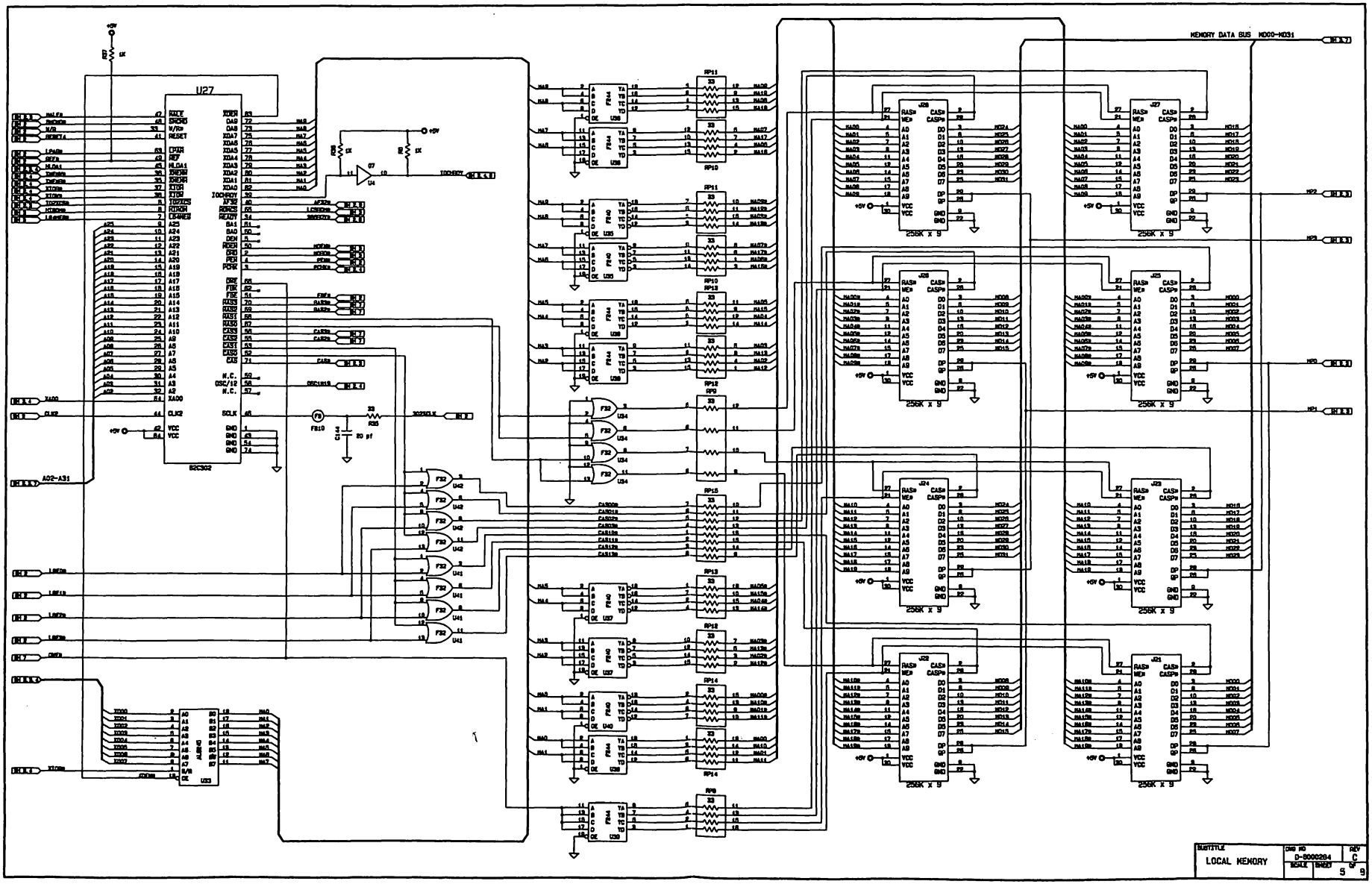
XA00 - XA25
U20
U21
U23
U24
82A303
82A304
82A305
SA00 - SA23
XD00 - XD07
R000 - R015
M000 - M031
SD00 - SD15
ADDRESS - DATA BUFFERS
D-8000284
C
3
9


BATTERY
U8
82C206
KEYBOARD INHIBIT
RESET
POWER
KEYBOARD
SPEAKER
LED
XA00 - XA23
XD00 - XD07
SUBTITLE
KEYBOARD - IPC
DWG NO
D-8000284
REV
A
SCALE
SHEET
4
OF
8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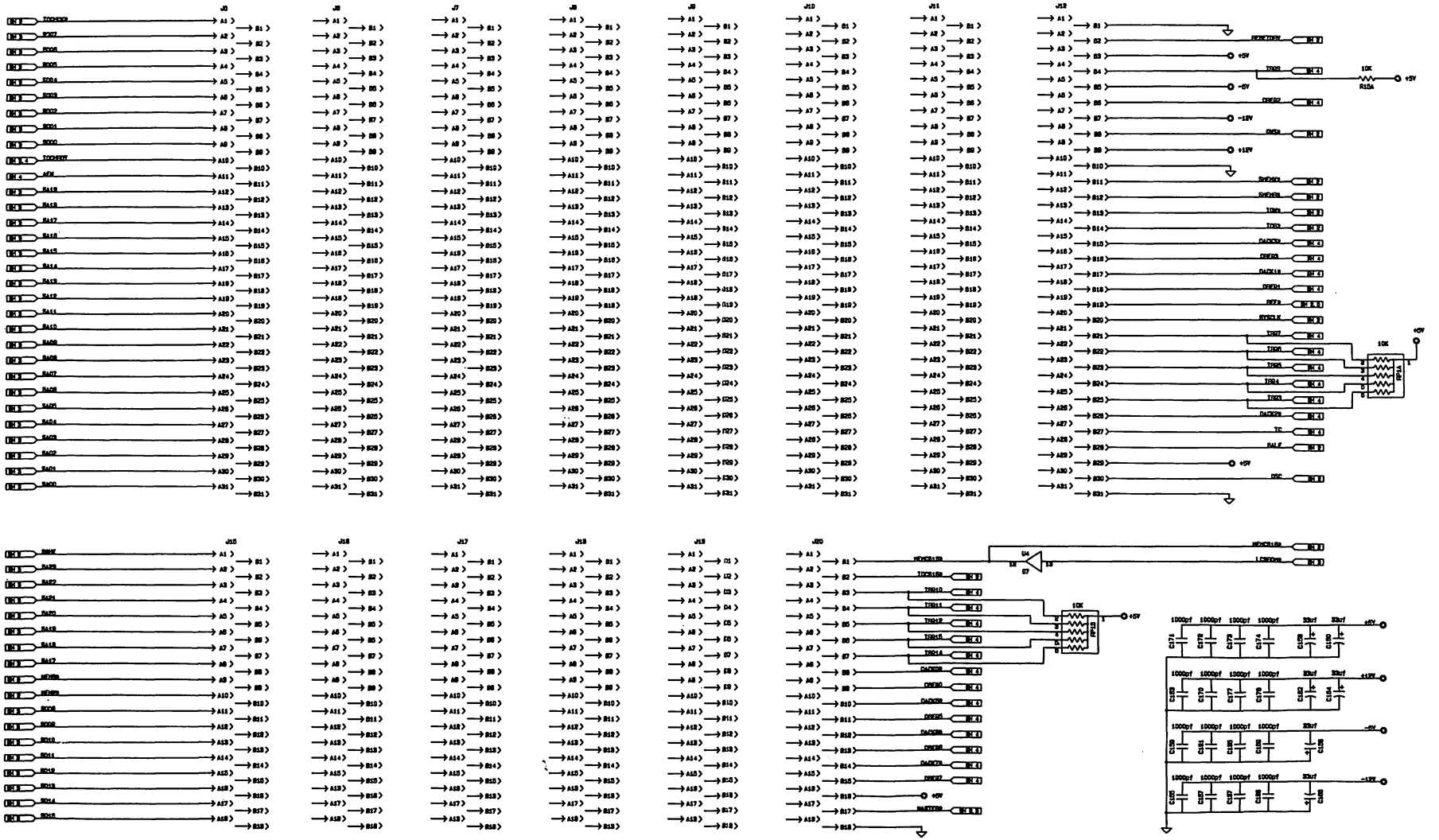
U27
82C302
256K x 9
LOCAL MEMORY
D-0000294
C
5
9



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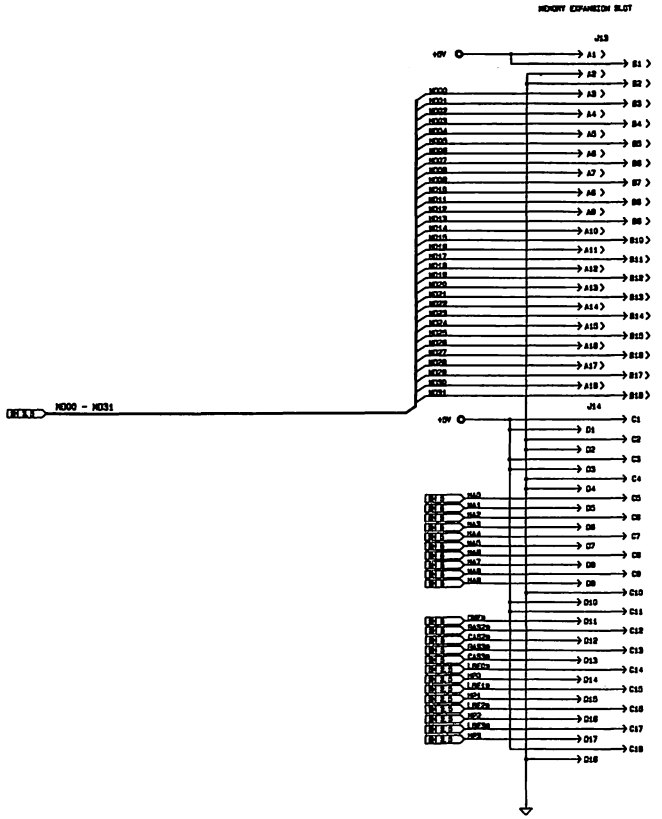

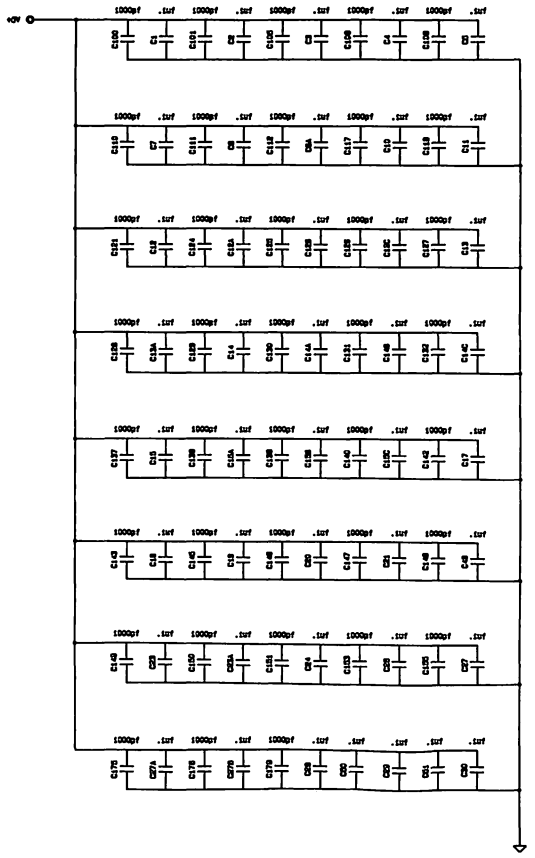

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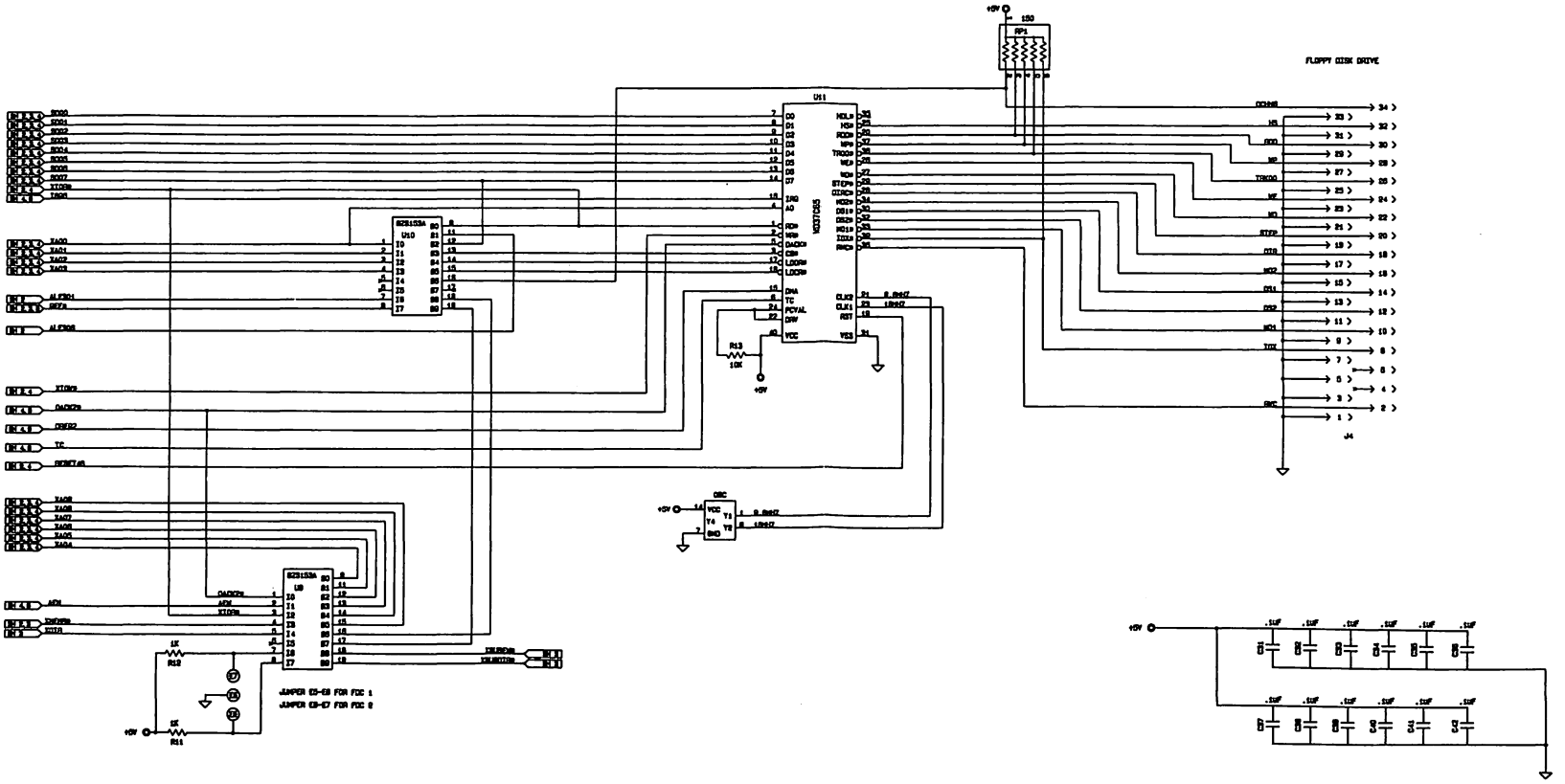
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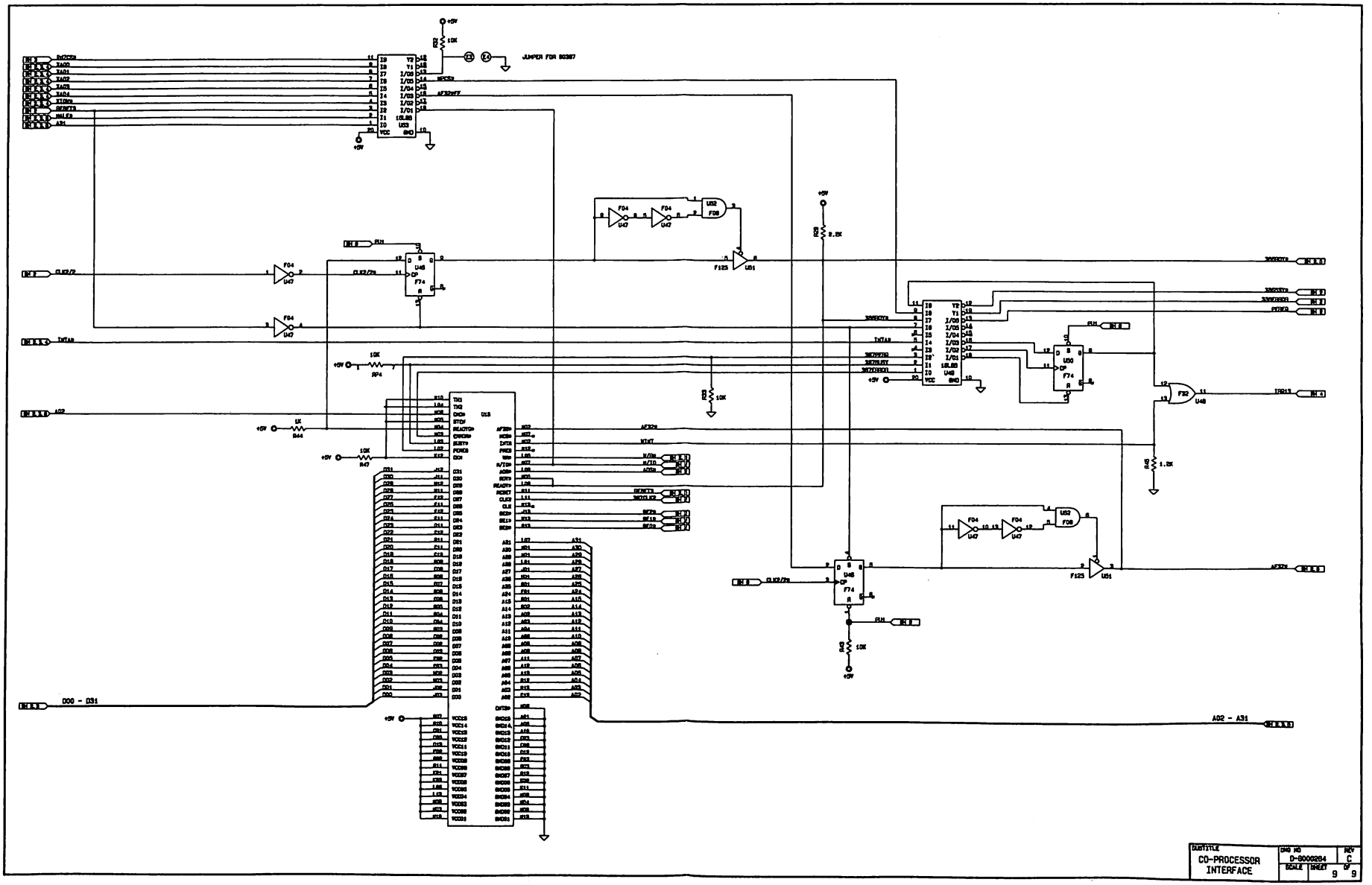
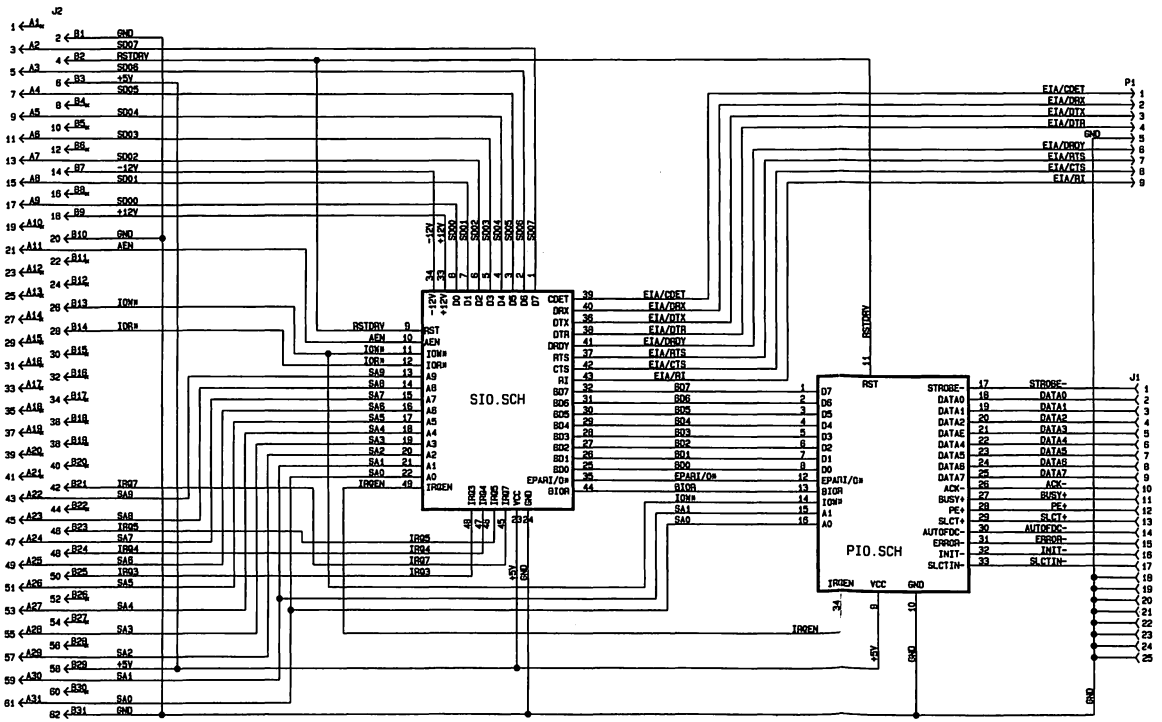
J4
U11
U10
U9
RP1
150
R13
10K
R12
1K
R11
5K
JUMPER C5-C8 FOR FDC 1
JUMPER C5-C7 FOR FDC 0
+5V
FDC


JUMPER FOR 80387
DO0 - D31
A02 - A31
CO-PROCESSOR INTERFACE
D-8000264
C
9
9

REVISION				
ZONE	LETTER	DESCRIPTION	DATE	APPROVED



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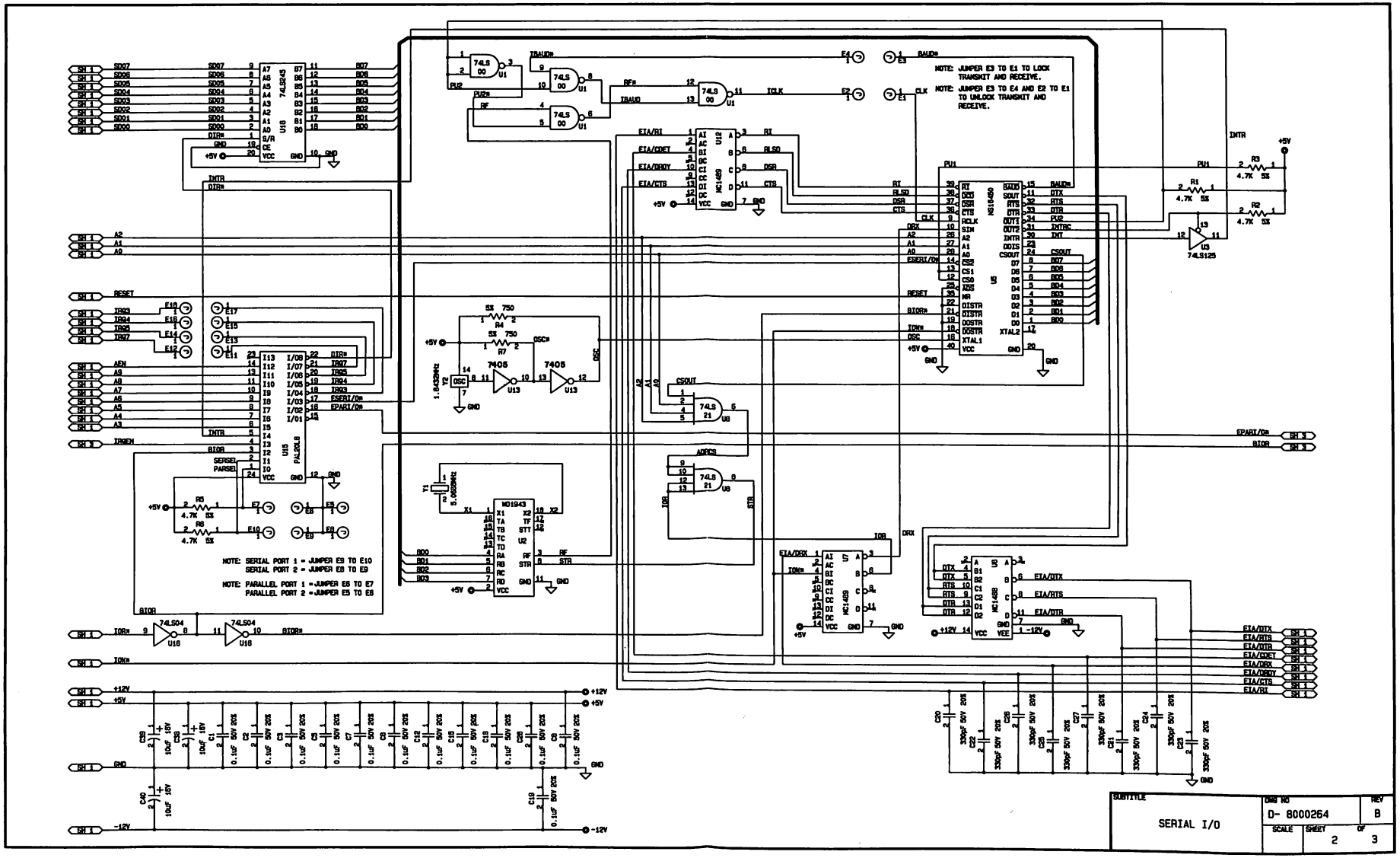
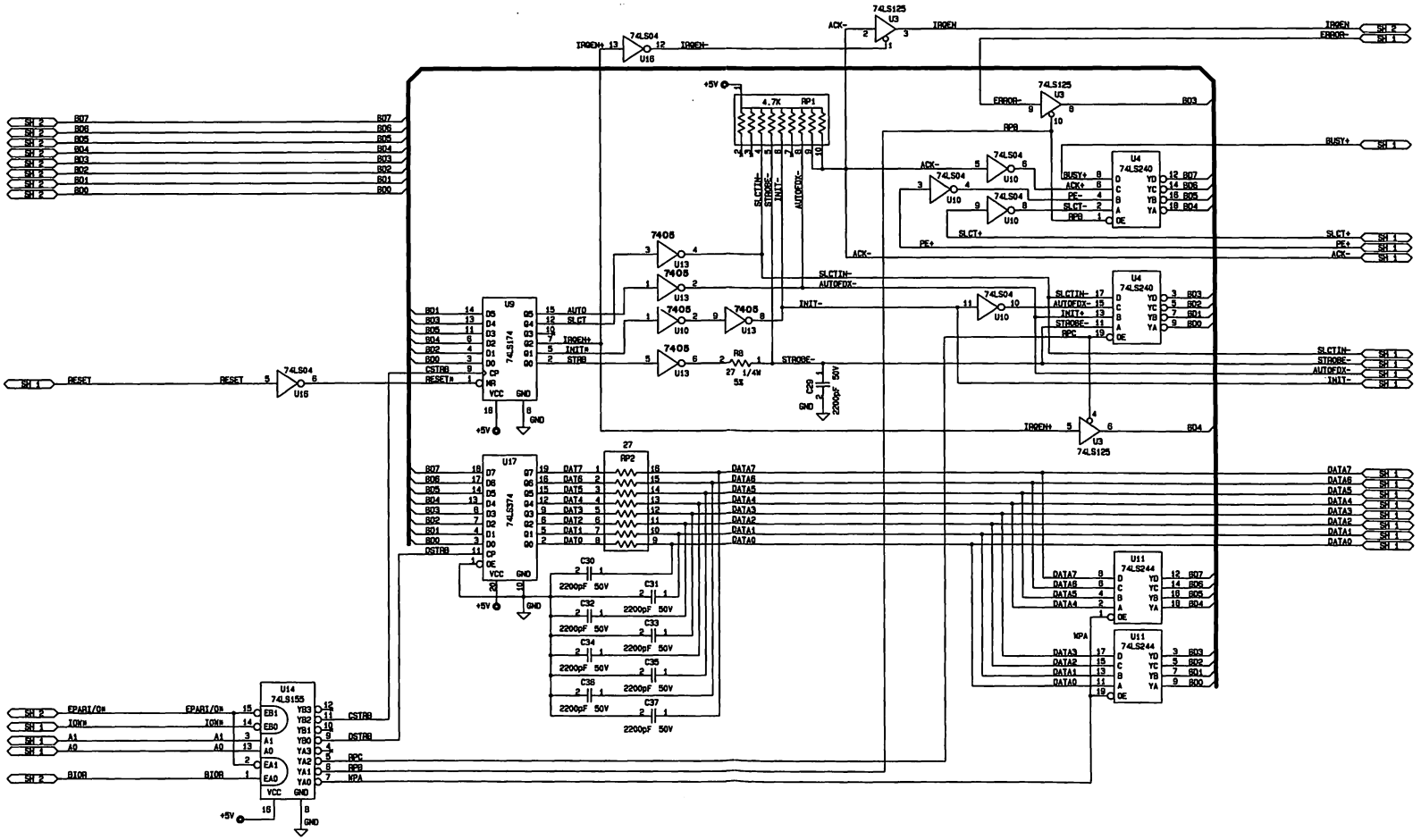
	CHECK	DATE		
	DESIGN	DATE		
	APPD	DATE		
	APPD	DATE		
629 USED ON	TANDY		DWG NO	D- 8000264
			SCALE	SHEET 1 OF 3


NOTE: JUMPER E3 TO E1 TO LOCK TRANSMIT AND RECEIVE.
NOTE: JUMPER E3 TO E4 AND E2 TO E1 TO UNLOCK TRANSMIT AND RECEIVE.
NOTE: SERIAL PORT 1 = JUMPER E9 TO E10
SERIAL PORT 2 = JUMPER E8 TO E9
NOTE: PARALLEL PORT 1 = JUMPER E6 TO E7
PARALLEL PORT 2 = JUMPER E5 TO E8
SUBTITLE
SERIAL I/O
DWG NO
D- 8000264
REV
B
SCALE
SHEET
2
OF
3



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PARALLEL I/O	D- 8000264		B
	SCALE	SHEET 3	OF 3

4000 Power Supplies

4000 Astec Power Supply

4000 Astec Power Supply
Contents

Section	Page
Introduction	1
Theory of Operation	1
Switch Setting	5

AA13265 THEORY OF OPERATION

I. Introduction

The Astec P/N AA13265 is a feed forward mode off-line switching power supply accepting either 115VAC or 230VAC nominal input and delivering four regulated DC outputs at a total of 192 watts.

II. General Theory

The AC voltage from the power is routed through the EMI filter, rectified, and develops approximately 300 VDC across the capacitive input filters. By turning on the switching transistor this 300 VDC is applied across the primary winding of the power transformer. Due to the phasing of the power transformer windings, the output rectifiers are forward biased during the primary conduction time. Energy is transferred to the output filters and then to the load.

The control circuit senses the +5 VDC and the +12 VDC outputs. It determines the point at which the turn-off circuitry disables the switching transistor.

The protection circuitry senses over and under voltage conditions on all four outputs, over current on the +/-12 VDC rails, and also generates a power good signal. Should the protection circuitry sense a fault, it shuts down the power converter until the power is recycled.

A. EMI Filter

The EMI Filter consists of a common mode choke (T201), differential mode chokes (L201, L202), line to line caps (C201, C202), and line and neutral to ground caps (C203, C204). The purpose of this circuit is to suppress conducted Electro Magnetic Interference which is being fed back into the AC mains by the power supply and the logic systems connected to the power supply.

B. Surge Protection

Because the AA13265 has a capacitive input filter, input surges can be very high due to the fact that the input capacitors act like a short circuit when power is first applied. Thermistors are designed into the input circuit to limit the turn-on surge. As current passes thru the thermistors (R202, R203, R204, R205) they heat up and consequently their resistance drops to near zero.

C. Capacitive Input Filter and Voltage Select

C205 and C206 make up the energy storage from which the power stage draws to deliver energy to the loads. These two capacitors are wired in series which allows us to tap off from the center point. When the voltage select is in the 230VAC position this center cap is left

unconnected. In this situation, the diode bridge is connected as a full wave bridge rectifier and produces a DC voltage equivalent to 1.414 times the input voltage (approximately 300VDC). When the voltage select is in the 115VAC position the center tap is connected to the neutral line. This converts the input capacitor array into a capacitive doubler, charging C206 down approximately 150VDC during the negative half-cycle of the AC waveform and charging C205 up 150VDC during the positive half-cycle of the AC waveform. This results in B+ voltage across the full capacitor array of approximately 300VDC. Consequently, the primary winding and switching transistor see the same B+ operating voltage at both voltage select positions.

D. Power Conversion

As explained in Section II, the power transistor (Q11) turns on, drawing current through the primary winding to return, developing a megnetic field with a linear current ramp. Please notice the dot location on this winding. When Q11 is on, the polarity is such that the dot and of the winding is positive. The secondary windings have the same polarity. With dots marking the positive end of the windings at this instant of the cycle, the output rectifiers (D12, D13) are forward biased and conduct Thus the energy being stored in the input caps is transferred to the output filters and the load.

A common core output choke (L2) is placed between the output rectifiers (D12,D13) and the output filters. This choke serve two purposes. One, it stores energy delivered from T1 in order to help compensate for load surges on the +12V and +5V outputs. Two, it acts as a transformer sourcing energy for the -12V and -5V outputs. The -12V and -5V outputs are derived from separate windings on L2.

The output filters are of Pi filter configuration with inductors preceded and followed by capacitors. For example, on the +5V output the filter consists of C19 followed by L4 followed by C26. The +12V and -12V outputs have similar filters. The -5V output is via a 3T regulator (IC3).

E. Control Circuit

The control circuit consists of an Astec developed chip (IC2), a pulse transformer (T2), and associated timing and reference generating components. IC2 compares the output with a generated reference voltage. When the output starts to rise beyond a preset limit, IC2 feeds a pulse thru the primary of T2. This pulse is transferred to the turn-off circuitry in the base control of switch transistor (Q11). Consequently, Q11 is quickly turned off preventing further energy transfer to the secondary of T1 on that cycle.

F. Turn-on/Turn-off Circuits

This section of the circuit consists of seven different parts.

1. The clock consists of Q6 and Q7 along with associated components. The clock timing is established by R12 and C4.

2. The clock is inhibited during Q11 on time by Q5. It is inhibited during Q11 recovery time by Q4.

3. When Q11 is turned on, positive feedback for base drive is supplied thru T3.

4. The normal method of turn-off for Q11 is via a pulsed signal fed back from the output thru T2 to the base of Q9. Q9 turns on and quickly robs Q11 of base drive, thereby turning Q11 off.

5. Q11 can also be turned off via the primary volt/second limiter. (R17, C6, Q8) or primary current limiter. When Q11 is conducting, a voltage is developed across R35. The voltage is directly proportional to the collector current of Q11. Should the current becomes too great, due to an overload on the secondary side of T1, the voltage across R35 will turn on Q8. This transistor then turns on Q10 and Q9, which turns off Q11.

6. If for some reason, control of Q11 can not be maintained, R23 which is a fusible resistor will open the collector current path preventing further damage to the power supply.

7. The shut down latch can also control Q11 turn-off by inhibiting the clock pulse. The latch is initially triggered from the secondary protection circuitry thru opto coupler (IC1). Q3 provides a regenerative latch in conjuction with the transistor side of IC1. R1, R2 and Z1 provide a regulated voltage source to keep the latch on until prime power is recycled. In addition, Q2 inhibits false triggering of the latch upon power supply startup.

G. Protection Circuit

As stated in the General Theory section, the protection circuit fulfills numerous functions.

1. +/-12V over current protection - +12V output current is drawn via transformer (T4). The secondary of T4 provides a voltage proportional to the output current that is rectified and then fed to the base of transistor (Q104). When Q104 turns on, it turns off Q105 which turns Q12 and the LED portion of IC1 on. The -12V current is sensed as a voltage potential across resistor (R48). This voltage is then applied to the base of Q104 in the same manner as the +12V sense voltage. Capacitor (C103) is used to provide surge ride thru capability on the two outputs.

2. Overvoltage protection (OVP) and undervoltage protection (UVP) are provided via Q101, Q102, Q103, Q104, Q105 and associated components. The precision reference for this circuit is generated by programmable zener IC101. Should any of the outputs be overvoltage (or be +5V undervoltage) this circuit will activate, Q12 and the LED portion of IC1 are turned on.

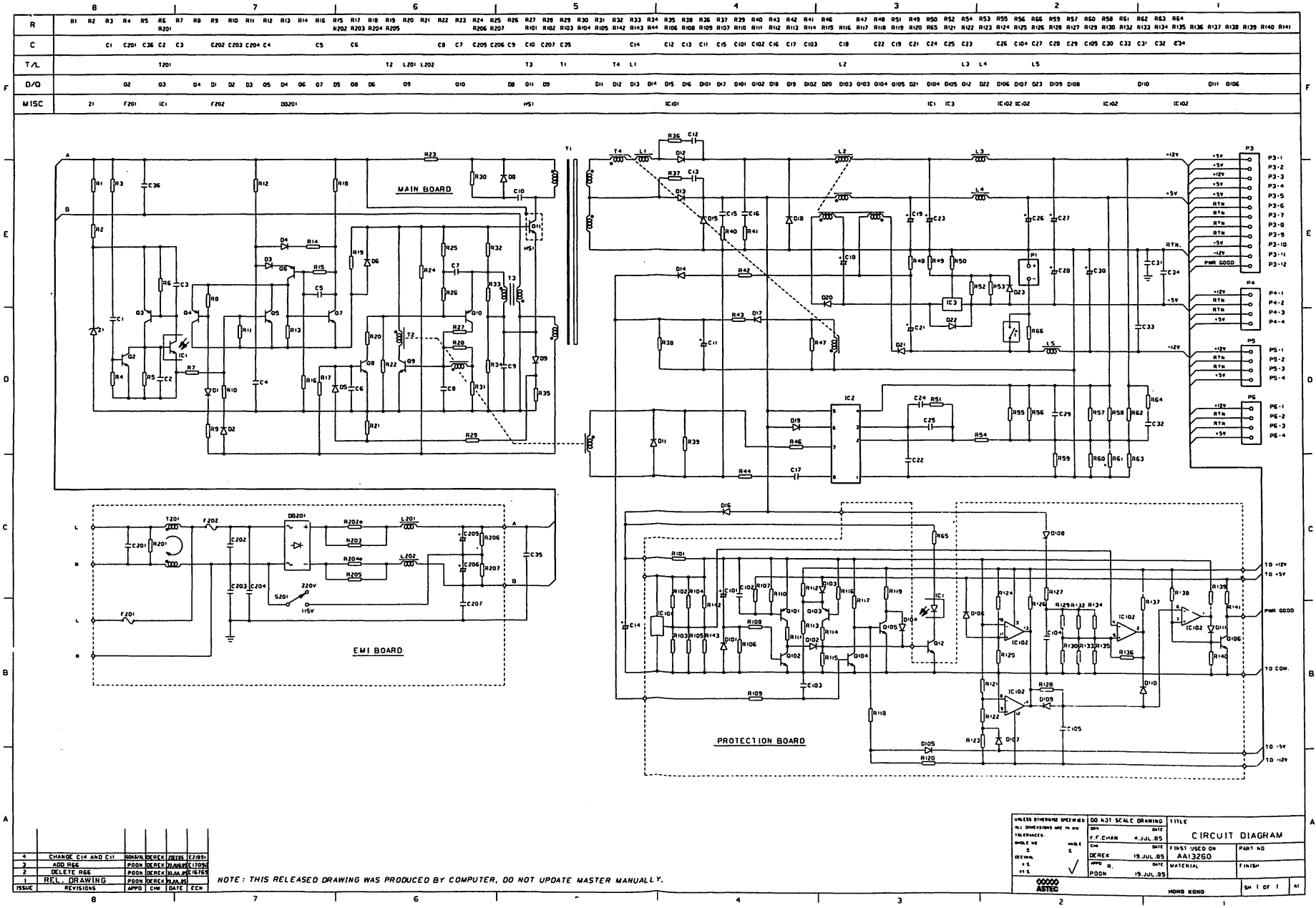
3. Power good is indicated by IC102 and its associated components. The power good signal is tied to the +5V output thru R141. This Circuit supervises the AC input voltage and the four DC output voltages. When transistor (Q106) is turned on, the power good signal is low and vice versa. The power good is low when AC input voltage or any one of the four output voltages are lower than predeterminded value.

H. Fan Control

A 12VDC fan is operated from the -12VDC output. This circuit contains a fan speed control consisting of a normally open thermal switch in parallel with a ten ohm resistor. Under normal operation, the switch is open and the fan operates at a low speed. Should the power supply become too warm, the switch closes, shorting out the resistor, and the fan operates at full speed. When the power supply cools down, the switch opens again, slowing down the fan. In this manner a nearly constant temperature is maintained within the power supply.

Astec Power Supply Switch Setting

Check to be sure that switch, S201,(on the power supplies' EMI/FILTER board) is set to the proper voltage for the location in which the system is to be installed.



ISSUE	REVISIONS	APPD	CHK	DATE	ECN
4	CHANGE C14 AND C11	SOHSAL	DEREK	7/6/85	E21051
3	ADD R66	POON	DEREK	19.JUL.85	E17095
2	DELETE R66	POON	DEREK	10.JUL.85	E16765
1	REL. DRAWING	POON	DEREK	19.JUL.85	

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER, DO NOT UPDATE MASTER MANUALLY.

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN MM TOLERANCES: SINGLE NO ± DECIMAL X ± XX ± ANGLE ±

DO NOT SCALE DRAWING

TITLE: CIRCUIT DIAGRAM

DRN Y.F.CHAN DATE 4.JUL.85

CHK DEREK DATE 19.JUL.85

APPD P. POON DATE 19.JUL.85

FIRST USED ON AA13260

PART NO

MATERIAL

FINISH

ASTEC HONG KONG

SH 1 OF 1 A1

4000 Tamura Power Supply

4000 Tamura Power Supply
Contents

Section	Page
Electrical Specifications	1
Mechanical Specifications	3
Block Diagram	5
Theory of Operation	7
Schematic	9

I. ELECTRICAL SPECIFICATION

1. INPUT VOLTAGE:
   90 to 135 VAC, 47 to 63 Hz or
   198 to 264 VAC, 47 to 63 Hz

2. INPUT SURGE CURRENT:
   Limit ---------- 50A max. (Cold start)

3. EFFICIENCY:
   At full rated load with 120/240 VAC input at 50/60Hz.
   Nominal ---------- 75%
   Limit ---------- 60% min.

4. OUTPUT VOLTAGE:

	NOMINAL VOLTAGE	REGULATION TOLERANCE	LIMITS
Vo1	+5.10 VDC	+/- 5%	4.85 to 5.35 VDC
Vo2	-5.10 VDC	+/- 10%	-5.61 to -4.59 VDC
Vo3	+12.0 VDC	+/- 5%	11.4 to 12.6 VDC
Vo4	-12.0 VDC	+/- 10%	-13.2 to -10.8 VDC
Vo5	+12 V (FAN)	+/- 10%	10.8 to 13.2 VDC

5. OUTPUT RIPPLE AND NOISE VOLTAGE:

OUTPUT		RIPPLE AND NOISE LIMIT
Vo1	+5.1V	50mV P-P
Vo2	-5.1V	100mV P-P
Vo3	+12V	100mV P-P
Vo4	-12V	150mV P-P
Vo5	+12V (fan)	500mV P-P

   Note: Ripple is defined as a composite of power line frequency component plus a high frequency component due to the power oscillator. Common mode noise which may be observed due to oscilloscope connections will be ignored.

6. OUTPUT OVER VOLTAGE PROTECTION:
   The +5.1V output shall be protected from overvoltage fault conditions by crowbar circuitry that is set to trip in the range of 5.8 to 6.6V.

7. OUTPUT STABILITY:
   The power supply must remain stable for any step load current change during any combination of input line voltage and output current loading between and including rated minimum and maximum values. The output loads may include capacitance of up to 1000 microfarads on the +5.1V output, up to 500 microfarads on either 12V output, and up to 50 microfarads on the -5.1V output.

8. OUTPUT TRANSIENT RESPONSE
For a step load current change of the positive twelve volt output between 0.6A and 6.55A the maximum voltage excursion of the positive twelve volt output shall be 500 millivolts and of the positive five volt output shall be 150 millivolts.

9. OUTPUT HOLDUP TIME
Nominal Line -------- 16 mSec. min.
Low line ---------- 10 mSec. min.

10. OUTPUT CURRENT

OUTPUT	MINIMUM LOAD	MAXIMUM LOAD
Vo1 +5.1V	5.0A	19.8A
Vo2 -5.1V	0.0A	0.3A
Vo3 +12V	0.6A	6.55A(9.0A surge for 15 seconds)
Vo4 -12V	0.0A	0.3A
Vo5 +12V (FAN)	0.3A	0.75A (Thermo Stat Terminal shorted)

(Thermostat Terminal Open)

11. OUTPUT CURRENT LIMITING
Over current protection will prevent damage to the power supply when any output is short circuited continuously with 100 milliohms or less. Each output will be internally limited to the following levels;

OUTPUT	CURRENT LIMIT LEVEL
A Vo1 +5.1V	27.5A
Vo2 -5.1V	8A
Vo3 +12V	12A
Vo4 -12V	8A

12. ENVIRONMENTAL REQUIREMENTS

Operating Temperature Range	0 degrees C to +50 degrees C
Storage Temperature Range	-40 degrees C to +85 degrees C
Operating Humidity	85% RH at 35 degrees C
Storage Humidity	95% RH at 55 degrees C

13. SAFETY REQUIREMENTS
The P.S.U. is complied with U.L. standard 114 and complied with CSA standard C22.2 No. 154-M1983 for 120/240 VAC or 120 VAC only operation.
The P.S.U. is complied with VDE 0806/8.81 (IEC 380) for Class I equipment for 120/240 VAC or 240 VAC only operation.

14. HI-POT TEST
The high potential test shall be conducted in accordance with IEC 380, subclauses 16.1 and 16.3. To perform the HI-POT test, connect all secondary outputs and secondary ground together. Also connect the input line and neutral together. Apply the voltages indicated below between the indicated points for a period of one minute.*
The HI-POT failure indicator should be set to trip at 500 micro-amperes.

Input to Output ---------- 1250V RMS, 50/60Hz or 1750 VDC
Input to Earth Ground ---------- 1250V RMS, 50/60Hz or 1750 VDC

* HI-POT TEST in production line.
Input to Output & Earth Ground -- 1500V RMS, 50/60Hz or 2120 VDC for 2 sec.

15. LINE CONDUCTED EMI
The power supply must exceed the VDE 0871/6.78 limit B for HF equipment and DF equipment with 3 dB margin at 10 KHz, increasing linearly to 8 dB at 0.10 MHz and with 8 dB margin for 0.10 to 30 MHz. Line conducted noise is measured at 120/240 VAC 50/60Hz input for all output loads from minimum to maximum. Line conducted EMI shall be mesured in a configuration representative of the intended application.

In the case of 120 VAC only operation, the power supply must exceed the FCC part 15J for Class B computing device with 3 dB margin at 450 KHz, increasing linearly to 8 dB margin from 1.0 to 30 MHz.

16. LINE TRANSIENT
The power supply shall meet the line transient requirements of IEE 472-1974 for Common Mode and Differential Mode operation.

17. OUTPUT SIGNAL
The power supply will provide a combination "ACLOW" and "RESET" signal to be called "DCOK". DCOK will be a TTL compatible signal, high is more than 2.4 VDC, low is less than 0.4 VDC, sink is more than 1.6 milliamperes when low.
The DCOK signal will go low whenever the input line voltage drops to less than 82.5 VAC (+/-2.5 VAC) for nominal input voltage of 120 VAC or less than 165 VAC (+/-5.0 VAC) for nominal input voltage of 240 VAC.
The DCOK signal will not go high untill 100 to 500 milliseconds after the +5 Volt output stabilizes at its operating value when the unit is turned on.

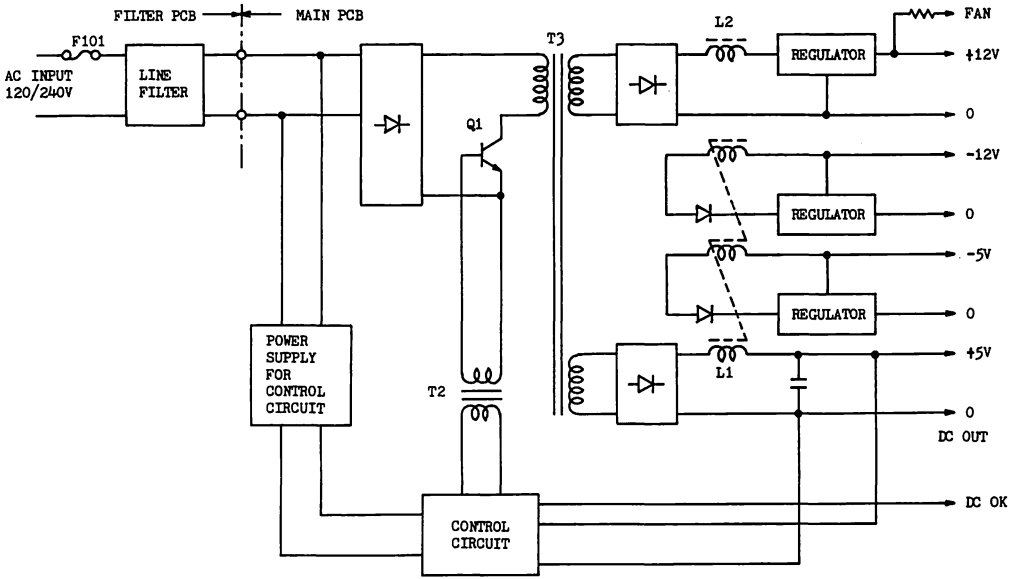
II. CIRCUIT DIAGRAM

As per attached DWG. No. 3P-M1-0373, 4P-M1-0375

III. MECHANICAL SPECIFICATIONS

1. DEMENSION : As per attached DWG. No. 3P-K1-0282

2. WEIGHT : Approx. 1.3 kg



POWER SUPPLY BLOCK DIAGRAM

A. THEORY OF OPERATION

The power supply model 8790095 is a 192 watts switching power supply. This power supply is composed of a filter PCB and main PCB.

1. Filter PCB

The filter PCB is connected to the AC line input, and a fuse is on this PCB.

The EMI Filter circuit reduces noise that leaks from the power source to the AC line.

2. Main PCB

The silicon bridge D1 rectifies the AC line to DC. The thermistors reduce the charging current of capacitors C1 and C2 when power is on.

The power converter circuit is generally called the "Forward converter". The main switching transistor Q1 chops the DC voltage of C1 and C2 at 50KHz. The chopped DC voltage is then transferred by transformer T3 to the isolated voltages and rectified to the required voltage.

+12V voltage is regulated by series dropper Q4.

-5V and -12V voltages are supplied from the flyback energy of L1, and are adjusted by the voltage regulators IC1 and IC2 (package of TO-220).

In the case of over current fault, the increased voltage of the current transformer CT1 or CT2 is fed to the control PCB.

- Control PCB (sub board on the main PCB)

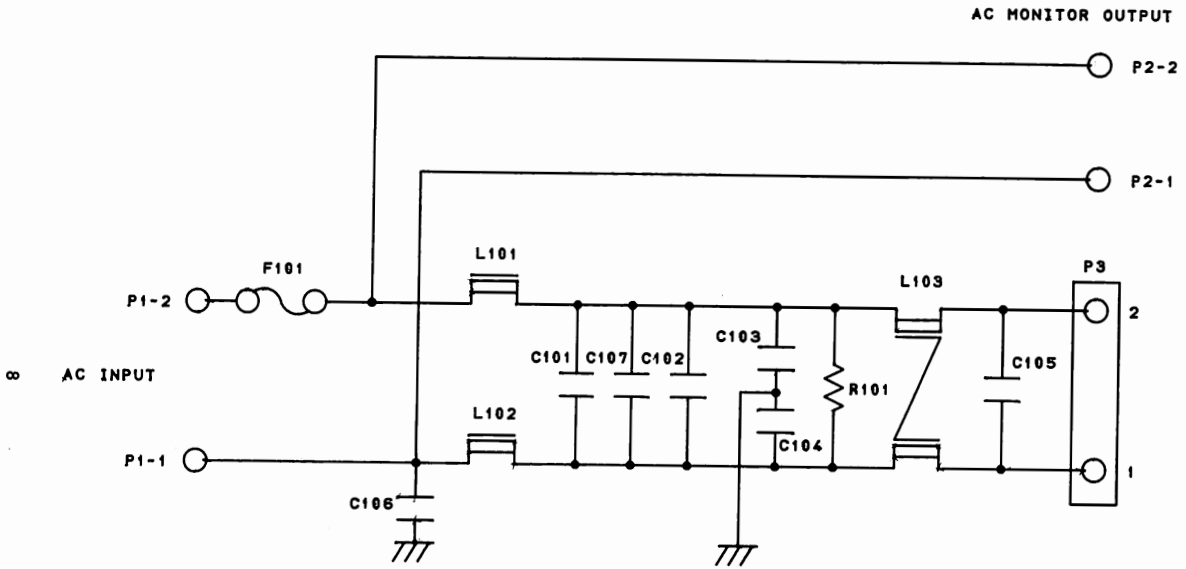
The control PCB contains the output voltage control circuit, +5V over voltage protection circuit, and the power good signal (to be called "DC-OK") circuit.

IC1 is a 16-pin DIP package which incorporates the functions of a pulse-width-modulation control circuit and is provided the voltage variation of +5V output.

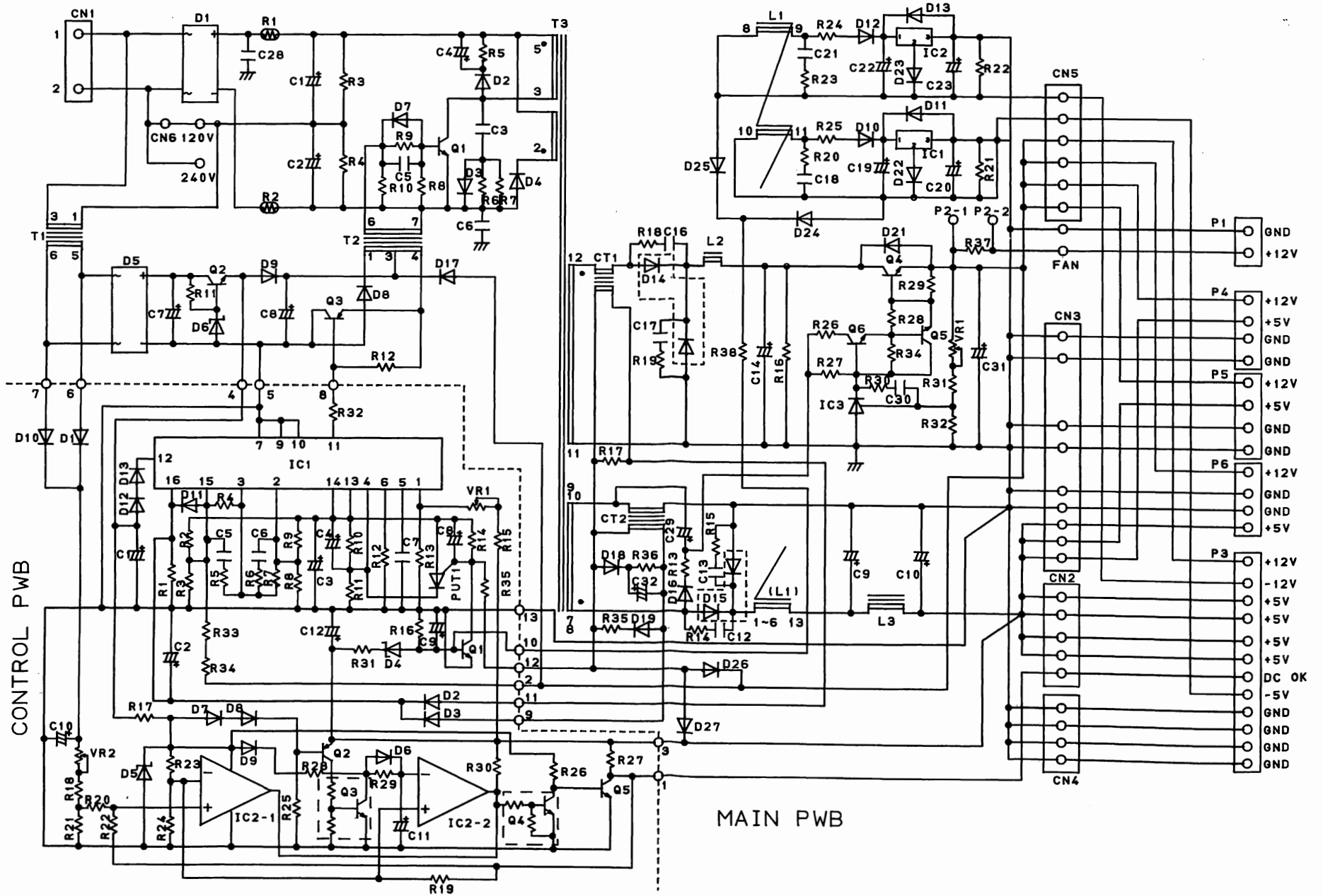
The main switching transistor (on the main PCB) is controlled by the pulse from IC1.

In the case of over voltage fault, the pulse oscillator in IC1 is stopped by PUT1 under the control of zener diode D4.

IC2 is a voltage comparator IC for the power good signal circuit.



model no. 8790095 LINE FILTER



model no. 8790095

4000 Keyboard

KEYBOARD SPECIFICATION

20425

FOR THE "101" KEYBOARD (E03370051)

Thomas E. Katona — 3-10-87

Engineer — Date

R. McVean — 3/11/87

Approved — Date

CONTENTS

		PAGE
1.0	GENERAL	5
2.0	SCOPE	5
3.0	APPLICABLE DOCUMENTS	5
4.0	MECHANICAL REQUIREMENTS	5
4.1	Switch Profiles	5
4.2	Key Layout, Legends, and Colors	5
4.3	Keyswitch.	9
4.3.1	Total Travel	9
4.3.2	Pre Travel	9
4.3.3	Force	9
4.3.4	Breakover Feedback	9
5.0	FUNCTIONAL REQUIREMENTS	9
5.1	Scan Codes	9
5.2	Protocol	23
5.2.1	Communication Mode 1 (PC/XT)	23
5.2.2	Communication Mode 2 (AT)	24
5.2.3	Commands From The Keyboard To The System	25
5.2.4	Commands From The System To The Keyboard	27
5.3	Key Rollover	31
5.4	Power-Up and Self Test	31
5.5	Autorepeat	31
5.6	Buffering	31
5.7	Mode Switch Settings	32
5.8	Auto-Discrimination	32
5.9	LED Indicators	33
5.10	Software "Watch Dog"	33
6.0	ELECTRICAL REQUIREMENTS	33
6.1	Signal Connector	34
6.2	Chassis Ground	34
6.3	Power Requirement	34

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		PAGE
7.0	ENVIRONMENTAL REQUIREMENTS	34
7.1	Temperature	34
7.2	Relative Humidity	34
7.3	Shock	34
7.4	Vibration	34
7.5	Altitude	34
7.6	Electrostatic Immunity (ESD)	35
7.7	EMI/RFI	35
7.8	Safety	35
8.0	RELIABILITY	35
8.1	Mean Time Before Failure (MTBF)	35
8.2	Switch Life	35
8.3	Maintainability	35

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1.0 GENERAL

The "101" keyboard (E03370051) shall be a direct, plug compatible replacement for the 101 IBM* PC, XT, AT, and compatible personal computer keyboards. No software modification or special interfaces shall be needed by the user.

2.0 SCOPE

This specification defines the functional, mechanical, electrical, environmental, and reliability characteristics of the E03370051 keyboard.

Specifically, the keyboard is encoded such that all keys produce a unique output code upon switch depression and a similar but unique output code upon switch release. The communication with the host system is via a synchronous serial link. The keytop layout, switch encoding, and serial communication are all compatible with, but not identical to, the IBM PC, XT, and AT keyboards.

3.0 APPLICABLE DOCUMENTS

0115562 Factory Test Procedure
36-02464 ESD Test Procedure, Part 18

4.0 MECHANICAL REQUIREMENTS

4.1 Switch Profiles

Figure 1 shows the keyboard profile.

4.2 Keytop Layout, Legends And Colors

Figure 2 illustrates the keytop layout and appropriate legends.

Table 1 specifies the color for each keytop. The Key Tronic color codes used are:

WA - Fog (Marbon P/N 2500)
GE - Sea Mist (Marbon P/N 20779).

* IBM PC, XT, and AT are trademarks of the International Business Machine Corporation.

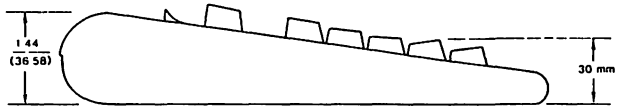

Figure 1: Keyboard Profile

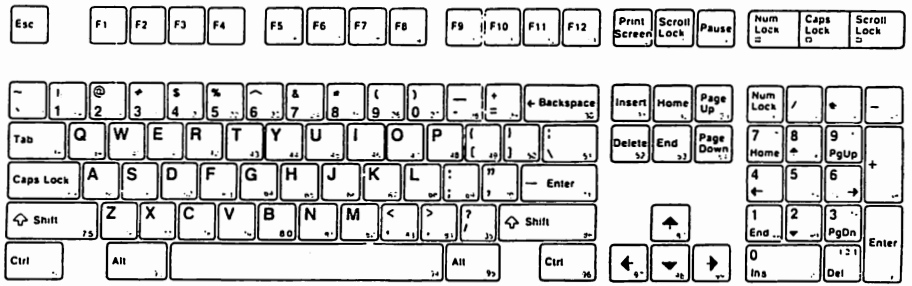

Figure 2: Keytop Layout and Legends

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TABLE 1

KEYTOP COLOR CODES

Key Station	Color	Key Station	Color	Key Station	Color
1	GE	34	GE	67	WA
2	WA	35	GE	68	WA
3	WA	36	GE	69	WA
4	WA	37	GE	70	WA
5	WA	38	GE	71	GE
6	GE	39	WA	72	WA
7	GE	40	WA	73	WA
8	GE	41	WA	74	WA
9	GE	42	WA	75	GE
10	WA	43	WA	76	WA
11	WA	44	WA	77	WA
12	WA	45	WA	78	WA
13	WA	46	WA	79	WA
14	GE	47	WA	80	WA
15	GE	48	WA	81	WA
16	GE	49	WA	82	WA
17	WA	50	WA	83	WA
18	WA	51	WA	84	WA
19	WA	52	GE	85	WA
20	WA	53	GE	86	GE
21	WA	54	GE	87	GE
22	WA	55	WA	88	WA
23	WA	56	WA	89	WA
24	WA	57	WA	90	WA
25	WA	58	GE	91	GE
26	WA	59	GE	92	GE
27	WA	60	WA	93	GE
28	WA	61	WA	94	WA
29	WA	62	WA	95	GE
30	GE	63	WA	96	GE
31	GE	64	WA	97	GE
32	GE	65	WA	98	GE
33	GE	66	WA	99	GE
				100	WA
				101	WA

4.3 Keyswitch

4.3.1 Total Travel - 0.150" ± .020"

4.3.2 Pre Travel - 0.075" ± 0.015"

4.3.3 Force - All keyswitches shall utilize a 2.0 oz. rubber sleeve.

4.3.4 Breakover Feedback - The keyswitches shall utilize a sensory feedback to assure the operator that the key has been depressed beyond its operating point.

5.0 FUNCTIONAL REQUIREMENTS

5.1 Scan Codes

The keyboard shall generate a unique Hex scan code for each and every keyswitch including codes for both depression (make) and release (break). For the AT, the break code is the same as the make code preceded by "FO". The keyswitch to scan code assignments are illustrated and listed on the following pages:

- Figure 3 shows the PC/XT scan codes and a detailed listing is provided in Table 2 (Scan Set 1).
- Figure 4 shows the AT scan codes and detailed listings are provided in Table 3 (Scan Set 2) and Table 4 (Scan Set 3).

Figure 3: PC/XT Scan Codes

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TABLE 2

SCAN SET 1, XT SCAN CODES

KEY NUMBER	MAKE CODE	BREAK CODE
1	01	81
2	3B	BB
3	3C	BC
4	3D	BD
5	3E	BE
6	3F	BF
7	40	C0
8	41	C1
9	42	C2
10	43	C3
11	44	C4
12	57	D7
13	58	D8
15	46	C6
17	29	A9
18	02	82
19	03	83
20	04	84
21	05	85
22	06	86
23	07	87
24	08	88
25	09	89
26	0A	8A
27	0B	8B
28	0C	8C
29	0D	8D
30	0E	8E
34	45	C5
36	37	B7
37	4A	CA
38	0F	8F
39	10	90
40	11	91
41	12	92
42	13	93
43	14	94
44	15	95
45	16	96
46	17	97
47	18	98
48	19	99
49	1A	9A
50	1B	9B

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TABLE 2 (Continued)

SCAN SET 1, XT SCAN CODES

KEY NUMBER	MAKE CODE	BREAK CODE
51	2B	AB
55	47	C7
56	48	C8
57	49	C9
58	4E	CE
59	3A	BA
60	1E	9E
61	1F	9F
62	20	A0
63	21	A1
64	22	A2
65	23	A3
66	24	A4
67	25	A5
68	26	A6
69	27	A7
70	28	A8
71	1C	9C
72	4B	CB
73	4C	CC
74	4D	CD
75	2A	AA
76	2C	AC
77	2D	AD
78	2E	AE
79	2F	AF
80	30	B0
81	31	B1
82	32	B2
83	33	B3
84	34	B4
85	35	B5
86	36	B6
88	4F	CF
89	50	D0
90	51	D1
91	E0 1C	E0 9C
92	1D	9D
93	38	B8
94	39	B9
95	E0 38	E0 B8
96	E0 1D	E0 9D
100	52	D2
101	53	D3

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TABLE 2 (Continued)

SCAN SET 1, XT SCAN CODES

KEY NUMBER	BASE CASE, OR SHIFT+NUM LOCK MAKE/BREAK	SHIFT CASE MAKE/BREAK	NUM LOCK ON MAKE/BREAK	
31		E0 52 /E0 D2	E0 AA E0 52 /E0 D2 E0 2A	E0 2A E0 52 /E0 D2 E0 AA
32		E0 47 /E0 C7	E0 AA E0 47 /E0 C7 E0 2A	E0 2A E0 47 /E0 C7 E0 AA
33		E0 49 /E0 C9	E0 AA E0 49 /E0 C9 E0 2A	E0 2A E0 49 /E0 C9 E0 AA
52		E0 53 /E0 D3	E0 AA E0 53 /E0 D3 E0 2A	E0 2A E0 53 /E0 D3 E0 AA
53		E0 4F /E0 CF	E0 AA E0 4F /E0 CF E0 2A	E0 2A E0 4F /E0 CF E0 AA
54		E0 51 /E0 D1	E0 AA E0 51 /E0 D1 E0 2A	E0 2A E0 51 /E0 D1 E0 AA
87		E0 48 /E0 C8	E0 AA E0 48 /E0 C8 E0 2A	E0 2A E0 48 /E0 C8 E0 AA
97		E0 4B /E0 CB	E0 AA E0 4B /E0 CB E0 2A	E0 2A E0 4B /E0 CB E0 AA
98		E0 50 /E0 D0	E0 AA E0 50 /E0 D0 E0 2A	E0 2A E0 50 /E0 D0 E0 AA
99		E0 4D /E0 CD	E0 AA E0 4D /E0 CD E0 2A	E0 2A E0 4D /E0 CD E0 AA

If the left Shift key is held down, the AA / 2A shift break/make codes are sent with the other scan codes. If the right Shift key is held down, B6 / 36 is sent. If both Shift keys are down, both sets of codes are sent with the other scan code.

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TABLE 2 (continued)

SCAN SET 1, XT SCAN CODES

KEY NUMBER	SCAN CODE MAKE / BREAK	SHIFT CASE MAKE / BREAK
35	E0 35/E0 B5	E0 AA E0 35 / E0 B5 E0 2A

If the left Shift key is held down, the AA / 2A shift make/break codes are sent with the other scan codes. If the right Shift key is held down, B6 / 36 is sent. If both Shift keys are down, both sets of codes are sent with the other scan codes.

KEY NUMBER	SCAN CODE MAKE / BREAK	CTRL CASE, SHIFT CASE MAKE / BREAK	ALT CASE MAKE / BREAK
14	E0 2A E0 37 /E0 B7 E0 AA	E0 37 / E0 E7	54 / D4

KEY NUMBER	MAKE CODE	CTRL KEY PRESSED
16	E1 1D 45 E1 9D C5	E0 46 E0 C6

This key is not typematic. All associated scan codes occur on the make of the key.

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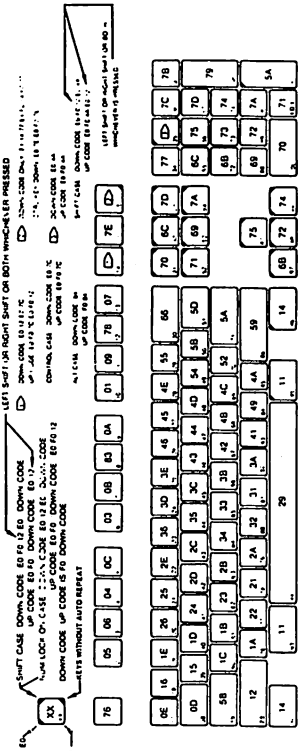

Figure 4: AT Scan Codes

TABLE 3

SCAN SET 2, AT SCAN CODES

KEY NUMBER	MAKE CODE	BREAK CODE
1	76	F0 76
2	05	F0 05
3	06	F0 06
4	04	F0 04
5	0C	F0 0C
6	03	F0 03
7	0B	F0 0B
8	83	F0 83
9	0A	F0 0A
10	01	F0 01
11	09	F0 09
12	78	F0 78
13	07	F0 07
15	7E	F0 7E
17	0E	F0 0E
18	16	F0 16
19	1E	F0 1E
20	26	F0 26
21	25	F0 25
22	2E	F0 2E
23	36	F0 36
24	3D	F0 3D
25	3E	F0 3E
26	46	F0 46
27	45	F0 45
28	4E	F0 4E
29	55	F0 55
30	66	F0 66
34	77	F0 77
36	7C	F0 7C
37	7B	F0 7B
38	0D	F0 0D
39	15	F0 15
40	1D	F0 1D
41	24	F0 24
42	2D	F0 2D
43	2C	F0 2C
44	35	F0 35
45	3C	F0 3C
46	43	F0 43
47	44	F0 44
48	4D	F0 4D
49	54	F0 54
50	5B	F0 5B

TABLE 3

SCAN SET 2, AT SCAN CODES

KEY NUMBER	MAKE CODE	BREAK CODE
51	5D	F0 5D
55	6C	F0 6C
56	75	F0 75
57	7D	F0 7D
58	79	F0 79
59	58	F0 58
60	1C	F0 1C
61	1B	F0 1B
62	23	F0 23
63	2B	F0 2B
64	34	F0 34
65	33	F0 33
66	3B	F0 3B
67	42	F0 42
68	4B	F0 4B
69	4C	F0 4C
70	52	F0 52
71	5A	F0 5A
72	6B	F0 6B
73	73	F0 73
74	74	F0 74
75	12	F0 12
76	1A	F0 1A
77	22	F0 22
78	21	F0 21
79	2A	F0 2A
80	32	F0 32
81	31	F0 31
82	3A	F0 3A
83	41	F0 41
84	49	F0 49
85	4A	F0 4A
86	59	F0 59
88	69	F0 69
89	72	F0 72
90	7A	F0 7A
91	E0 5A	E0 F0 5A
92	14	F0 14
93	11	F0 11
94	29	F0 29
95	E0 11	E0 F0 11
96	E0 14	E0 F0 14
100	70	F0 70
101	71	F0 71

TABLE 3 (Continued)

SCAN SET 2, AT SCAN CODES

KEY NUMBER	BASE CASE, OR SHIFT+NUM LOCK MAKE/BREAK	SHIFT CASE MAKE/BREAK	NUM LOCK ON MAKE/BREAK
31	E0 70 / E0 F0 70	E0 F0 12 E0 70 /E0 F0 70 E0 12	E0 12 E0 70 /E0 F0 70 E0 F0 12
32	E0 6C / E0 F0 6C	E0 F0 12 E0 6C /E0 F0 6C E0 12	E0 12 E0 6C /E0 F0 6C E0 F0 12
33	E0 7D / E0 F0 7D	E0 F0 12 E0 7D /E0 F0 7D E0 12	E0 12 E0 7D /E0 F0 7D E0 F0 12
52	E0 71 / E0 F0 71	E0 F0 12 E0 71 /E0 F0 71 E0 12	E0 12 E0 71 /E0 F0 71 E0 F0 12
53	E0 69 / E0 F0 69	E0 F0 12 E0 69 /E0 F0 69 E0 12	E0 12 E0 69 /E0 F0 69 E0 F0 12
54	E0 7A / E0 F0 7A	E0 F0 12 E0 7A /E0 F0 7A E0 12	E0 12 E0 7A /E0 F0 7A E0 F0 12
87	E0 75 / E0 F0 75	E0 F0 12 E0 75 /E0 F0 75 E0 12	E0 12 E0 75 /E0 F0 75 E0 F0 12
97	E0 6B / E0 F0 6B	E0 F0 12 E0 6B /30 F0 6B E0 12	E0 12 E0 6B /E0 F0 6B E0 F0 12
98	E0 72 / E0 F0 72	E0 F0 12 E0 72 /E0 F0 72 E0 12	E0 12 E0 72 /E0 F0 72 E0 F0 12
99	E0 74 / E0 F0 74	E0 F0 12 E0 74 /E0 F0 74 E0 12	E0 12 E0 74 /E0 F0 74 E0 F0 12

If the left Shift key is held down, the F0 12/12 shift make/break codes are sent with the other scan codes. If the right Shift key is held down, F0 59/59 is sent. If both Shift keys are down, both sets of codes are sent with the other scan code.

TABLE 3 (Continued)

SCAN SET 2, AT SCAN CODES

KEY NUMBER	SCAN CODE MAKE / BREAK	SHIFT CASE MAKE / BREAK
35	E0 4A/E0 F0 4A	E0 F0 12 E0 4A / E0 F0 4A E0 12

If the left Shift key is held down, the F0 12/12 shift make/break codes are sent with the other scan codes. If the right Shift key is held down, F0 59/59 is sent. If both Shift keys are down, both sets of codes are sent with the other scan codes.

KEY NUMBER	SCAN CODE MAKE / BREAK	CTRL CASE, SHIFT CASE MAKE / BREAK	ALT CASE MAKE / BREAK
14	E0 12 E0 7C /E0 F0 7C E0 F0 12	E0 7C / E0 F0 7C	84/F0 84

KEY NUMBER	MAKE CODE	CTRL KEY PRESSED
16	E1 14 77 E1 F0 14 F0 77	E0 7E E0 F0 7E

This key is not typematic. All associated scan codes occur on the make of the key.

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TABLE 4

SCAN SET 3, AT DEFAULT KEY STATE

KEY NUMBER	MAKE CODE	BREAK CODE	DEFAULT KEY STATE
1	08	F0 08	Make only
2	07	F0 07	Make only
3	0F	F0 0F	Make only
4	17	F0 17	Make only
5	1F	F0 1F	Make only
6	27	F0 27	Make only
7	2F	F0 2F	Make only
8	37	F0 37	Make only
9	3F	F0 3F	Make only
10	47	F0 47	Make only
11	4F	F0 4F	Make only
12	56	F0 56	Make only
13	5E	F0 5E	Make only
14	57	F0 57	Make only
15	5F	F0 5F	Make only
16	62	F0 62	Make only
17	0E	F0 0E	Typematic
18	16	F0 16	Typematic
19	1E	F0 1E	Typematic
20	26	F0 26	Typematic
21	25	F0 25	Typematic
22	2E	F0 2E	Typematic
23	36	F0 36	Typematic
24	3D	F0 3D	Typematic
25	3E	F0 3E	Typematic
26	46	F0 46	Typematic
27	45	F0 45	Typematic
28	4E	F0 4E	Typematic
29	55	F0 55	Typematic
30	66	F0 66	Typematic
31	67	F0 67	Make only
32	6E	F0 6E	Make only
33	6F	F0 6F	Make only
34	76	F0 76	Make only
35	77	F0 77	Make only
36	7E	F0 7E	Make only
37	84	F0 84	Make only
38	0D	F0 0D	Typematic
39	15	F0 15	Typematic
40	1D	F0 1D	Typematic
41	24	F0 24	Typematic
42	2D	F0 2D	Typematic
43	2C	F0 2C	Typematic
44	35	F0 35	Typematic

TABLE 4 (Continued)

SCAN SET 3, AT DEFAULT KEY STATE

KEY NUMBER	MAKE CODE	BREAK CODE	DEFAULT KEY STATE
45	3C	F0 3C	Typematic
46	43	F0 43	Typematic
47	44	F0 44	Typematic
48	4D	F0 4D	Typematic
49	54	F0 54	Typematic
50	5B	F0 5B	Typematic
51	5C	F0 5C	Typematic
52	64	F0 64	Typematic
53	65	F0 65	Make only
54	6D	F0 6D	Make only
55	6C	F0 6C	Make only
56	75	F0 75	Make only
57	7D	F0 7D	Make only
58	7C	F0 7C	Typematic
59	14	F0 14	Make/Break
60	1C	F0 1C	Typematic
61	1B	F0 1B	Typematic
62	23	F0 23	Typematic
63	2B	F0 2B	Typematic
64	34	F0 34	Typematic
65	33	F0 33	Typematic
66	3B	F0 3B	Typematic
67	42	F0 42	Typematic
68	4B	F0 4B	Typematic
69	4C	F0 4C	Typematic
70	52	F0 52	Typematic
71	5A	F0 5A	Typematic
72	6B	F0 6B	Make only
73	73	F0 73	Make only
74	74	F0 74	Make only
75	12	F0 12	Make/Break
76	1A	F0 1A	Typematic
77	22	F0 22	Typematic
78	21	F0 21	Typematic
79	2A	F0 2A	Typematic
80	32	F0 32	Typematic
81	31	F0 31	Typematic
82	3A	F0 3A	Typematic
83	41	F0 41	Typematic
84	49	F0 49	Typematic
85	4A	F0 4A	Typematic
86	59	F0 59	Make/Break
87	63	F0 63	Typematic
88	69	F0 69	Make only

TABLE 4 (Continued)

SCAN SET 3, AT DEFAULT KEY STATE

KEY NUMBER	MAKE CODE	BREAK CODE	DEFAULT KEY STATE
89	72	F0 72	Make only
90	7A	F0 7A	Make only
91	79	F0 79	Make only
92	11	F0 11	Make/Break
93	19	F0 19	Make/Break
94	29	F0 29	Typematic
95	39	F0 39	Make only
96	58	F0 58	Make only
97	61	F0 61	Typematic
98	60	F0 60	Typematic
99	6A	F0 6A	Typemetic
100	70	F0 70	Make only
101	71	F0 71	Make only

5.2 Protocol

5.2.1 Communication Mode 1 (PC/XT)

The keyboard shall communicate with the system using synchronous serial protocol. When no communication is in process, the keyboard holds the data line low and the clock line high. Transmissions consist of a 10 bit data word shown as follows (terminology assumes positive logic.):

0	1	x	x	x	x	x	x	x	x
Keyboard	Start	B0	B1	B2	B3	B4	B5	B6	B7

The system may hold the clock line low for a minimum of 12.5 milliseconds to initiate a keyboard reset (see Power-Up Sequence). The keyboard shall not attempt to transmit data while the clock line is being held by the system.

Before initiating a transmission, the keyboard lowers the clock line as a Request To Send (RTS). The keyboard then checks the state of the data line. If the system is holding the data line low, then the keyboard interface is inhibited. The keyboard shall retain the keycode in the buifer, return the clock and data lines to the idle state, and resume scanning until the interface is enabled.

If the interface is enabled, the keyboard shall transmit its data in the previously described format. Data is valid during the time that the clock is high and for a minimum of 2.5 microseconds after the falling edge of the clock. See Figure 5 for the timing diagram.

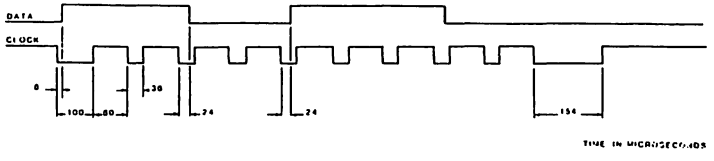

Figure 5: PC/XT Timing Diagram

5.2.2 Communication Mode 2 (AT)

The keyboard shall communicate with the system using synchronous serial protocol. This communication is bidirectional, with the keyboard clocking all data transfers (the terminology assumes positive logic).

When there is no communication in process, the clock and data lines shall idle in the high state. Transmissions consist of an 11 bit data word shown below and in Figure 6.

0	x	x	x	x	x	x	x	x	P	1
Start	B0	B1	B2	B3	B4	B5	B6	B7	Parity	Stop
(Low)	(LSB)							(MSB)	(Odd)	(High)

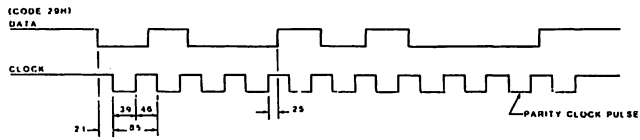

Figure 6A Keyboard to System

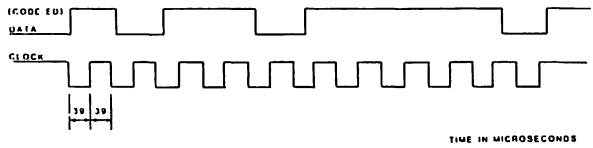

Figure 6B System to Keyboard

Figure 6: AT Timing Diagram

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5.2.3 Commands From The Keyboard To The System

Prior to initiating a transmission of a code, the keyboard shall first check the state of the clock and data lines. If the clock line is low, then the keyboard interface is inhibited, and the code shall be kept in the keyboard buffer until the inhibit is removed. If the clock line is high and the data line is low, then the host is issuing an RTS, and the keyboard shall keep the code in the keyboard buffer and prepare to receive data.

If the keyboard interface is enabled and no RTS is detected, then the keyboard shall initiate a transmission by sending a low start bit, followed by the rest of the code. Keyboard data shall be valid prior to the falling edge of the clock and after the rising edge of the clock. See Figure 6A for the timing diagram.

During the transmission of a code, the keyboard shall check the state of the clock line at intervals of not less than 60 microseconds. If the clock line is detected low prior to the rising edge of the parity bit clock, then a data collision occurs. The keyboard will stop transmission, place the code back in the keyboard buffer, and prepare to respond to the next action by the system.

The keyboard shall send commands to the system. The commands and their function are listed as follows:

<u>00 hex - Keyboard Buffer Overrun, Scan Sets 2 or 3</u>

If the keyboard buffer overflows, and the keyboard is currently in Mode 2, then it will issue a hex 00 to indicate this condition.

<u>AA hex - Self test passed</u>

This command is issued after successful completion of the keyboard self test. The self test may be initiated by a Reset command from the system, or by a Power On Reset.

<u>EE hex - Echo</u>

The Echo command is sent in response to an Echo command from the system.

<u>FA hex - Acknowledge</u>

The keyboard sends an Acknowledge in response to any valid command from the system except for Resend and Echo.

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FC hex - Self Test Failure

This response is issued by the keyboard in place of the AA hex if the keyboard detects a problem during its self test. Refer to Power-Up and Self Test, Paragraph 5.4.

FE hex - Resend

The keyboard issues a Resend command in response to inputs which have parity or framing errors, or if the input is invalid.

FF hex - Keyboard Buffer Overrun, Scan Set 1

If the keyboard is in Communication Mode 1 and the keycode buffer overflows, then it indicates this situation to the system by transmitting FF hex to the host.

83AB hex - Keyboard ID

The keyboard ID is a 2 byte number issued in response to a Read ID command from the system. The keyboard responds to a Read ID with an Acknowledge, followed by the ID bytes. After the output of the ID bytes, the keyboard begins scanning.

5.2.4 Commands From The System To The Keyboard

Before the system can transmit data to the keyboard, it must first check to see if the keyboard is sending data. If the keyboard is sending, and the data is past the parity clock pulse, then the system must accept that data prior to initiating its own transmission.

If the keyboard data string has not yet reached the tenth clock pulse, or it is not currently transmitting data, then the system takes control by lowering the clock line for at least 60 microseconds, then releasing it after clamping the data line low for a start bit. The keyboard will respond to the RTS within 5 milliseconds by clocking the start bit in. The keyboard will continue clocking data as shown in the timing diagram (Figure 6B). The system should insure that the data is valid before the rising edge of the keyboard clock pulse and after the falling edge.

After the parity bit the system should raise the data line for a stop bit. The keyboard shall check for the "1" stop bit, then clamp the data line low prior to clocking the stop bit. This action signals the system that the keyboard has received its data. If the system has not raised the data line, then the keyboard receives a framing error and shall continue to clock until the data line is raised by the system. After receiving either a framing or parity error the keyboard will respond by issuing a RESEND.

All commands from the system require some sort of a response from the keyboard. This keyboard response shall occur within 20 milliseconds of the receipt of the command.

The following commands may be sent to the keyboard at any time, following the protocol described in Paragraph 5.2.3. These commands are only valid in Communication Mode 2. The keyboard shall issue a response within 20 milliseconds of the receipt of any of these commands except for Reset. The commands and their function are listed as follows:

ED hex - Set Status Indicators

The keyboard shall respond to this command with an Acknowledge, stop scanning and wait for the status byte. The status byte has a bit for each of the LED's on the keyboard. If the bit is set (1) then the LED is on, if it is clear (0) then the corresponding LED is off. Default disable and Set disable commands do not affect status indicators.

Bit 0 corresponds to the Scroll Lock indicator, bit 1 is Num Lock and bit 2 is Caps Lock. The rest of the byte must be zeros.

After responding to the command the keyboard shall resume scanning if it was previously enabled. If, instead of a status byte, the system follows the Set Status Indicators command with a valid command, no change to the LED's occur and the keyboard executes the new command instead.

EE hex - Echo

This is provided for diagnostic purposes. The keyboard shall respond with EE instead of Acknowledge.

F0 hex - Select Scan Set

This is used to select one of the three Scan Sets or tell the system which Scan Set is currently in use. After receiving this command, the keyboard shall transmit an Acknowledge to the system. The system then sends the request byte and the keyboard transmits an Acknowledge. A request byte value of 00 hex will cause the keyboard to respond with the Scan Set currently in use. A request byte value of 01 hex selects Scan Set 1, 02 hex selects Scan Set 2, 03 hex selects Scan Set 3.

The keyboard returns to the scanning state it was in before the select Scan Set.

F2 hex - Read ID

This command causes the keyboard to send two identification bytes (83AB). The keyboard shall send an Acknowledge and stop scanning. Then the two ID bytes are sent. The second byte follows the first byte within 500 microseconds. After both identification bytes are sent the keyboard begins scanning.

F3 hex - Set Typematic Values

This is a two-byte command to change the typematic rate and delay, with each byte answered by the keyboard with an Acknowledge. The second byte is the delay byte and defines both the delay before typematic action as well as the typematic rate. Bits 0 (LSB), 1, 2, 3 and 4 define the typematic rate by the following equation:

```
Period = (8+B0) * (2**B1) * 0.00417
** indicates exponentiation

B0 = Binary value of bits 2, 1, and 0
B1 = Binary value of bits 4 and 3
```


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The delay is defined as follows:

T = (BJ+1) * 250 milliseconds

BJ = Binary value of bits 6 and 5
Bit 7 (MSB) is always 0

F4 hex - Enable

This command enables the keyboard. The keyboard shall respond with an Acknowledge, clear the output buffer, clear the last repeating key, and begin scanning.

F5 hex - Default Disable

The keyboard stops scanning and resets to default status. The keyboard transmits an Acknowledge, clears the output buffer, sets the default key types for Scan Set 3, sets default repeat rate/delay, and clears last repeating key.

F6 hex - Set Default

This command resets the keyboard to Power-Up state. The keyboard responds with an Acknowledge, clears the output buffer, set default key types for Scan Set 3, sets default repeat rate/delay, and clears the last typematic key.

F7 hex - Set All Keys - Typematic

F8 hex - Set All Keys - Make/Break

F9 hex - Set All Keys - Make

FA hex - Set All Keys - Typematic/make/Break

See common explanation below.

The keyboard shall send an Acknowledge, clear the output buffer, set all keys to the type requested by the command, and continue scanning if it was previously enabled. These commands can be sent using any scan set but affect Scan Set 3 operation only.

FB hex - Set Key Type - Typematic

FC hex - Set Key Type - Make/Break

FD hex - Set Key Type - Make

See common explanation below.

The keyboard shall send an Acknowledge, clear the output buffer, and wait for the key scan code. The key scan code identifies which key will be set to the function requested by the command. Only Scan Set

3 values are valid. Only Scan Set 3 operation will be affected, but command can be sent using any scan set.

FE hex - Resend

After receiving this command, the keyboard shall transmit the last byte sent. If the last byte was Resend, the keyboard shall transmit the previous byte sent before the Resend command.

FF hex - Reset

After receiving this command, the keyboard shall transmit an Acknowledge to the system. The keyboard shall wait till the system accepts the Acknowledge response. The system will accept the Acknowledge by raising the CLOCK and DATA lines for a minimum of 500 microseconds. The keyboard shall be disabled until system accepts Acknowledge or a new command is sent.

The keyboard than executes the self test routine. (See Power-Up and and Self Test, Paragraph 5.4. After the power up routines, the keyboard shall be in the default state.

EF hex - Invalid Command

F1 hex - Invalid Command

See common explanation below.

After receiving the EF or F1 command, the keyboard shall transmit Resend.

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5.3 Key Rollover

The keyboard shall incorporate N-Key Rollover (NKRO) to avoid loss of keystroke data during high speed entry. NKRO is defined as all key depressions and releases correctly detected in any sequence regardless of how many keys are being held depressed.

5.4 Power-Up and Self Test

The keyboard shall contain reset circuitry. The duration of the keyboard Power-On Reset (POR) shall be greater than 150 and less than 2000 milliseconds from power-up.

After executing POR the keyboard shall execute a self test. The self test shall consist of a ROM checksum test, a RAM test and a test for stuck key switches. After completion of the test, the keyboard shall send the result of the diagnostic to the host. The code will be AA hex to indicate successful completion of the self test or FC hex to indicate failure of some portion of the test. If the keyboard fails the self test, it shall be disabled and wait for a command from the system.

Results of the self test are transmitted between 450 and 2500 milliseconds after POR and between 300 and 500 milliseconds after the self test is initiated.

5.5 Autorepeat

The power-on default condition shall cause the last key depressed to repeat at 10 characters per second after a 500 millisecond delay. This may be changed by the system when the keyboard is using Communication Mode 2.

5.6 Buffering

The keyboard shall be capable of storing 16 scan codes in a first in - first out (FIFO) circular buffer. If buffer overflow occurs, the last code in the buffer is replaced by a hex 00 in Communication Mode 2, and hex FF in Communication Mode 1.

5.7 Mode Switch Settings

The keyboard shall use the mode switch settings shown in Table 5.

TABLE 5

MODE SWITCH SETTINGS

Host	Communication Mode	Settings*	Scan Set Used
Enhanced XT/AT	1 or 2	#1 OFF #2 OFF	1, 2, or 3
PC or XT	1	#1 ON #2 OFF	1
AT	2	#1 ON #2 ON (See Note 1)	2

* Switch positions 3 and 4 are not used.

5.8 Auto-Discrimination

If Switch #1 is OFF, the keyboard shall power-up in Communication Mode 2 with Scan Set 2 as the active scan set. If the system clamps the data line on the last clock of power-up completion (code "AA"), for at least 45 microseconds, the keyboard shall be in Communication Mode 1 with Scan Set 1. See Figure 7.

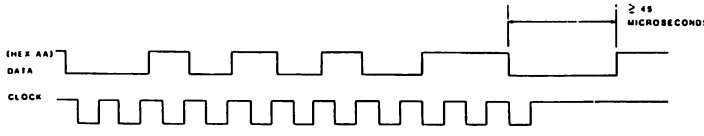

Figure 7: Power-Up Auto-Discrimination Timing

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5.9 LED Indicators

The keyboard shall include three LED indicators, namely, Num Lock, Caps Lock, and Scroll Lock.

The indicators shall be located at the right hand end of the Function key row, and directly above the Numeric Keypad. (Refer to the F0 hex command in Paragraph 5.2.4.)

The keyboard shall power-up with all LED's OFF.

5.10 Software "Watch Dog"

The keyboard software shall contain a "watch dog" timer which attempts to keep the microprocessor running properly at all times (in spite of possible noise "glitches" on the power supply or ESD events).

The watch dog sets certain RAM locations during the scanning routine. Then, during the internal timer interrupt routine, these locations are tested. If the expected values are found it is assumed that the microprocessor is still scanning properly. The RAM locations are reset to some other values for the next test and normal execution continues. If the reset values are not in the RAM locations (or any other value besides the one set during scanning are found) it is assumed that a problem has occurred and a complete reset is performed by the microprocessor.

The results of this reset are identical to the response to a reset command from the host.

6.0 Electrical Requirements

The interface shall consist of two bidirectional lines, clock and data, which can be controlled by open collector drivers on either side. The keyboard side shall be terminated by 3300 ohm resistors. Voltage levels shall be TTL compatible, and the keyboard drivers capable of sinking a minimum of 20 mA including the current sourced by the pullup resistors on the keyboard).

6.1 Signal Connector

The signal connector shall be a 5 pin DIN connector, Manufacturing Switch Craft (PN 05BL5M), or equivalent. Connections shall be as follows:

Pin	Signal
1	Clock
2	Data
3	No Connection
4	Logic Ground
5	+ 5 VDC

Connector on the cable of keyboard (looking in).

6.2 Chassis Ground

The chassis ground shall be isolated from logic ground.

6.3 Power Requirement

The keyboard shall require 5 volts +/-5% at 400 milliamps maximum.

7.0 ENVIRONMENTAL REQUIREMENTS

7.1 Temperature

Operating . . . . . 0 to 55 degrees C
Non-operating . . . . . -40 to 70 degrees C

7.2 Relative Humidity

20% to 95% non-condensing

7.3 Shock

Operating. . . . 10G 1/2 sine wave, 10ms duration, any axis
Non-operating . 100G 1/2 sine wave, 10ms duration, any axis

7.4 Vibration

Operating. . . . 0.4 inch double amplitude 5 to 50 Hz
Non-operating . 0.4 inch double amplitude 2 to 10Hz
(In original cartons)

7.5 Altitude

Operating. . . . -1,000 ft to +12,000 ft
-1,000 ft to +12,000 ft

7.6 Electrostatic Immunity

The keyboard shall meet the electrostatic immunity requirements described in Key Tronic document 36-02464, Part 18.

7.7 EMI/RFI

The keyboard shall be certified to comply with FCC rules, Subpart J of Part 15 for class B equipment when used in conjunction with an IBM PC,XT, or AT. The keyboard shall not hinder any other properly designed product from obtaining certification.

7.8 Safety

The keyboard shall not be manufactured from any material that will prevent or obstruct the obtaining Underwriter's Laboratories (UL) rocognition.

Materials shall conform to the following UL requirements:

- Printed Circuit Board UL94V-0
- Keytops and Enclosure UL94HB
- Cables . . . . . UL2960 and 20197

8.0 RELIABILITY

8.1 Mean Time Before Failure (MTBF)

The MTBF of the keyboard is calculated in excess of 100,000 hours based on failure rates determined through either actual life testing or MIL-HDBK-217C calculations.

8.2 Switch Life

Switch life shall be a minimum of 100 million cycles based on life test data.

8.3 Maintainability

The mean time to repair the keyboard by a qualified repair technician shall be 15 minutes.

APPLICATION NOTE

CAPACITANCE MATRIX INTERROGATION CHIP

PART NUMBER 22-00958-000

KEY TRONIC DOCUMENT NUMBER 36-1829

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REVISIONS

Revision	Description	Date	By
---	Original Draft	08/1/84	RLN
A	Production Release	08/15/84	RLN
B	Iill was -400uA, is -900uA Iil2 was 5mA, is 3mA tss max. was: 16.9us is: 18us	03/05/85	RLN 20 June 85

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1.0 GENERAL DESCRIPTION:

The 22-00958-000 is a full-custom, CMOS, integrated circuit, which provides for a low power matrix scanning and detection capability to be used on encoded capacitance keyboards. The device will accommodate 128 keys with the capacitance matrix configured in a 16 X 8 matrix (16 drive lines and 8 sense lines). The device will operate from a 5VDC ± 10% power supply and is available in a plastic or ceramic 40-pin dual-in-line package.

1.1 APPLICATION:

The unique capacitance sensing circuitry (which is particularly insensitive to keyboard PCB loading effects) makes this device very versitile for use in encoded capacitiance keyboard applications.

One primary application will be where low power operation is required. This device is also used in the emulation of the single chip keyboard controller 20-90049-XXX. A typical keyboard configuration is shown in Figure 1. The device pinout is shown in figure 2. The device will typically be used with the 8048 family of single chip microcomputers such as the 8048, 8049, 8035, 8039, etc., and their CMOS equivalents.

2.0 DEVICE INTERFACES

2.1 The microcomputer interfaces are

A. A0-A3: A four-bit matrix address, which typically is provided by the lower order PORT 2 pins of the microcomputer. The input structures are a Schmitt trigger with an internal resistive pullup.

B. $\overline{\text{RST}}$: A reset pulse typically provided by the PROG output of the microcomputer, which latches the matrix address, initializes the Y line counter and the comparator sensing circuitry. The input structure is a Schmitt trigger with an internal resistive pullup.

C. $\overline{\text{STB}}$: A strobe signal provided by a PORT 1 line, which initiates the actual scanning operation by internally enabling the timing and control logic of the device on the falling edge of the signal. This signal is generated by the microcomputer for each key location within the matrix. The input structure is a Schmitt trigger with an internal resistive pullup.

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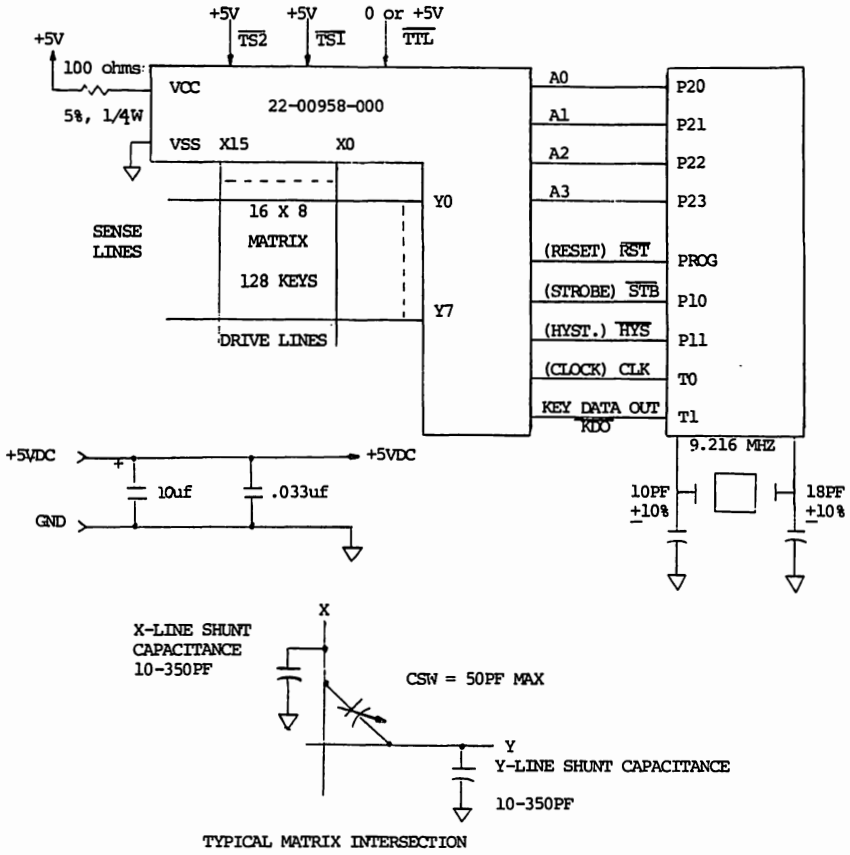

FIGURE !: TYPICAL KEYBOARD CONFIGURATION

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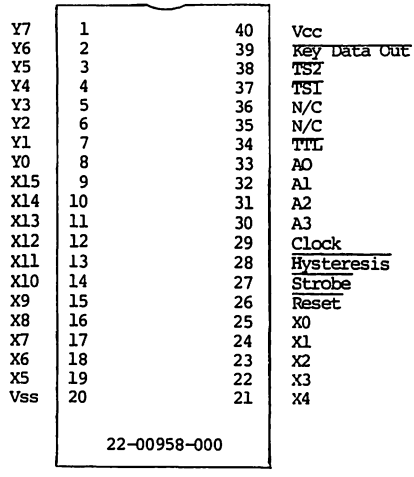

FIGURE 2: DEVICE PINOUT

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D. CLK: A clock line from the TO pin of the 8048 microcomputer family with a frequency of approximately 1/3 the timing crystal frequency. The timing parameters specified herein are based upon a clock frequency rance of 2.67 MHz to 3.67 MHz. However, the device will operate with a clock frequency down to 1 MHz if required. All internal timing and control is derived from this signal. The input structure is LSTTL compatible.

E. HYS: A hysteresis select signal from the controlling electronics, usually a PORT 1 pin, which alters the threshold of the key detection circuitry by disabling the smaller of two internal reference capacitors. The signal is normally high. When this signal is toggled to a low level, it increases the detection sensitivity. The input structure is a Schmitt trigger with an internal resistive pullup.

F. KDO: The key data out signal represents the latched serial data output to the microcomputer which is driven to a low state for each detected key closure.

2.2 The capacitive keyboard interfaces are:

A. X0-X15: Sixteen normally low matrix drive lines (referred to as X lines) which are sequentially pulsed high at the rising edge of the strobe pulse for each switch location within the matrix.

B. Y0-Y7: Eight matrix sense lines (referred to as Y lines) which connect to a single analog charge difference detector through an 8 to 1 multiplexing function within the device. The detector senses the effective charge present at the Y input, and outputs a digital signal to a data latch. When selected, each of the eight matrix sense lines is biased nominally at +2.0V with Vcc = 5.0V. Unselected Y lines are terminated through a pull down resistance of <1K ohms. The input impedance at each input is 19.2K ohm $\pm$ 30% when selected.

2.3 Drive Select Pin:

TTL: Pin #34 is provided to allow selection of either standard LSTTL or CMOS interface capability. The pin is to be connected to VSS when the device is being driven by TTL outputs and is to be connected to VCC when the device is being driven by CMOS outputs. When TTL is low, pullup resistors are connected to A0-A3, HYS, STB, and RST inputs.

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2.4 Two pins are used to invoke test modes for the device:

$\overline{TS1}$: When pin 37 is connected to VSS, test mode 1 is enabled, which presents five internal timing signals to pins 9 through 13. The normal X11 through X15 outputs are disabled in this mode. In normal operation, $\overline{TS1}$ is connected to VCC.

$\overline{TS2}$: When pin 38 is connected to VSS, test mode 2 is enabled. This test mode disables two internal bias resistors on the Y lines and allows measurement of the prebias voltage, which is used during device qualification and production screening. In normal operation, $\overline{TS2}$ is connected to VCC.

3.0 CAPACITANCE THRESHOLD

The capacitance threshold of the device is 8.1 pF $\pm$ 21% (6.4 pF $\leq$Cth $\leq$9.8 pF). This threshold limit applies over the supply range of 5v $\pm$ 10%, temperature range of 0 degrees C to 70 degrees C and Y line shunt capacitance of 10 pF to 350 pF and X line shunt capacitance of 10 pF to 350 pF and a y line input impedance of 19.2K ohm $\pm$ 30%.

If a key capacitance, connected between an X drive line and a Y sense line, is equal to or less than 6.4 pF, KDO will be high, indicating an open key. Similarly, if a key capacitance is equal to or greater than 9.8 pF, KDO will be low, indicating a closed key.

4.0 HYSTERESIS CONTROL

Under software control, the capability exists to internally alter the threshold of the device. The hysteresis control is active when the microcomputer detects a key closure at any one key address. Upon such detection, the effective capacitance threshold is decreased by approximately 20%. For example, if the capacitance threshold was at a nominal 8.1 pF initially, upon software control, it is alterable to 6.5 pF.

ESD LATCHUP PROTECTION

5.0 Since all keyboard installations are inherantly susceptable to electrostatic discharges (ESD) due to constant human interaction, a 100 ohm to 1K ohm, 5%, 1/4W resistor should be installed in series with the +5VDC connection to this device. This precaution will ensure that the device (in varying degrees, all CMOS devices are inherantly suceptable to SCR latch up phenomena) will withstand a minimum ESD level of 15KV applied directly to the keyboard.

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6.0 DC SPECIFICATION (Ta = 0 to 70 degrees C, VCC = 5V ± 10%)

PARAMETER	TEST CONDITIONS	SIGNAL NAME	LIMITS MIN	LIMITS MAX	UNITS
Icc	$\overline{TTL}$ = VSS; Static	Supply Current Drain		3	mA
Vih1	$\overline{TTL}$ = VSS Iihl = -40uA**	$\overline{STB}$, $\overline{RST}$, $\overline{HYS}$, $\overline{A0-A3}$, $\overline{TS1}$, $\overline{TS2}$	3.8		V
Vil1	$\overline{Iil1}$ = -900uA** $\overline{TTL}$ = VSS	$\overline{STB}$, $\overline{RST}$, $\overline{HYS}$, $\overline{A0-A3}$, $\overline{TS1}$, $\overline{TS2}$		.6	V
Vil2	Y inputs unselected Iil2 = 3mA	Y0 through Y7		.4	V
Vih3 Vil3		CLK, $\overline{TTL}$ CLK, $\overline{TTL}$	2	 .8	V V
Voh1	Ioh1 = -800uA	X0-X15	2.4		V
Vol1	Iol1 = 5mA	X0-X15		.45	V
Voh2	Ioh2 = -1.6 mA	$\overline{KDO}$	2.4		
Vol2	Iol2 = 1.6 mA	$\overline{KDO}$		.45	V
Vt+ Positive Going Threshold Voltage		$\overline{RST}$, $\overline{STB}$, $\overline{HYS}$, A0-A3	1.8	3.0	V
VT- Negative Going Threshold Voltage		$\overline{RST}$, $\overline{STB}$, $\overline{HYS}$, A0-A3	1.3	2.1	V
Hysteresis [(Vt+) - (Vt-)]		$\overline{RST}$, $\overline{STB}$, $\overline{HYS}$, A0-A3	0.5		V
Cin	fc = 1MHz	Pin Input Capacitance		10	pF

** An internal resistor pullup is included to allow these pins to be driven by LSTTL levels.

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7. TIMING REQUIREMENTS:

The following AC specifications refer to the timing diagram of Figure 3. The values apply over a temperature range of 0 to 70 degrees C, Vcc = 5V + 10% and clock frequency of 2.67 to 3.67 MHz. Load capacitance for $\overline{KDO}$ = 50 pF.

SYMBOL	PARAMETERS	VALUE		UNITS
		MIN.	MAX.	
tcy	Clock period	273	375	ns
tch	Clock high	91	125	ns
tcl	Clock low	182	250	ns
tpp	$\overline{RST}$ pulse width	500	---	ns
tdp	A0-A3 stable to rising edge of $\overline{RST}$	300	---	ns
tpd	A0-A3 hold time from rising $\overline{RST}$	30	---	ns
ta	Time for full column scan (8 keys)	100.7	---	us
th	$\overline{HYS}$ stable to falling edge of $\overline{RST}$	-0-	---	ns
trs	$\overline{RST}$ rising edge to $\overline{STB}$ falling edge	9.3	12.8	us
tss	$\overline{STB}$ period	12.3	18.	us
ts	$\overline{STB}$ low	2.73	---	us
tr	$\overline{STB}$ high	9.56	---	us
tc	$\overline{STB}$ rising edge to next $\overline{RST}$ falling edge	2.46	---	us
trd	$\overline{RST}$ falling edge to $\overline{KDO}$ data invalid	---	5.0	us
td	$\overline{STB}$ falling edge to valid data on $\overline{KDO}$	2.7	---	us

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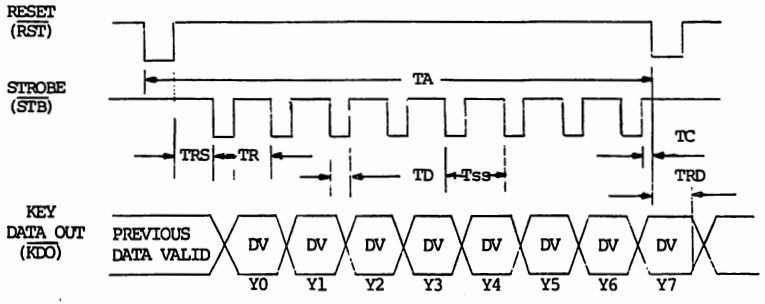
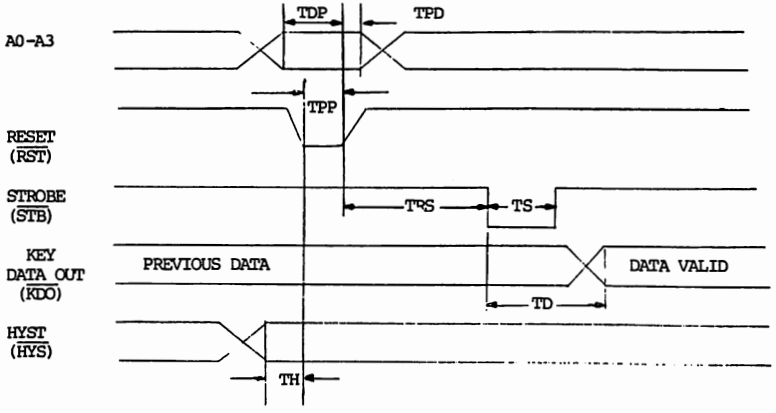
SCAN OF 8 KEYS (1 X LINE)



SINGLE KEY SCAN



CLOCK TIMMING

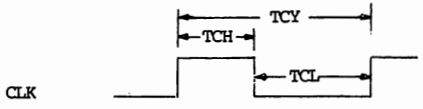


FIGURE 3

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key tronic
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7.1 DEVICE TIMING AND OPERATION:

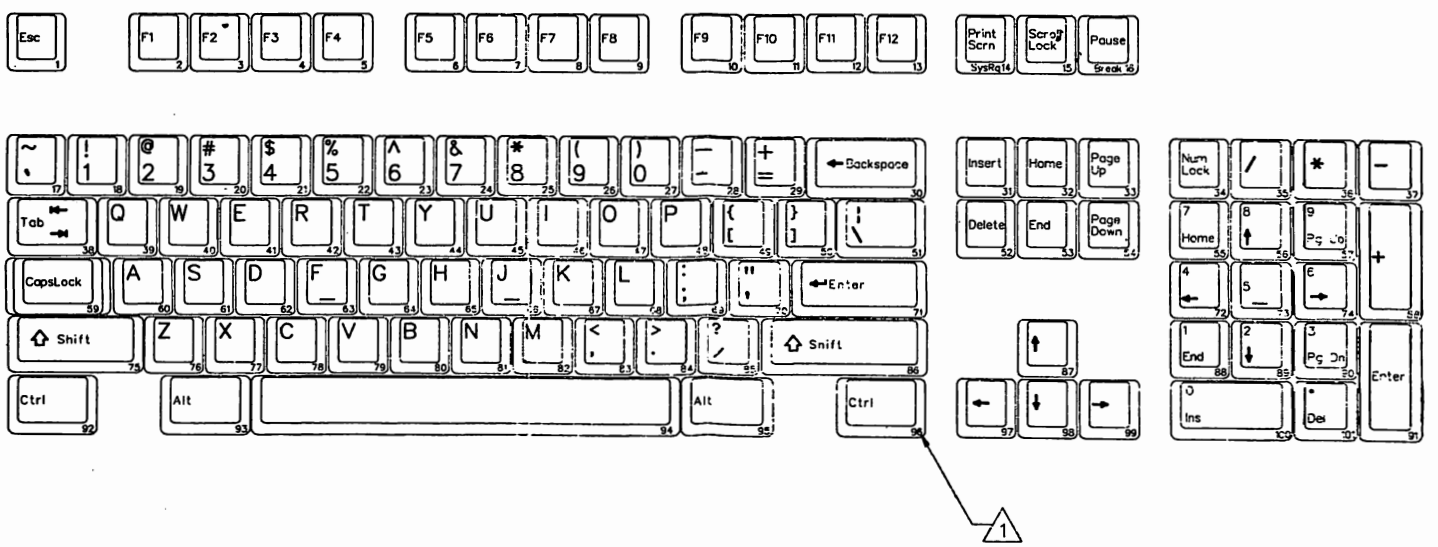
Figure 3 shows the timing for the scan of eight keys on one drive line. The reset pulse is issued prior to any key scanning sequence. After the generation of a reset pulse, eight strobe signals will be sent by the processor, as shown. The switch matrix is scanned eight keys at a time. The matrix is interrogated by addressing one of the drive lines and checking all of the sense lines to determine the up/down condition of the keys at the drive/sense intersections of that particular X line. The following command sequence is an example of how the above timing relationships can be derived using the 8049 microcomputer. The example assumes that a reset pulse is generated from the PROG output of the 8049, the strobe signal is derived from PORT 10, the hysteresis signal is derived from PORT 11 and the clock signal from the T0 output.

```
INTRGT:  MOV  A,SRADDR          GET X-LINE ADDRESS
         MOVD P7,A               OUTPUT THE X-LINE, CLEAR LATCH
         MOV  DLYCNT,#8          LOAD Y LINE COUNTER
         CLR  A
         ORL  P1,#001H           LOAD P10 WITH A ONE (STROBE)
NEXTY:   ANL  P1,#0FEH           BRING P10 LOW (INTERROGATE
                                   FIRST Y LINE)
         ORL  P1,#001            BRING P10 HIGH AGAIN
         JT1  $+3                CHECK KDO FOR KEY CLOSURE
         INC  A
         RR   A
         DJNZ DLYCNT,NEXTY       IF 8 STROBES NOT COMPLETE, GENERATE
                                   ANOTHER ONE
         XRL  A,@SRADDR          COMPARE TO PREVIOUS DATA
```

NOTICE OF PROPRIETARY INFORMATION

INFORMATION CONTAINED HEREIN IS PROPRIETARY AND IS FURNISHED WITH THE UNDERSTANDING THAT IT WILL NOT BE REPRODUCED IN WHOLE OR IN PART, OR USED AS THE BASIS FOR DESIGN, MANUFACTURE OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION. IN ACCEPTING THIS PROPOSAL THE RECIPIENT AGREES TO MAKE USE OF THE INFORMATION ONLY FOR THE PURPOSES SPECIFIED AND TO LIMIT ACCESS TO THE INFORMATION TO THOSE OF HIS EMPLOYEES WHO HAVE A NEED FOR SUCH ACCESS FOR THE PURPOSES STATED. FOR ANY OTHER COMPANY THE INFORMATION SHALL NOT BE USED OR DISCLOSED BY THE RECIPIENT, FOR ANY OTHER PURPOSE, WHATSOEVER, WITHOUT THE PRIOR WRITTEN CONSENT OF KEY TRONIC CORP. REGISTERED IN U.S. PATENT AND TRADEMARK OFFICE.

REV	ECO	BY	DESCRIPTION	APP	DATE
–	–	RJE	PROTO	JW	6/20/85
A	–	GLN	MFG. RELEASE	PSR	10-7-86
B	30856	MC	LEGEND CHNG	TET	7/17/87



2. THIS DRAWING IS INTENDED TO AID IN THE PROPER ARRANGEMENT OF KEYTOPS ON THE KEYBOARD. THE KEYTOP LEGENDS ARE SHOWN FOR REFERENCE ONLY. ANY DISCREPANCIES BETWEEN LEGEND SHOWN AND EXACT LEGEND AS TOOLED SHOULD BE RESOLVED BY REFERRING TO THE KEYTOP BILL OF MATERIAL AND KEYTOP CODE BOOK.

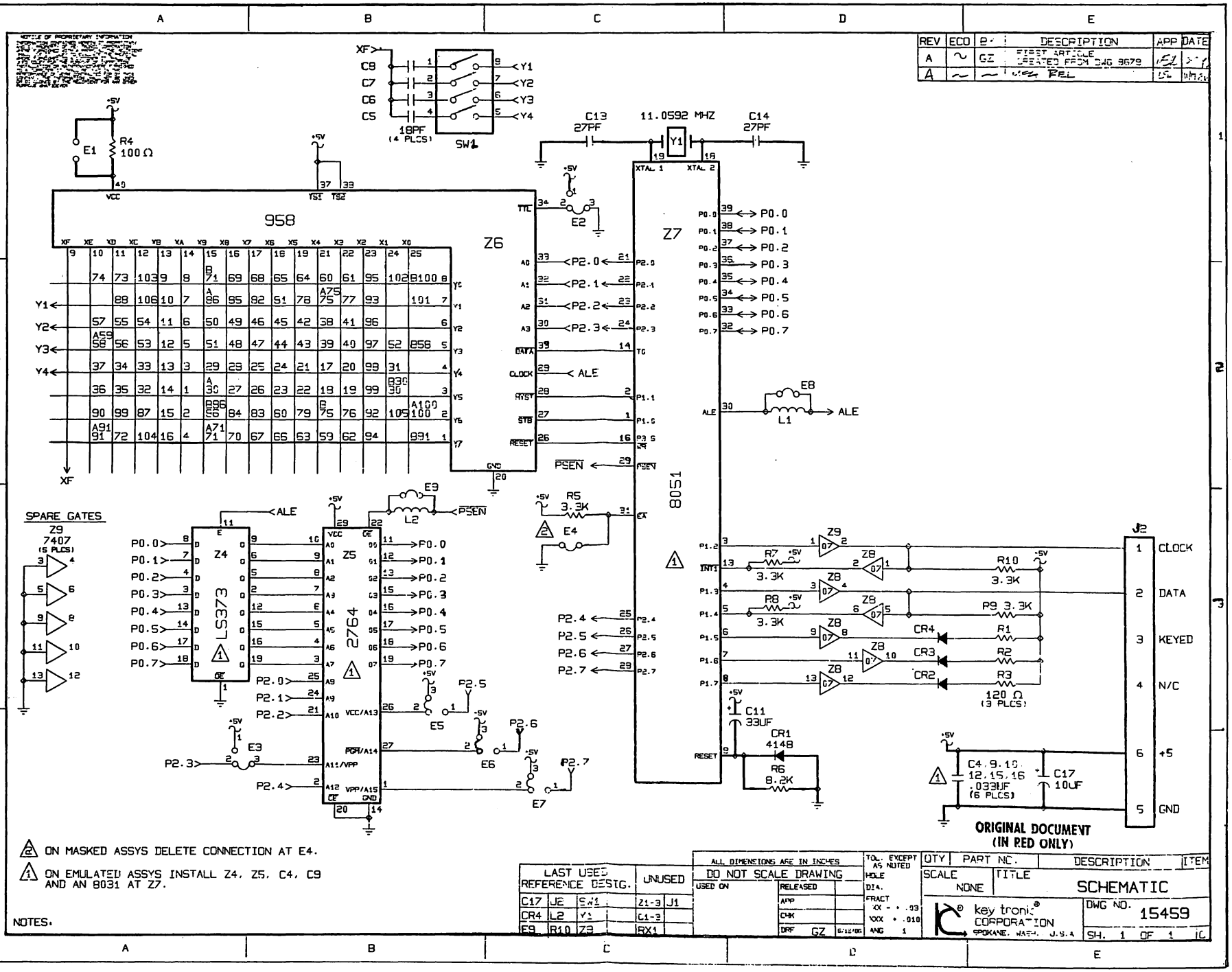
⚠1 NO'S INDICATE KEYTOP B.O.M. ITEM NUMBERS.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING
USED ON
RELEASED
APP
CHK
DRF RJE 5-30-86
TOL. EXCEPT AS NOTED
HOLE
DIA
FRACT
XX ±.03
XXX ±.010
ANG 1°

QTY	PART NO.	DESCRIPTION	ITEM

SCALE NONE
TITLE SET, KEYTOP
key tronic® CORPORATION SPOKANE, WASH., U.S.A.
DWG NO. 15597
SHEET 1 OF 1
DIST. V


NOTICE OF PROPRIETARY INFORMATION
REV | ECO | BY | DESCRIPTION | APP | DATE
A | ~ | GZ | FIRST ARTICLE CREATED FROM DWG 8679
A | ~ | ~ | NEW REL
XF
C9
C7
C6
C5
18PF (4 PLCS)
SW1
Y1
Y2
Y3
Y4
+5V
E1
R4 100Ω
VCC
40
37
38
TS1
TS2
C13 27PF
11.0592 MHZ
Y1
C14 27PF
19
18
XTAL 1
XTAL 2
958
Z6
Z7
8051
TTL
E2
ALE
PSEN
RESET
EA
P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
P0.7
P2.0
P2.1
P2.2
P2.3
P2.4
P2.5
P2.6
P2.7
P1.1
P1.5
P3.5
E8
L1
ALE
SPARE GATES
Z9
7407
(5 PLCS)
Z4
LS373
Z5
2764
E9
L2
PSEN
R5 3.3K
E4
E3
E5
E6
E7
Z8
R7 3.3K
R8 3.3K
R10 3.3K
P9 3.3K
R1
R2
R3 120Ω (3 PLCS)
CR4
CR3
CR2
C11 33UF
CR1 4148
R6 8.2K
C4,9,10, 12,15,16 .033UF (6 PLCS)
C17 10UF
J2
CLOCK
DATA
KEYED
N/C
+5
GND
ORIGINAL DOCUMENT (IN RED ONLY)
2 ON MASKED ASSYS DELETE CONNECTION AT E4.
1 ON EMULATED ASSYS INSTALL Z4, Z5, C4, C9 AND AN 8031 AT Z7.
NOTES.
LAST USED REFERENCE DESIG.
UNUSED
C17 J2 SW1 Z1-3 J1
CR4 L2 Y1 C1-3
E9 R10 Z3 RX1
ALL DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING
TOL. EXCEPT AS NOTED
HOLE
DIA.
FRACT
XX ± .03
XXX ± .010
ANG 1
USED ON
RELEASED
APP
CHK
DRF GZ 6/12/86
QTY | PART NO. | DESCRIPTION | ITEM
SCALE NONE
TITLE SCHEMATIC
key tronic CORPORATION SPOKANE, WASH. U.S.A.
DWG NO. 15459
SH. 1 OF 1 1C

4000 Disk Drive

Specifications

of

MP-F73W-70D

Double Sided 80 Tracks
Recording Capacity 2MBytes
Transfer Rate 500 Kbits/sec at 2MB mode
250 Kbits/sec at 1MB mode

VALID for MP-F73W-70D,
with the following serial numbers :

30,000,001			

SONY CORPORATION

MFD TECHNICAL INFORMATION 00-0060 REV. 11-87 July 28, '87

*** Contents ***

1. Intrduction

2. Specifications

2.1 Configuration

2.2 Physical Dimensions

2.3 Performance

2.3.1 Capacity
2.3.2 Transfer Rate
2.3.3 Access Time
2.3.4 Functional
2.3.5 Reliability

2.4 Input Power Requirements

2.4.1 Power Consumption
2.4.2 Supply Voltages

2.5 Environmental Limits and Orientation

2.5.1 Temperature Range
2.5.2 Humidity Range
2.5.3 Vibration
2.5.4 Shock
2.5.5 Orientation

3. Signal Interface

3.1 Pin Assignment

3.1.1 Signal Connector
3.1.2 Signal Connector Pin Assignment
3.1.3 Power Supply Connector
3.1.4 Power Supply Connector Pin Assignment

3.2 DC Characteristics of Interface Signals

3.2.1 Output Signals from Drive
3.2.2 Inputs Signal to Drive
3.2.3 Recommended Circuit for Signal Interface

3.3 Signal Definitions

3.3.1 DRIVE SELECT 0,1,2,3
3.3.2 MOTOR ON
3.3.3 STEP
3.3.4 DIRECTION
3.3.5 HEAD SELECT
3.3.6 WRITE GATE
3.3.7 WRITE DATA
3.3.8 INDEX
3.3.9 TRACK 00
3.3.10 WRITE PROTECT
3.3.11 READ DATA
3.3.12 DISK CHANGE

3.4 Timing Requirements

3.4.1 Head Access
3.4.2 TRACK 00 Signal
3.4.3 Write Data Timing
3.4.4 Read Data Timing
3.4.5 Index Pulse
3.4.6 Disk Change

3.5 Power on and Power off Requirements

3.5.1 Data Protection
3.5.2 Power Supply Sequencing
3.5.3 Power-On Reset Timing

3.6 Disk Motor Rotation and Disk Insertion.

4. Safety

5. Power On Initialization

1. Introduction

This document describes the specifications of the MP-F73W-70D which has the capability to read and write up to 2MB data (unformatted) on a HD disk as well as read and write up to 1MB (unformatted) data on a 1MB disk. The main features of the MP-F73W-70D are: low power consumption, low height, and high reliability with a simple mechanism and electric circuit.

This drive maintains the 300rpm of the disk motor rotational speed constantly, therefore,

a. When a 2MB disk is inserted into the MP-F73W-70D, both read and write operations can be carried out and the data transfer rate is 500 kbits/sec.
b. When a 1MB disk (proposed ANSI standard) is inserted into the MP-F73W-7 D, the data transfer rate becomes 250 kbits/second.

2. Specifications

2.1 Configuration

The drive consists of Read/Write heads, head positioning mechanism, disk motor, interface logic circuit and Read/Write circuit.

2.2 Physical Dimensions

The detailed physical dimensions are shown in Figure 2.1. The main dimensions are:

1) Height : 30 mm (1.18 in.)
2) Width : 101.6 mm (4.00 in.)
3) Depth : 150 mm (5.91 in.)
4) Weight : 480g (1.06 pounds) max.

2.3 Performance

2.3.1 Recording Capacity (unformatted, MFM)

2MB mode	1MB mode
2.0 Mbytes/disk	1.0 Mbytes / disk
1.0 Mbytes/surface	0.5 Mbytes / surface
12.5 Kbytes/track	6.25 Kbytes / track

2.3.2 Transfer Rate

Burst transfer rate : 500 Kbits/sec for MFM in a 2MB mode
250 Kbits/sec for MFM in a 1MB mode

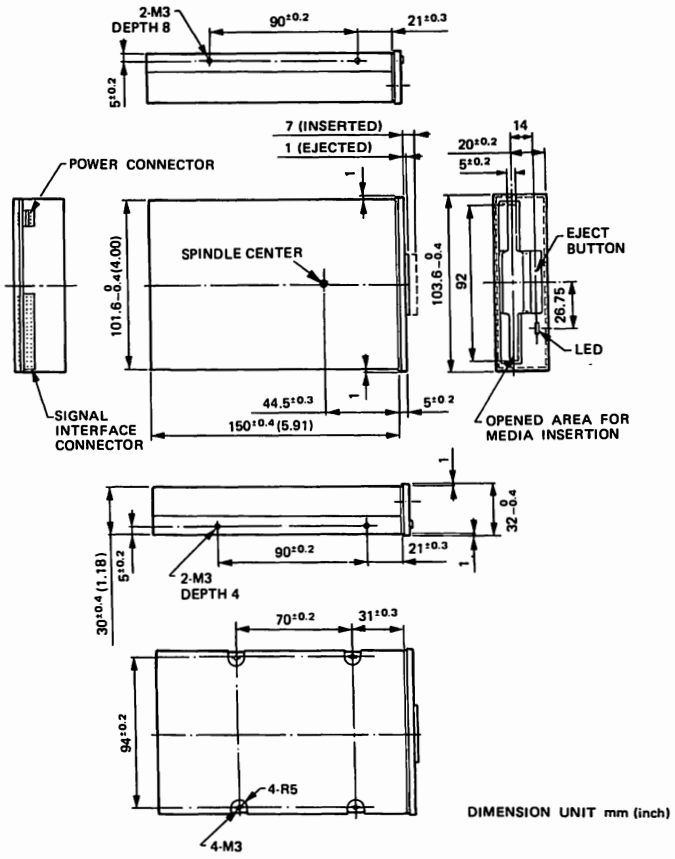


Fig. 2.1 Physical Dimensions

2.3.3 Access Time

a. Track to Track Slew Rate : 3 msec max.

b. Head Settling Time : 15 msec max.

The value of 15msec is the time necessary to stabilize the head within 0.035mm of its absolute position.

c. Motor Start Time : 500 msec max.
(700 msec max.*)

Motor start time is defined as the time period necessary to stabilise the Motor Rotational Speed variance to less than +/-1.5% after turning the MOTOR ON signal on.

NB. When a disk is inserted in the drive, the Motor Start Time will be 700 msec at maximum, but, after that it will be 500 msec max. as long as the disk is kept inserted.

2.3.4 Functional

a. Rotation Speed : 300 rpm
The continuous speed variation is within +/-1.5%.
The instantanuous speed variation is within +/-1.5%.

b. Recording Density : 17434 BPI (Side 1, Track 79) in a 2MB mode.
8717 BPI (Side 1, Track 79) in a 1MB mode.

c. Track Density : 135 TPI

d. Cylinders : 80

e. Tracks : 160

f. R/W Heads : 2

2.3.5 Reliability

a. Mean Time Between Failures (MTBF) : 10,000 POH

b. Mean Time to Repair (MTTR) : 30 minutes

c. Preventive Maintenance (PM) : Not Required

d. Components life : 5 years or 15000 POH

e. Error Rate :

1. Soft Read Error : Less than 1 per 10^9 bits read

2. Hard Read Error : Less than 1 per 10^{12} bits read

3. Seek Error : Less than 1 per 10^6 seeks

2.4 Input Power Requirements

2.4.1 Power Consumption

	TTL Interface
Standby	255 mW
Operation (read/write mode)	2.8 W

2.4.2 Supply Voltages

Voltage	Max. Ripple	Current
+12.0V +/-5%	0.1Vpp	Standby 0.3 mA Average 130 mA (Read) Peak 500 mA (Motor Start) Peak 450 mA (stepping during Motor On)
+5.0V +/-5%	0.1Vpp	Standby 50 mA Operating 240 mA

2.5 Environmental Limits

2.5.1 Temperature Range

Operating : 5°C to 50°C ambient (40°F to 122°F)

Transportation : -40°C to 60°C (-40°F to 140°F).

Storage : -20°C to 60°C (-20°F to 140°F)

2.5.2 Humidity Range

Operating : 8% to 80% relative humidity with a wet bulb temperature of 29°C (85F) and no condensation.

Transportation and Storage : 5% to 95% relative humidity and no condensation

2.5.3 Vibration

Operating : The unit can perform Read/Write operations without an error rate beyond that specified while withstanding continuous vibrations at a frequency of 10 to 500 Hz with an acceleration of no more than 0.5G along each of the three mutually perpendicular axes.

Transportation and Storage : The unit can withstand continuous vibrations from 10 to 300 Hz with a maximum acceleration of 2.0G along each of the three mutually perpendicular axes without any degradation of any characteristics below the performance specifications.

2.5.4 Shock

Operating : The unit can withstand a 5.0G shock for 11 msec with a 1/2 sine wave shape in each of the three mutually perpendicular axes while performing normal Read/Write functions without damage or any loss of data.

Transportation and Storage : The unit when unpacked can withstand an 11 msec with a 1/2 sine wave shock of 60G on any of the three mutually perpendicular axes.

2.5.5 Orientation

The drive does not necessarily need to be horizontally positioned. In fact, as seen in figure 2-3, there are many other possible orientations.

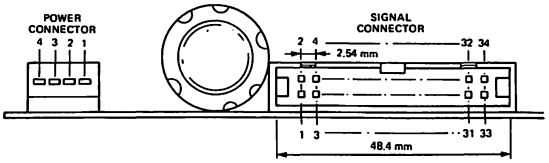
3. Signal Interface

3.1 Connector and Pin Assignments

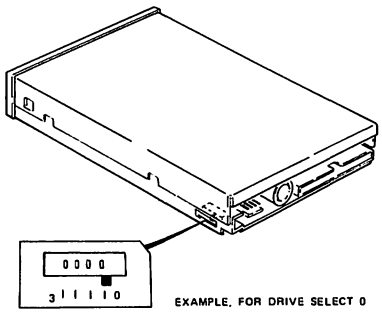
3.1.1 Signal connector

Receptacle : 3M 3414-6500xx or Equivalent

Cable : 3M 3365/34 or Equivalent



PIN ASSIGNMENT (REAR VIEW OF DRIVE)



EXAMPLE, FOR DRIVE SELECT 0

DRIVE SELECT SWITCH

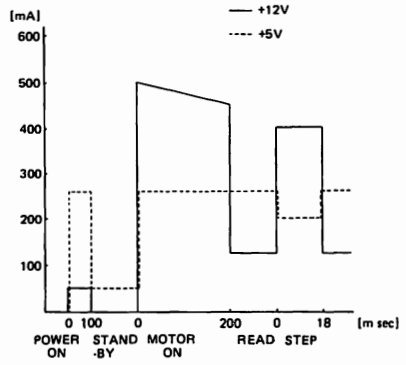


Fig. 2.2 DC Current Profile(typical)

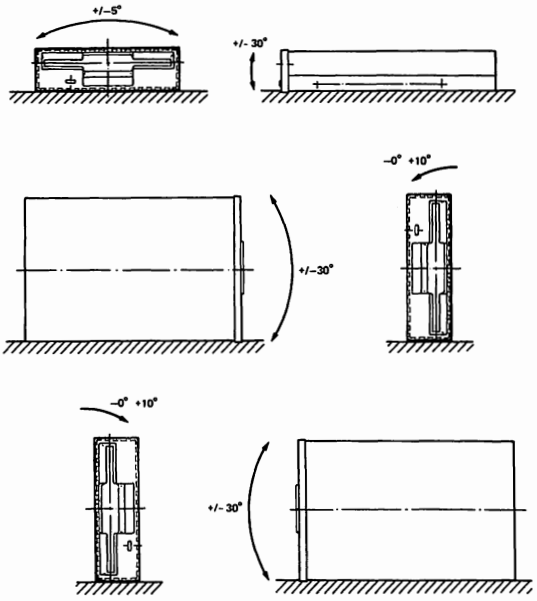


Fig. 2.3 Orientations

3.1.2 Signal Connector Pin Assignment

PIN	SIGNAL DESCRIPTION	PIN	SIGNAL DESCRIPTION
1	N.C.	2	N.C.
3	+5V	4	N.C.
5	+5V	6	DRIVE SELECT 3
7	+5V	8	INDEX
9	+5V	10	DRIVE SELECT 0
11	+5V	12	DRIVE SELECT 1
13	RETURN	14	DRIVE SELECT 2
15	RETURN	16	MOTOR ON
17	RETURN	18	DIRECTION
19	RETURN	20	STEP
21	RETURN	22	WRITE DATA
23	RETURN	24	WRITE GATE
25	RETURN	26	TRACK 00
27	RETURN	28	WRITE PROTECT
29	+12V	30	READ DATA
31	+12V	32	HEAD SELECT
33	+12V	34	DISK CHANGE

3.1.3 Power Supply Connector

Receptacle : AMP 171822-4 or Equivalent

Contact : AMP 170262-1 or Equivalent

Wire : AWG 20

3.1.4 Power Supply Connector Pin Assignment

PIN	SIGNAL DESCRIPTION
1	+5V
2	GND (+5V Return)
3	GND (+12V Return)
4	+12V

3.2 DC Characteristics of Interface Signals

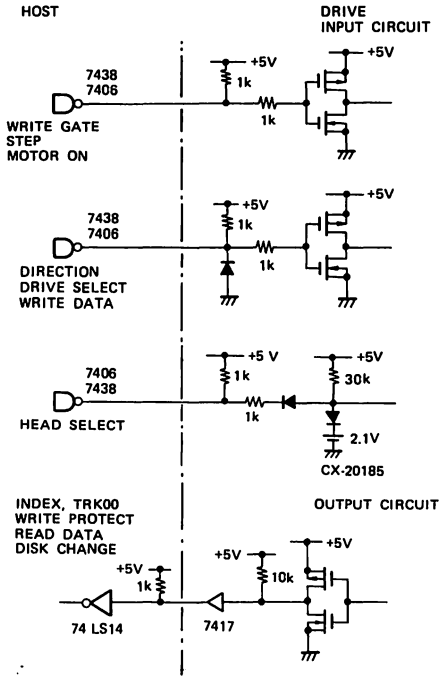
3.2.1 Output Signal from Drive

Name	Output Current IOH(mA)	Current IOL(mA)	Output Voltage VOH(V)	Voltage VOL(V)
TTL interface All outputs	0.25	40		0.7

3.2.2 Input Signal to Drive

Name	Input Current VIN=0.4V IIL(mA)	Input Voltage Threshol VIH(V)	VIL(V)
TTL interface All inputs	-5.0	2.2	0.8

3.2.3 Recommended Circuit for Signal Interface



1 K ohm pull-up resister is recommended to be implemented on the output line from the drive.

The cable length must be less than 1.5m.

Recommended driver IC : 7406, 7438

3.3 Signal Definitions

3.3.1 DRIVE SELECT 0,1,2,3

The SELECT lines are used to enable or disable all other interface lines except a MOTOR ON line. When the SELECT line is true (low), the drive is enabled and considered active. When the SELECT line is false (high), all controller inputs except the MOTOR ON line are ignored and all output lines are disabled.

NB. IN USE (LED) LAMP:
When a drive is selected, the IN USE lamp on the selected drive is turned on, and when a drive is not selected, it is turned off.

3.3.2 MOTOR ON

When this input is true (low) and a disk is inserted, the spindle motor starts to run. When this line is made false (high) or a disk is ejected, the spindle motor decelerates and stop.

However, if the MOTOR ON signal becomes false(high) during either a write or erase operation, the disk motor does not stop rotating until both the ERASE GATE signal and the WRITE GATE signal become high (false).

3.3.3 STEP

When a drive is selected, a true (low) pulse on this line causes the Read/Write head to move to the adjacent track. The direction of the head movement is determined by the status of the DIRECTION input at the trailing edge of the pulse.
The step operation can be performed even if there is no disk inserted in the drive.

3.3.4 DIRECTION

When a drive is selected, a false (high) level on this input causes a STEP input to move the Read/Write head away from the disk spindle. A true (low) level causes a STEP pulse input to move the Read/Write head toward the drive spindle.

3.3.5 HEAD SELECT

When a drive is selected, a true (low) level on this input causes Head 1 (upper) to be selected. A false (high) level on this input will cause Head 0 (lower) to be selected.

If the HEAD SELECT signal changes during either write or erase operation, the head will not be changed until both ERASE GATE and WRITE GATE signal becomes high (false).

3.3.6 WRITE GATE

When this line is made true (low) while a drive is selected, the write current circuits are enabled and information may be written under control of the WRITE DATA input.

3.3.7 WRITE DATA

If the WRITE GATE is true (low), a true pulse (low) on the WRITE DATA line signal causes a bit to be written on the disk. Pulses on this line is neglected when WRITE GATE signal is false (high). No pre-compensation is required.

3.3.8 INDEX

When the drive is selected, a true (low) pulse is generated on this line by each revolution of the spindle.

3.3.9 TRACK 00

This line is true (low) when the drive is selected and the Read/Write head is positioned on track 00.

3.3.10 WRITE PROTECT

If a write-protect disk is inserted while a drive is selected, this line becomes true (low) and the drive is not able to write data. At all other times, except when a disk is ejected while the drive is selected, this line becomes false (high).

3.3.11 READ DATA

When the drive is selected, a true (low) pulse is generated on this line every time a bit is detected.

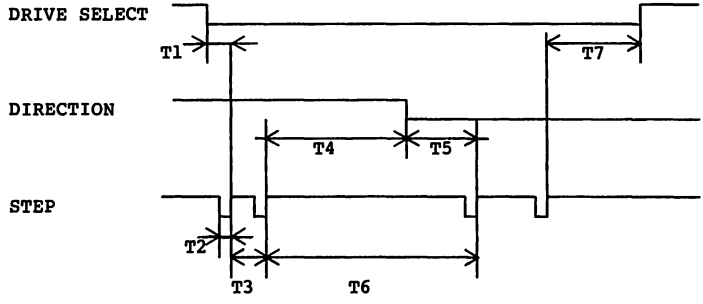
3.3.12 DISK CHANGE

This line is true (low) whenever a disk is removed from the drive. The line will remain true (low) until both the following conditions have been met:

1. A disk is inserted,
and
2. A STEP pulse has been received when the drive is selected.

3.4 Timing Requirements

3.4.1 Head Access



T1 : 0.5 us min.

T2 : 1.3 us min.

T3 : 3.0 ms min.

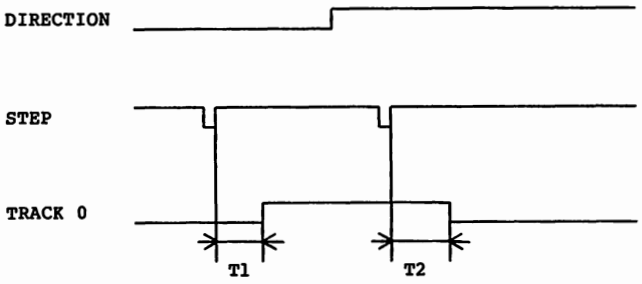
T4 : 2.4 us min.

T5 : 0.5 us min.

T6 : 18 ms min.

T7 : 2.5 us min.

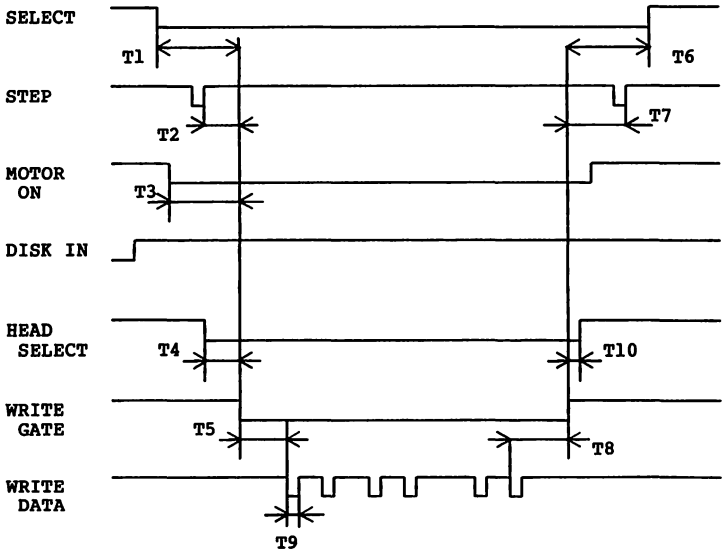
3.4.2 TRACK 00 Signal



T1 : 2.9 msec max.

T2 : 2.9 msec max.

3.4.3 Write Data Timing

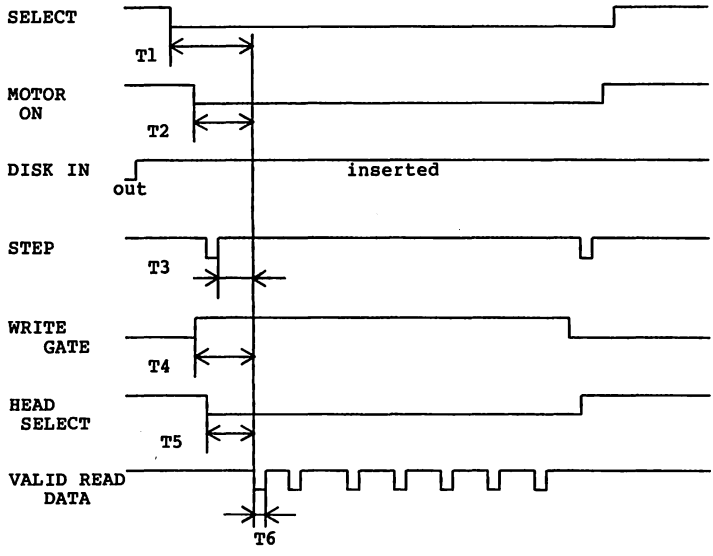


T1	:	0.5 us min.	T6	:	0.5 us min.
T2	:	18 ms min.	T7	:	585 us min. (1020 us min.)
T3	:	500 ms max.**	T8	:	4 us min. (8 us min.)
T4	:	100 us min.	T9	:	150 ns min., 1000 ns max. (150 ns min., 2000 ns max.)
T5	:	4 us max. (8 us max.)	T10	:	See 3.3.4

*NB. DISK IN, the disk-in sensor signal inside the drive, is high when a disk is inserted in the drive.

**NB. When a disk is inserted in the drive, the Motor Start Time will be 700 msec at maximum, but, after that it will be 500 msec max. as long as the disk is kept inserted.

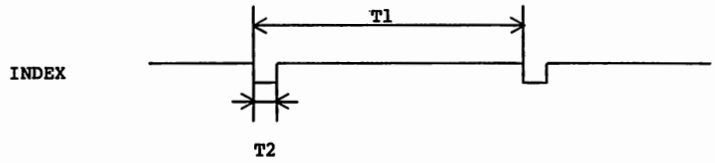
3.4.4 Read Data Timing



T1	:	0.5 us max.	T4	:	615 us max. (1050 us max.)
T2	:	500 ms max.*	T7	:	100 us max
T3	:	18 ms max.	T8	:	350 ns min., 550 ns max.

NB. When a disk is inserted in the drive, the T2, is 700 msec at maximum, but, after that T2 is 500 msec max as long as the disk is kept inserted.

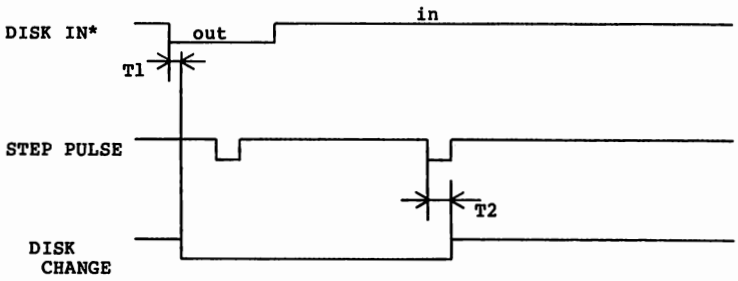
3.4.5 Index Pulse



T1* : 197 ms min., 203 ms max.

T2 : 1.25 ms min., 1.45 ms max.

3.4.6 Disk Change



T1 : 0.5 us max. T2 : 1.6 us max

*DISK IN, the disk-in sensor signal inside the drive, is high when a disk is inserted in the drive.

3.5 Power On and Power off Requirements

3.5.1 Data Protection

Turning power on or off will not cause any damage to recorded data on the disk as long as the drive is not in the midst of writing when the power is shut off or supplied.

3.5.2 Power Supply Sequencing

When the power is turned on, no special power supply sequencing is required. When the power is turned off, although there are no sequencing or timing requirements, both power supplies must fall monotonically to zero volts.

3.5.3 Power-On Reset Timing

Because it takes up to 200 msec to reset the control IC after the power has been turned on, the MP-F73W-70D cannot correctly perform any operations for this period of time after Power-On.

3.6 Disk motor rotation and Disk Insertion.

Even if the MOTOR ON signal is low (true), the disk motor will not rotate until a disk is inserted.

4. Safety Standards

MP-F73W-70D will meet the following product safety regulations:

U.L. 478
C.S.A. C.22.2, No.154
U.L. 94V-0 for Front Bezel

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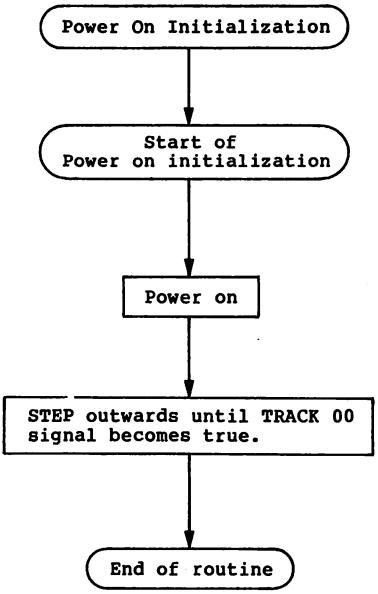
5. Power On Initialization

In order to reduce the peak current requirement when used in a daisy chain, the MP-F73W-70D has been disigned not to seek track 00 automatically. If all the drives connected in the daisy chain sought track 00 simultaneously, this would place a significant power drain on the host system. Thus, the host system must perform the following routine just after power on in order to reset the track counter inside the drive.



Setting the Chip Selector Switch

Set the chip selector switch, S5, according to the first character,"K" or "L", which is printed on the head carriage. See Figures 1 through 3.

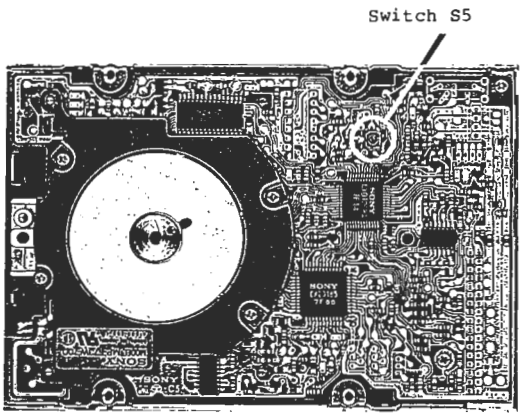


Fig. 1. Bottom view of MP-F73W-70D

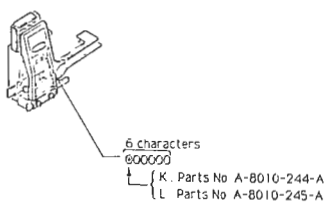


Fig. 2. Head Carriage Ass'y

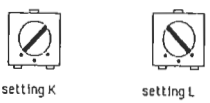
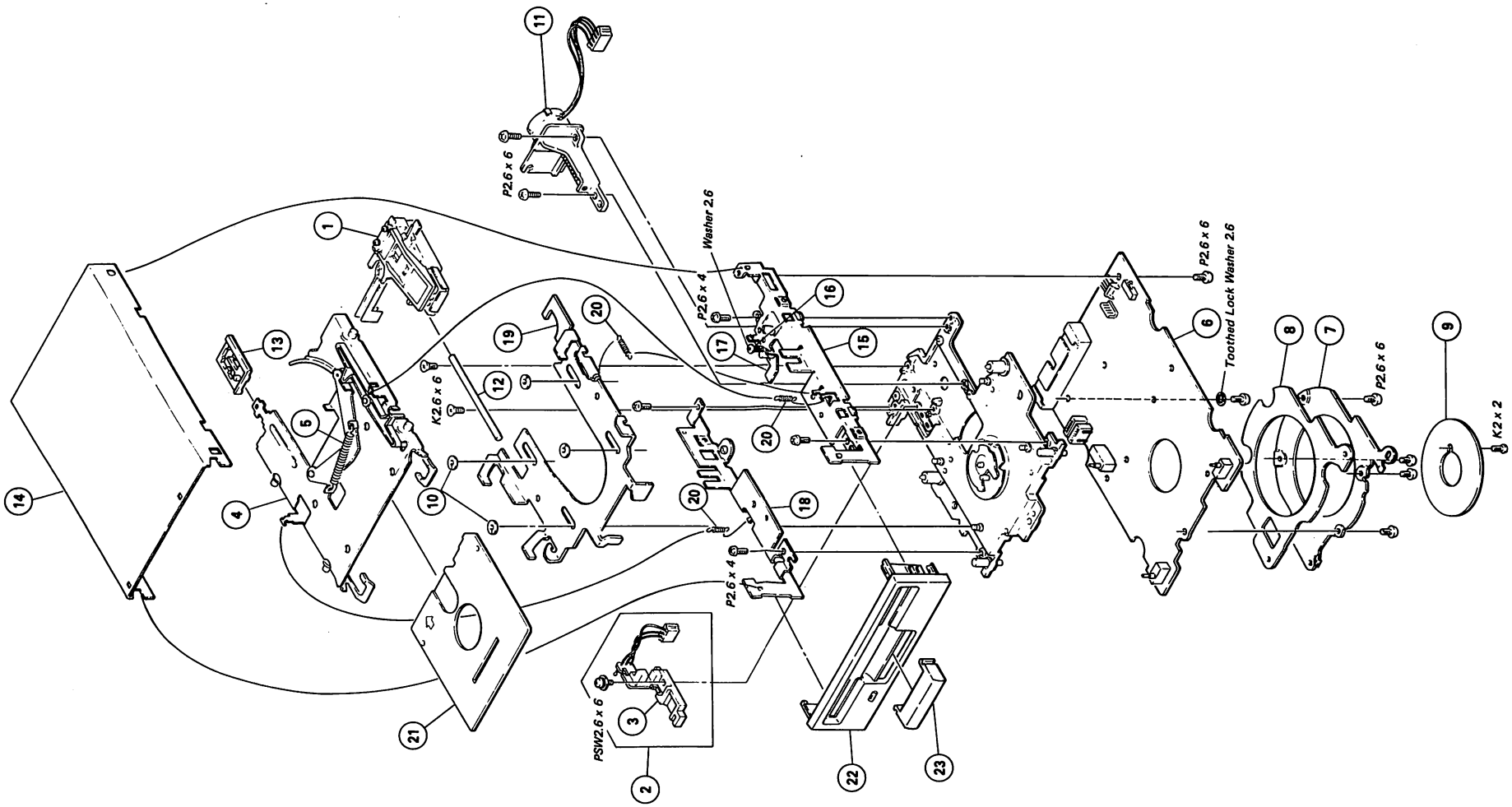


Fig. 3. setting position

Set the position of switch S5 according to the first character, K or L

PARTS ASS'Y LOCATION



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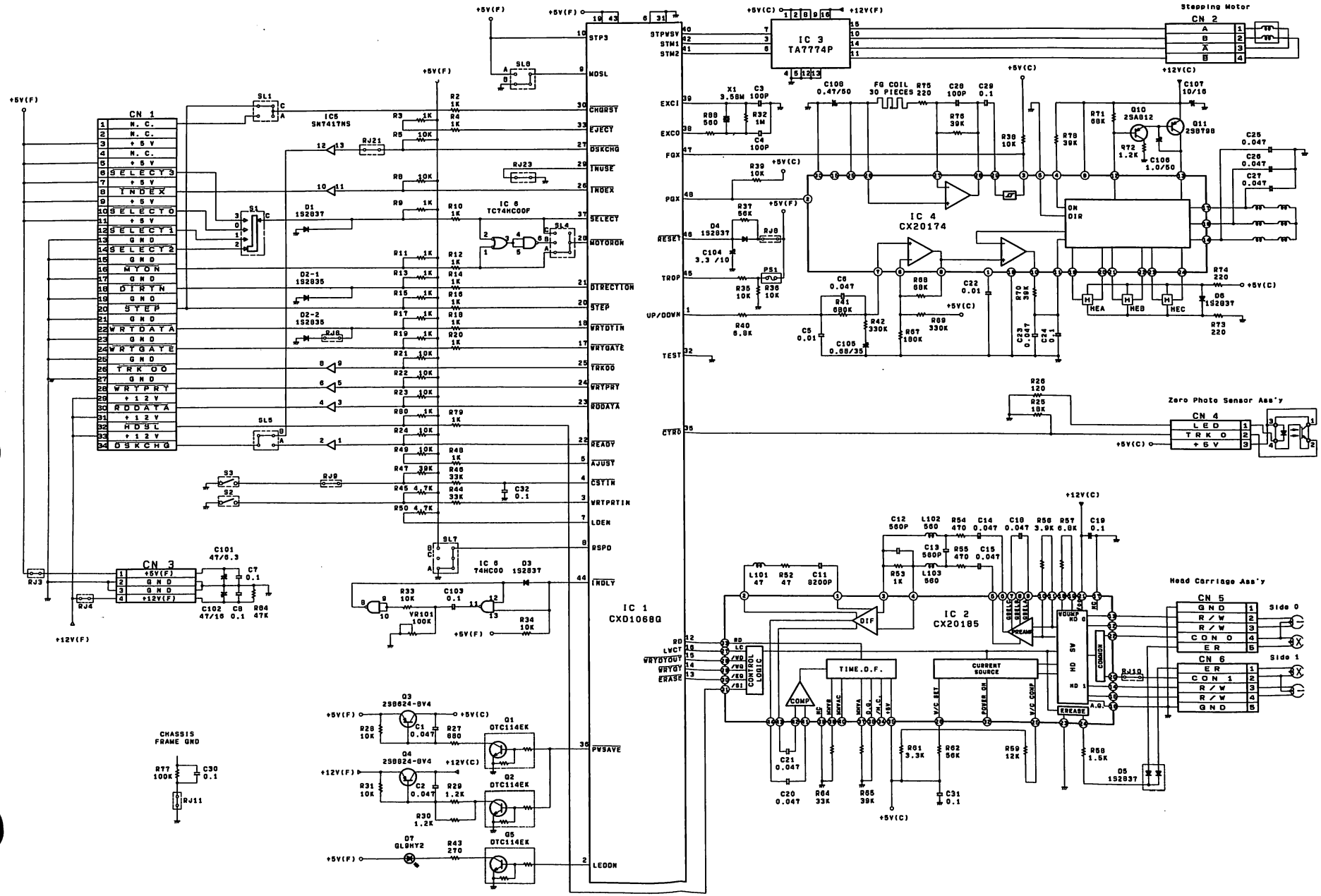
CN 1
CN 2
CN 3
CN 4
CN 5
CN 6
IC 1
CXD1068Q
IC 2
CX20185
IC 3
TA7774P
IC 4
CX20174
IC 5
SN7417NS
IC 6
TC74HC00F
Stepping Motor
Zero Photo Sensor Ass'y
Head Carriage Ass'y
CHASSIS
FRAME GND
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4000 Options