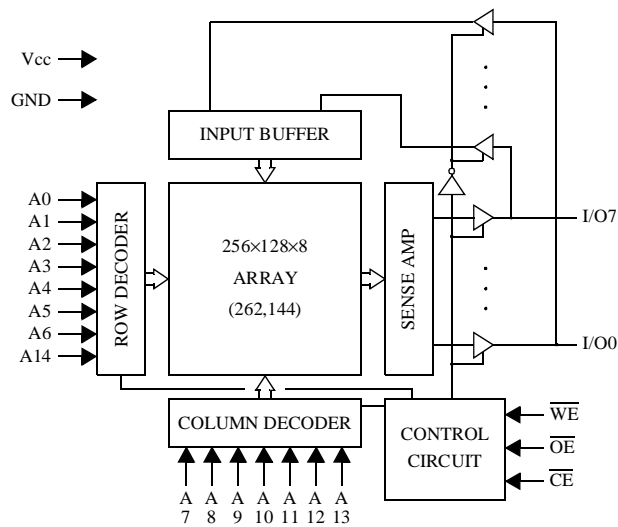


32K×8 CMOS SRAM (Common I/O)

FEATURES

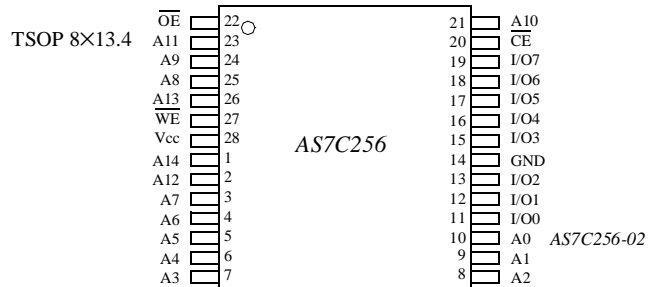
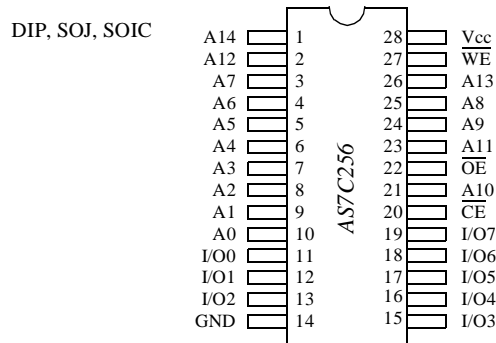
- Organization: 32,768 words × 8 bits
- High speed
 - 10/12/15/20/25/35 ns address access time
 - 3/3/4/5/6/8 ns output enable access time
- Low power consumption
 - Active: 660 mW max (10 ns cycle)
 - Standby: 11 mW max, CMOS I/O
2.75 mW max, CMOS I/O, L version
 - Very low DC component in active power
- 2.0V data retention (L version)
- Equal access and cycle times
- Easy memory expansion with \overline{CE} and \overline{OE} inputs
- TTL-compatible, three-state I/O
- 28-pin JEDEC standard packages
 - 300 mil PDIP and SOJ
Socket compatible with 7C512 and 7C1024
 - 330 mil SOIC
 - 8×13.4 TSOP
- ESD protection > 2000 volts
- Latch-up current > 200 mA

LOGIC BLOCK DIAGRAM



AS7C256-01

PIN ARRANGEMENT



AS7C256-02

SELECTION GUIDE

	7C256-10	7C256-12	7C256-15	7C256-20	7C256-25	7C256-35	Unit
Maximum Address Access Time	10	12	15	20	25	35	ns
Maximum Output Enable Access Time	3	3	4	5	6	8	ns
Maximum Operating Current	120	115	110	100	90	80	mA
Maximum CMOS Standby Current	2.0	2.0	2.0	2.0	2.0	2.0	mA
	L	0.5	0.5	0.5	0.5	0.5	mA



FUNCTIONAL DESCRIPTION

The AS7C256 is a high performance CMOS 262,144-bit Static Random Access Memory (SRAM) organized as 32,768 words \times 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 10/12/15/20/25/35 ns with output enable access times (t_{OE}) of 3/3/4/5/6/8 ns are ideal for high performance applications. A chip enable (\overline{CE}) input permits easy memory expansion with multiple-bank memory organizations.

When \overline{CE} is HIGH the device enters standby mode. The standard AS7C256 is guaranteed not to exceed 11 mW power consumption in standby mode; the L version is guaranteed not to exceed 2.75 mW, and typically requires only 500 μ W. The L version also offers 2.0V data retention, with maximum power consumption in this mode of 300 μ W.

A write cycle is accomplished by asserting chip enable (\overline{CE}) and write enable (\overline{WE}) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of \overline{WE} (write cycle 1) or \overline{CE} (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}).

A read cycle is accomplished by asserting chip enable (\overline{CE}) and output enable (\overline{OE}) LOW, with write enable (\overline{WE}) HIGH. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is HIGH, or write enable is LOW, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C256 is packaged in all high volume industry standard packages.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Voltage on Any Pin Relative to GND	V_t	-0.5	+7.0	V
Power Dissipation	P_D	-	1.0	W
Storage Temperature (Plastic)	T_{stg}	-55	+150	$^{\circ}$ C
Temperature Under Bias	T_{bias}	-10	+85	$^{\circ}$ C
DC Output Current	I_{out}	-	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

\overline{CE}	\overline{WE}	\overline{OE}	Data	Mode
H	X	X	High Z	Standby (I_{SB} , I_{SB1})
L	H	H	High Z	Output Disable
L	H	L	D_{out}	Read
L	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH



RECOMMENDED OPERATING CONDITIONS

(T_a = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input Voltage	V _{IH}	2.2	–	V _{CC} +1	V
	V _{IL}	–0.5*	–	0.8	V

*V_{IL} min = –3.0V for pulse width less than t_{RC}/2.

DC OPERATING CHARACTERISTICS¹

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test Conditions	-10		-12		-15		-20		-25		-35		Unit	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input Leakage Current	I _{L L}	V _{CC} = Max, V _{in} = GND to V _{CC}	–	1	–	1	–	1	–	1	–	1	–	1	µA	
Output Leakage Current	I _{L O}	$\overline{CE} = V_{IH}$, V _{CC} = Max, V _{out} = GND to V _{CC}	–	1	–	1	–	1	–	1	–	1	–	1	µA	
Operating Power Supply Current	I _{CC}	$\overline{CE} = V_{IL}$, f = f _{max} , I _{out} = 0 mA		–	120	–	115	–	110	–	100	–	90	–	80	mA
			L	–	115	–	110	–	105	–	95	–	85	–	75	mA
Standby Power Supply Current	I _{SB}	$\overline{CE} = V_{IH}$, f = f _{max}		–	45	–	40	–	30	–	30	–	25	–	25	mA
			L	–	40	–	35	–	25	–	25	–	20	–	20	mA
	I _{SB1}	$\overline{CE} > V_{CC} - 0.2V$, f = 0, V _{in} ≤ 0.2V or V _{in} ≥ V _{CC} - 0.2V	L	–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	mA
Output Voltage	V _{OL}	I _{OL} = 8 mA, V _{CC} = Min	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	V	
	V _{OH}	I _{OH} = –4 mA, V _{CC} = Min	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	V	

CAPACITANCE²

(f = 1 MHz, T_a = Room Temperature, V_{CC} = 5V)

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input Capacitance	C _{IN}	A, \overline{CE} , \overline{WE} , \overline{OE}	V _{in} = 0V	5	pF
I/O Capacitance	C _{I/O}	I/O	V _{in} = V _{out} = 0V	7	pF



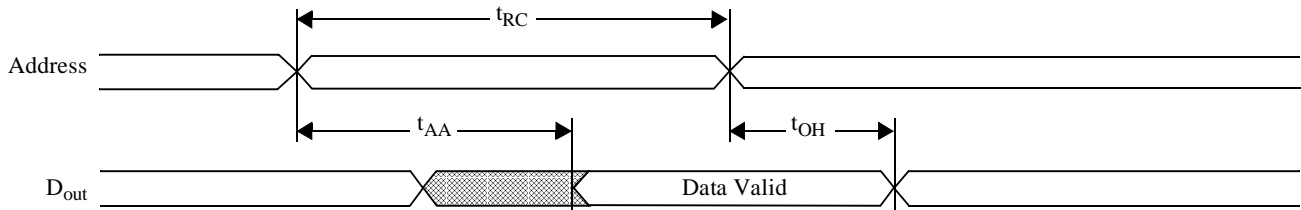
READ CYCLE^{3, 9}

($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0^\circ C$ to $+70^\circ C$)

Parameter	Symbol	-10		-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	10	-	12	-	15	-	20	-	25	-	35	-	ns	
Address Access Time	t_{AA}	-	10	-	12	-	15	-	20	-	25	-	35	ns	3
Chip Enable (\overline{CE}) Access Time	t_{ACE}	-	10	-	12	-	15	-	20	-	25	-	35	ns	3
Output Enable (\overline{OE}) Access Time	t_{OE}	-	3	-	3	-	4	-	5	-	6	-	8	ns	
Output Hold from Address Change	t_{OH}	2	-	3	-	3	-	3	-	3	-	3	-	ns	5
\overline{CE} LOW to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	3	-	3	-	3	-	ns	4, 5
\overline{CE} HIGH to Output in High Z	t_{CHZ}	-	3	-	3	-	4	-	5	-	6	-	8	ns	4, 5
\overline{OE} LOW to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	0	-	0	-	ns	4, 5
\overline{OE} HIGH to Output in High Z	t_{OHZ}	-	3	-	3	-	4	-	5	-	6	-	8	ns	4, 5
Power Up Time	t_{PU}	0	-	0	-	0	-	0	-	0	-	0	-	ns	4, 5
Power Down Time	t_{PD}	-	10	-	12	-	15	-	20	-	25	-	35	ns	4, 5

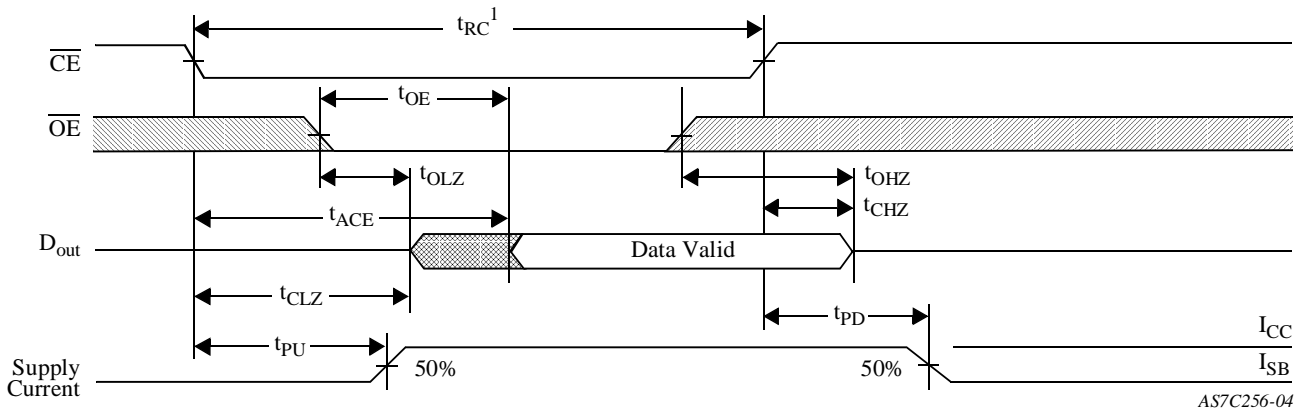
TIMING WAVEFORM OF READ CYCLE 1^{3, 6, 7, 9}

(Address Controlled)



TIMING WAVEFORM OF READ CYCLE 2^{3, 6, 8, 9}

(\overline{CE} Controlled)



AS7C256-04



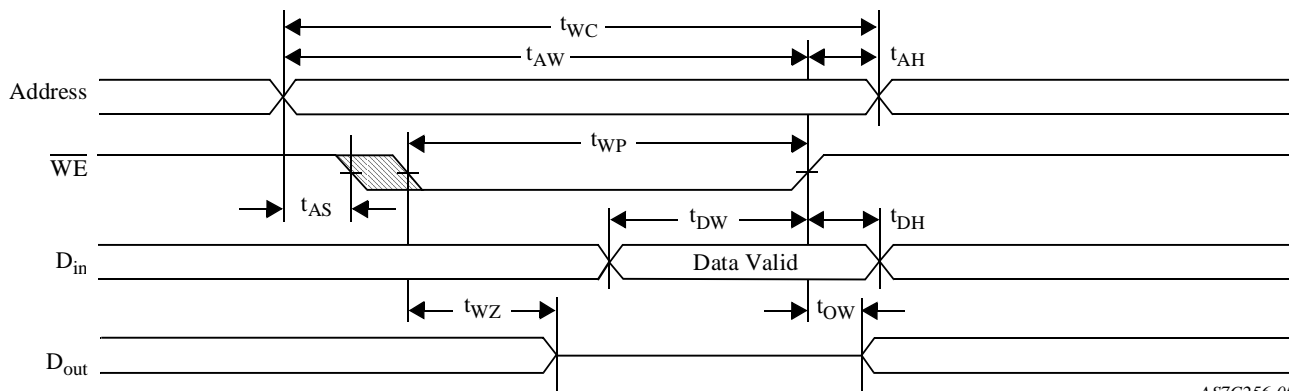
WRITE CYCLE ¹¹

($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0^\circ C$ to $+70^\circ C$)

Parameter	Symbol	-10		-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	10	-	12	-	15	-	20	-	20	-	30	-	ns	
Chip Enable to Write End	t_{CW}	9	-	10	-	12	-	12	-	15	-	20	-	ns	
Address Setup to Write End	t_{AW}	9	-	10	-	12	-	12	-	15	-	20	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	7	-	8	-	9	-	12	-	15	-	17	-	ns	
Address Hold From End of Write	t_{AH}	0	-	0	-	0	-	0	-	0	-	0	-	ns	
Data Valid to Write End	t_{DW}	6	-	6	-	8	-	10	-	10	-	15	-	ns	
Data Hold Time	t_{DH}	0	-	0	-	0	-	0	-	0	-	0	-	ns	4, 5
Write Enable to Output in High Z	t_{WZ}	-	5	-	5	-	5	-	5	-	5	-	5	ns	4, 5
Output Active from Write End	t_{OW}	3	-	3	-	3	-	3	-	3	-	3	-	ns	4, 5

TIMING WAVEFORM OF WRITE CYCLE 1 ^{10, 11}

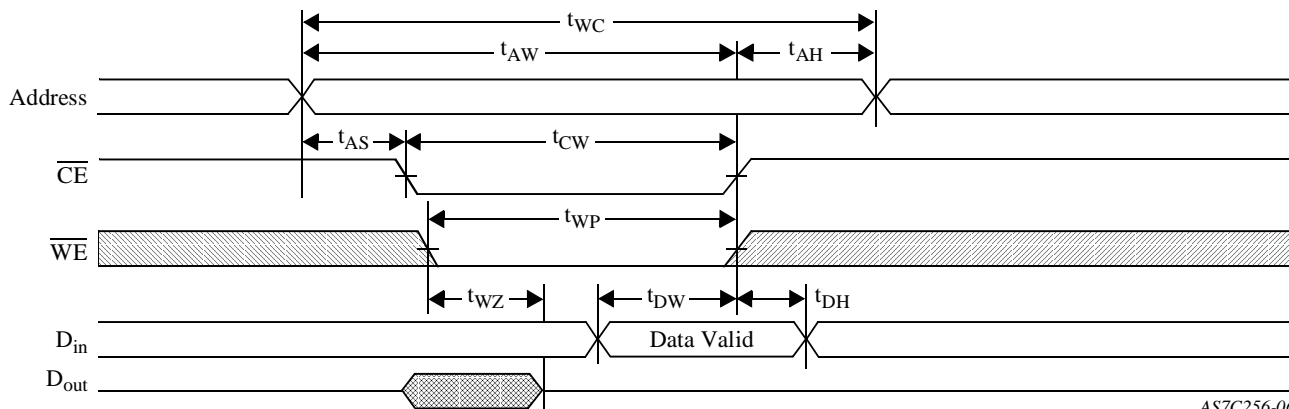
(\overline{WE} Controlled)



AS7C256-05

TIMING WAVEFORM OF WRITE CYCLE 2 ^{10, 11}

(\overline{CE} Controlled)



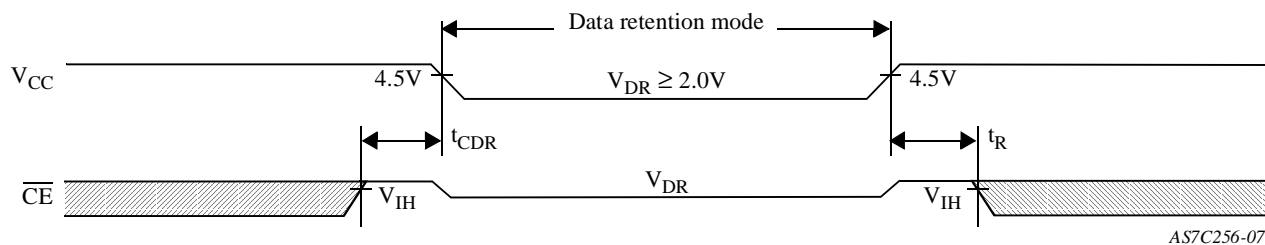
AS7C256-06



DATA RETENTION CHARACTERISTICS (L Version Only)

Parameter	Symbol	Test Conditions	Min	Max	Unit
V _{CC} for Data Retention	V _{DR}	V _{CC} = 2.0V	2.0	–	V
Data Retention Current	I _{CCDR}	$\overline{CE} \geq V_{CC}-0.2V$	–	150	μA
Chip Enable to Data Retention Time	t _{CDR}	V _{in} ≥ V _{CC} -0.2V or V _{in} ≤ 0.2V	0	–	ns
Operation Recovery Time	t _R		t _{RC}	–	ns
Input Leakage Current	I _{LI}		–	1	μA

DATA RETENTION WAVEFORM (L Version Only)



AS7C256-07

AC TEST CONDITIONS

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

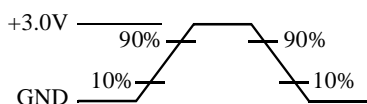


Figure A: Input Waveform
AS7C256-08

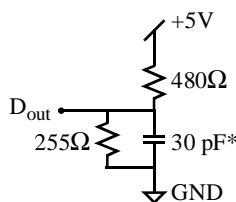


Figure B: Output Load
AS7C256-09

Thevenin Equivalent:
D_{out} ← 168Ω → +1.728V

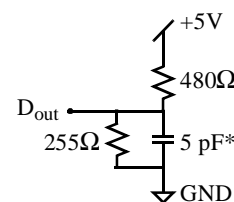


Figure C: Output Load for t_{CLZ}, t_{CHZ}
AS7C256-10

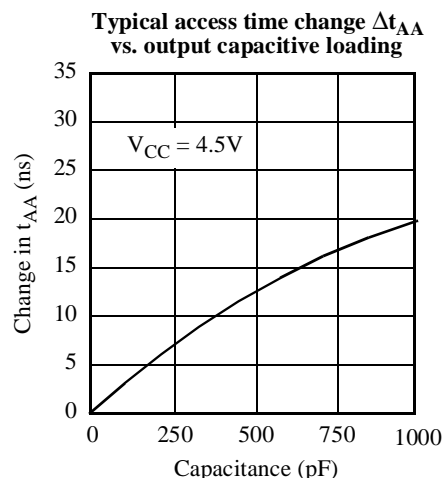
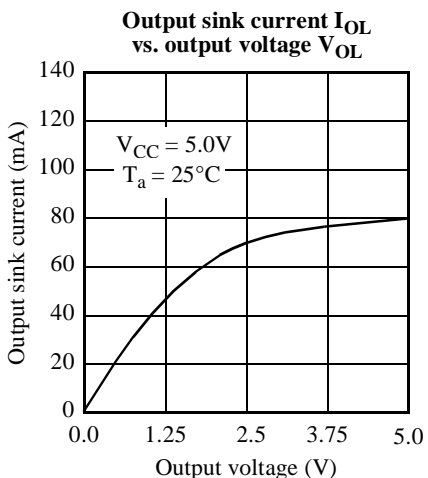
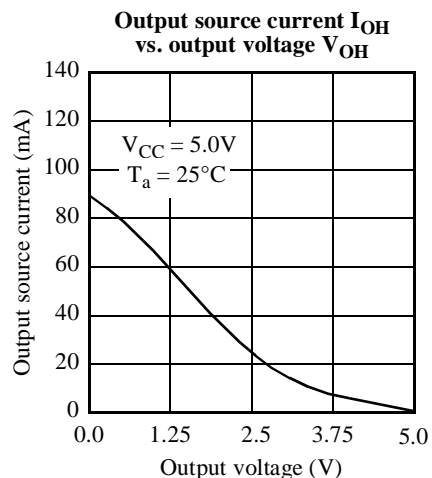
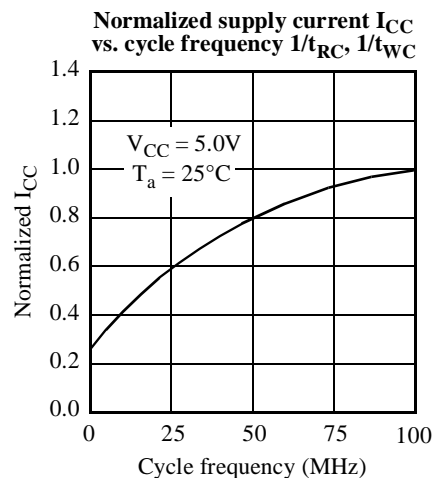
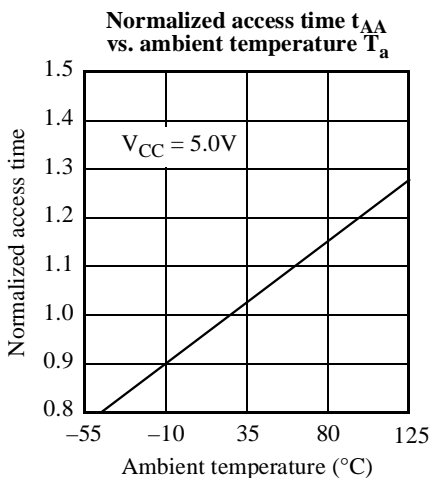
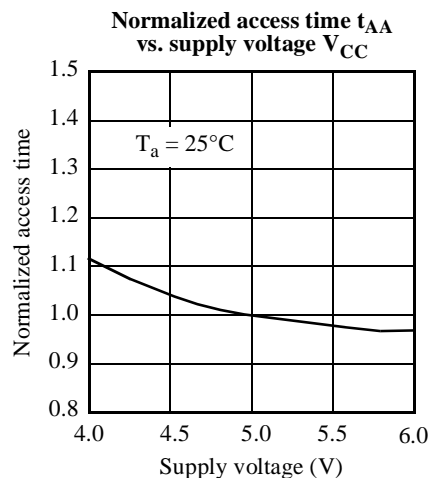
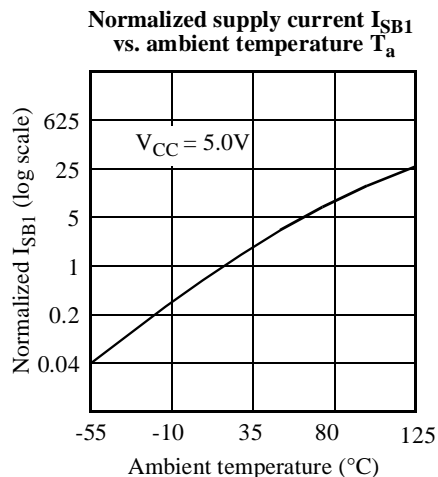
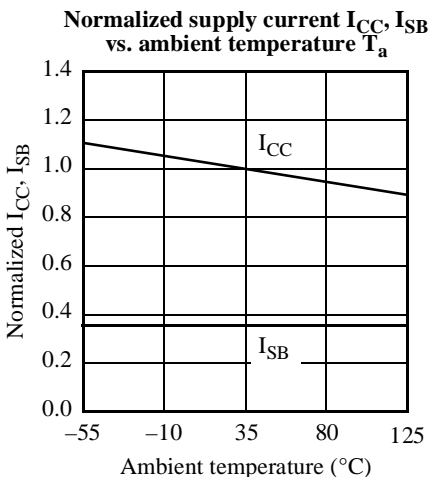
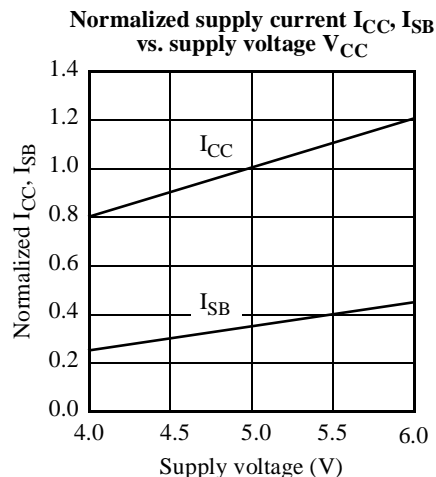
*including scope and jig capacitance

NOTES

1. During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification.
2. This parameter is sampled and not 100% tested.
3. For test conditions, see AC Test Conditions, Figures A, B, C.
4. t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5. This parameter is guaranteed but not tested.
6. \overline{WE} is HIGH for read cycle.
7. \overline{CE} and \overline{OE} are LOW for read cycle.
8. Address valid prior to or coincident with \overline{CE} transition LOW.
9. All read cycle timings are referenced from the last valid address to the first transitioning address.
10. \overline{CE} or \overline{WE} must be HIGH during address transitions.
11. All write cycle timings are referenced from the last valid address to the first transitioning address.



TYPICAL DC AND AC CHARACTERISTICS





ORDERING CODES

Package / Access Time	10 ns	12 ns	15 ns	20 ns	25 ns	35 ns
Plastic DIP, 300 mil	AS7C256-10PC AS7C256L-10PC	AS7C256-12PC AS7C256L-12PC	AS7C256-15PC AS7C256L-15PC	AS7C256-20PC AS7C256L-20PC	AS7C256-25PC AS7C256L-25PC	AS7C256-35PC AS7C256L-35PC
Plastic SOJ, 300 mil	AS7C256-10JC AS7C256L-10JC	AS7C256-12JC AS7C256L-12JC	AS7C256-15JC AS7C256L-15JC	AS7C256-20JC AS7C256L-20JC	AS7C256-25JC AS7C256L-25JC	AS7C256-35JC AS7C256L-35JC
Plastic SOIC, 330 mil	AS7C256-10SC AS7C256L-10SC	AS7C256-12SC AS7C256L-12SC	AS7C256-15SC AS7C256L-15SC	AS7C256-20SC AS7C256L-20SC	AS7C256-25SC AS7C256L-25SC	AS7C256-35SC AS7C256L-35SC
TSOP 8x13.4	AS7C256-10TC AS7C256L-10TC	AS7C256-12TC AS7C256L-12TC	AS7C256-15TC AS7C256L-15TC	AS7C256-20TC AS7C256L-20TC	AS7C256-25TC AS7C256L-25TC	AS7C256-35TC AS7C256L-35TC

PART NUMBERING SYSTEM

AS7C	256	X	-XX	X	C	
SRAM Prefix	Device Number	Blank L	= Standard Power = Low Power	Access Time	Package: P = PDIP 300 mil J = SOJ 300 mil S = SOIC 330 mil T = TSOP 8x14	Commercial Temperature Range, 0°C to 70 °C

REPRESENTATIVES, DISTRIBUTORS, AND SALES OFFICES

DOMESTIC REPS	INDIANA CC Electro Sales (317) 921-5000	NEW HAMPSHIRE Kitchen & Kutchin Inc. (617) 229-2660	SOUTH CAROLINA Concord Component (919) 846-3441	CANADA Tech Trek Ltd. Mississauga: (905) 238-0366 Montreal: (514) 337-7540 Ottawa: (613) 599-8787 Vancouver: (604) 276-8735 Calgary: (403) 291-6866	PUERTO RICO Micro-Electronic Comp. (809) 746-9897
ALABAMA Concord Component (205) 772-8883	KANSAS CenTech (816) 358-8100	NEW JERSEY North: ERA Associates (800) 645-5500 South: Vantage Sales (609) 424-6777	SOUTH DAKOTA D. A. Case Associates (612) 831-6777		TAIWAN Asian Specific Tech. +886-2-521-2363 Puteam International +886-2-729-0373
ARIZONA Competitive Technology (602) 265-9224	KENTUCKY CC Electro Sales (317) 921-5000	NEW MEXICO Competitive Technology (602) 265-9224	TENNESSEE Concord Component (205) 772-8883		
ARKANSAS Southern States Marketing (214) 238-7500	LOUISIANA Southern States Marketing North: (214) 238-7500 South: (713) 868-5180	NEW YORK NYC: ERA Associates (516) 543-0510 Upstate: Tri-Tech Rochester (716) 385-6500 Birmingham (607) 722-3580 Fishkill (914) 897-5611	TEXAS Southern States Marketing Austin: (512) 835-5822 Dallas: (214) 238-7500 Houston: (713) 868-5180		DISTRIBUTORS All-American Locations Nationwide Headquarters: (305) 621-8282 Axis Components Sunnyvale, CA (408) 522-9595 Axis Components Irvine, CA (714) 459-5510 Future Electronics Locations Worldwide Headquarters: (514) 594-7710 Interface Electronics Hopkinton, MA (800) 632-7792 (508) 435-0100
CALIFORNIA North: Brooks Technical (415) 960-3880 LA Area: Competitive Tech. (714) 450-0170 San Diego: ATS (619) 634-1488	MAINE Kitchen & Kutchin Inc. (617) 229-2660	NORTH CAROLINA Concord Component (919) 846-3441	UTAH Charles Fields & Assoc. (801) 299-8228	EUROPE Britcomp Sales Surrey, England +44-1932 347077 +44-1932 346256 Munich, Germany +49-894488496 Athismons, France +33-1-69387678	
COLORADO Technology Sales (303) 792-8835	MARYLAND Chesapeake Technology (301) 236-0530	NORTH DAKOTA D. A. Case Associates (612) 831-6777	VERMONT Kitchen & Kutchin Inc. (617) 229-2660	HONG KONG Eastele Technology +85-2-798-8860	
CONNECTICUT Kitchen & Kutchin Inc. (203) 239-0212	MASSACHUSETTS Kitchen & Kutchin Inc. (617) 229-2660	OHIO Midwest Marketing Assoc. Lyndhurst: (216) 381-8575 Dayton: (513) 433-2511	VIRGINIA Chesapeake Technology (301) 236-0530	INDIA Priya Electronics, Inc. San Jose, CA USA (408) 954-1866	
DELAWARE Vantage Sales (609) 424-6777	MICHIGAN Enco Group (810) 338-8600	OKLAHOMA Southern States Marketing (214) 238-7500	WASHINGTON ES/Chase (206) 823-9535	ISRAEL Eldis Technology +972-9-562-666	
FLORIDA Micro-Electronic Comp. Deerfield Beach (305) 426-8944 Tampa (813) 393-5011	MINNESOTA D. A. Case Associates (612) 831-6777	OREGON ES/Chase (503) 684-8500	WEST VIRGINIA Chesapeake Technology (301) 236-0530	JAPAN Actes Engineering Tokyo +81-3-3769-3029 Rohm Co. Ltd. Kyoto +81-75-311-2121	SALES OFFICES HEADQUARTERS Alliance Semiconductor San Jose, CA (408) 383-4900 NORTHEAST AREA Alliance Semiconductor Boston, MA (617) 239-8127
GEORGIA Concord Component (404) 416-9597	MISSOURI East: CenTech (314) 291-4230 West: CenTech (816) 358-8100	PENNSYLVANIA East: Vantage Sales (609) 424-6777 West: Midwest Marketing (216) 381-8575	WISCONSIN D. A. Case Associates (612) 831-6777	KOREA FM Korea +822-575-9720 Woo Young Tech +822-369-7099	
HAWAII Brooks Technical (415) 960-3880	MISSISSIPPI Concord Component (205) 772-8883	RHODE ISLAND Kitchen & Kutchin Inc. (617) 229-2660	WYOMING Technology Sales (303) 777-9726	MALAYSIA, SINGAPORE Technology Distr. Pte Ltd. +65-299-7811	TECHNICAL CENTER TAIWAN Alliance Semiconductor +886-2-723-9944
IDAHO ES/Chase (503) 684-8500	MONTANA ES/Chase (503) 684-8500		INTERNATIONAL AUSTRALIA NJS Technology Pty Ltd. Mulgrave, Victoria +61-3-562-1244 R&D Electronics Dingley, Victoria +61-3-558-0444		
ILLINOIS North: El-Mech (312) 794-9100 South: CenTech (314) 291-4230	NEBRASKA CenTech (816) 358-8100				
	NEVADA North: Brooks Technical (415) 960-3880 South: Competitive Tech. (602) 265-9224				

Alliance Semiconductor reserves the right to make changes in this data sheet at any time to improve design and supply the best product possible. Alliance Semiconductor cannot assume responsibility for circuits shown or represent that they are free from patent infringement. Alliance products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Alliance. The Alliance logo is a trademark of Alliance Semiconductor Corporation. All other trademarks are property of their respective holders.

ALLIANCE SEMICONDUCTOR
3099 North First Street San Jose, CA 95134
(408) 383-4900 Fax (408) 383-4999