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PRELIMINARY

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CHIPS 82C5059
Single Chip PC-AT
Controller Solution
Reference Manual
Revision B

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Revision History

Revision	Change Activity	Date	Approved
A	First Release	4/28/89	BJM
B	Second Release	?	

PREFACE

AUDIENCE

This manual is intended for firmware design engineers who are interested in programming or supporting the CHIPS 82C5059 PC-AT Single Chip Controller Solution; however, such topics as pin descriptions that would be of interest to hardware design engineers are also addressed.

SCOPE

This manual contains the information a firmware design engineer needs to program this chip to implement the CHIPS 82C5059 PC-AT Single Chip Controller Solution on a device controller. **It is assumed the reader already has a working knowledge of controllers.**

CONTENTS

The information in this manual is divided into four chapters, four appendixes, an index, and a glossary.

- Chapter 1 provides an overview of the CHIPS 82C5059 PC-AT Single Chip Controller Solution.
- Chapter 2 which is intended for hardware design engineers describes the CHIPS 82C5059 hardware specifications. It supplies physical and functional pin specifications, signal descriptions, electrical specifications, and packaging specifications.
- Chapter 3 which is directed at firmware engineers describes the operational modes of the 82C5059 Registers.
- Chapter 4 which is intended for firmware engineers provides a detailed description of the commands and operation of the 82C5059.
- Appendix A contains the track format options for MFM, RLL2,7, and ESDI soft and hard sectored track formats.
- Appendix B contains a figure and an example of a table setup to initialize the Format Parameter Register File.
- Appendix C provides the DRAM from SRAM pin conversion.

- Appendix D contains schematics for a typical controller configuration with the 82C5059 and 256K x 9 DRAM, 64K x 9 DRAM, or 64K x 8 SRAM configuration options.
- Appendix E contains the crystal circuit application notes.
- The glossary provides a list of abbreviations, and definitions of the key terms used throughout this manual.

RELATED PUBLICATIONS

- *CHIPS 5055B Memory Controller & Programmable Data Sequencer Reference Manual.* (Document Number: 3001469, Revision C, September 30, 1988).
- *ESDI Specification, ANSI Working Document.*
- *Seagate STXXX Micro Winchester OEM Manual.*

NOTATIONAL CONVENTIONS

The following conventions are used throughout this manual:

UPPERCASE	is used to indicate names of commands and signals.
-	a minus sign prefix to a signal name indicates an active low polarity.
+	a plus sign prefix to a signal name indicates an active high polarity.

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INTRODUCTION

The CHIPS 82C5059 PC-AT Single Chip Controller Solution is a CMOS LSI Applications Specific Integrated Circuit (ASIC) designed to be the primary component in a high-performance intelligent PC-AT Winchester disk controller system. The 82C5059 provides three essential functions in a disk controller system: It manages the flow of data for a serial peripheral, it controls access to the external RAM buffer memory that is required for such transfers and it directly interfaces to an PC-AT type system bus. The 82C5059 is designed to be used with a microprocessor having either a Z8- or 8051-type bus structure.

The 82C5059 consists of three functional sections:

1. A DMA controller.
2. A Data sequencer.
3. An PC-AT interface controller.

The CHIPS 82C5059 incorporates a dual-bus architecture, providing separate ports for microprocessor and memory buffer operations. With the goal of achieving the highest possible performance, this dual-bus structure is used so that disk data transfers can occur simultaneously with microprocessor operations.

In the DMA Controller, Channel 0 is used for moving blocks of data between the Data Sequencer and the external buffer, while Channel 1 is used for moving blocks of data between the PC-AT host interface and the buffer. When the data sequencer is not using Channel 0, this channel can also be used to allow the microprocessor to access the RAM buffer. DMA controller operation is programmed by writing the DMA Controller Registers, while operation may be monitored by reading the DMA Controller Registers.

The programmable data sequencer provides format control, error detection, and serial/parallel (SERDES) conversion functions normally associated with disk controllers. It is designed to be used with NRZ (Non-Return to Zero) interfaces such as those used in the ESDI (Enhanced Small Device Interface) or any of the CHIPS family of encode/decode VCO devices. Flexible operation of the sequencer is made possible by write registers that program its operation, while read registers allow the firmware to monitor operation. In addition, complete flexibility in disk formatting is permitted by a 64-byte on device format RAM, which is accessed through three of the Data Sequencer Write Registers (WR25, WR30 & WR31).

In addition to an external RAM buffer, a byte-oriented microprocessor such as the Z8 or 8051, with its associated memory, the CHIPS 82C5059 may be connected with the CHIPS 5070 Encode/Decode/PLL for MFM encoding/decoding up to 5 Mbits/second, or the CHIPS 5027 Encode/Decode/PLL for RLL 2,7 encoding/decoding up to 10 Mbits/second thus providing a complete controller solution for an embedded PC-AT interfacing disk drive.

ARCHITECTURAL OVERVIEW

The following is a brief description of the major circuit blocks of the CHIPS 82C5059 (See Figure 1-1).

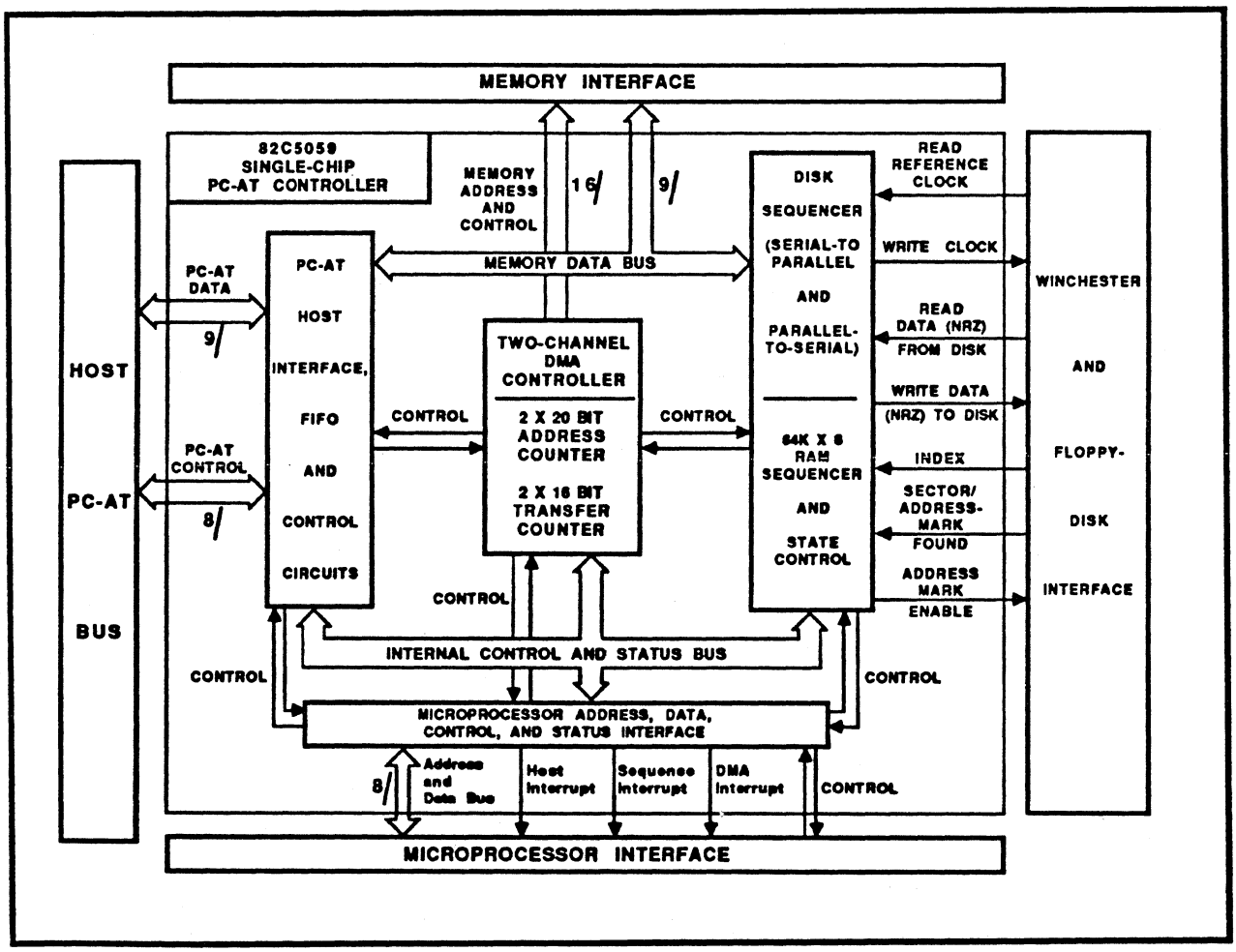


Figure 1-1. Functional Block Diagram

The first five blocks constitute the DMA section of the device:

1. **Parallel DMA Interface.** All parallel data transfers from either the sequencer, the buffer, or the microprocessor are transferred through this block.

2. **Counters.** This block consists of two address up-counters and two transfer down-counters. Each are 16 bits allowing $65{,}536_{10}$ maximum. There is one address counter and one transfer counter for each of the two channels, providing independent channel control and **concurrent operation**. Both channels share a common memory, the buffer RAM.

3. **Address Multiplexer.** As a function of DMA priority and resolution (see next block), this block puts the address for Channel 0 or Channel 1 onto the external memory address pins (MEM A0-14). Channel 0 is the highest priority channel; Channel 1 is the lowest. Priority is only important when there is a conflict; that is, if there is a collision, Channel 0 wins. When the 82C5059 is configured with a dynamic RAM (DRAM) buffer, Refresh is the lowest priority.

4. **Priority Resolver/Channel Control.** This block, through the microprocessor and the micro control and decode logic (see below), determines which channel is enabled and the polarity of the control lines to the host buffer interface.

The following block is shared by the DMA controller and the data sequencer functions:

5. **Micro Control and Decode.** This block does all register address decoding. It decodes the microprocessor addresses (AD0-7), providing the required control to the address counters and the transfer counters. This block also contains registers that provide information for the priority resolver/channel control block. These are the Channel 0 and Channel 1 Control Registers (WR08 and WR09) and the Memory Cycle Timing Register (WR10). Thus this block serves both the DMA controller and the data sequencer functions.

The following describes the data sequencer portion of the circuitry:

6. **Format RAM.** The format RAM is a 64 X 8 bit RAM that allows for 16 pairs of 8-bit bytes to be used as count and value numbers associated with format states. This allows for 16 format states having associated count and value numbers. A state corresponds to a type of field encountered on a disk. Depending upon the type of field on the disk, a value may or may not be used, like a sync field would have a value associated with it but a CRC/ECC field would not. A count is always used, since it is the number of byte times that the sequencer remains in its current state (i.e., loops back on itself).

Refer to Appendix A for track format examples and descriptions.

7. **Sequencer.** This block is fed by the format RAM. The sequencer addresses the format RAM and gets back a count. The sequencer loads an internal counter with this number and begins to count down. This number programs the device to be in a given field for a certain amount of time, or for a certain number of bytes. There are sixteen different states with each state representing a specific field in the overall disk format.

Refer to Appendix B, Table B-1 and Figure B-1 for an example of ST506/412 soft sector format.

8. **State Decode Control and Generation.** The sequencer block feeds the state decode control and generation block, which in turn feeds nearly all other blocks in the data sequencer portion of the 82C5059. control signals are derived from the sequencer state and the current field count.

9. **CRC/ECC Generator.** In read mode, NRZ data comes into this block and, based on state and timing from the state control generation logic, the data is checked for the proper CRC or ECC bits. The data is then fed to the serial/parallel converter (SERDES) block.

In write mode, NRZ data arrives from the serial/parallel converter (SERDES) block and CRC or ECC bits are generated according to user-programmable registers (WR11 and Bit 6 of WR28). In addition, the signal WRT CLK (write clock) is generated and output. For the various CRC/ECC polynomials that can be used, see the "CRC/ECC" section that follows.

10. **Serial/Parallel Converter (SERDES).** In the read direction, this block converts serial data to parallel; in the write direction it converts parallel data to serial. NRZ DATA IN is synchronized to RD REFCLK and NRZ DATA OUT is synchronized to WRTCLK.

11. **ID Compare Error.** This block compares, on a real-time, byte-by-byte basis, data being read from the sector ID of a disk to the ID registers programmed (WR20-23) by the user. The output of this block goes to the state decode control and generation block, which has the power to stop processing, retries, etc.

12. **AD I/O Buffer.** This is an I/O buffer. Internal to the 82C5059 is a bidirectional data bus, and this block buffers data between the internal bus and the microprocessor.

From the microprocessor AD(7:0) interface bus (multiplexed low order address and data), (data) or address/data come into an internal buffer and this block drives the internal data bus, D(7:0). D(7:0) also goes to the micro control and decode block, which picks off the address at ALE (8051 mode) or -AS (Z8 mode) time.

Note: The AD(7:0) bus, via the internal bus, D(7:0), supplies the address and transfer counters with their initial values. The two address counter pairs are WR0 and WR1 for Channel 0, and WR4 and WR5 for Channel 1; the two transfer counters are effectively WR2 and WR3 for Channel 0, and WR6 and WR7 for Channel 2. While AD0-7 provides the initial values, the micro control and decode block decodes the addresses from AD0-7 and generates the appropriate controls.

Inside the 82C5059, the AD I/O buffer drives that portion of the device that is microprocessor controlled.

INTERFACES

There are four interfaces on the CHIPS 82C5059:

1. The PC-AT host interface consists of a 16-bit data bus D_(15:0), and all the control signals each with 16 ma. tri-state drivers and Schmidt trigger receivers.

2. The memory interface consists of an 8-bit data bus with parity (MEM D(0-7) & P), an address bus, along with the memory control signals. Note that the address bus is 15 bits (MEMA0-14), addressing up to 32K bytes. Using two chip selects, 64K bytes may be addressed in SRAM mode, and 1 Megabyte may be addressed in DRAM mode.

Refer to Appendix C for DRAM addressing.

3. The microprocessor interface consists of an 8-bit multiplexed address/data bus (AD(7:0), and various microprocessor bus control signals.

4. The drive interface contains the serial data lines to and from the disk (or the Encoder/Decoder, PLL circuitry) and various control signals required for reading and writing a disk.

REGISTERS

There are five groups of registers in the 82C5059. One group is used for controlling and monitoring DMA controller operation. This group consists of Write Registers WR00-15 and Read Registers RR00-15. Another group is used for controlling and monitoring data sequencer operation. These are Write Registers WR16-34, and Read Registers RR16-31. All of these registers can be directly written or read.

Still another group is used for controlling and monitoring PC-AT interface operation. These are Write Registers WR64-79, and Read Registers RR64-79. All of these registers can be directly written or read.

The format control group is available for formatting of the disk. This group is indirectly accessed by WR30 (Value Register) and WR31 (Count Register) and WR25. The format RAM is viewed as sixteen register pairs containing information that determines the overall format of the disk. This information is written by indexing via WR25 and writing the **value** of the field into WR30 and the **count** (the number of times the value is repeated in the stream) in WR31.

A summary of the registers available in the 82C5059 is provided in Chapter 3, Tables 3-1, 3-2, 3-3 and 3-4.

CRC/ECC

The CRC/ECC block generates and checks the CRC or ECC bytes that are appended to the sector ID and data fields. WR11 and WR28 determine the selection of the **computer generated polynomial.** Bits 1 and 2 of WR11 determine the selection of the polynomial for the data fields:

16-bit CRC: (X16)+(X12)+(X15)+1 (Floppy Compatible CRC)
32-bit ECC: (X32)+(X24)+(X18)+(X15)+(X14)+(X11)+(X8)+(X7)+1
32-bit ECC: (X32)+(X28)+(X26)+(X19)+(X17)+(X10)+(X6)+(X2)+1
48-bit ECC: Proprietary. *
56-bit ECC: Proprietary. *

If Bit 6 of WR28 is cleared (0), then the ID field will use the same polynomial as selected for the data field above. If Bit 6 is set (1), then the ID field will use the 16-bit CRC polynomial--regardless of the selection of the polynomial for the data field. This allows for great flexibility in the choice of error detection schemes. The actual correction is achieved by the microprocessor use of the syndrome returned from the device upon receipt of an error. Sector size, and the level of code optimization have an impact upon both detection and correction capability.

* Contact CHIPS for sublicense of the polynomials.

FEATURES

Memory Controller Features:

- High-performance dual-bus architecture
- Two independent DMA channels
- 10 megabyte device bandwidth at 40 Mhz clock
- 20-bit address and 16 bit transfer count registers for each channel
- Holding registers for address counts for non-contiguous memory transfers
- Independent mask for channel-end interrupt
- Bus access resolved on channel priority basis
- Programmable interrupt polarity
- Programmable auto-count reinitialization
- Programmable memory access cycle timing (2 to 5 clock cycles)
- Buffer memory address for 64K SRAM (2 memory chip enables for 32Kx8 SRAM)
- DRAM support for up to 1 MegaByte
- Data memory parity generate and check option
- Channel 1 optional level request (for synchronous transfer)

PC-AT Interface Features:

- Direct interface to PC-AT compatible systems
- High current drivers for host interface
- Schmidt trigger inputs form host interface
- Configurable primary or secondary address
- 2 word FIFO
- Automatic BUSY, INTRQ and ECC Mode
- Compatible with PC-AT drive 40-pin bus interface
- Flexible interrupt capability

Programmable Data Sequencer Features:

- High-level instruction set including:
  - Read/Write
  - Individual sector formatting
  - Track formatting
  - Read ID
  - Read/Write long
  - Read syndrome
  - Verify (with data in buffer)
  - Check data ECC
  - Check track format
- Supports up to 20 MHz serial bit rate (NRZ)
- Programmable disk format:
  - Programmable sector size up to 65,536 bytes per sector
  - Programmable ID data and size
  - Programmable gap sizes and fill characters
  - User-definable Header Flag Byte or Nibble
  - Selectable 32, 48, or 56 bit ECC polynomial and ID CRC or ECC or flexible disk compatible ID and data field CRC
- Hard or soft sector modes
- NRZ serial disk interface
- Direct interface to ESDI-type drives, both hard and soft sectored
- Multi-sector transfer capability with automatic sector increment
- Programmable automatic ID retries
- Low power consumption (CMOS)
- Logic to transfer data between the micro bus and buffer memory
- ESDI ID Sync Timeout programmable
- ESDI Write Gate to AM ENABLE programmable
- Format Track with data from buffer
- Programmable Write Gate disable for embedded servo

82C5059 Hardware Specifications 2

This chapter is directed at hardware engineers intending to design the CHIPS 82C5059 PC-AT Single Chip Controller Solution into their systems. Physical and functional pin specifications, signal descriptions, timing specifications, and electrical specifications are provided.

PHYSICAL SPECIFICATIONS

The CHIPS 82C5059 device is available in an 100-pin QFP package. Package specifications and pin-out diagrams are provided for this package.

100-pin QFP Package

Refer to Figure 2-1 for physical pin out of the 100-pin QFP package. Table 2-1 provides a pin list for the 100-pin QFP package. Note an active low polarity is indicated by a minus sign (-) prefix; a plus sign (+) prefix indicates high polarity. For information on this package's pin functions, refer to the section "Signal Descriptions" and Table 2-1 later in this chapter.

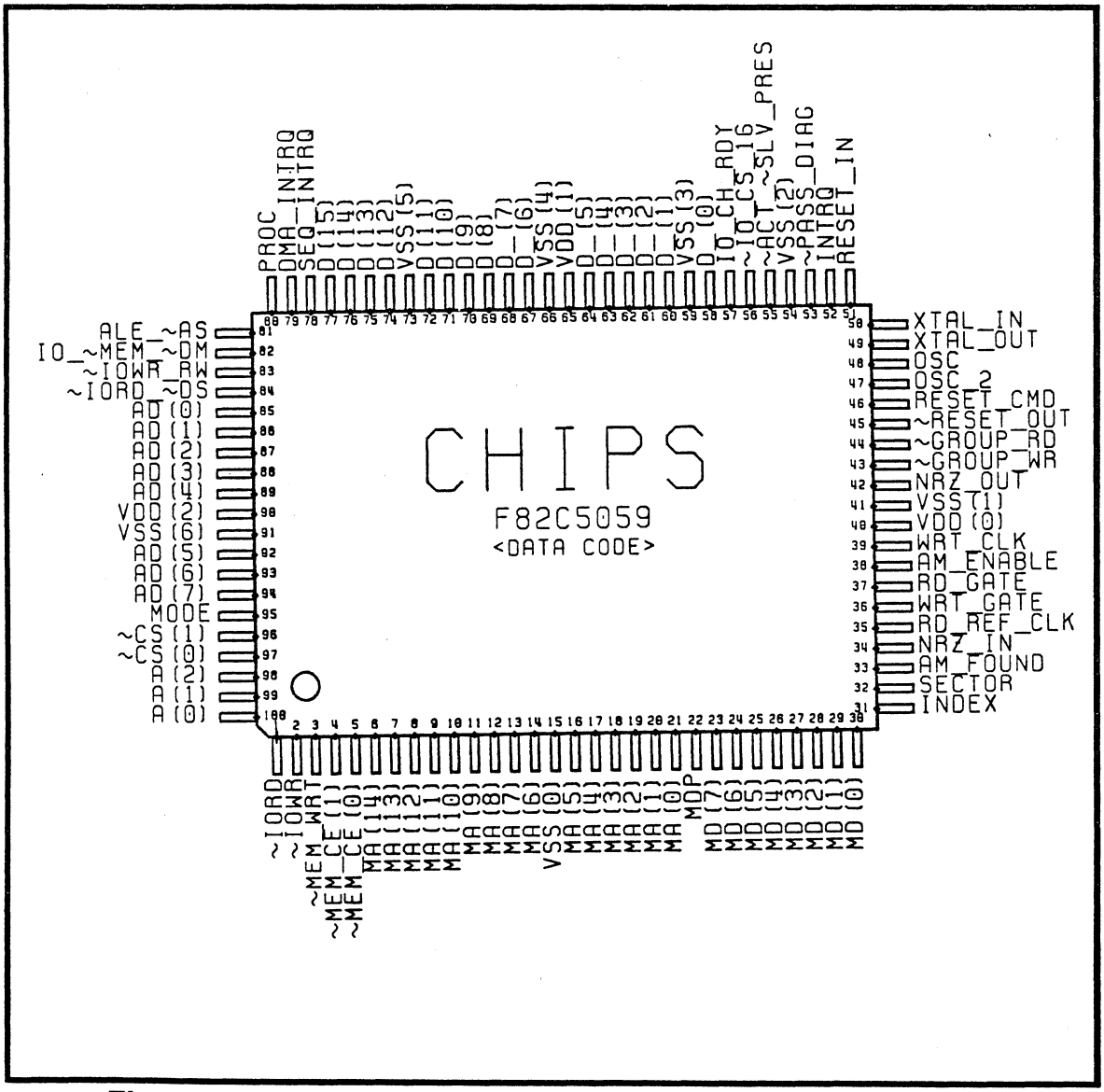


Figure 2-1. Physical Pin out of the 100-pin QFP Package

Table 2-1. A Pin List of the 100-pin QFP Package

Pin Number	Pin Name	I/O	Pin Number	Pin Name	I/O
1	-IORD	I	51	RESET_IN	I
2	-IOWR	I	52	INTRQ	O
3	-MEM_WRT	O	53	-PASS_DIAG	I/O
4	-MEM_CE(1)	O	54	VSS	
5	-MEM_CE(0)	O	55	-ACT_-SLV_PRES	I/O
6	MEM_A(14)	O	56	-IO_CS_16	O
7	MEM_A(13)	O	57	IO_CH_RDY	O
8	MEM_A(12)	O	58	D_(0)	I/O
9	MEM_A(11)	O	59	VSS	
10	MEM_A(10)	O	60	D_(1)	I/O
11	MEM_A(9)	O	61	D_(2)	I/O
12	MEM_A(8)	O	62	D_(3)	I/O
13	MEM_A(7)	O	63	D_(4)	I/O
14	MEM_A(6)	O	64	D_(5)	I/O
15	VSS		65	VDD	
16	MEM_A(5)	O	66	VSS	
17	MEM_A(4)	O	67	D_(6)	I/O
18	MEM_A(3)	O	68	D_(7)	I/O
19	MEM_A(2)	O	69	D_(8)	I/O
20	MEM_A(1)	O	70	D_(9)	I/O
21	MEM_A(0)	O	71	D_(10)	I/O
22	MEM_DP	I/O	72	D_(11)	I/O
23	MEM_D(7)	I/O	73	VSS	
24	MEM_D(6)	I/O	74	D_(12)	I/O
25	MEM_D(5)	I/O	75	D_(13)	I/O
26	MEM_D(4)	I/O	76	D_(14)	I/O
27	MEM_D(3)	I/O	77	D_(15)	I/O
28	MEM_D(2)	I/O	78	INT_SEQ	O
29	MEM_D(1)	I/O	79	INT_DMA	O
30	MEM_D(0)	I/O	80	CNFG	I
31	INDEX	I	81	ALE/-AS	I
32	SECTOR_AMF	I	82	IO_MEM/_DM	I
33	AM_FOUND	I	83	-IOWR/R-W	I
34	NRZ_IN	I	84	-IORD/-DS	I
35	RD_REF_CLK	I	85	A/D_(0)	I/O
36	WRT_GATE	O	86	A/D_(1)	I/O
37	RD_GATE	O	87	A/D_(2)	I/O
38	AM_ENABLE	O	88	A/D_(3)	I/O
39	WRT_CLK	O	89	A/D_(4)	I/O
40	VDD		90	VDD	
41	VSS		91	VSS	
42	NRZ_OUT	O	92	A/D_(5)	I/O
43	-GRP_WRT	O	93	A/D_(6)	I/O
44	-GRP_RD	O	94	A/D_(7)	I/O
45	-RESET_OUT	O	95	MODE	I
46	RESET_CMD	O	96	-CS(1)	I
47	OSC_2	O	97	-CS(0)	I
48	OSC	O	98	A(2)	I
49	XTALOT	O	99	A(1)	I
50	XTALIN	I	100	A(0)	I

100-pin QFP Package Specifications

Figure 2-2 provides a diagram of the package specifications for the 100-pin QFP package.

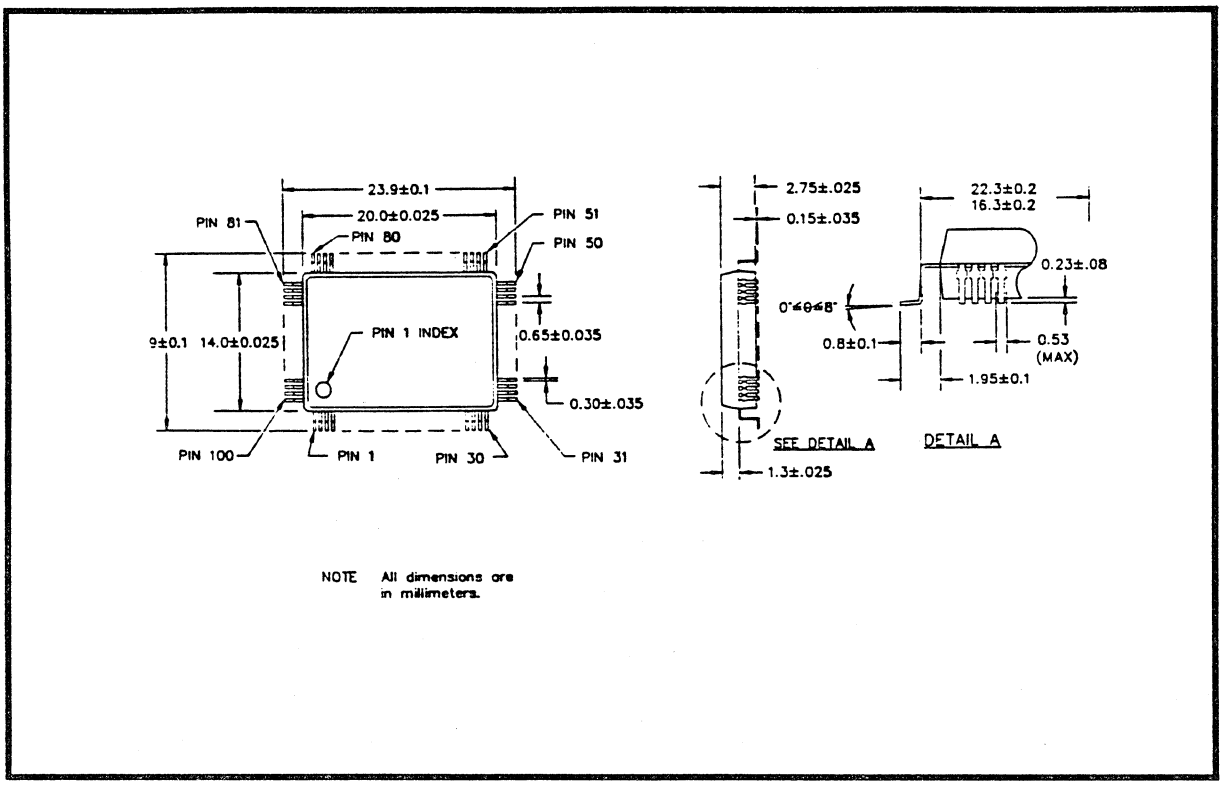


Figure 2-2. Diagram of the 100-pin QFP Package Specification

A TYPICAL SYSTEM

Figure 2-3 shows a typical system configuration using the CHIPS 82C5059 PC-AT Single Chip Controller Solution with a RAM buffer, a data separator, and a microcomputer with an associated ROM.

See Appendix D for schematics of a typical system configuration using the CHIPS 82C5059 with a static RAM buffer configuration.

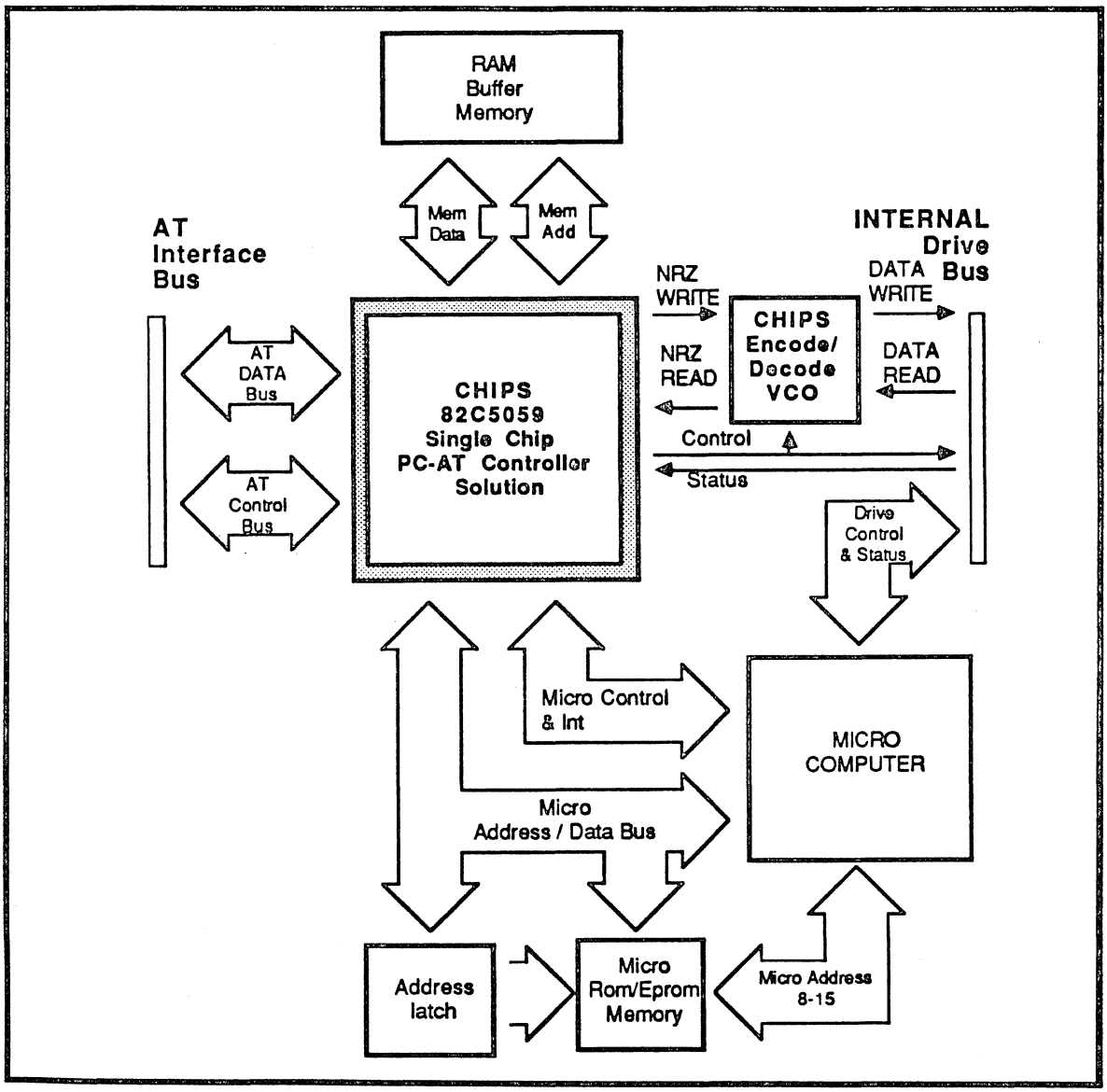


Figure 2-3. A Typical System Configuration Using the CHIPS 82C5059

SIGNAL DESCRIPTIONS

Table 2-2 is a list of the signals in alphabetical order. Note that in all the tables an active low state is indicated by a negative sign (-) prefix. When the pin(s) can be configured for more that one function, such as ALE_-AS, the other functions are listed as a subset.

Input/Output Signals

Table 2-2 lists the 82C5059 input/output signals and their functions.

Table 2-2 Input/Output Signals

Signal Symbol	Signal Name	I/O	Pin Number	Function
A_(2:0)	Address Bus (Host) (Active High)	I	100-98	These input signals constitute the 3 bit Host Address Bus that are internally decoded by the 82C5059 for selection of internal registers.
-ACT_-SLV_PRES	Active Slave_Present (Active Low) (Open Drain)	I/O	55	This input/output signal is asserted to indicate this device has received a command from the host. If the 82C5059 is configured as a Master, this signal will be configured as an input used to determine if a Slave is present during Power-on Reset and diagnostic commands. In the Slave Mode, this signal is always in an output mode.
AD(0-7)	Address/Data (Active High) (Tri state)	I/O	85-89 92-94	This is the multiplexed 8-bit address/data bus from the microprocessor. In 8051 mode (CONFIG grounded), addresses are latched into the Address Register on the falling edge of ALE in Z8 mode (CONFIG left open), addresses are latched on the rising edge of -AS. See the signal ALE/-AS below.) If the address is within the range of the internal chip select (AD7 =0), data is either written to or read from the Memory Controller/Data Sequencer Registers, depending on: in 8051 mode, whether -IOWR or -IORD is active; in Z8 mode, assuming -DS is low, whether R/-W is low or high.
ALE_-AS ALE	Address Latch Enable (8051 mode) (Active High)	I	81	In 8051 mode, the falling edge of ALE is used to latch the address portion of AD(0-7) on the microprocessor bus into the (Active High) internal address buffer.
-AS	Address Strobe (Z8 mode) (Active Low)			In Z8 mode, the rising edge of -AS is used to latch the address.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
AM ENABLE	Address Mark Enable (Active High)	O	38	If ESDI mode is selected, this output is active at state 1 strobe time. This function is used for writing an Address Mark to the disk if the ESDI device is configured in soft sectored mode. If ESDI mode is not selected, AM_ENABLE is active for state strobe 3 and 9, and may be used to enable external encoding of a "illegal pattern" Sync Byte.
AM FOUND	Address Mark	I	33	This signal is used by the sequencer during a read operation for byte synchronization. It is an output from the VCO/Encode/Decode device, and is used for MFM or 2,7 RLL byte synchronization. If internal synchronization is configured, this input should be grounded.
-CS(1:0) along	Chip Select (Host) (Active Low)	I	96-97	These input signals are used by the 82C5059 with the A_(2:0) signals to select each of the internal registers within the 82C5059. If the MODE in input is left open , the -CS(0) input is used to select the register group of 1FX while the -CS(1) input is used to select the 3FX group. It the MODE input is grounded, the -CS(0) input is used as a global select and the -CS(1) input is used for host address A_(9).
CONFIG	Configuration (Active High)	I	80	This internally pulled up input signal is used to select the microprocessor bus type configuration option for the 82C5059. When CONFIG is grounded, the device is configured for an 8051 type processor. When CONFIG is left open, the device is configured for Z8 type processor.
D_(7:0)	Data Bus (Host) (Active High)	I/O	58,60-64 67-68	These bi-directional, tri-state signals are used to transfer data between the host and the 82C5059 internal registers. During word data transfers, this bus is the least significant byte of the data word.
D_(15:8) Register.	Data Bus (Host) (Active High)	I/O	69-72 74-77	These bi-directional, tri-state signals are used to transfer the most significant byte of the host data to or from the 82C5059 Data
-GRPRD	Group Read Strobe (Active Low)	O	44	This signal is strobed whenever the microprocessor reads any of the following registers: RR12 through RR15. It may be used to enable status onto the microprocessor bus (AD0-7). It may also be used as an external peripheral chip select for devices such as the Intel 8255 PIO or 8273 FDC.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
-GRPWRT	Group Write (Active Low)	O	43	This signal is strobed whenever the microprocessor accesses any of the following registers: WR12 through WR15 and RR11. It may be used to latch data from the microprocessor data bus (AD0-7) into an external register. It may also be used as an external peripheral chip select as noted under -GRPRD above.
INDEX	Index (Programmable)	I	31	This is a Schmidt trigger input signal from the disk that is received once per revolution. The data sequencer uses the rising edge of the INDEX pulse for synchronization during formatting, and for timing-out commands.
INT MEM	Interrupt, Memory Controller (Programmable)	O	79	Assuming that interrupts are enabled for a channel (Bit 3=1 of WR08 for Channel 0 or W9 for Channel 1) and that Transfer Count=0 disables the channel, (Bit 4=0 of WR08 or WR09) then the signal INT MEM is asserted when Channel Enable (Bit 0, same register) goes to 0 for that channel (i.e. on the deasserting edge of the Channel Enable signal). INT MEM is deasserted when the microprocessor writes to the Channel Control Register (WR08 or WR09) of the channel that caused the interrupt. The polarity of INT MEM is controlled by Bit 2 of the Memory Cycle Timing Register (WR10).
INT SEQ	Interrupt, Sequencer (Programmable)	O	78	If sequencer interrupts are enabled (Bit 7 of WR29 is set), this output is asserted when the sequencer has completed a command or for any function that causes Busy to transition from Busy to not-Busy. It is deasserted when the microprocessor reads the Sequencer Status Register (RR16).
IO_CH_RDY	I/O Channel Ready (Active High)	O	57	This open drain, 24 mA. output signal is deasserted to lengthen an I/O data cycle. This signal is only active during WORD mode data transfers at I/O Address 1F0(170) if data is not available.
-IO_CS_16	I/O Select 16 (Active Low)	O	56	This open drain, 24 mA. output signal is asserted to indicate that the present host data transfer is a 16-bit, 1 wait-state I/O cycle. It is derived from the 82C5059 Data Register 1F0(170) decode.
IO_-MEM_-DM				
IO/-MEM	I/O/-Memory (8051 mode) (I/O Active High)	I	82	In 8051 mode, this line is connected to an 8051 address line to differentiate between an I/O cycle and a memory cycle.
-DM	-Data Memory (Z8 mode) (Active Low)			In Z8 mode, it is an active low chip enable and connected to the Z8 -DM line.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
-IORD_-DS				
-IORD	I/O Read (8051 mode) (Active Low)	I	84	In 8051 mode, this input, when low, enables the information from the register selected by the previously latched address onto the microprocessor bus (AD0-7).
-DS	Data Strobe (Z8 mode) (Active Low)			In Z8 mode, this input provides the timing for data movement to or from selected registers and the microprocessor bus (AD0-7).
-IOWR_R/-W				
-IOWR	I/O Write (8051 mode) (Active Low)	I	83	In 8051 mode, this input, when low, enables the information from the microprocessor bus (AD0-7) into the register selected by the previously latched address.
R/-W	Read/Write (Z8 mode) (Read Active High) (Write Active Low)			In Z8 mode, assuming -DS is low, this input specifies the direction of the data transfer. When low with -DS low, data is written low from the microprocessor bus (AD0-7) to the sequencer. When high with -DS high, data is read from the selected register to the microprocessor.
-IORD	I/O Read (Host) (Active Low)	I	1	This input signal asserted by the host to read data from an I/O address (A2:0) while -CS(0) or -CS(1) is asserted.
-IOWR	I/O Write (Host) (Active Low)	I	2	This input signal asserted by the host to write data to an I/O address (A2:0) while -CS(0) or -CS(1) is asserted.
INTRQ	Interrupt (Host) (Active High)	O	52	This tri-state output signal indicates the 82C5059 needs Host Attention. It is enabledor disabled by writing a 0 or 1 respectively to bit 1 of Host Write Register 3F6(376).It is asserted by writing a "1" to bit 6 of the Internal Control Register 4A and is de-asserted by the host reading or writing register1F7(177). If this device is programmed in the Master/Slave mode, this output is only activewhile selected.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
MEMA(0-14)	Memory Address (Active High)	O	21-16 14-6	The Memory Address bus is used to output the contents of the Memory Address Register of the selected channel to the external RAM buffer. The 82C5059 can address a 32K SRAM buffer. If the 82C5059 is configured for two chip selects, then MEMA0 is converted to MEMA15 (output pin), and MEMA0 is internally used to select between the twochip selects (2x32K SRAMs), -MEMCE0 and -MEMCE1. In SRAM mode this allows addressing up to 64K bytes. For various DRAM configurations (64K x 8, 128K x 8, 256K x 8, 512K x 8, and 1M x 8), refer to Appendix C.
-MEMCE0	Memory Chip Enable Zero (Active Low)	O	5	This output is an active low chip enable for the external RAM buffer memory addressed by MEMA0-14. When this output and -MEMWRT are asserted, data is written to the selected address in the RAM buffer memory. When this output is asserted and -MEMWRT is deasserted, data is read from the RAM buffer memory. When two chip selects are enabled, this output is asserted when MEMA0 is low or Channel 1 is in word mode, while a memory cycle is in process.
-MEMCE1	Memory Chip Enable One (Active Low)	O	4	This output is an active low chip enable for the external buffer memory addressed by MEMA0-14 when two chip selects are enabled. When this output and -MEMWRT are asserted, data is written to the selected address in the buffer memory. When this output is asserted and -MEMWRT is deasserted, data is read from the buffer memory. This output is asserted when MEMA0 is high or Channel 1 is in word mode, while memory cycle is in process.
MEMD(0-7)	Memory Data (Active High) (Tri-state)	I/O	31-23	This is an 8-bit bi-directional bus used to transfer data to and from the RAM buffer. The MEMD0-7 are driven when ACK0 is low, and data is transferred from the 82C5059 to the buffer memory.
MEMDP	Memory Data Parity Bit (Active High) (Tri-state)	I/O	22	This bit is the bi-directional odd parity for the memory data bus. Odd parity is always generated by this device to write in external buffer memory but is only checked if programmed for memory parity.
-MEMWRT	Memory Write (Active Low)	O	3	This output is an active low write enable for the external RAM buffer.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
MODE	Mode select (Active Low)	I	95	This internally pulled up input controls the configuration of the RESET_IN and -CS(1:0) inputs. If this input is open, the RESET_IN input is an active high reset and the -CS(0) input is a global chip select for this device while -CS(1) is used for A_(9) from the host. If this input is grounded, the RESET_IN input is an active low reset and both of the -CS(1:0) inputs are there respective group chip select.
NRZ IN	NRZ Data In (Non-Return to Zero) (Active High)	I	34	This serial data input line is the NRZ read data from the drive or data separator/PLL: CHIPS 5070 MFM Encode/Decode/VCO. CHIPS 5027 2,7RLL Encode/Decode/VCO. ESDI-type disk drive.
NRZ OUT	NRZ Data Out (Non-Return to Zero) (Active High)	O	42	When WRTGATE is active, this line outputs serial NRZ write data from the sequencer. All data are output to: CHIPS 5070 MFM Encode/Decode/VCO. CHIPS 5027 2,7R.LL Encode/Decode/VCO. ESDI-type disk drive.
OSC	Oscillator (Active High)	O	48	This is a TLL clock at the XTAL (crystal) frequency.
OSC_2	Oscillator/2 (Active High)	O	47	This is a TLL clock at one-half the XTAL (crystal) frequency.
-PASS_DIAG	Pass Diagnostic (Active Low)	I/O	53	This input/output signal is used in a multiple PC-AT drive system and allows the Slave to inform the Master if it has passed diagnostic.
RDGATE	Read Gate (Active High)	O	37	This signal is asserted during a sequencer read operation; it indicates that the drive or data separator should present read data on the NRZ IN line. When in external Sync mode (Bit 4 of WR29 is set), the data separator must provide AM FOUND.
RD_REF_CLK	Read/Reference (Active High)	I	35	This signal has two functions: When WRTGATE is true, this signal is used as a write (reference) clock to generate the write data at the NRZOUT pin. When RDGATE is true, a read clock, locked to the read data on the NRZIN line, must be supplied. **Note: A clock must always be present on this pin.**
RESET_CMD	Reset (Host) Command (Active Low)	O	46	This output signal is asserted to indicate that a command has been written into Write Register 1F7(177). It is de-asserted by writing the internal control Register WR48 bit 2 with a 1 or a Reset.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
RESET_IN	Reset In (Host) (Programmable)	I	51	This input signal is asserted by the host to indicate a power-on or a low voltage condition exists. If the MODE input is grounded, the polarity of this input signal is inverted to perform a reset function, this input must be asserted low.
-RESET_OUT	Reset Out (Active Low)	O	46	This output signal is an inverted copy (unless in Chip Select mode) of the RESET_IN signal or is asserted for 1 microsecond when this device detects a power-on reset.
SECTOR/AMF	Sector/Address Mark Found (Programmable)	I	32	This Schmidt trigger input can be used for either the Sector line from a hard-disk drive or the Address Mark Found line from a soft-sectored ESDI drive
WRTCLK	Write Clock (Active High)	O	39	This output is a clock at the RD_REF_CLK frequency. The high to low edge of this clock is used to clock the NRZOUT write data signal.
WRTGATE	Write Gate (Active High)	O	36	This signal is asserted during a sequencer write operation; it indicates that data on the NRZOUT line should be written on the disk.
XTALIN, XTALOT	Crystal 0-1 (Active High)	I O	50,49	The XTAL lines may be connected to an external crystal oscillator, or if an external clock source is available, a clock input may be connected to the XTALIN input with XTALOT left open. In either case OSC,and OSC_2, are derived from the XTALIN frequency. Note that if an external crystal source is used, it must be a fundamental parallel resonant type in the range of 1 MHz to 24MHz, or a third overtone to 40 MHz. Also, an external resistor must be connected across the crystal with a capacitor to ground from both sides. **Note: See Appendix E, the applications section for critical circuit description, layout and crystal selection.**
VDD	Vdd +5		40,65,90	
VSS	Vss Ground		15,41,54,59 66,73,91	

ELECTRICAL SPECIFICATIONS

The CHIPS 82C5059 is manufactured using a proven low-power CMOS technology process. It operates from a single +5 volt supply. Refer to the following sections and tables for information on absolute ratings, standard test conditions, D.C. characteristics, A.C. parameters and timings.

D.C. SPECIFICATIONS

1. Absolute Maximum Ratings:

The absolute maximum ratings are as follows:

- A power supply voltage of -0.3 to 7.0 VDC.
- An ambient operating temperature of 0 to 70.0 degrees C.
- A storage temperature of -65.0 to +150.0 degrees C.

Caution: Stresses greater than those indicated may cause permanent damage to the device. Operation of the device at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

2. Standard Test Conditions:

The characteristics listed below are the test conditions, unless otherwise noted, for the "D.C. Characteristics" that follow. Note that voltages are referenced to GND and that positive current flows into the reference pin. The standard conditions are as follows:

- Vdd = 5.0 VDC $\pm$ 0.25 VDC
- GND = 0 VDC
- 0 degrees C< TA< 70 degrees C

3. D.C. Characteristics:

Table 2-3. D.C. Characteristics

PARAMETER	CONDITION	MIN	MAX	UNITS	NOTES
Voh-Output High Voltage	Vdd = min	2.4		Volts	Ioh=Iohmax*
Vol-Output Low Voltage	Vdd = min	0.4		Volts	Iol=Iolmax*
Vol-Output Low Voltage	Vdd = min	0.5		Volts	Iol=Iolmax* 48 ma. Driver
Vih-Input High Voltage		2.2		Volts	
Vil-Input Low Voltage			0.8	Volts	
Ii Input Current	Vdd = max		±10.0	uA	
Oiz			±10.0	uA	
Icc-Read Cycle 20 MHz, 40 MHz Clock	Vdd = max		100	mA	Ta = 70 deg. C

Note: See Table 2-4 for Signal Drive Strengths.

4. Output Driver Characteristics

Output signals have one of several types of drive strengths:
Type 2: Iolmax = 2.0 mA, Iohmax = -2.0 mA
Type 4: Iolmax = 4.0 mA, Iohmax = -4.0 mA
Type 8: Iolmax = 8.0 mA, Iohmax = -8.0 mA
Type 16: Iolmax = 16.0 mA, Iohmax = -16.0 mA
Type 24: Iolmax = 24.0 mA, Iohmax = -24.0 mA
Type 48: Iolmax = 48.0 mA

Table 2-4 below indicates the drive strength for each output driver signal.

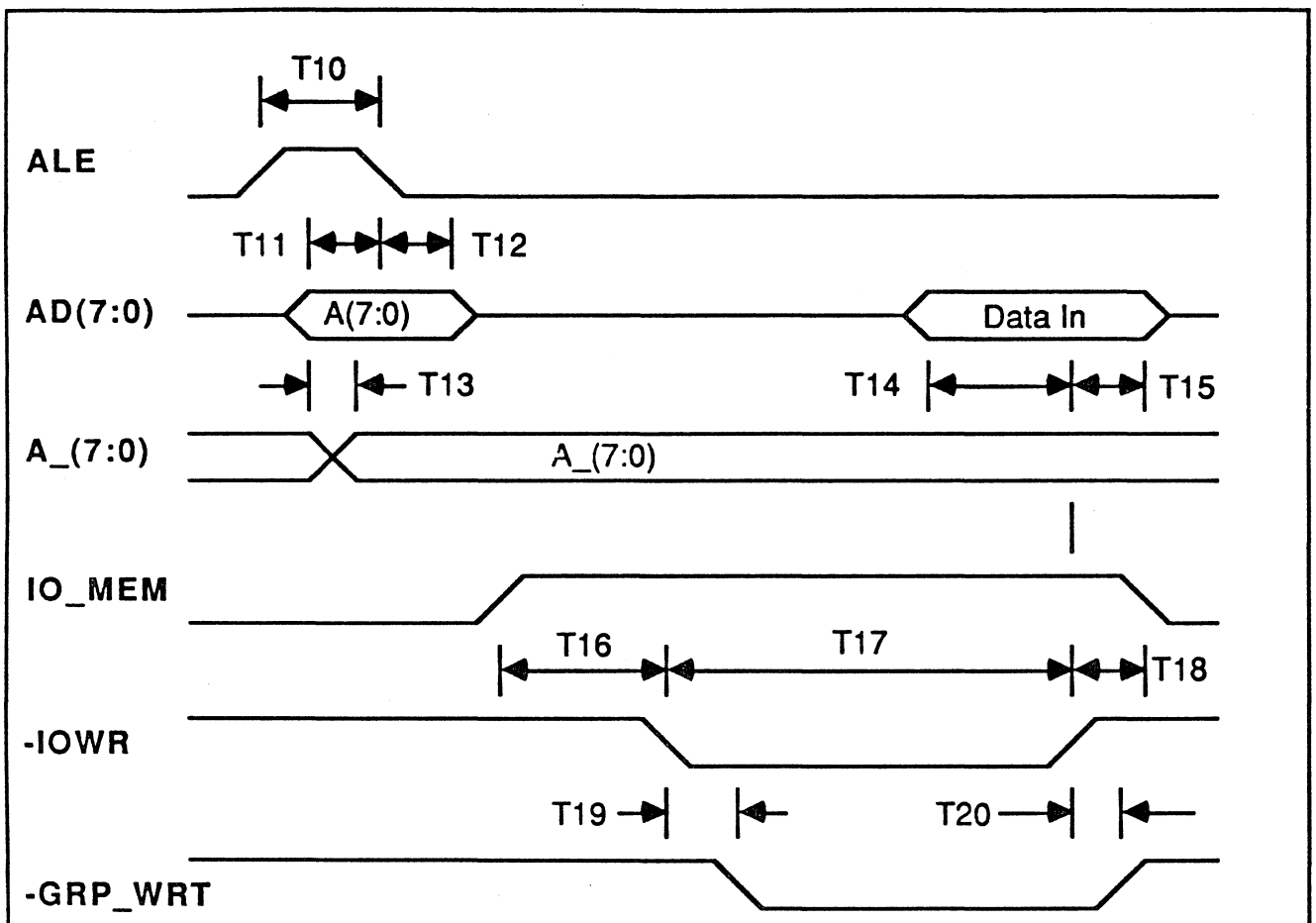
Table 2-4. Output Driver Signal Strength

Signal	Driver Type
-ACT_-SLV_PRES	24 MA
A/D(7:0)	2 MA
AM_ENABLE	2 MA
D_(15:0)	16 MA
-GRP_RD	2 MA
-GRP_WT	2 MA
INTRQ	8 MA
INT_MEM	2 MA
INT_SEQ	2 MA
-IO_CS_16	24 MA
IO_CH_RDY	24 MA
MEMA_(0-14)	2 MA
-MEMCE_(0-1)	2 MA
-MEMD0-7&P	2 MA
-MEMWRT	2 MA
NRZ_OUT	2 MA
OSC	2 MA
OSC_2	8 MA
-PASS_DIAG	24 MA
-RESET_OUT	2 MA
RESET_CMD	2 MA
RD_GATE	2 MA
WRT_CLK	2 MA
WRT_GATE	2 MA

5. A.C. SPECIFICATIONS

The relevant timing diagrams and A.C. characteristics for interfacing the CHIPS 82C5059 are provided in the following timing specification sections. These specifications are valid over the standard test conditions. All output timing assumes a capacitive load of 30 pf.

Microprocessor WRITE Internal Register Operation (Configuration=0, 8051 mode)

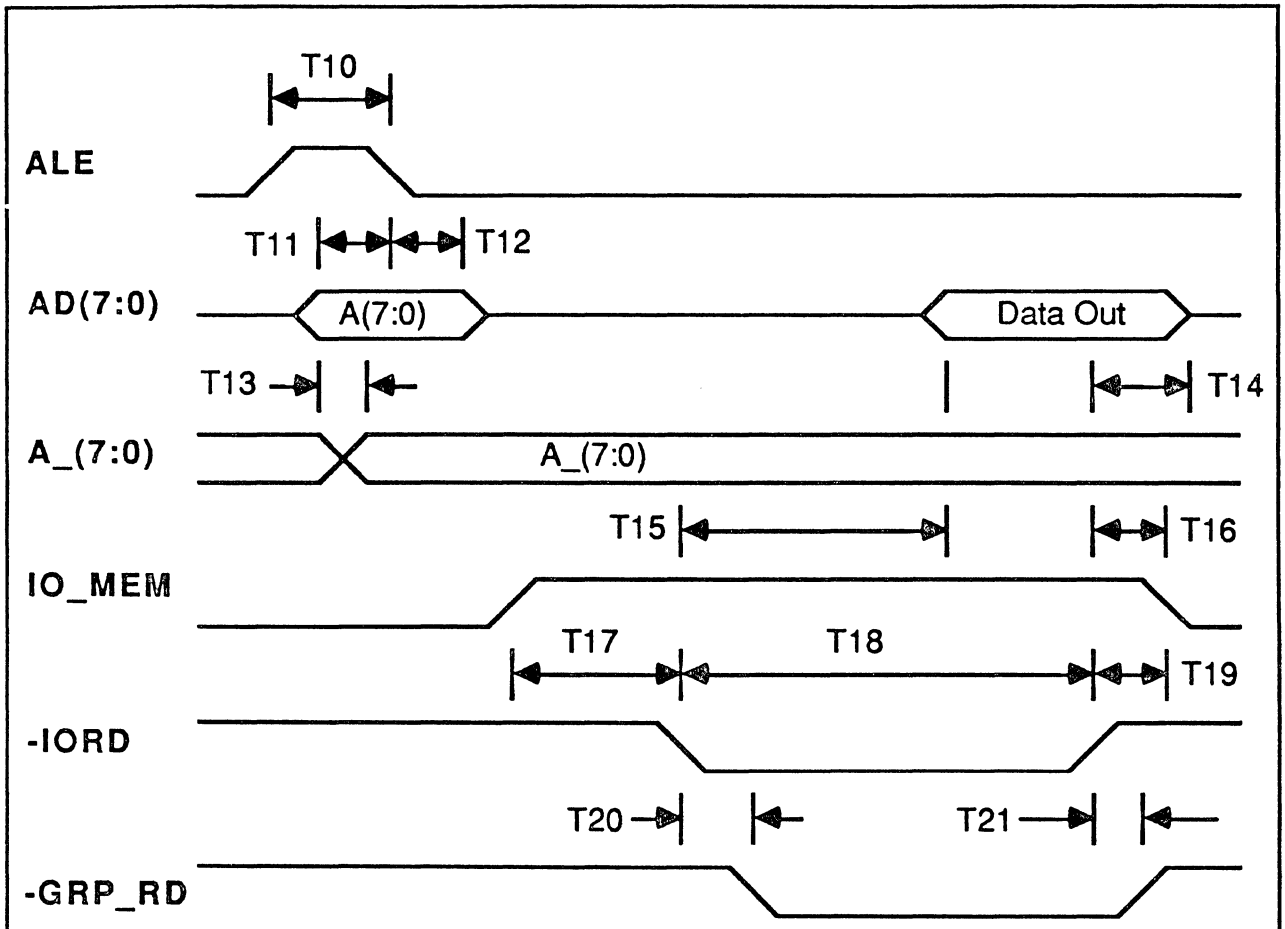


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	ALE pulse width	25		ns
T11	Address setup to ALE low	10		ns
T12	Address hold to ALE low	10		ns
T14	Data setup to -IOWR high	15		ns
T15	Data hold to -IOWR high	15		ns
T16	IO_MEM setup to -IOWR low	15		ns
T17	-IOWR pulse width	50		ns
T18	-IO_MEM hold to -IOWR high	15		ns
T19	-GRPWRT low delay from -IOWR low		25	ns
T20	-GRPWRT high delay from -IOWR high		25	ns

Note: 1. -GRPWRT is only asserted for address range 0Ch to 0Fh.

Figure 2-4. Microprocessor WRITE Internal Register Operation

Microprocessor READ Internal Register Operation (Configuration=0, 8051 mode)

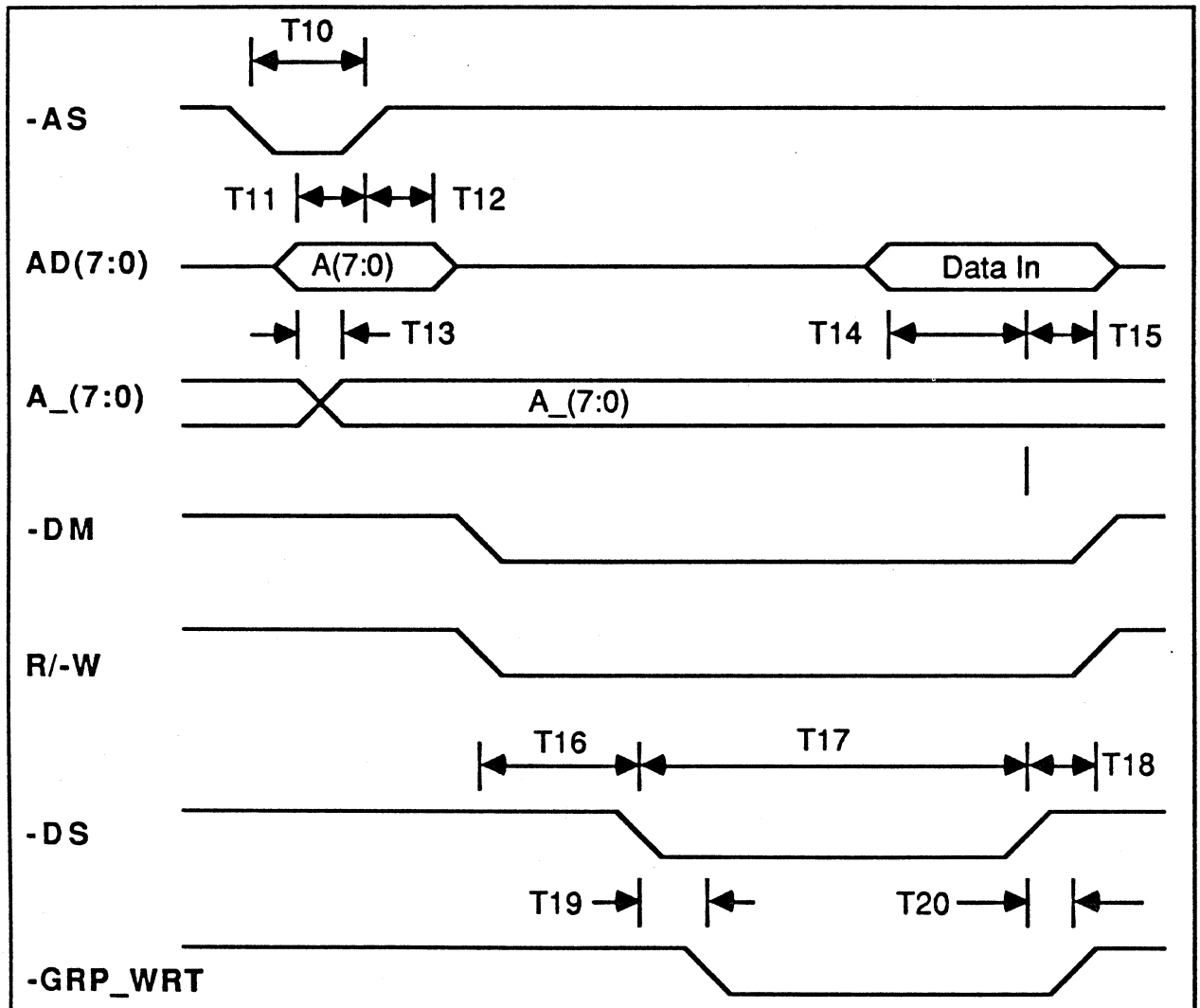


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	ALE pulse width	25		ns
T11	Address setup to ALE low	10		ns
T12	Address hold to ALE low	10		ns
T14	-IORD high to data hi-z		25	ns
T15	-IORD low to data valid		40	ns
T16	-IORD high to data invalid	0		ns
T17	IO_MEM setup to -IORD low	15		ns
T18	-IORD pulse width	50		ns
T19	IO_MEM hold to -IORD high	15		ns
T20	-GRPRD low delay from -IORD low		25	ns
T21	-GRPRD high delay from -IORD high		25	ns

Note: 1. -GRPRD is only asserted for address range 0Ch to 0Fh.

Figure 2-5. Microprocessor READ Internal Register Operation

Microprocessor WRITE Internal Register Operation (Configuration=1, Z8 mode)

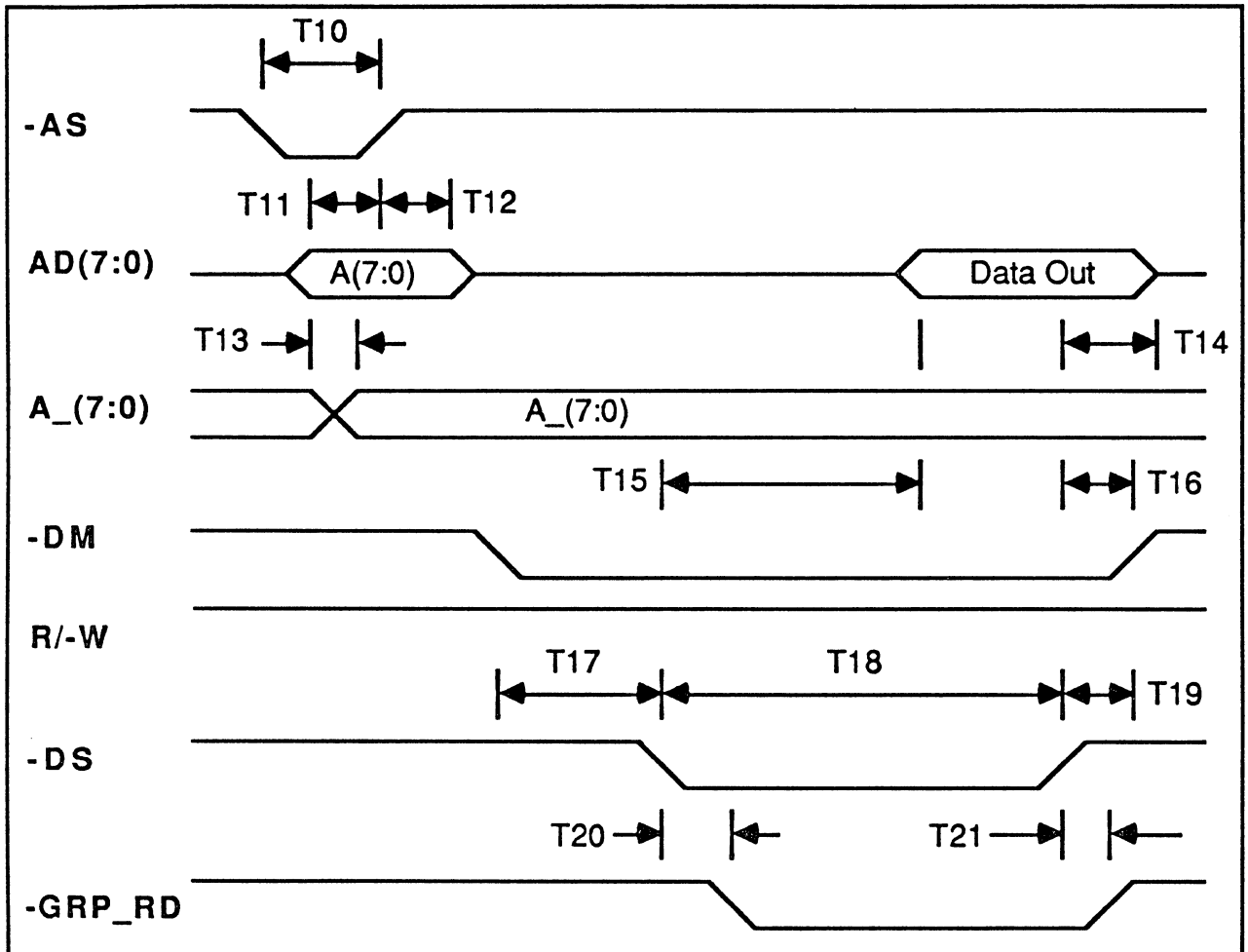


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-AS pulse width	25		ns
T11	Address setup to -AS high	10		ns
T12	Address hold to -AS high	10		ns
T14	Data setup to -DS high	15		ns
T15	Data hold to -DS high	15		ns
T16	-DM & R/-W setup to -DS low	15		ns
T17	-DS pulse width	50		ns
T18	-DM & R/-W hold to -DS high	15		ns
T19	-GRPWRT low delay from-DS low		25	ns
T20	-GRPWRT high delay from -DS high		25	ns

Note: 1. -GRPWRT is only asserted for address range 0Ch to 0Fh.

Figure 2-6. Microprocessor WRITE Internal Register Operation

Microprocessor READ Internal Register Operation (Configuration=1, Z8 mode)

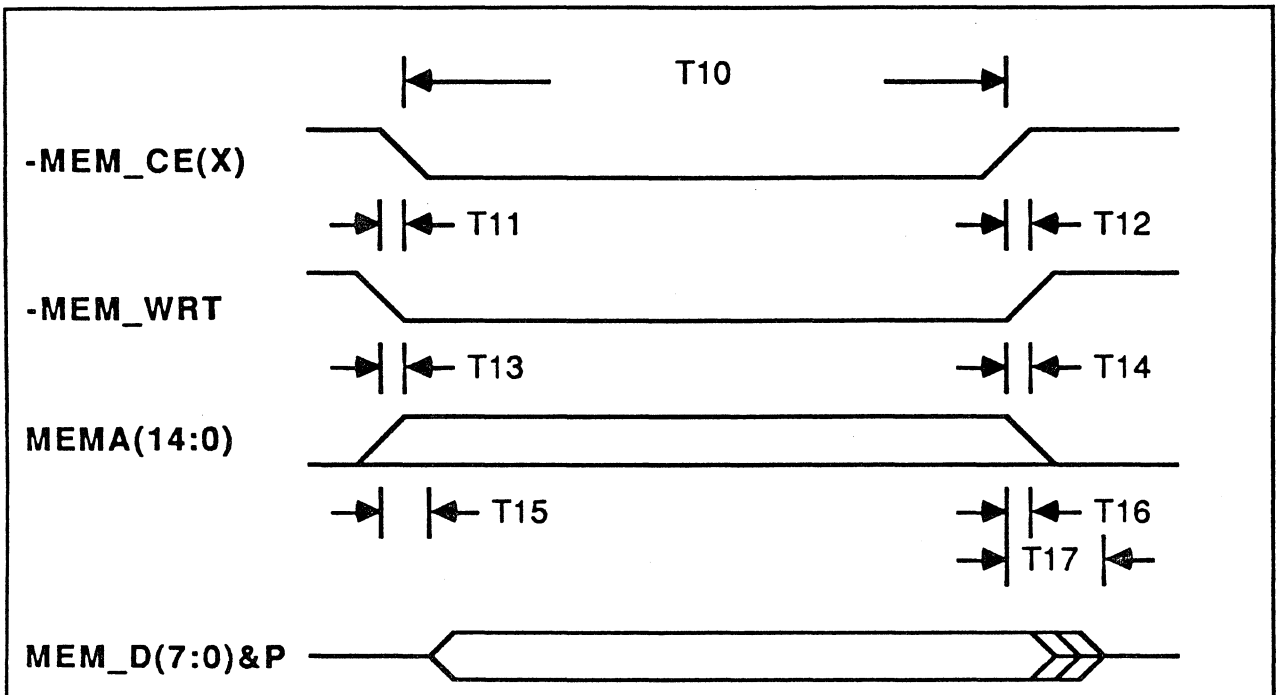


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-AS pulse width	25		ns
T11	Address setup to -AS high	10		ns
T12	Address hold to -AS high	10		ns
T14	-DS high to data hi-z		25	ns
T15	-DS low to data valid		40	ns
T16	-DS high to data invalid	0		ns
T17	-DM & R-/W setup to -DS low	15		ns
T18	-DS pulse width	50		ns
T19	-DM & R/-W hold to -DS high	15		ns
T20	-GRPRD low delay from -DS low		25	ns
T21	-GRPRD high delay from -DS high		25	ns

Notes: 1. -GRPRD is only asserted for address range 0Ch to 0Fh.

Figure 2-7 Microprocessor READ Internal Register Operation

DMA Buffer WRITE Operation (Static Ram)

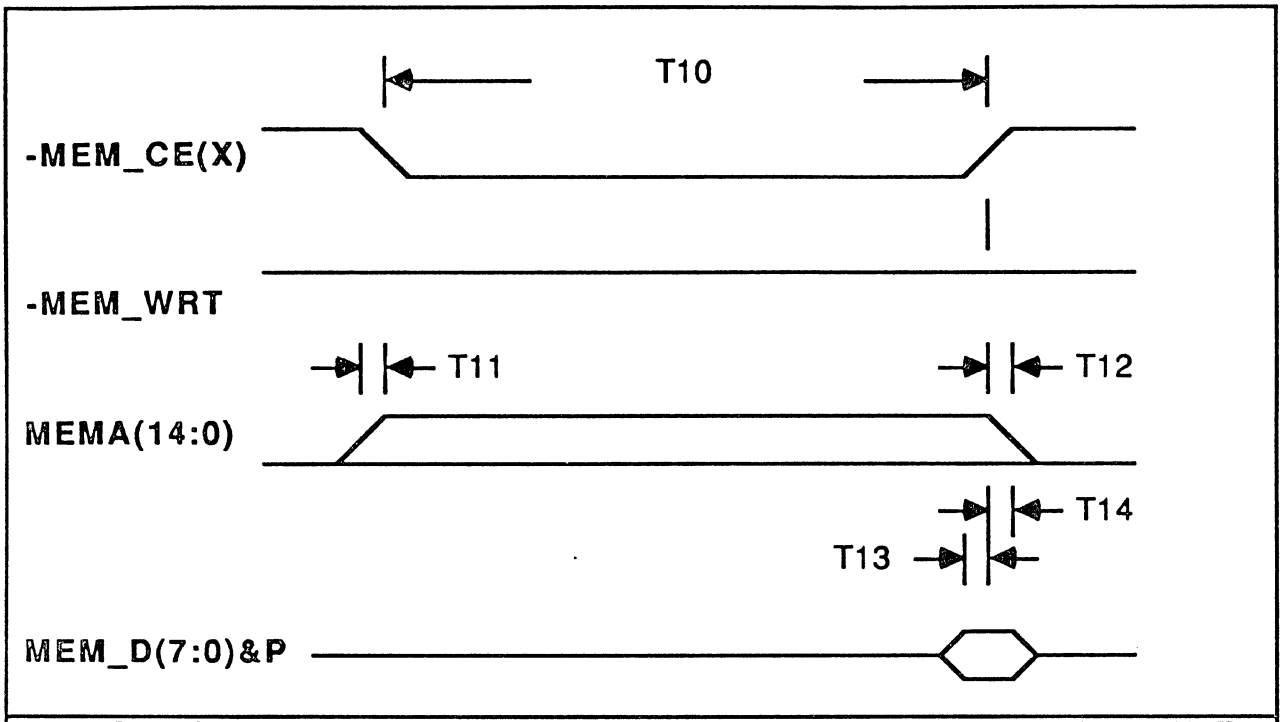


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-MEM_CE (0-1) low pulse width	n CP - 5		ns
T11	-MEM_WRT setup from -MEM_CE (0-1) low	2		ns
T12	-MEM_WRT hold from -MEM_CE (0-1) high	5		ns
T13	MEMA (0-14) setup from -MEM_CE (0-1) low	2		ns
T14	MEMA (0-14) hold from -MEM_CE (0-1) high	5		ns
T15	MEM_D (0:7) & P valid from -MEM_CE (0-1) low		0	ns
T16	MEM_D (0:7) & P invalid from -MEM_CE (0-1) high	5		ns
T17	MEM_D (0:7) & P tri-state from -MEM_CE (0-1) high		15	ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. MEM_D (0-7) and MEM_D-P driven by the 82C5059.

Figure 2-8. DMA Buffer WRITE Operation

DMA Buffer READ Operation (Static RAM)

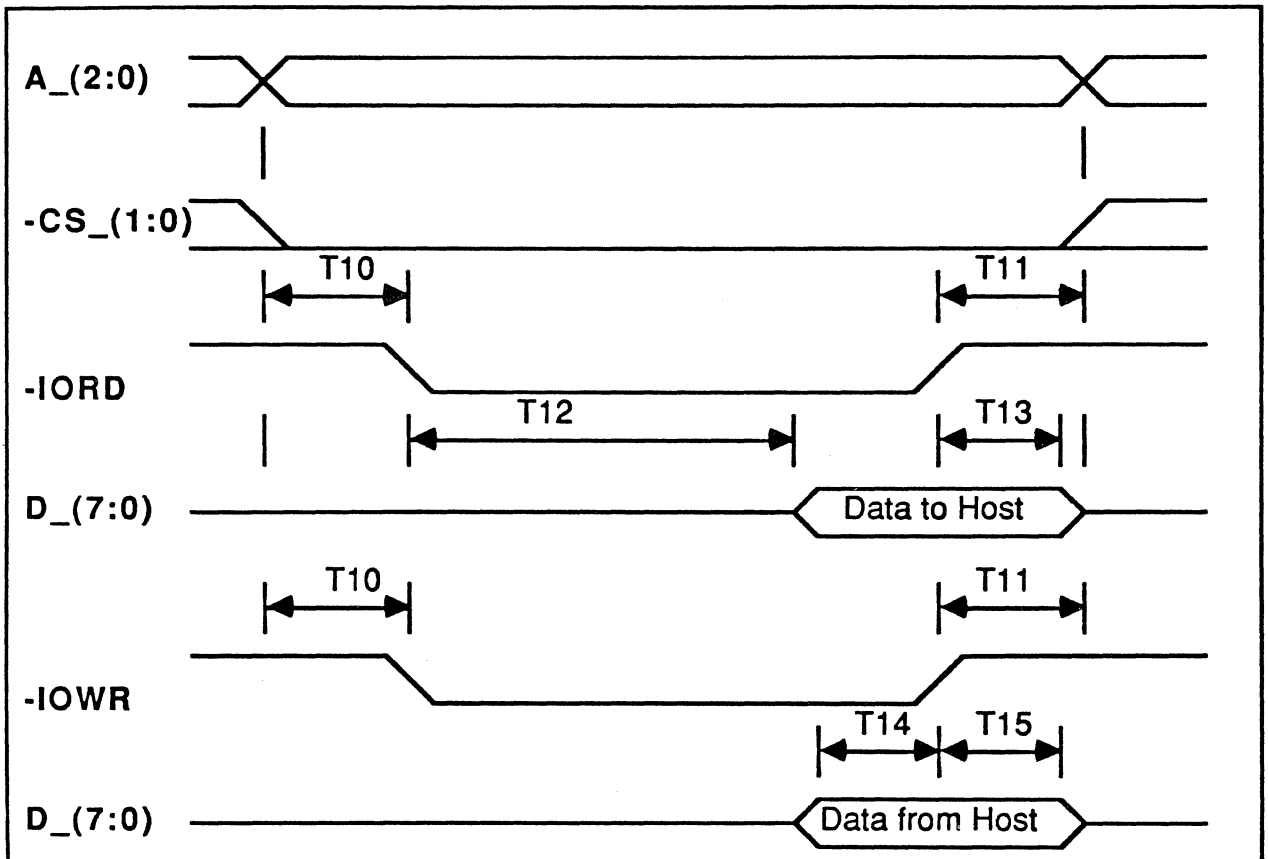


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-MEM_CE (0-1) low pulse width	n CP - 5		ns
T11	MEMA (0-14) setup from -MEM_CE (0-1) low	2		ns
T12	MEMA (0-14) hold from -MEM_CE (0-1) high	5		ns
T13	MEM_D (0:7) & P setup from -MEM_CE (0-1) high		5	ns
T14	MEM_D (0:7) & P hold from -MEM_CE (0-1) high	0		ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. MEM_D (0:7) driven by MEMORY device.
4. MEM_D-P driven by MEMORY device if PARITY ENABLED.

Figure 2-9. DMA Buffer READ Operation

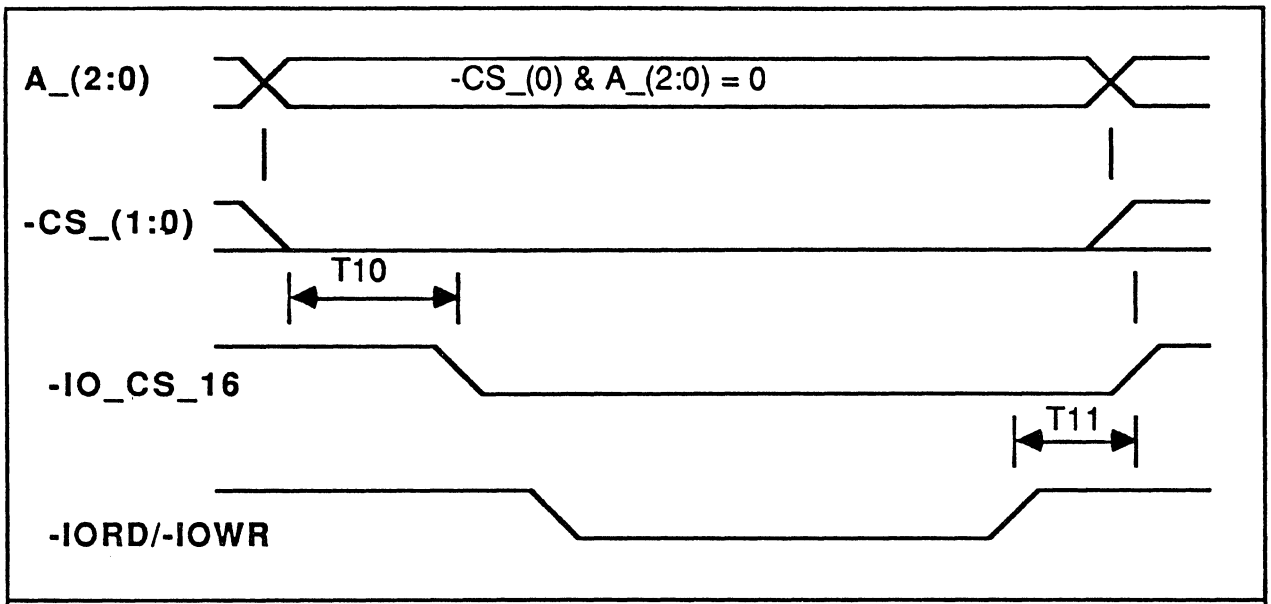
Host Interface Read/Write Internal Register Operation



SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	Address/-CS setup to -IORD/-IOWR low	30		ns
T11	Address/-CS hold to -IORD/-IOWR high	0		ns
T12	-IORD low D(7:0) valid		35	ns
T13	-IORD high D(7:0) invalid		25	ns
T14	D_(7:0) setup to -IOWR low	10		ns
T15	D_(7:0) Hold after -IOWR high	20		ns

Figure 2-10. Host Interface Read/Write Register Operation

Host Interface IO_CS_16 Timing

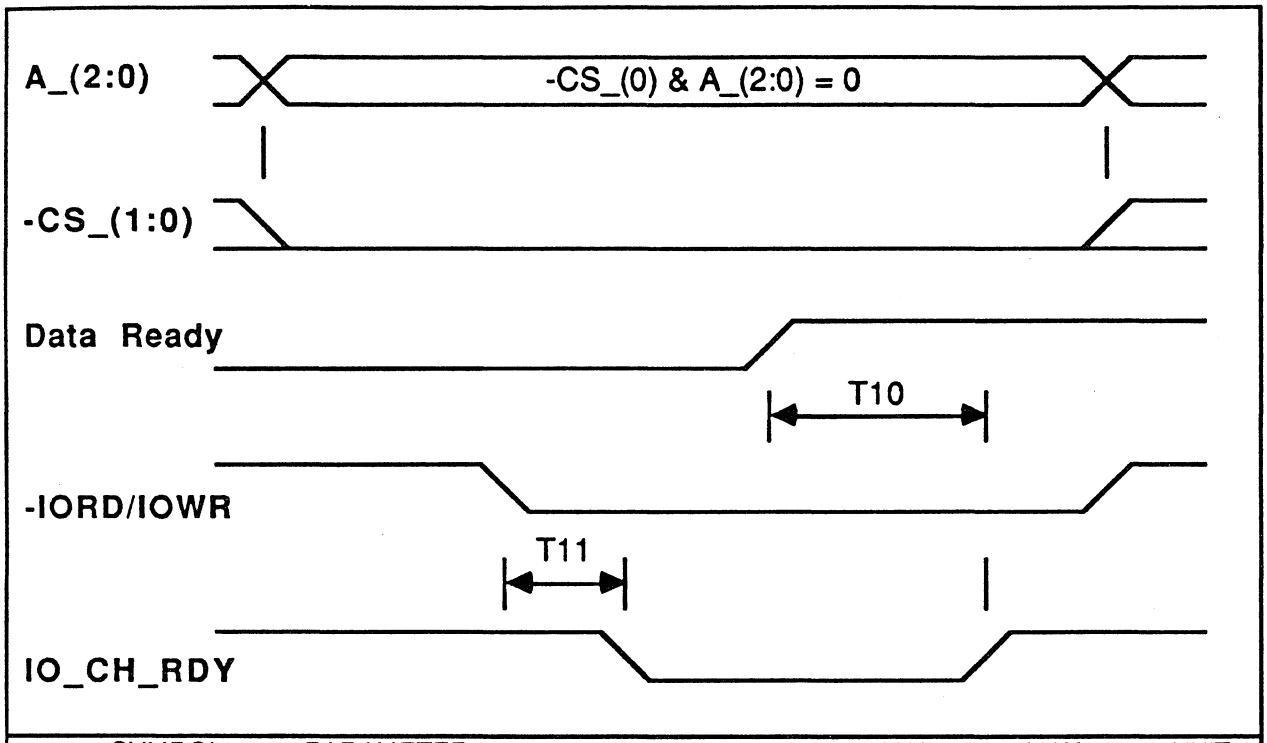


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-IO_CS_16 asserted from A(9:0)/AEN/ALE valid		35	ns
T11	-IO_CS_16 de-asserted from -IORD/-IOWR low to high		55	ns

Notes:
1. -IO_CS_16 only asserted for WR or RR & -CS_(0) & A_(2:0) = 0.
2. -IO_CS_16 rise time is a function of an external pull-up resister.

Figure 2-11. Host Interface IO_CS_16 Timing

Host Interface IO_CH_RDY Timing

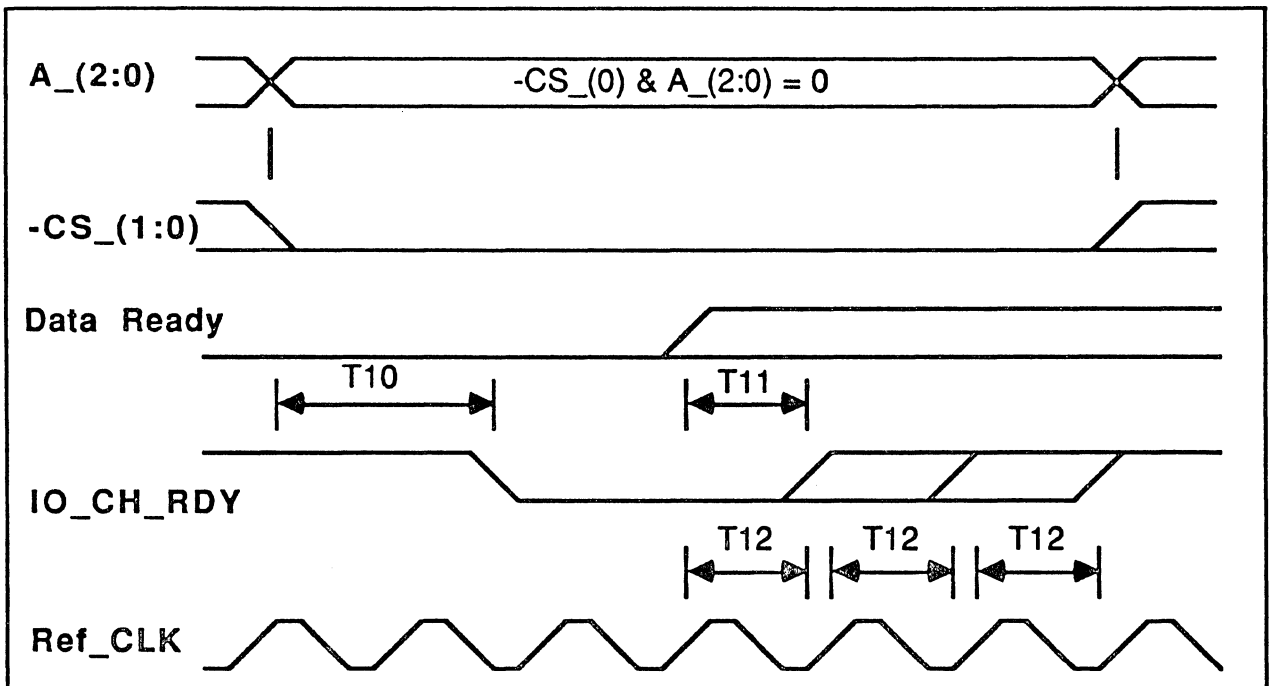


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	IO_CH_RDY high from Data Ready high		30	ns
T11	IO_CH_RDY low from -IORD/-IOWR low		25	ns

Notes: 1. IO_CH_RDY rise time is a function of an external pull-up resister.

Figure 2-12. Host Interface IO_CH_RDY Timing

Host Interface IO_CH_RDY Reference Clock Timing



SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	IO_CH_RDY low from A(2:0)/-CS/Data not Ready		45	ns
T11	IO_CH_RDY high from Data Ready high		30	ns
T12	IO_CH_RDY high from SYS_CLK high		40	ns

Notes:
1. IO_CH_RDY (T11) from A(2:0) & -CS_(0) valid whichever is last
2. Data Ready always assert IO_CH_RDY (high).
3. Ref_CLK's for IO_CH_RDY low programmable from 1 to 7 cycles.
4. IO_CH_RDY rise time is a function of an external pull-up resister.

Figure 2-13. Host Interface IO_CH_RDY Reference Clock Timing

82C5059 Registers 3

The CHIPS 82C5059 is designed to offer the system designer greater flexibility by offering a broad range of choices in such matters as operational control, error recovery, timing parameters, physical media organization and format as well as the mode of communication with the PC-AT or compatible interface. For this purpose, the 82C5059 presents the microprocessor with an easily accessed and programmable interface consisting of a collection of individually addressable byte-wide registers in four groups.

THE FOUR MICROCOMPUTER REGISTER GROUPS

The four functional groups of registers for the microcomputer interface are:

- Memory Controller Registers
- Programmable Data Sequencer Registers
- PC-AT Interface Registers
- Media Format Registers

The Memory Controller Registers and the Programmable Data Sequencer Registers are directly addressable. The Memory Controller Registers are used to control and monitor data block transfers between the data sequencer and the external RAM buffer and between the external RAM buffer and the PC-AT interface. The Programmable Data Sequencer Registers are used to control and monitor the Data Sequencer (i.e., the data flow between the disk and the 82C5059); several of these registers are also used to indirectly access the media format RAM and hence to configure the disk media. The PC-AT Interface Registers are used to configure this device for the proper mode of communication with the host and also perform a one time initialization for configuration and mode of operation.

For the memory controller, there are 16 Write and 16 Read Registers--WR00-15 and RR00-15, respectively. Similarly, for the data sequencer there are 19 Write and 16 Read Registers, WR16-34 and RR16-31, and the PC-AT interface has 16 Write and 10 Read Registers, WR64-78 and RR64-71.

The Media Format Registers (indirectly accessed as mentioned above) are a sequence of 16 pairs of byte-wide registers which are set to define the complete bit-sequential organization of each data track on a disk drive. Since disk format is rarely reconfigured after initialization, these registers are accessed indirectly; i.e., via the Programmable Data Sequencer Registers.

ACCESS TO MICROCOMPUTER REGISTERS

The registers in the CHIPS 82C5059 are accessed (written or read) in much the same way they are in any microprocessor peripheral component: a particular register is addressed and data is transferred over a byte-wide, bi-directional address/data bus on the microprocessor interface, AD(7:0). Note that the individual control signals and protocol recognized by the 82C5059 will vary according to the microprocessor (Z8 or 8051 type) and strapping the CONFIG (Configuration) control input pin to the 82C5059. In any case, the microprocessor first drives the selected I/O address onto the bus. The address latching signal, ALE (8051 type) or -AS (Z8 type), is then generated by the microprocessor and used by the 82C5059 to internally latch the address for register decoding. Finally, a single byte of data is then transferred over the bus under control of the appropriate microprocessor access signals. Detailed timing information for these transfers is described in Chapter 2.

This addressable interface covers an I/O address range of 48 locations for the 82C5059--about one third of the typical microprocessor's I/O address space. In order to minimize external hardware requirements, the 82C5059 contains internal address decoding hardware which compares the full 8-bit I/O address as it is presented by the microprocessor and only responds to addresses in the low order 128 locations. Peripheral components connected to the AD(7:0) bus are now free to decode higher-order addresses (where the most significant bit is a one) for device or register selection.

WRXX stands for Write Register XX and RRXX stands for Read Register XX, where XX is the decimal equivalent of the 8-bit address placed on AD-07.

I/O read or write operations may be performed by the microprocessor at any time; however, the firmware must take into account that access to some registers may only be appropriate at specific times during command processing.

Table 3-1 lists the Memory Controller Registers. Table 3-2 lists the Data Sequencer Registers. Table 3-3 lists the PC-AT Interface Control Registers. Table 3-4 lists Media Format Registers (RAM). (Note that the latter are actually pairs of registers indirectly accessed through the Sequencer Registers.) Following these tables is a complete description of these registers.

Table 3-1. Memory Controller Registers

Control (Write) Registers

Write	Function
WR00 (00h)	Channel 0 Address 7-0
WR01 (01h)	Channel 0 Address 15-8
WR02 (02h)	Channel 0 Transfer Count 7-0
WR03 (03h)	Channel 0 Transfer Count 15-8
WR04 (04h)	Channel 1 Address 7-0
WR05 (05h)	Channel 1 Address 15-8
WR06 (06h)	Channel 1 Transfer Count 7-0
WR07 (07h)	Channel 1 Transfer Count 15-8
WR08 (08h)	Channel 0 Control
WR09 (09h)	Channel 1 Control
WR10 (0Ah)	Memory Cycle Timing
WR11 (0Bh)	CRC/ECC Selection and Control
WR12 (0Ch)	Group Write Strobe
WR13 (0Dh)	Group Write Strobe
WR14 (0Eh)	Group Write Strobe
WR15 (0Fh)	Group Write Strobe

Status (Read) Registers

Read	Function
RR00 (00h)	Channel Status
RR01 (01h)	Not used
RR02 (02h)	Channel 0 Transfer Count 7-0
RR03 (03h)	Channel 0 Transfer Count 15-8
RR04 (04h)	Not used
RR05 (05h)	Not used
RR06 (06h)	Channel 1 Transfer Count 7-0
RR07 (07h)	Channel 1 Transfer Count 15-8
RR08 (08h)	Not used
RR09 (09h)	Not used
RR10 (0Ah)	Not used
RR11 (0Bh)	Memory to Peripheral Write Strobe
RR12 (0Ch)	Group Read Strobe
RR13 (0Dh)	Group Read Strobe
RR14 (0Eh)	Group Read Strobe
RR15 (0Fh)	Group Read Strobe

Table 3-2. Data Sequencer Registers

Control (Write) Registers

Write	Function
WR16 (10h)	Sequencer Command
WR17 (11h)	Sequencer Loop Count
WR18 (12h)	Index Time-Out
WR19 (13h)	Sub-Block Count
WR20 (14h)	Cylinder (High Byte)
WR21 (15h)	Cylinder (Low Byte)
WR22 (16h)	Head/Flag
WR23 (17h)	Sector Number
WR24 (18h)	Micro to Memory
WR25 (19h)	Sequencer Start/Restart
WR26 (1Ah)	Sequencer Loop State and Format RAM Bank Select
WR27 (1Bh)	Bit Ring Start Count and Added Control
WR28 (1Ch)	ECC Control
WR29 (1Dh)	Configuration Control
WR30 (1Eh)	Seq Value Register @ Seq Start
WR31 (1Fh)	Seq Count Register @ Seq Start
WR32 (20h)	Optional DMA Control
WR33 (21h)	DMA Bank Control
WR34 (22h)	Optional Sequencer Control
WR35 (23h)	Additional DMA Control
WR36 to (23h)	Reserved
WR63 (3Fh)	Reserved

Status (Read) Registers

Read	Function
RR16 (10h)	Sequencer Status
RR17 (11h)	Extended Sequencer Status
RR18 (12h)	Retry Count/State Address
RR19 (13h)	Flag Byte
RR20 (14h)	Cylinder (High Byte)
RR21 (15h)	Cylinder (low Byte)
RR22 (16h)	Head/Flag
RR23 (17h)	Sector Number
RR24 (18h)	Memory to Micro
RR25 (19h)	Sequencer Loop Count
RR26 (1Ah)	Test Register
RR27 (1Bh)	Force Index Register
RR28 (1Ch)	Force Sequencer Reset
RR29 (1Dh)	Not used (Reserved)
RR30 (1Eh)	Seq Value Register @ Seq Start
RR31 (1Fh)	Seq Count Register @ Seq Start
RR32 to (20h)	Reserved
RR63 (3Fh)	Reserved

Table 3-3. PC-AT Interface Registers

Control (Write) Registers

Write	Function
WR64 (40h)	Master/Slave Control Register
WR65 (41h)	Error Register
WR66 (42h)	Sector Count Register
WR67 (43h)	Sector Number Register
WR68 (44h)	Cylinder Low Register
WR69 (45h)	Cylinder High Register
WR70 (46h)	Size/Drive/Head Register
WR71 (47h)	Status Register
WR72 (48h)	Busy Control Register
WR73 (49h)	Buffer Transfer Count
WR74 (4Ah)	Internal Control Register
WR75 (4Bh)	Drive Control Register
WR76 (4Ch)	Host Control Register
WR77 (4Dh)	Additional Control Register

Status (Read) Registers

Read	Function
RR64 (40h)	Internal Status Register
RR65 (41h)	Precompensation Register
RR66 (42h)	Sector Count Register
RR67 (43h)	Sector Number Register
RR68 (44h)	Cylinder Low Register
RR69 (45h)	Cylinder High Register
RR70 (46h)	Size/Drive/Head Register
RR71 (47h)	Command Register

Table 3-4. Media Format Registers (RAM)

Indirectly Addressed

Register Pair	Name
0	ESDI Sector Gap
1	Post-Index Gap
2	ID Preamble
3	ID Sync
4	ID Address Mark
5	ID Header
6	ID CRC/ECC
7	ID Postamble
8	Data Preamble
9	Data Sync
10	Data Address Mark
11	Data Field
12	Data CRC/ECC
13	Data Postamble
14	Inter-Sector Gap
15	Pre-Index/Sector Gap

REGISTER DESCRIPTIONS

1. MEMORY CONTROLLER REGISTERS

1.1 Write Registers

Write Register 00 and Write Register 04--Memory Addresses 7 - 0

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

The Memory Address Register (7-0) specifies the least significant byte of the starting address in the buffer RAM of the memory block where data is available (for read), or where data is to be stored (for write). **This address is automatically incremented after each byte of data is transferred.** WR00 is for Channel 0; WR04 is for Channel 1.

Write Register 01 and Write Register 05--Memory Address 15 - 8

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

The Memory Address Register (15-8) specifies the most significant eight bits of the starting address in the buffer RAM of the memory block where data is available (for read), or where data is to be stored (for write). **This address is automatically incremented by the overflow of the Memory Address 7-0 Register (7-0).** WR01 is for Channel 0; WR05 is for Channel 1.

Write Register 02 and Write Register 06--Transfer Count 7 - 0

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

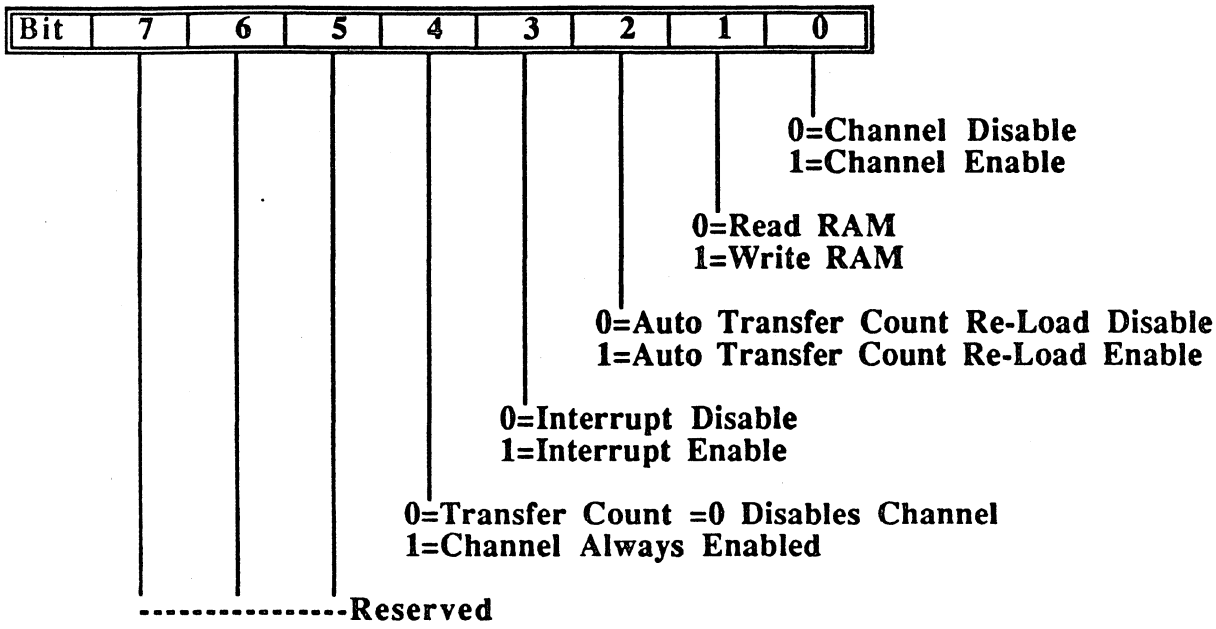
The Transfer Count 7-0 register specifies the least significant byte of the number of transfers to be performed. **The transfer count is automatically decremented after each transfer.** WR02 is for Channel 0; WR06 is for Channel 1.

Write Register 03 and Write Register 07--Transfer Count 15 - 8

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

The Transfer Count bits 15-8 register specifies the most significant eight bits of the number of transfers to be performed. **The transfer count is automatically decremented by the underflow of the corresponding Transfer Count Register (7-0).** WR03 is for Channel 0; WR07 is for Channel 1.

Write Register 08--Channel 0 Control



BIT 0 = Channel Control

Setting bit 0=1, enables the channel; setting bit 0=0 aborts a transfer in progress and disables the channel.

BIT 1 = Channel Read/Write

Bit 1 specifies the direction of the data transfer. When cleared, data is transferred from the RAM buffer memory to the Data Sequencer (or the RR24 in a Memory-to-Micro transfer). When set, data is transferred from the Data Sequencer (or from WR24 in a Micro-to-Memory transfer) to the RAM buffer memory.

BIT 2 = Transfer Count Reload

When bit 2 is set, and a block transfer is complete (Transfer Count = 0) the channel's Transfer Count Register is automatically reloaded with its value prior to the transfer. This option allows transfer of a sequence of records without resetting the channel's Transfer Count Registers between individual record transfers.

Note: For continuous operation, bit 0 and bit 4 must also be set to 1.

BIT 3 = Interrupt Enable/Disable

Bit 3 set enables interrupts (the assertion of INT MEM at the end of a block transfer when Transfer Count = 0); bit 3 clear disables interrupts.

Note: The deasserting edge of the channel enable signal actually triggers INT MEM. Thus if bit 4 (see below) is set (the channel is always enabled), then no interrupt will occur--even if bit 3 is set.

Note: It is not recommended to set bit 3 for interrupts unless bit 4 is clear; i.e., the combination, bit 3 = 1 and bit 4 = 1, is not logical. When bit 3 is set (and bit 4 = 0), the microprocessor would normally respond by reading the Channel Status Register RR00, which tells what channel caused the interrupt, etc.

When bit 3 is clear, interrupts from the channel are disabled. This option is available because, when only a single channel is being used, the memory interrupt (INT MEM) may not be required. The Sequencer Interrupt (INT SEQ) could be used to tell when a command has been completed.

BIT 4 = Channel Auto Disable

With bit 4 cleared, the channel is automatically disabled when the Transfer Count reaches 0. To begin another operation on the channel, the Enable bit (bit 0) must be set by writing the Control Register.

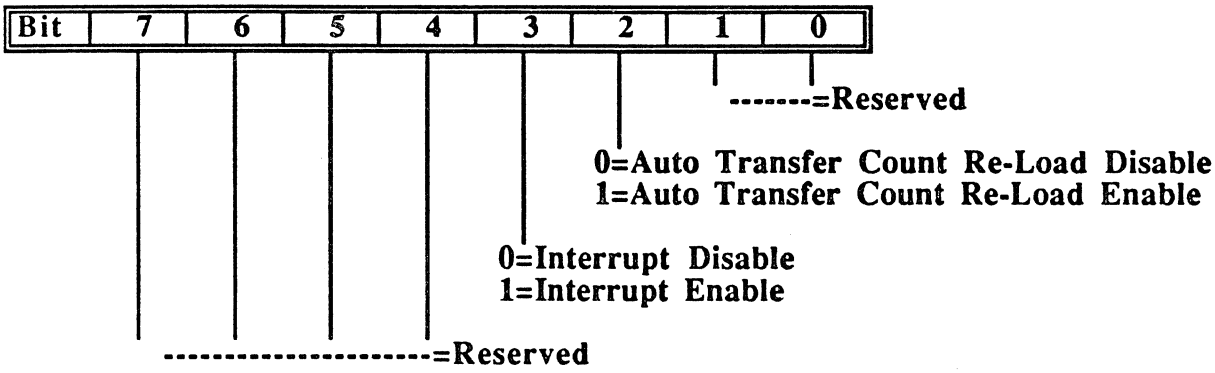
With bit 4 set, the channel remains enabled after the Byte Count equals 0.

Note: Not all combinations of bit 4 and bit 3 are logical. See the note under bit 3 above.

BITS 5-7 = Reserved

These bits are reserved and must be set to 0.

Write Register 09--Channel 1 Control



BITS 0&1 = Reserved

Bits 0 and 1 are reserved and must be set to 0.

BIT 2 = Transfer Count Reload

With bit 2 set, when a block transfer is complete (Transfer Count = 0) the channel's Transfer Count Register is automatically reloaded with its value prior to the transfer. This option allows the transfer of a sequence of records without resetting the channel's Byte Count Registers between individual record transfers.

BIT 3 = Interrupt Enable/Disable

Bit 3 set =1 enables interrupts (the assertion of INT MEM at the end of a block transfer when Transfer Count = 0); bit 3 set=0 disables interrupts.

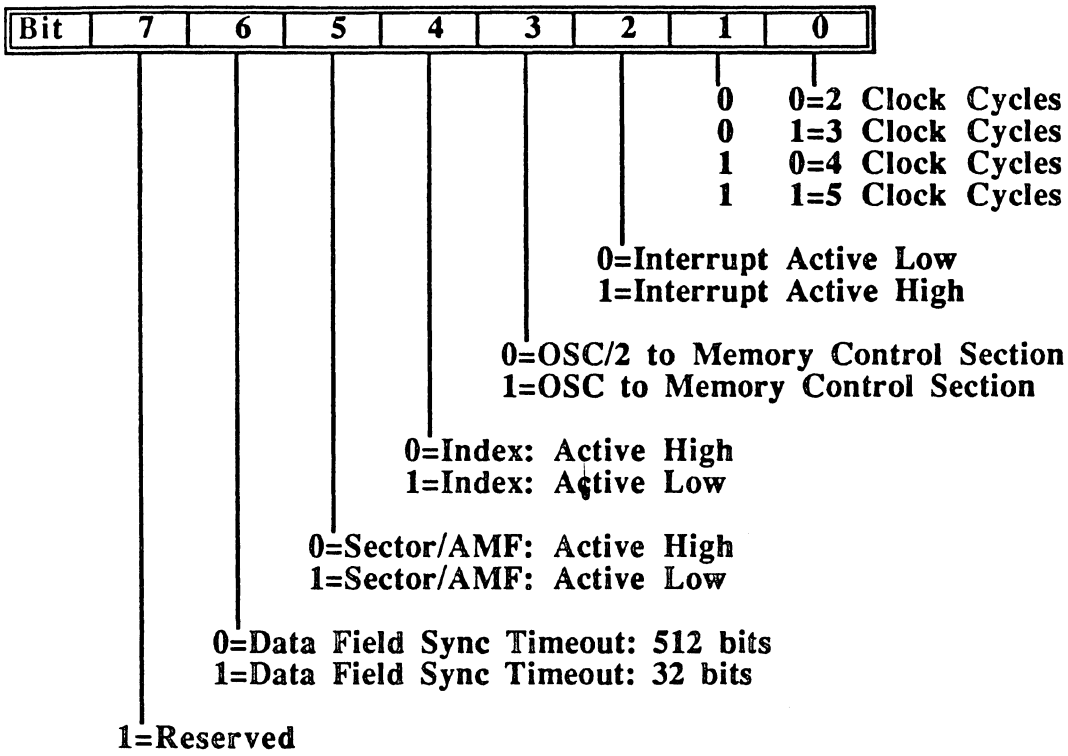
When bit 3 is set the microprocessor would normally respond by reading the Channel Status register RR00, which tells what channel caused the interrupt, etc.

When bit 3 is set=0, interrupts from the channel are disabled. This option is available because, when only a single channel is being used, the Memory Interrupt (INT MEM) may not be required. The Sequencer Interrupt (INT SEQ) could be used to tell when a command had been completed.

BITS 4-7 = Reserved

Bits 4 and 6 are reserved and must be set to 0.

Write Register 10 (0Ah)--Memory Cycle Timing



BITS 0-1 = Memory Cycle

Bits 0 and 1 specify the number of clock cycles to be used in the memory cycle for each transfer. A transfer will be a word transfer (8, 16, or 32 bits as programmed by WR32 bits 6 and 7). This option is provided to accommodate a range of RAM buffer memory speeds.

Bits	Clock Cycle
00	2
01	3
10	4
11	5

BIT 2 = Interrupt Polarity

Bit 2 specifies the polarity of the memory controller's interrupt line (INT MEM). The polarity (high or low) of INTMEM will follow the state of the bit (i.e. if set=1, the INTMEM if positive true).

BIT 3 = Memory Clock Select

Bit 3 specifies the clock signal frequency to be used within the memory control section of the device. When bit 3 is set=1, the clock signal will be at the same frequency as the crystal (XTAL). When set=0, the clock frequency will be one half the crystal (1/2 XTAL).

BIT 4 = Index Polarity

Bit 4 specifies the polarity of the INDEX input signal. If set=1, then INDEX will be low to high true. If set=0, INDEX will be high to low true.

BIT 5 = Sector/AMF Polarity

Bit 5 specifies the polarity of the SECTOR/AMF input signal. If set = 1, then SECTOR/AMF will be low to high true. If set=0, SECTOR/AMF will be high to low true.

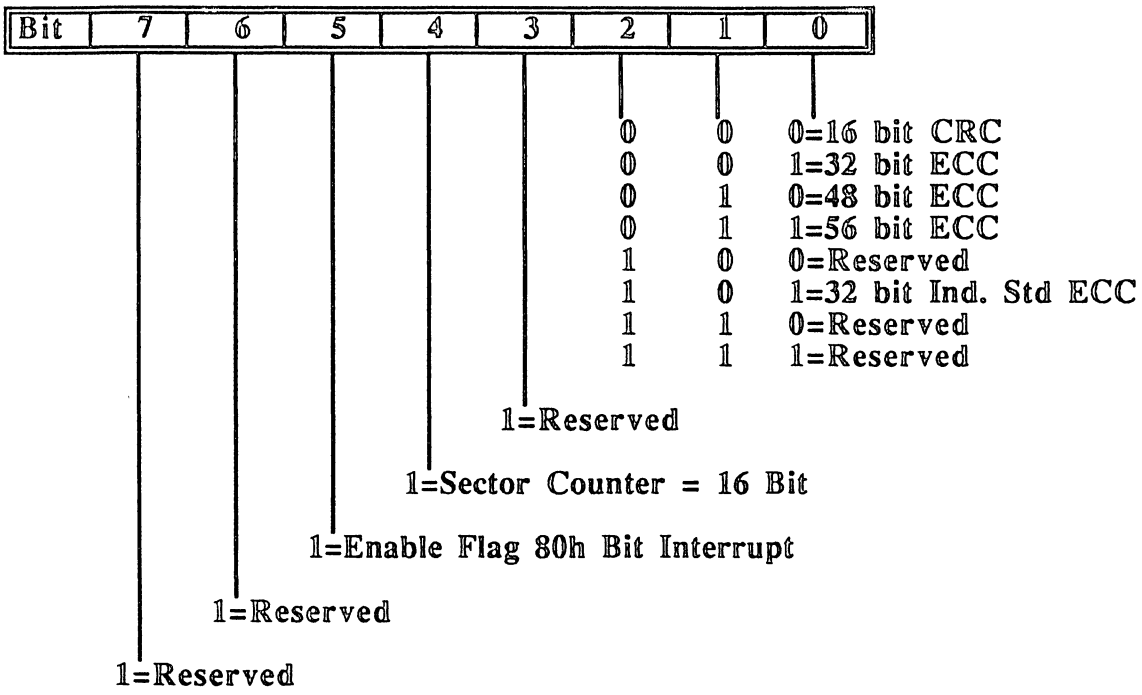
BIT 6 = Data Field Timeout Select

Bit 6 specifies the value of Data Sync Field Timeout (when enabled by bit 7 or WR28). When bit 6 is set=0, the timeout value is 512 bits for normal operation; when bit 6 is set, the timeout is 32 bits for test purposes.

Bit 7 = Reserved

Bits 7 is reserved and must be set to 0.

Write Register 11 (0Bh)--CRC/ECC Polynomial Selection and Control



BITS 0-2 = ECC/CRC Select

Bits 0 and 1 select the CRC or ECC polynomial to be used for the data field. If bit 6 of WR28 is cleared, the same polynomial will also be used for the ID field. If bit 6 of WR28 is set, however, then the ID field will use the CRC polynomial (first selection listed below) regardless of the selection by Bits 0 and 1 (WR11).

The five possible selections by bits 0 and 1 are:

0-0-0: (X16)+(X12)+(X5)+1 (floppy compatible, CRC)
0-0-1: (X32)+(X24)+(X18)+(X15)+(X14)+(X11)+(X8)+(X7)+1
0-1-0: Proprietary, 48 bit ECC*
0-1-1: Proprietary, 56 bit ECC*
1-0-0: Reserved
1-0-1: (X32)+(X28)+(X26)+(X19)+(X17)+(X10)+(X6)+(X2)+1
1-1-0: Reserved
1-1-1: Reserved

* Contact SMS for Sublicense.

BIT 3 = Reserved

This bit is reserved and must be set to 0.

BIT 4 = Sector Count Select

If bit 4 is set = 1, the data field length will be equal to the number of a 16 bit counter comprised of the count in State 11, as the low order byte of the counter, and the number loaded into the Sub-block Count WR19, as the high order byte of the counter. This feature is to provide any integer from 1 to 65535 byte per sector. If this bit is set = 0, the data field length will be equal to the product of the Sub-block Count minus 1 times the count in State 11.

BIT 5 = ID Interrupt Control

If bit 5 is set = 1, this enables a sequencer interrupt that is the result of an ID Head Flag/Flag Byte having the 80h bit on. If this option is enabled and the most significant flag bit is on, a sequencer interrupt will be generated after the ID has been processed. If other flag bits are on, the sequencer will not abort on flag conditions even if the Ignore ID Flag bit in the Sequencer Command Register was not set. This sequencer interrupt will be cleared after the microprocessor reads the Extended Status Register RR17.

BITS 6-7 Reserved

These bits are reserved and must be set to 0.

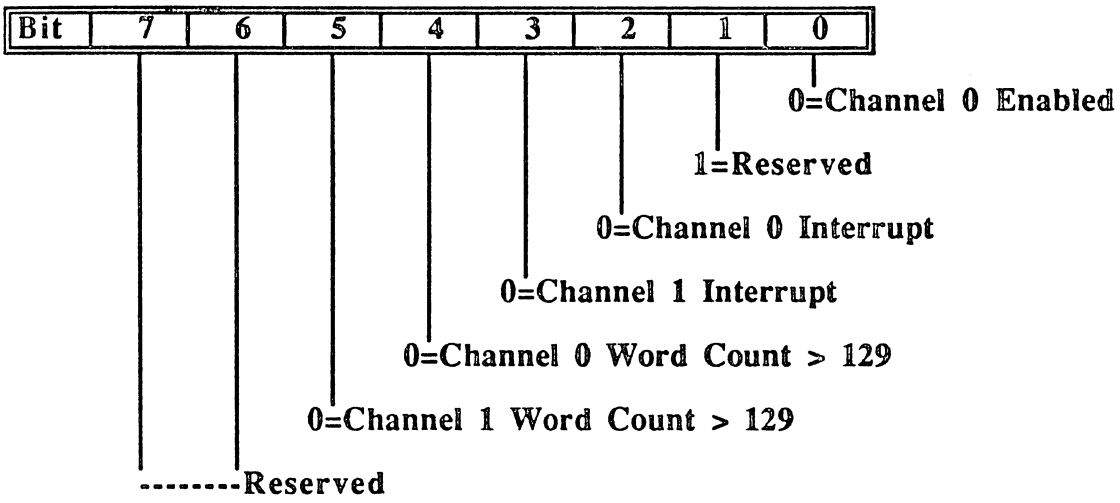
Write Register 12 through 15 (0Ch-0Fh)--External Group Strobe

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

When any of these registers is written, -GRPWRT is asserted. -GRPWRT can be used to strobe information from the microprocessor's data bus (AD(7:0)) into a peripheral device.

1.2 Read Registers

Read Register 00--Channel Status.



BIT 0 = Channel Status

Bit 0 reflect the status ("0" enabled, "1" disabled) of Memory Controller Channels 0.

BIT 1 = Reserved

Bit 1 is reserved and will always equal a 0.

BITS 2-3 = Channel Interrupt Status

Bits 2 and 3 reflect the interrupt status ("0" = interrupt, "1" = no interrupt) for Channels 0 and 1, respectively.

BITS 4-5 = Transfer Count Status

Bits 4 and 5 are set=0 for each channel when the last 128 transfers are in progress.

BITS 6-7 = Reserved

Bits 6 and 7 are reserved and always 1.

Read Register 02 and Read Register 06--Transfer Count 7 - 0

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

These registers contain the least significant byte (bits 0-7) of the current count in the Transfer Count Register. RR02 is for Channel 0; RR06 is for Channel 1.

Read Register 03 and Read Register 07--Transfer Count 8 - 15

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

These registers contain the most significant byte (bits 8 to 15) of the current count in the Transfer Count Register. RR03 is for Channel 0; RR07 is for Channel 1.

Read Register 11--Memory to Peripheral Write Strobe

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

RR11 is used in RAM buffer to peripheral transfers (see RR24 for a complete description of such transfers). When the microprocessor reads RR11, the sequencer generates -GRPWRT for writing data from RR24 into a peripheral device on the microprocessor address/data bus, AD0-7.

Read Register 12 through Register 15 (0Ch-0Fh)--External Group Strobe

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

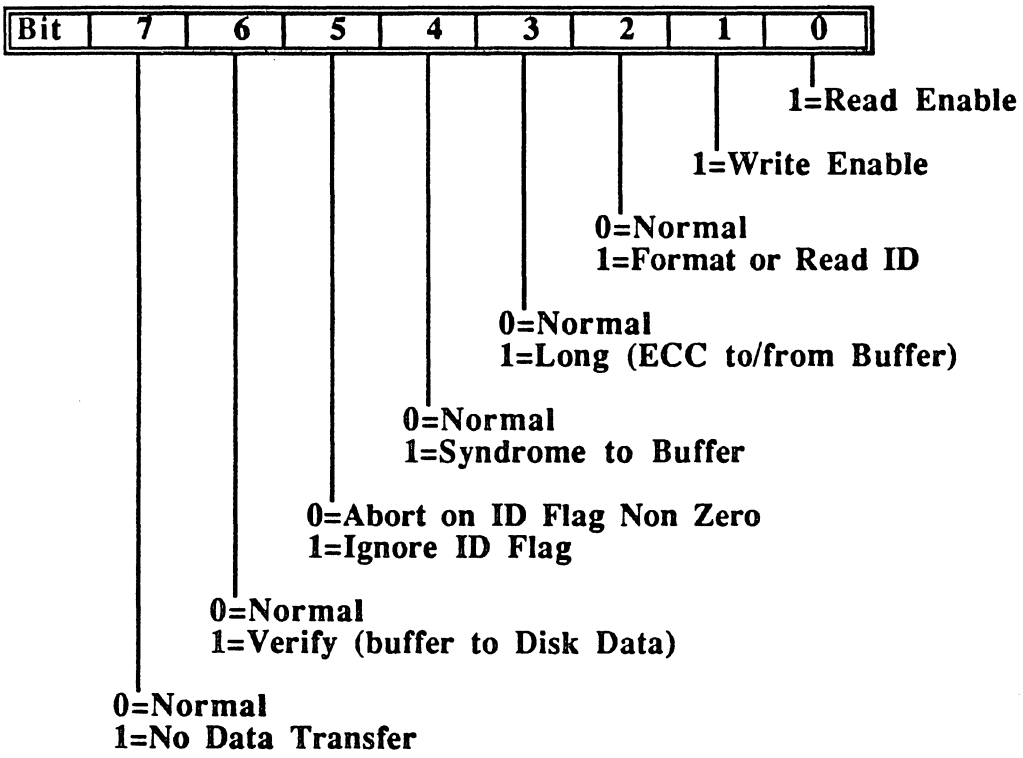
When any of these registers are read, -GRPRD is asserted. -GRPRD may be used to strobe information from a peripheral device onto the microprocessor's data bus.

When the Transfer Enable bit (bit 5) in the CRC/ECC Control Register (WR28) is set=1, a read of RR15 will enable data to be latched into the Micro-to-Memory Register (WR24). The rising edge of the strobe (-GRP_RD) will cause a DMA request and transfer the data from WR24 to the buffer.

2. DATA SEQUENCER REGISTERS

2.1 Write Registers

Write Register 16 (10h)--Sequencer Command



A write to the Command Register initiates a command. The command is defined by the bit combination in this register and other data transfer registers. Valid combinations in this register are listed in Chapter 4 (Operation) in Table 4-1 (Sequencer Command Registers). The effect of each command (valid combination) is also provided in these sections. **Only the effect of each bit is described in this section.**

BIT 0 = READ Type Command

When bit 0 is set=1, the operation is a READ command: data is transferred from the disk to the RAM buffer.

BIT 1 = WRITE Type Command

When bit 1 is set=1, the operation is a WRITE command: data is transferred from the RAM buffer to the disk.

If bit 0 is set=1, then bit 1 must not be set, and vice versa.

The remaining bits (2-7) are command modifiers and, depending on whether an operation is a read or a write, have different meanings.

BIT 2 = FORMAT Option

If bit 2 is set=1 and the operation is a read (bit 0 set=1), then only the ID fields will be read (READ ID command).

If bit 2 is set=1 and the operation is a write (bit 1 set=1), then the command is one of the format commands (FORMAT TRACK, FORMAT TRACK LONG, or FORMAT SECTOR).

BIT 3 = LONG Option

If bit 3 is set=1, then both the data and the CRC/ECC check bits will be written to or read from the RAM buffer. (These are the various LONG operations described in the command set.)

BIT 4 = SYNDROME Option

If bit 4 is set=1 and the operation is a READ LONG type (bit 0 is set=1, bit 3 is set=1), then both the data and the syndrome bytes (the result of the ECC check) are written to the RAM buffer. This applies to READ SYNDROME LONG, READ ID SYNDROME LONG, READ SYNDROME (LONG)-IGNORE FLAG, VERIFY SYNDROME LONG, and the VERIFY SYNDROME LONG-IGNORE FLAG Commands.

BIT 5 = FLAG Option

If bit 5 is set=0, operation will abort if a flag condition exists.

Note: Flag information is contained in either bits 7-4 of byte 2 (Flag/Head Byte) of the ID Header field, or it is contained in byte 5 of the ID Header field (see WR29, bit 2). In the former case it is referred to as the Flag Nibble; in the latter case it is referred to as the Flag Byte. When a read or write occurs to a sector that contains non-zero flag information, the Flag Byte/Nibble bit (bit 3) of the Extended Status Register (RR17) is set.

When a command is aborted, the processor can read the Status Registers (RR16 and RR17) to determine the cause. Having determined the cause, the microprocessor may choose to read or write the sector anyway, in which case it should set this bit=1 to ignore the ID Flag and reissue the command.

When bit 5 is set=1 on a READ or WRITE command, the Flag Byte or Flag Nibble will be ignored.

When bit 5 is set=1 on a Format command, the command becomes a FORMAT SECTOR command and keys off of the SECTOR line instead of the INDEX line. For this function the sequencer must be in hard sectored mode. **(Note: bit 5 is dual-function in this regard: In the context of format commands, it has nothing to do with ignoring the ID flag information; it simply toggles between a FORMAT TRACK and a FORMAT SECTOR command.)**

BIT 6 = VERIFY Option

When bit 6 is set=1 on a read-type command (bit 0 is set=1), the command becomes a VERIFY command. A VERIFY command is a convenience for checking data written to the disk. The VERIFY command (1) reads data from the disk into the 82C5059; (2) reads data out of the RAM buffer; and (3) performs a byte-by-byte, on the fly comparison. **Unlike the various read commands, this command does not destroy data in the RAM buffer.**

BIT 7 = NO TRANSFER Option

When bit 7 is set=1 on a read-type command (bit 0 is set=1), data is read from the disk but it is not transferred to the RAM buffer. This is for checking purposes: it allows data fields to be read and checked for CRC/ECC errors without transferring the data to the RAM buffer.

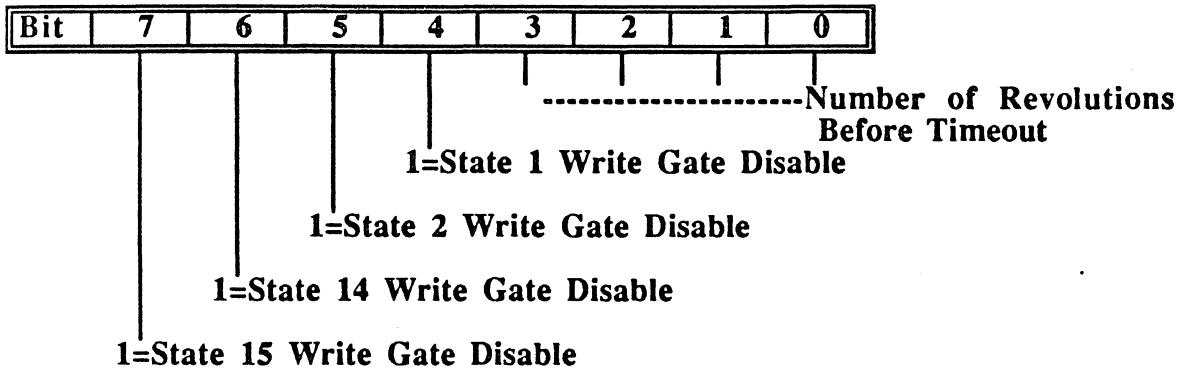
Write Register 17 (11h)--Sequencer Loop Count

Bit	7	6	5	4	3	2	1	0
Byte	Number of Sectors							

This register specifies the number of sectors to be read or written, or in the case of a FORMAT command, the number of sectors on the track. **(Note: Precisely stated, the value in this register specifies the number of times the loop is executed in the predefined state sequence for the particular command.)** This number is decremented for each sector processed by the command. As a convenience for repeated commands involving the same number of sectors, an internal register stores the initial value of the register and automatically reloads it when a command is complete.

Once a command has been issued, the real time contents of this register can be obtained by reading the Sequencer Loop Count (RR25).

Write Register 18 (12h)--Index Timeout and Format Write Gate Control



BIT 0-3 = Index Timeout Count

Bits 0-3 of this register specifies the number of disk revolutions, as measured by the number of INDEX pulses, before a command is aborted. **Valid values are X2h through XFh.** This feature allows the sequencer to do automatic retries when it cannot find the ID. The register gets reinitialized after every successful transfer for multi-sector commands. When a command is aborted because Index Timeout is exceeded, the Extended Status Register (bit 2, RR17) will be set.

A holding register retains the value of this register so that it has to be loaded only when a change is required.

BIT 4-7 = Disable WRT_GATE Option

Bits 4-7 allow disabling of WRT GATE for the specified state (1, 2, 14, or 15, respectively).

Write Register 19 (13h)--Sub-block Count

Bit	7	6	5	4	3	2	1	0
Byte	Number of Sub-blocks per Sector							

The Sub-block Count is used to determine the number of data bytes per sector (Sector Size).

Sector Size = (Sub-block Count + 1) * Data Field Count

Data Field Count is the count byte from the format RAM for the Data Field in the Data Segment. Note that Sub-block Count is simply a multiplier that allows the number of bytes for the Data Field to be greater than the maximum count value (256) would allow.

Note: This register should be loaded at initialization and at any time a different Sector Size is used.

Examples:

Sector Size (Bytes)	Sub Block Count	Data Count
128	7h	10h.
256	Fh	10h.
512	1Fh	10h.
1,024	3Fh	10h.
2,048	7Fh	10h.
65,536	FFh	00h
		(00=256)

Write Register 20 through 23 (14h-17h)--ID Registers

These four registers are loaded with ID Header information (Cylinder High, Cylinder Low, Head Add, and Sector numbers) to identify a desired sector on a disk. They are then compared to the first four bytes of the ID Header encountered on the disk. Before any command is issued, with the exception of FORMAT and CHECK TRACK FORMAT, these registers should be loaded with the first four bytes of the desired ID Header.

Write Register 20 (14h)--CYLINDER HIGH (ID BYTE 0)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Write Register 21 (15h)--CYLINDER LOW (ID BYTE 1)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Write Register 22 (16h)--Head Number (ID BYTE 2)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh OR X0-XFh							

This byte specifies the value of the third byte of the ID Header.

Note: If the the Head/Flag mode is selected (bit 2 of WR29 clear), then only the low nibble (bits 3-0) contains Head Number information and only this low nibble is compared. If Flag Byte mode is selected (bit 2 of WR29 set), then the entire byte contains the head number and is compared.

When Head/Flag mode is selected, valid values are 00h through 0Fh; when Flag Byte mode is selected, valid values are 00h through FFh.

Write Register 23 (17h)--Sector Number (ID BYTE 3)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register specifies the value of the fourth byte of the ID Header--normally the Sector number to be read or written. It is a counter that is auto-incremented at the end of a valid data field operation. This feature allows sequential operations on one track without having to reload the ID Write Registers.

Write Register 24 (18h)--Micro/Peripheral to Memory

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is used to transfer data from the microprocessor, or a peripheral device on the microprocessor bus, to the RAM buffer.

Microprocessor to RAM Buffer Transfers

When the microprocessor writes WR24, the microprocessor data is latched into WR24. The Sequencer then generates a Channel 0 DMA request (REQ0). On the acknowledge from the DMA circuit (ACK0) the data will be transferred from WR24 to the RAM buffer.

Note: Before beginning such a sequence, it is necessary to configure DMA Channel 0 to be in Write mode. Note also that if the DMA does not respond to the Channel 0 request (REQ0), the Micro Memory Over/Under Run bit in the Extended Status Register (bit 1 of RR17) will be set along with the Extended Status Non-Zero bit in the Sequencer Status Register (bit 7 or RR16).

Peripheral to RAM Buffer Transfers

The sequencer can also transfer data from a peripheral device that is connected to the microprocessor address/data bus (AD0-7) to the RAM buffer. To transfer data from the peripheral to the RAM buffer, the microprocessor reads RR15.

Note that the transfer Enable bit in the CRC/ECC Control Register must be set; i.e., bit 5 of WR28. Also, as noted above, the DMA Channel 0 must be initialized before starting the transfer.

When the microprocessor reads RR15, the sequencer generates the read strobe signal -GRPRD for reading the data from the peripheral so that it can be latched into WR24. On the trailing edge of -GRPRD, a Channel 0 DMA cycle is initiated, using REQ0 and ACK0 to write the contents of WR24 into the RAM buffer.

Write Register 25 (19h)--Sequencer Start/Restart

Bit	7	6	5	4	3	2	1	0
Byte	Re-Start State 0X-FXh				Start State X0-XFh			

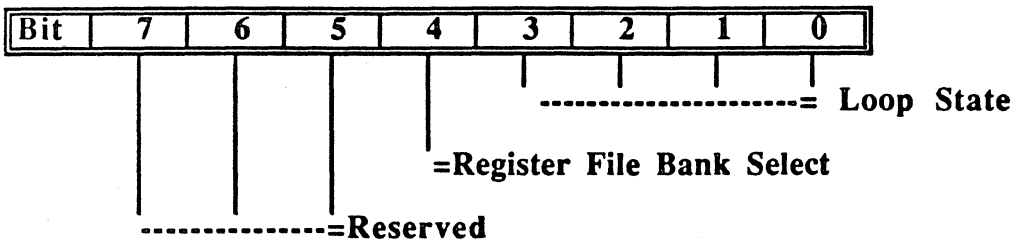
During the executing of a command: Bits 3-0 specify the state number at which the sequencer will begin execution; bits 7-4 specify the state number from which the sequencer will restart after the Sequencer Loop State (specified by WR26) has been reached.

(Note: The 82C5059 allows sixteen possible states, 0 to 15. A state corresponds to a type of media field. Specifically, a State 0 corresponds to the byte pair (Value, Count) at address 0 in the format RAM; State 1 corresponds to the byte pair at address 1, and so on. The Value Byte gives the specific value to be encountered in the field; the Count Byte tells the number of times the State loops back on itself (i.e., holds), with the exception of the Data Field, whose total number of bytes is the product of Count and Sub-block Count (a multiplier to allow a greater number of bytes in this field). See format RAM in the next section for a complete explanation.

These values depend on the command and the particular disk configuration. Normally, values will be 33h (start and restart on sync field) for all commands except format-type commands, which will use 21h (start with Post-Index Gap Field, restart with ID Preamble).

This register is also used to address the format RAM. Valid addresses are 00h to 0Fh.

Write Register 26 (1Ah)--Sequencer Loop State and Format RAM Select



BITS 0-3 = Loop State

Bits 0-3 of this register determine the state number from which the sequencer jumps back to the Restart State. The value depends on the command and the particular disk configuration, but most commands have a Sequencer Loop State of 0Eh.

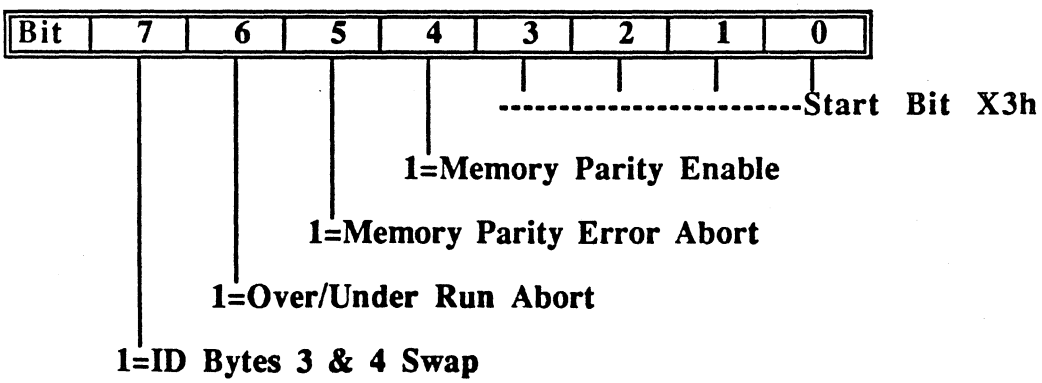
BIT 4 = Bank Select

Bit 4 selects between the two banks of 32 bytes in the format RAM.

BITS 5-7 = Reserved

These bits are reserved and must be set to 0.

Write Register 27 (1Bh)--Bit Ring Start Count and Added Control



BITS 0-3 = Bit Ring Control

Bits 0-3 of this register allow the user to specify the bit-level timing relationship between Sync Detect (AMF in External Sync mode indicates synchronization detection) and Byte Clock (the internal signal that sets the byte boundaries). **This register should be initialized with 03h.**

BIT 4 = Memory Parity Select

Bit 4 controls memory parity checking. If set=1, parity is enabled 0.

Note: If memory parity is enabled, then the functions of bit 0 and bit 1 in RR17 (Drive Data Over/Under Run and Micro Mem Over/Under Run) will be OR'd in bit 0 of RR17, and bit 1 of RR17 will be used to indicate a parity error.

BIT 5 = Abort On Parity

If bit 5 is set, a memory parity error will cause an abort, and the Memory Parity Error bit (bit 1 of RR17) will be set. (See note above.) If bit 5 is set=0, a memory parity error will not cause an abort.

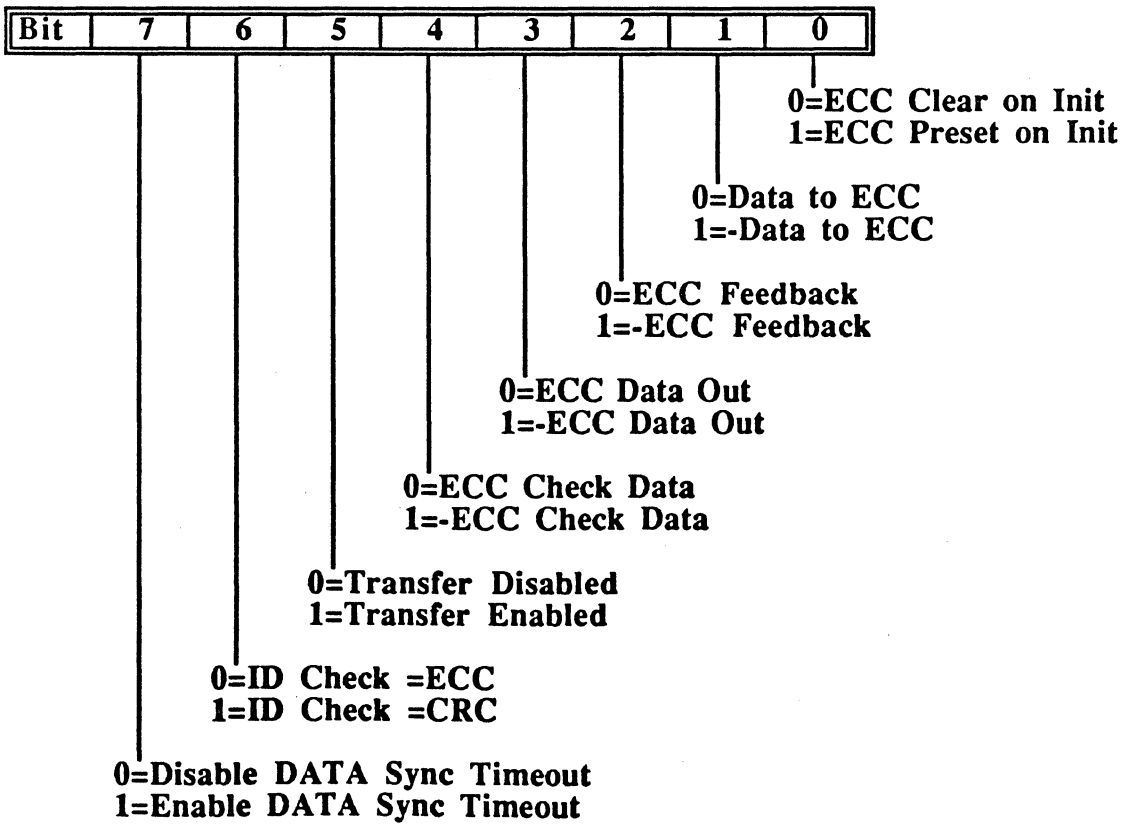
BIT 6 = Abort On Over/Under Run

If bit 6 is set=1, an Over/Under Run condition will cause an abort.

BIT 7 = Swap ID Bytes

Setting bit 7=1 swaps the ID Bytes 3 and 4. This is used for floppy disk compatibility.

Write Register 28 (1Ch)--CRC/ECC Control



The CRC/ECC Control register allows format and media compatibility with a variety of peripheral devices and error correction schemes.

BIT 0 = ECC Initialization

Bit 0 determines whether or not initialization of the CRC/ECC Shift Register String is cleared (to all 0's) or preset (to all 1's).

BIT 1 = NRZ To ECC Polarity

Bit 1 determines the polarity of the NRZ input data to the CRC/ECC circuitry, and will follow the polarity of this bit. (If set=1, then ECC= -NRZ, if set =0, ECC = +NRZ.)

BIT 2 = ECC Feedback Polarity

Bit 2 determines the polarity of the CRC/ECC feedback signal, and will follow the polarity of this bit. (If set=1, then NRZ= +NRZ, if set =0, NRZ= -NRZ.)

BIT 3 = ECC Out Polarity

Bit 3 determines the polarity of the CRC/ECC write data output, and will follow the polarity of this bit. (If set=1, then -ECC=Data Out, if set =0, ECC=Data Out)

BIT 4 = ECC Check Syndrome Polarity

Bit 4 determines the polarity of the CRC/ECC check signal, and will follow the polarity of this bit. (If set=1, then -ECC=Check Data, if set =0, ECC=Check Data.)

BIT 5 = Micro-DMA Enable

Bit 5 enables the automatic I/O Read/DMA Write function. In this mode data is transferred from an external peripheral device to the RAM buffer via RR15 (see RR15 for details of such a transfer).

BIT 6 = ID ECC/CRC Select

Bit 6 is used to select what type of error detection is used in the ID field.

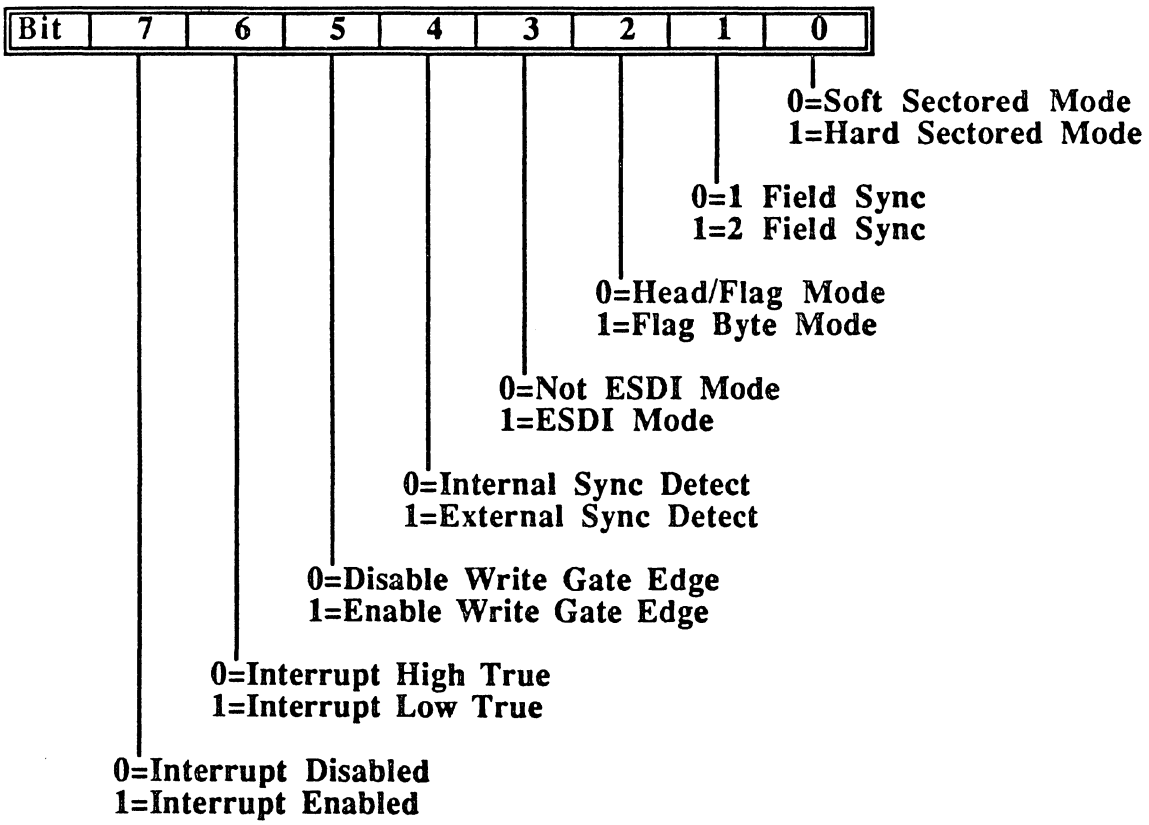
When bit 6 is set=1, the 16-bit CRC polynomial is used for the ID field: (X16)+(X12)+(X5)+1

When bit 6 is set=0, the polynomial selected by WR11 will be used for the ID field as well as the data field.

BIT 7 = Data Timeout Select

When bit 7 is set =1 and the ID Segment has been properly read (ID Match), failure to find the Data Sync field within the period specified by bit 6 of WR10 (512 bits for normal operation, 32 bits for test purposes) will cause a Data Sync Field Timeout error (bit 4 of RR17 set).

Write Register 29 (1Dh)--Configuration Control



BIT 0 = Hard/Soft Sector Select

Bit 0 selects between hard- and soft-sectored drives. In hard-sectored mode the sector line is used to re-synchronize the sequencer at State 15 and thereby determine the sector boundaries. If set=0, soft sector mode. If set=1, hard sector mode.

BIT 1 = 1-2 Field Select

Bit 1 selects between formats, 1 Field Sync (Sync field used, no Address Mark field used) and 2 Field Sync (both Sync and Address Mark fields used). Setting this bit=1, selects a 2 field sync format. Setting this bit=0, selects a 1 field sync format. The 1 Field Sync is normally used by ESDI drive interfaces; the 2 Field Sync (Sync byte, Address Mark byte) is used by ST506/412 drive types, including the CHIPS 5070 and 5027 Encode/Decode/PLL ASIC devices.

BIT 2 = Flag Mode Select

Bit 2 selects between two different modes of storing flag information in the ID Header. This information can be used to alert the firmware that a flag condition exists within the sector, thereby stopping a command if the Ignore ID Flag bit (bit 5 of WR16) is not set.

If bit 2 is set=0, then the flag information is contained in bits 4-7 of the 3rd byte (Head/Flag Byte) of the ID Header field. If bit 2 is set=1 only, the flag information resides in the 5th byte of the ID Header.

Note: Bit 2 also determines which Read Register contains the flag bits that are read from the disk. If bit 2 is cleared (Head/Flag mode), the Head/Flag Register (RR22) contains the flag information (bits 7-4); if bit 2 is set (Flag Byte mode), the Flag Byte Register (RR19) contains the flag information.

BIT 3 = ESDI Select

Bit 3 selects between an ESDI and a non-ESDI interface.

If ESDI mode is set=0, the sequencer is in ST506/412 mode, and it asserts RDGATE as soon as any Non-format command is issued. This mode must be used to interface to the CHIPS 5070 MFM and 5027 RLL 2,7 Encode/Decode/PLL ASIC devices.

If bit 3 is set=1, ESDI mode is configured, and the sequencer assumes the ESDI Search Address/Address Mark Found mode of handshake.

BIT 4 = Internal/External Sync Select

Bit 4 selects between internal synchronization detection (used for ESDI type interfaces) and external synchronization detection (used when the sequencer is configured with the CHIPS 5070 or 5027 Encode/Decode/PLL ASIC device.

If bit 4 is set=0, the sequencer performs bit-to-byte synchronization (determination of the byte boundary) by comparing (bit to bit) the incoming serial data in the shift register with the Sync Field.

If bit 4 is set=1, the sequencer uses the AMF line to perform bit-to-byte synchronization.

BIT 5 = Enable WRITE GATE Edge

If bit 5 is set=1 it disables WRTGATE on a FORMAT TRACK command for two bit times after the ID Postamble field--thereby providing an edge of WRTGATE for every PLL Sync Field. **This is required by some ESDI-type drives.**

BIT 6 = Interrupt Polarity

Bit 6 selects between interrupt (INT SEQ) active high or low.

If bit 6 is set=0 and interrupt enable is set (bit 7), an interrupt will be generated active high. If bit 6 is set =1 and interrupt enable is set=1 (bit 7), an interrupt will be active low.

BIT 7 = Interrupt Enable

Bit 7 set=1 enables interrupts; bit 7 set=0 disables interrupts. If enabled, an interrupt is generated by any condition that causes the sequencer to change status from Busy to Not Busy. The interrupt is cleared by reading the Status Register, RR16. **(Note: Busy/Not Busy status can be read in bit 0 of RR16.)**

Write Register 30 (1Eh)--Value Register @ Sequencer Start

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

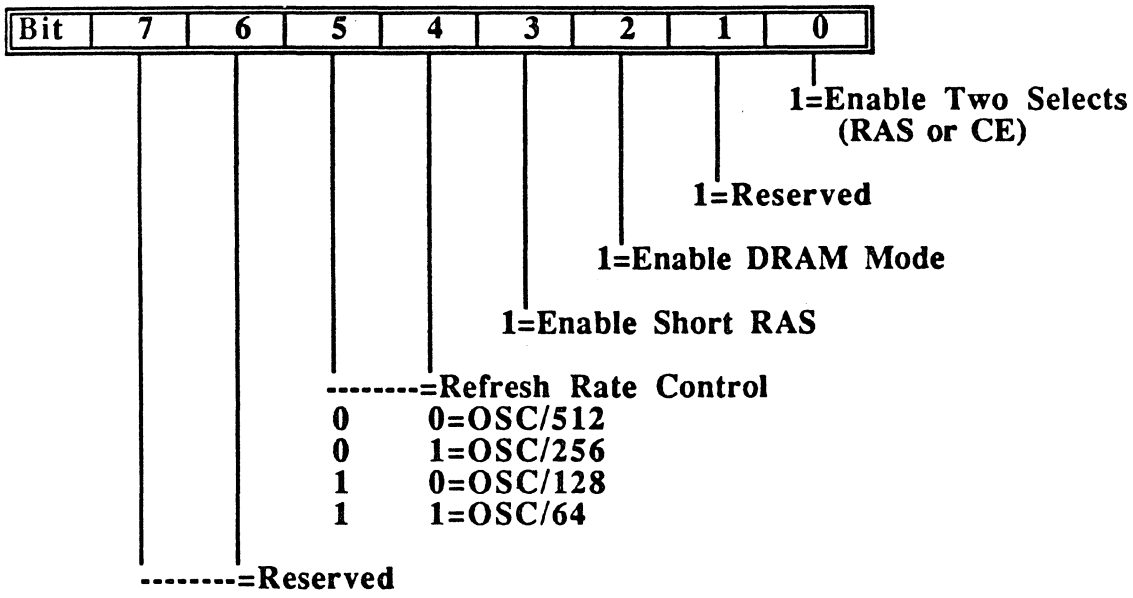
This register is used to write the Value Byte of the format RAM as indexed by WR25.

Write Register 31 (1Fh)--Count Register @ Sequencer Start

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is used to write the Count Byte of the format RAM as indexed by WR25.

Write Register 32 (20h)--Additional DMA Control



BIT 0 = MEM_CE Control

Setting this bit =1 enables two memory (RAM buffer) chip selects to support 64K Byte SRAM (2x(32Kx8): -MEMCE0 and -MEMCE1. (These can function as either Chip Enable (CE), in SRAM mode; or as Row Address Strobes (RAS), in DRAM mode.)

Note: When this bit is set=1, MEMA15 is routed to the MEMA0 pin, while MEMA0 is used internally to determine -MEMCE0 and -MEMCE1. (When MEMA0 is low, -MEMCE0 goes active; when MEMA0 is high, -MEMCE1 goes active.)

BIT 1 = Reserved

This bit is reserved and must be set to 0.

BIT 2 = SRAM/DRAM Control

Bit 2 enables DRAM mode; i.e., multiplexed addresses, RAS, CAS, and -REFSH are generated. If set=1, DRAM mode. If set=0, SRAM mode.

BIT 3 = Enable Short RAS

Bit 3 enables a shorter RAS time; i.e., RAS is one clock less than it would be as configured by WR10, bits 0 and 1. This is for extended precharge time. If set=1, short RAS, if set=0, normal.

BITS 4-5 = Refresh Rate

These bits set the refresh rate (internal refresh counter) as a function of the oscillator. Bits 5, and 4 value, see table below:

Bit 5	Bit 4	Value
0	0	OSC/512
0	1	OSC/256
1	0	OSC/128
1	1	OSC/64

BITS 6-7 = Reserved

These bits are reserved and must not be set to a 1.

Write Register 33 (21h)--DMA Bank Control

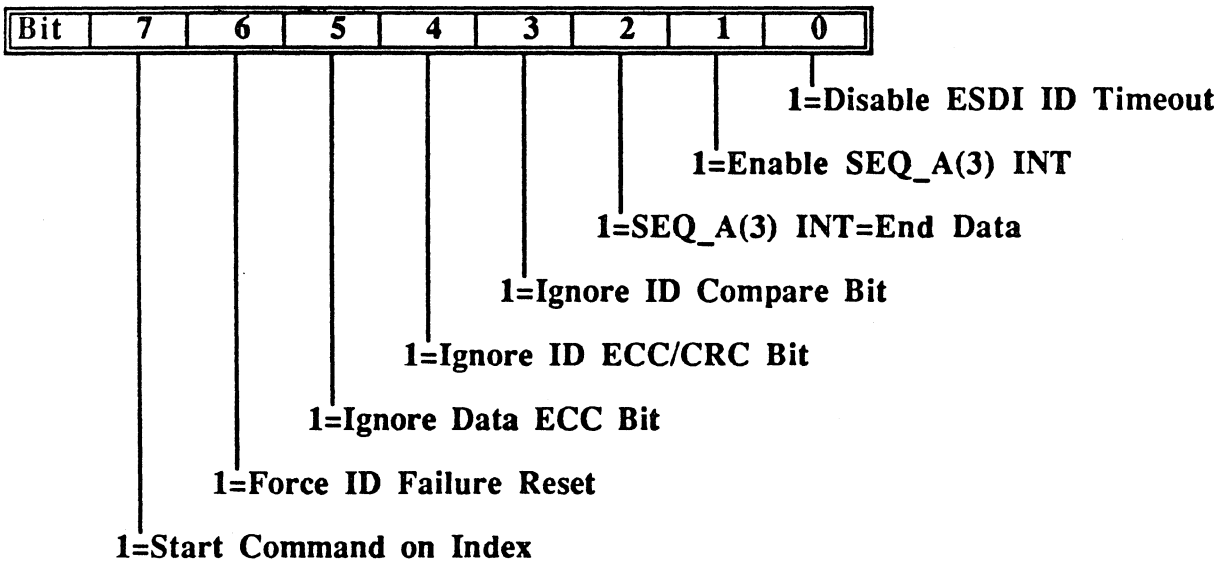
Bit	7	6	5	4	3	2	1	0
Byte	Channel 1 0X-FXh				Channel 0 X0-XFh			

Bits 0-3 select the memory (RAM buffer) bank for Channel 0; bits 4-7 select the memory bank for Channel 1.

Note: These bits are actually used as Address bits 16-19 in DRAM mode to provide 20-bit addressing; that is, addresses 0-15 are input via registers WR00 and WR01 (Channel 0) or WR04 and WR05 (Channel 1) and are incremented by internal counters, while addresses 16-19 (called "Bank Selects") are input by writing to WR33 and are not automatically incremented. These additional bits (16-19) allow addressing of DRAMs greater than 64K, and they are irrelevant unless the user has more than 64K of memory and DRAM mode is used.

See Appendix C for DRAM configurations and pin out.

Write Register 34 (22h)--Optional Control



BIT 0 = ID Timeout Control

Setting this bit =1 will disable the ESDI ID 256 RD_REF_CLK ID timeout.

BIT 1 = Sector Interrupt Control

This bit enables an interrupt (INT SEQ) when SEQA3 goes from 0 to 1 or 1 to 0 as discussed below. If set=1, enable interrupt (SEQA3). If set=0, disable interrupt (SEQA3).

BIT 2 = Sector Interrupt Enable

If this bit is set=0 (and bit 1 is set=1), an interrupt occurs when SEQA3 goes from 0 to 1; i.e., on State 8. This indicates the beginning of the Data Segment. If this bit is set=1 (and bit 1 is set=1), then an interrupt occurs when SEQA3 goes from 1 to 0, thus indicating, in normal operation the end of the Data Segment in a multi-sector operation.

BITS 3-5 = Ignore Error Control

Bits 3, 4, and 5 allow the firmware to override some of the embedded control logic. Respectively, these bits allow ignoring of the ID Compare, ID CRC/ECC, and Data CRC/ECC bits. Bit 3=Ignore ID Compare, bit 4= Ignore ID CRC/ECC, and bit 5=Ignore Data CRC/ECC.

With bit 3 set=1, the firmware can read or write the first sector that it encounters with valid Sync and CRC/ECC fields.

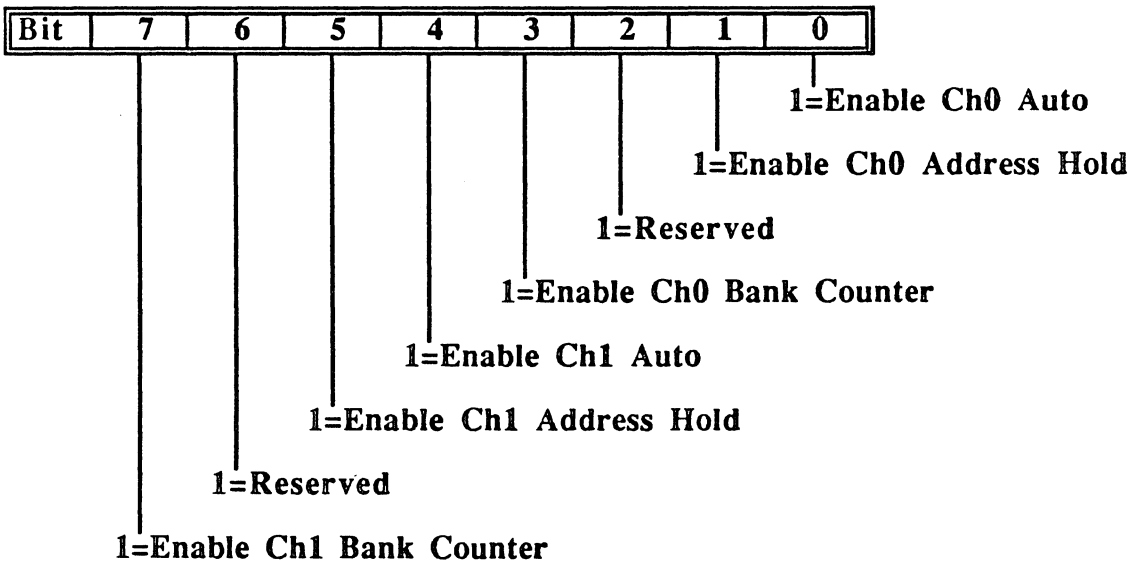
BIT 6 = ID Failure Control

With bit 6 set=1, the sequencer behaves as if an ID failure has occurred; therefore it does not process the data in the sector.

BIT 7 = Start On Index Control

With bit 7 set=1, the sequencer will not start any command until the leading edge of INDEX. **This option may be useful in a CHECK TRACK FORMAT Command.**

Write Register 35 (23h)--Additional DMA Control



The Additional DMA Control Register is cleared at Power-on or an PC-AT Reset to provide backward compatibility with the CHIPS 5055B device. This register is used to enable new features in both DMA Channel 0 and 1 for greater flexibility and higher performance.

BIT 0 and 4 = Enable Auto Channel

Setting bit 0=1 for Channel 0 or bit 4=1 for Channel 1 enables the respective channel to continue operation after the Transfer Count has expired. This option is useful for a multi-sectored operation. If the interrupt for the appropriate channel is enabled, an interrupt will be generated after the last transfer from that channel has occurred but, the channel will remain enabled and further transfers will occur. It is the responsibility of the firmware to re-issue a command to the interrupting channel to clear the interrupt so firmware can maintain sector interlock.

BIT 1 and 5 = Enable Channel Address Hold Register

Setting bit 1=1 for Channel 0 or bit 5=1 for Channel 1 enables the respective channel Address Holding Register. This option is useful for a non-contiguous buffer data with a multi-sectored operation. If the firmware updates either the low or high address register for a channel, when the transfer count has expired for that channel, the new updated address will be used as a reference for the next sector's buffer address. If the Low or High Address Registers are not updated while a transfer is in progress, the next sector's address will only be incremented from the previous sector's last byte transferred address.

BIT 2 and 6 = Reserved

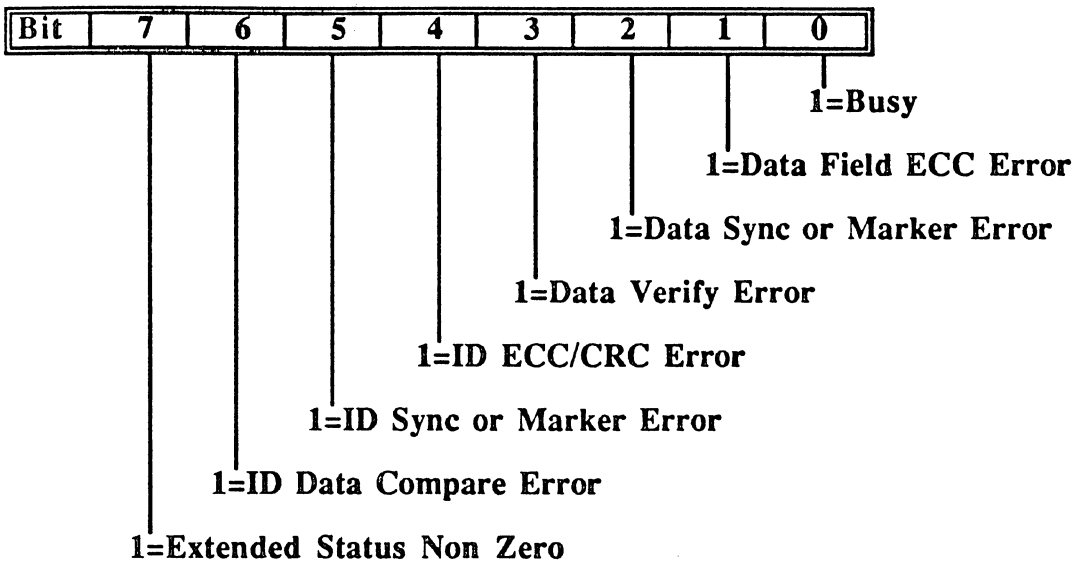
Bits 2 and 6 are reserved and must be loaded with a 0.

BIT 3 and 7 = Bank Address Control

Setting bit 3=1 for Channel 0 or bit 7=1 for Channel 1 enables the respective channel bank address as a counter and not just a holding register. If this bit is set, the bank address will increment as the lower 16 bit address counter increments from FFFFh to 0000h.

2.2 Read Registers

Read Register 16 (10h)--Sequencer Status



This register contains sequencer status information. It is read at the completion of every command to determine whether execution was successful. During command execution it may be read by the microprocessor to examine specific status information on a sector-by-sector, real-time basis. For example, when a timeout has occurred, the microprocessor can determine whether or not an ID was read successfully (even though the ID did not compare); or whether any IDs were read successfully. If it is determined an ID was not read successfully it means the disk may be improperly formatted or incompatible with the controller.

BIT 0 = Busy

Bit 0 is set=1 when a command is in progress. It is cleared when the sequencer is inactive.

BIT 1 = Data ECC

Bit 1 is set=1 during read operations when the sequencer detects a CRC/ECC error in the data field.

BIT 2 = Data Sync

Bit 2 is set=1 in External Sync mode when the Address Mark is detected (AMF is true) but the byte value of either the Sync Field or the Address Mark Field, as read from the disk, does not compare with the value in the format RAM. This applies to a read operation on the Data Segment.

BIT 3 = Data Verify

Bit 3 is set=1 when an error is detected during any VERIFY command.

BIT 4 = ID ECC/CRC

Bit 4 is set=1 when the CRC/ECC bits in the ID Field do not match those generated by the CRC/ECC generator.

BIT 5 = ID Sync

Bit 5 is set=1 during execution of read/write operations if the sector's ID Sync and/or ID Address Mark were in error. The number of disk revolutions that may occur before this bit is set is determined by the value of Index Timeout (WR18).

BIT 6 = ID Compare

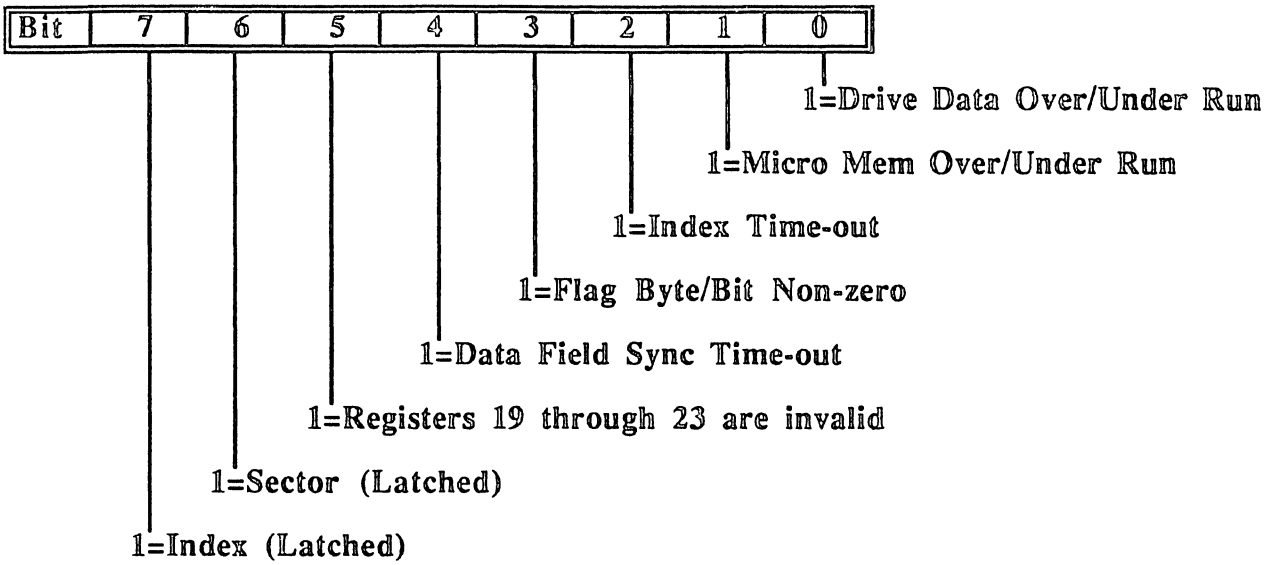
Bit 6 is set=1 when the sequencer detects that the 4-byte ID Header does not correspond to the contents of WR20 to WR23. Bit 6 is cleared when a matching ID Header is found.

BIT 7 = Extended Non-Zero

Bit 7 is set=1 whenever specific bits in the Extended Status Register (RR17) are set.

When any command other than ABORT is issued to the sequencer, RR16 is preset. Refer to Table 3-5, Status Registers.

Read Register 17 (11h)--Extended Status



The Extended Status Register contains additional sequencer status information regarding command execution.

BIT 0 = Over/Under Run 0

Bit 0 is set=1 when DMA Channel 0 does not respond within one byte time with acknowledge (ACK0) to a data sequencer request (REQ0) for a data transfer. If memory parity is enabled (bit 4 of WR27 is set), see note under bit 1 below.

BIT 1 = Over/Under Run 1

Bit 1 is set=1 whenever DMA Channel 0 does not respond after the microprocessor reads RR24 or writes WR24.

Note: If memory parity is enabled (bit 4 of WR27 is set), then the functions of bit 0 and 1 in RR17 (Drive Data Over/Under Run and Micro Memory Over/Under Run) will be OR'd in bit 0 of RR17, and bit 1 of RR17 will be used to indicate a parity error.

BIT 2 = Index Timeout

Bit 2 is set=1 because of an index time-out function. This occurs when a valid ID has not been detected within the programmable number of revolutions.

BIT 3 = Flag Non-Zero

Bit 3 is set=1 on a read or write command after the sequencer has found the proper ID but there is non-zero flag information in the Head/Flag Byte or the Flag Byte.

BIT 4 = Data Sync Timeout

Bit 4 is set=1 on a read command if the sequencer finds the proper ID but the Data Sync Field has not been detected after 512 or 32 bit times (choice determined by bit 6 or WR10)--assuming Data Sync Field Timeout has been enabled (bit 7 of WR28 is set).

BIT 5 = ID Register Valid

Bit 5 is initially set=1 by any command to the sequencer but is cleared (set=0) after the sequencer has processed any valid ID and RR19-RR23 have a valid ID stored. If this bit is cleared (set=0) after an Index timeout, RR19-RR23 hold the last valid ID processed.

BIT 6 = Sector

Bit 6 is a means for the microprocessor to poll a SECTOR/AMF pulse from the disk. **This bit is latched so that a narrow pulse from the disk may be captured.**

BIT 7 = Index

Bit 7 is a means for the microprocessor to poll for an INDEX pulse from the disk. **This bit is latched so that a narrow pulse from the disk may be captured.**

When any command is issued to the Sequencer, RR16 and RR17 are preset as follows:

Table 3-5. Status Registers

STATUS REGISTER

BIT VALUE	NAME	BIT
0	Busy	1
1	Data ECC Error	0
2	Data Sync + Marker Error	0
3	Data Verify Error	0
4	ID ECC/CRC Error	1
5	ID Sync + Marker Error	1
6	ID Compare Error	1
7	Extended Status Non Zero	X

Note: X - Indicates an OR Condition from specific extended status bits.

Table 3-6. Extended Status Registers

EXTENDED STATUS REGISTER BIT

BIT 7	NAME	BIT VALUE	OR STATUS BIT
0	Disk Data Over/Under-run	X	YES
1	Micro Memory Over/Under-run	X	YES
2	Index Time-out	0	YES
3	Flag Bit/Byte Non Zero	X	YES
4	Data Field Sync Time-out	0	YES
5	Invalid ID	1	NO
6	Sector	X	NO
7	Index	X	NO

Notes: YES - Indicates that it is an OR condition for RR16 status bit 7.
X- Indicates that a previous setting remains.

Read Register 18 (12h)--Sequencer State/Retry Count

Bit	7	6	5	4	3	2	1	0
Byte	0X-FXh=Sequencer State				X0-XFh=Retry Count			

BITS 0-3 = Retry Count

Bits 0 through 3 contain the number of disk revolutions counted to find a requested sector on a read or write type command.

BITS 4-7 = Sequencer State

Bits 4-7 of this register contain the real-time state number of the sequencer. This number ranges from 0 to 15, and as noted earlier, **it is also the address of the format RAM.** This information is useful for synchronizing the microprocessor firmware to the sequencer. **Note: It is necessary to de-bounce this data, since the internal state machine runs asynchronously to the microprocessor.**

Read Register 19 (13h)--Flag Byte (ID Byte 4)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh=Flag Byte							

This register contains the fifth byte of ID Header information read from the disk in real time. If the format of the disk does not use five bytes of ID Header, then this register will not contain any valid information. If the sequencer is configured in Flag Byte mode (bit 2 of WR29 is set) and the Flag Byte/Nibble bit in the Extended Status Register is set (bit 3 of RR17), then this register will contain the flag information.

Read Register 20 through 23 (14h-17h)--ID Header

These four registers contain the current ID Header bytes read from the disk. They are updated for every sector that has a valid ID Sync Byte-- regardless of the results of checking the ID CRC/ECC bits. RR20 is the first ID Header Byte; RR23 is the fourth. If the sequencer is configured in Head/Flag mode (bit 2 of WR29 is cleared), then the high nibble of RR22 will contain the flag information; otherwise, the flag information will be contained in RR19 as noted above.

Read Register 20 (14h)--CYLINDER HIGH (ID BYTE 0)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Read Register 21 (15h)--CYLINDER LOW (ID BYTE 1)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Read Register 22 (16h)--Head/Flag Byte (ID BYTE 2)

Bit	7	6	5	4	3	2	1	0
Byte	Flag				Head Address			

If Head/Flag mode has been selected (bit 2 of WR29 is set=0), then Bits 4-7 of this register contain flag information, and bits 3-0 will contain the Head number. If Flag Byte mode has been selected (bit 2 of WR29 is set), then bits 0-7 will contain the Head number, Byte 2 of the ID Header Field.

Read Register 23 (17h)--Sector Number (ID BYTE 3)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Read Register 24 (18h)--Memory to Micro/Peripheral

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is used to transfer data from the RAM buffer to the microprocessor or to a peripheral device on the microprocessor bus.

RAM Buffer to Microprocessor Transfers

When the microprocessor reads RR24, the data in the register is transferred to the microprocessor. The sequencer then does a Channel 0 DMA request (REQ0) in preparation for the next microprocessor request.

Note: Before beginning a RAM buffer read sequence, it is necessary to configure DMA Channel 0 to be in read memory/write peripheral mode. Also, the microprocessor should discard the first read of RR24, as it will contain old information. If the DMA does not respond to the Channel 0 request (REQ0), the Micro Memory Over/Under Run bit in the Extended Status Register (bit 1 of RR17) will be set along with the Extended Status Non-Zero bit in the Sequencer Status Register (bit 7 or RR16).

RAM Buffer to Peripheral Transfer

The sequencer can also transfer data from the RAM buffer to a peripheral device that is connected to the microprocessor address/data bus (AD0-7). To transfer from the RAM buffer to the peripheral, the microprocessor reads RR11. **Note: As above, DMA Channel 0 must be initialized before starting the transfer. Also, the first transfer will contain old information and so should be discarded.**

When the microprocessor reads RR11, the sequencer generates the write strobe signal -GRPWRT for writing the data from the RR24 into the peripheral device. On the trailing edge of the strobe, a Channel 0 DMA cycle is initiated, using REQ0 and ACK0 to read the next RAM buffer location into RR24 in preparation for the next transfer.

An alternative is to first read RR24, which causes a request for new data but does not strobe data into the peripheral; thus data does not have to be discarded.

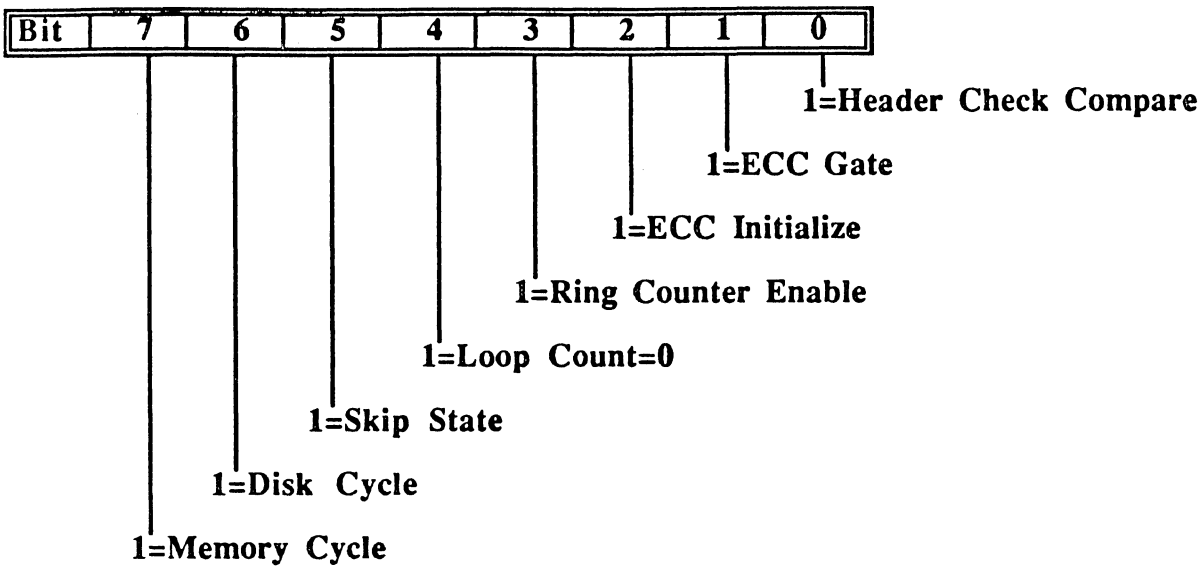
Read Register 25 (19h)--Sequencer Loop Count

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the real-time value of the Sequencer Loop Count, which is initially set to the number of sectors to be read or written--or in the case of a format-type command, to the number of sectors on the disk--and then is decremented each time the sequencer goes from the Sequencer Loop State to the Restart State.

This information is valuable for synchronization of the microprocessor and the sequencer in commands that involve more than one sector. **Note: It is necessary to debounce this data since the internal state machine runs asynchronously to the microprocessor.**

Read Register 26 (1Ah)--Test Register



This register allows access to various internal signals for test purposes.

Read Register 27 (1Bh)--Force INDEX

Bit	7	6	5	4	3	2	1	0
Byte	XXh							

Whenever the microprocessor reads this register an internal INDEX signal is generated with the same timing as the -IORD input signal.

Note: There is no information provided to the microprocessor by reading this register.

Read Register 28 (1Ch)--Force Sequencer Reset

Bit	7	6	5	4	3	2	1	0
Byte	XXh							

Whenever the microprocessor reads this register an internal RESET signal is generated with the same timing as the -IORD input signal. This function is useful for the firmware to ABORT the sequencer and preserve the status and loop-count information.

Note: There is no information provided to the microprocessor by reading this register.

Read Register 30 (1Eh)--Value Register @ Sequencer Start

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register returns the Value Byte in the format RAM as indexed by WR25.

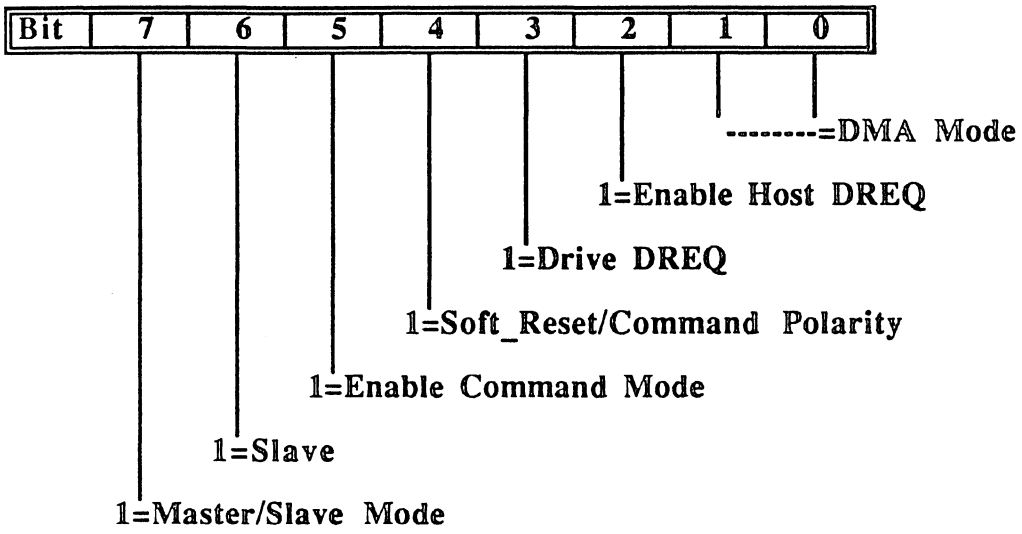
Read Register 31 (1Fh)--Count Register @ Sequencer Start

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register returns the Count Byte in the format RAM as indexed by WR25.

3.1 PC-AT Interface Write Registers

Write Register 64 (40h)--master/slave Control Register



This register programs the master/slave and DMA mode. It is set to 0 at POWER-ON RESET or writing bit 2 of Host Write Register -CS_(1) with A_(2:0) equal to 6 with a 1. These bits are defined as follows:

BITS 0-1 = Host DMA Mode

These bits define the DMA mode. The DMA modes are defined as:

BIT	1	0	DMA Mode of Transfer
	0	0	DMA, Demand
	0	1	DMA, Single/Block
	1	0	Reserved
	1	1	Group Read/Write

The DMA mode defined is recommended when using a 8237 DMA controller or equivalent.

BIT 2 = Enable Host DREQ

Writing a 1 to this bit will allow the host to enable the DREQ signal. Writing a 0 to this signal disables the host's access to the DREQ signal.

BIT 3 = Enable Drive Host DREQ

Writing a 1 to this bit will cause the 82C5059 to drive the DREQ signal. Writing a 0 to this bit will tri-state the DREQ signal.

BIT 4 = Soft_Reset/Command Polarity

Writing a 1 to this bit configures the polarity of the RESET_CMD output signal to be active low. Writing a 0 to this bit configures the polarity of the RESET_CMD output signal to be active high.

BIT 5 = Enable Command Mode

Writing a 1 to this bit configures the the RESET_CMD output signal to be asserted when a command is issued by the host to this device. Writing a 0 to this bit configures the the RESET_CMD output signal to be asserted when a the host issues a soft reset to this device

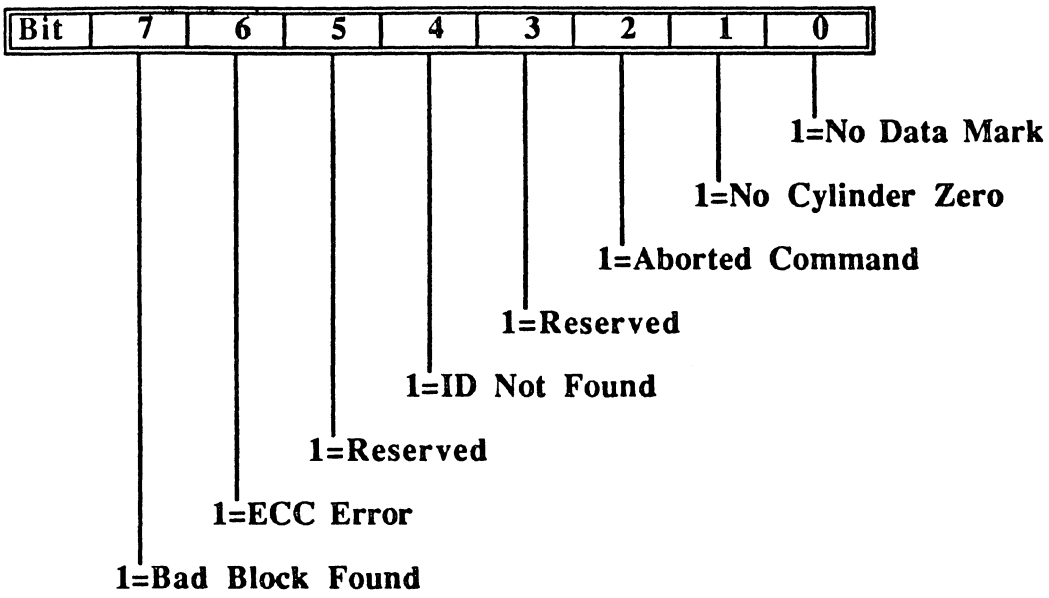
BIT 6 = Enable Slave

Writing a 1 to this bit will cause the 82C5059 to be a slave controller. A slave is only selected when bit 4 of Host Write Register -CS_(0) with A_(2:0) equal to 6 is a 1. Writing a 0 to this bit causes the 82C5059 to be a master. A master is only selected when bit 4 of Host Write Register -CS_(0) with A_(2:0) equal to 6 is a 0. This bit has no effect if the master/slave mode is not enabled.

BIT 7 = Enable Master/Slave Mode

Writing a 1 to this bit will cause the 82C5059 to enter the master/slave mode. Writing a 0 to this bit causes the normal operating mode. In this case, bit 6 has no effect.

Write Register 65 (41h)--Error Register



BIT 0 = No Data Mark

Setting bit 0=1 indicates the controller was able to locate the desired Sector's ID but, was unable to locate the Data Mark for that sector.

BIT 1 = No Cylinder Zero

Setting bit 1=1, indicates that during a Recalibration Command or if retries are enabled, No Cylinder 0 status from the drive was detected. This error occurs after the controller issues 2048 step pulsed toward the Cylinder 0 and the selected drive does not respond with the Track 0 Status Signal.

BIT 2 = Aborted Command

Setting bit 2=1, indicates that the current command issued by the host has been aborted due to an undefined Command Opcode, or a Write Fault/Not Ready condition exists on the selected drive.

BIT 3 = Reserved

Bit 3 is reserved and must not be set to 1.

BIT 4 = ID Not Found

Setting bit 4=1 indicates the controller was able to locate the desired Cylinder and Head number but, was unable to locate the correct Sectors ID. An ID CRC error can also generate this error condition.

BIT 5 = Reserved

Bit 5 is reserved and must not be set to 1.

BIT 6 = ECC Error

Setting bit 6=1, indicates a non-zero syndrome was detected in the desired sector data field. If the data was corrected by ECC, bit 2 of the Status Register will also be set and the command will continue if more sectors are specified. If the data error was NOT corrected by ECC, bit 0 of the Status Register will be set and the command terminated.

BIT 7 = Bad Block Found

Setting bit 7=1, indicates the specified track has previously been formatted with the Bad Track flag set in the ID field. It is not possible to access data on this track and the command will terminate.

Write Register 66 (42h)--Sector Count Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is written with the number of sectors processed by the controller. It is read by the host only after a command has been executed by the controller.

Write Register 67 (43h)--Sector Number Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is written with the sector number that has an error by the controller. It is read by the host only after a command has been executed by the controller.

Write Register 68 (44h)--Cylinder Low Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

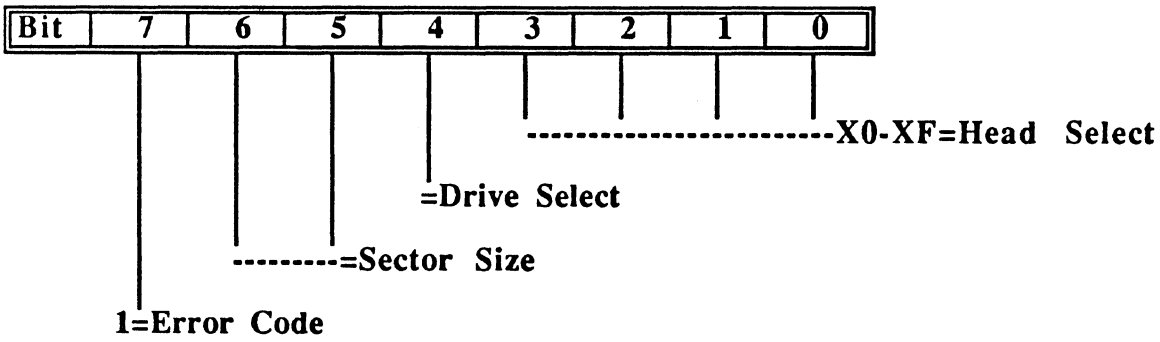
This register is written with the least significant cylinder number that has an error by the controller. It is read by the host only after a command has been executed by the controller.

Write Register 69 (45h)--Cylinder High Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is written with the most significant cylinder number that has an error by the controller. It is read by the host only after a command has been executed by the controller.

Write Register 70 (46h)--Size/Drive/Head Register



This register is written with the size, drive and head that has an error by the controller. It is read by the host only after a command has been executed by the controller. It is set to 0 at POWER-ON RESET or writing bit 2 of Host Write Register -CS_(1) with A_(2:0) equal to 6 with a 1. The bits of this register are defined as the following:

BITS 0-3 = Head Select

These four bits indicate which head has the error condition.

BIT 4 = Drive Select

This bit indicates the selected drive. If this bit is set to 0, drive zero is selected. If this bit is set to 1, drive one is selected.

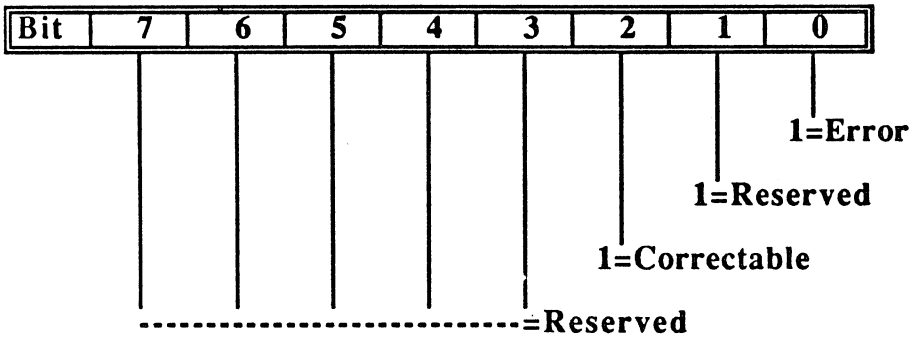
BITS 5-6 = Sector Size

These bits select the sector size. For each combination of these bits Write Register 6 and 7 define the sector size.

BIT 7 = Error Code

This bit indicates the error code selected. If this bit is set to 1, the data field will be appended with an ECC Field. If this bit is set to 0, the data field will be appended with a CRC Field.

Write Register 71 (47h)--Status Register



BIT 0 = Error

Setting bit 0=1, indicates that an error has occurred. Writing this bit with a 1 will set bit 0 of Host Read Register -CS_(0) with A_(2:0) equal to 7. Writing a 0 to this bit will clear bit 2 of Host Read Register -CS_(0) with A_(2:0) equal to 7. This device will clear this bit to a 0 when the host writes to register -CS_(0) with A_(2:0) equal to 7.

BIT 2 = Correctable

Setting bit 2=1, indicates that ECC was applied to the data field. Writing this bit with a 1 will set bit 2 of Host Read Register -CS_(0) with A_(2:0) equal to 7. Writing a 0 to this bit will clear bit 2 of Host Write Register -CS_(0) with A_(2:0) equal to 7. This device will clear this bit to a 0 when the host writes to register -CS_(0) with A_(2:0) equal to 7.

BITS 1 & 3 -7 = Reserved

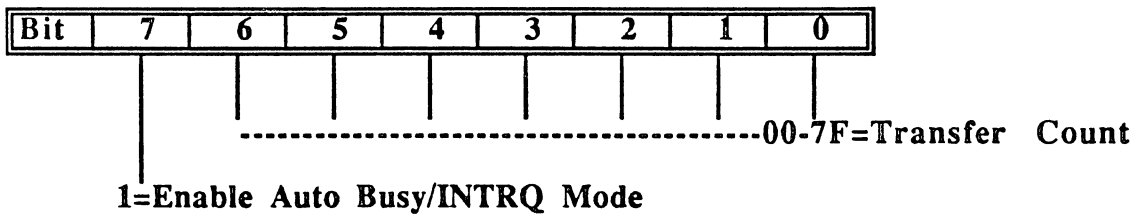
Bits 1 and 3 through 7 are reserved and must not be set to 1.

Write Register 72 (48h)--Busy Command Compare Register

Bit	7	6	5	4	3	2	1	0
Byte	X0h-XFh & 0Xh-FXh							

This register is written by the controller and is used to allow for two commands that will not cause the 82C5059 to indicate BUSY status. It is organized into two nibbles. Bits (7:4) represent the first command, bits (3:0) represent the second. These nibbles correspond to bits (7:4) of Host Register -CS_(0) with A_(2:0) equal to 7. This register must be initialized prior to writing a command to the 82C5059.

Write Register 73 (49h)--



This register is written with the number of concurrent sectors to be transferred to the host in a multi-sectored operation without any firmware intervention required.

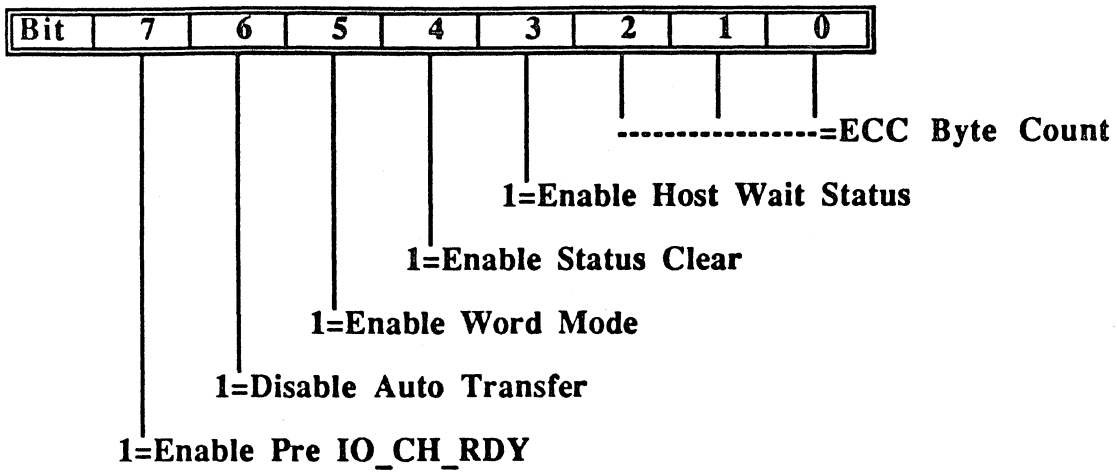
BITS 0-6 = Block Transfer Count

These seven bits determine the total sectors to be transferred to the host per INTRQ.

BIT 7 = Enable Auto Busy/INTRQ Mode

Writing a 1 to this bit will cause the 82C5059 to automatically set INTRQ and clear BUSY when data is ready to be transferred to or from the host. Writing a 0 to this bit will leave this function to the microcomputer.

Write Register 74 (4Ah)--Internal Control Register



This register is written by the controller and is used to control the internal operations of the 82C5059. It is set to 0 at POWER-ON RESET or writing bit 2 of Host Write Register -CS_(1) with A_(2:0) equal to 6 with a 1. The bits are defined as follows:

BITS 0-2 = ECC Byte Count

These bits define the number of ECC bytes to transfer. The counts for the ECC Field transfer are defined as:

BIT	2	1	0	Bytes of ECC Transfer
	0	0	0	One Byte
	0	0	1	Two Bytes
	0	1	0	Three Bytes
	0	1	1	Four Bytes
	1	0	0	Five Bytes
	1	0	1	Six Bytes
	1	1	0	Seven Bytes
	1	1	1	Eight Bytes

BIT 3 = Enable Wait Host Status

Writing a 1 to this bit will cause the 82C5059 to wait for the Host to read the Status Register -CS_(0) with A_(2:0) equal to 7 before starting another data phase. Writing a 0 to this bit causes the 82C5059 to Not wait for a Status Read. In this case, the Microcomputer should wait for the status read.

BIT 4 = Enable Status Clear

This bit enables or disables the Status Clear function. Writing a 1 to this bit causes the 82C5059 to clear Host Read Register -CS_(0) with A_(2:0) equal to 1, Host Read Register -CS_(0) with A_(2:0) equal to 7. Bit 0 and bit 2 signals a Drive Ready and Seek Complete status in Host Read Register -CS_(0) with A_(2:0) equal to 7. Writing a 0 causes the 82C5059 to always display the previous commands status until firmware clears the status.

BIT 5 = Enable Word Mode

This bit enables or disables word (16 bit) data transfers. Writing a 1 to this bit enables word data transfers during read or writes to Host Register -CS_(0) with A_(2:0) equal to 0. Writing a 0 causes byte (8 bit) data transfers during read or writes to Host Register -CS_(0) with A_(2:0) equal to 0. In this case, the -IO_CS_16 signal is disabled.

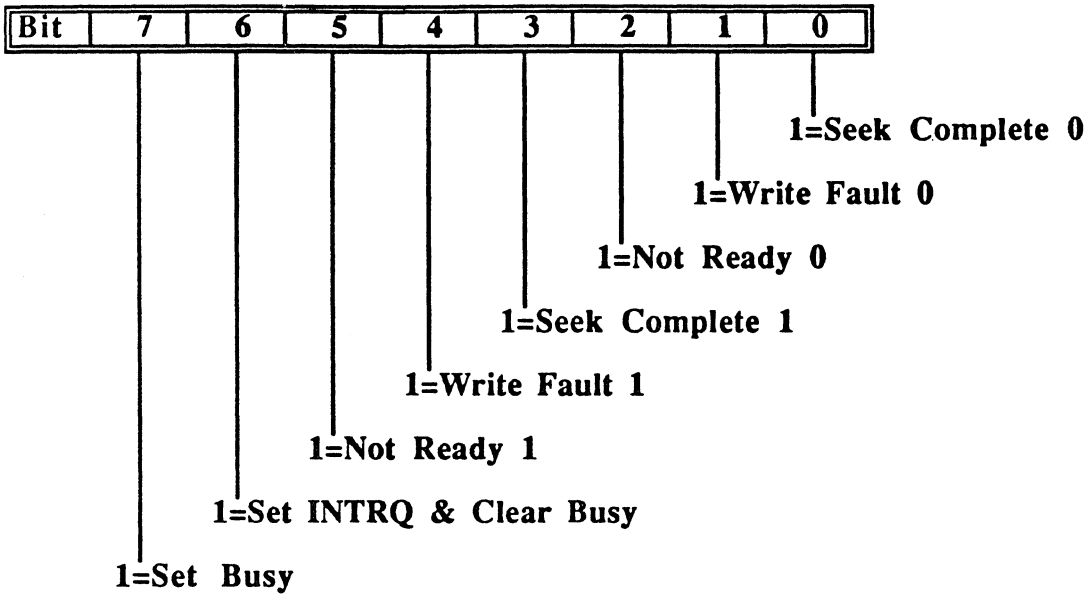
BIT 6 = Disable Auto Transfer

Writing a 1 to this bit will cause the 82C5059 not to enable host data transfers on a Write or Format Command. In this mode, the microcomputer must initiate the first data transfer by writing to WR70. Writing a 0 to this bit will cause the 82C5059 to perform this function automatically. In this case, the 82C5059 will generate a DRQ immediately after receiving a Write or Format Command.

BIT 7= Enable Pre IO_CH_RDY

Writing a 1 to this bit will cause the 82C5059 to de-assert the IO_CH_RDY signal after the -CS_(0) with A_(2:0) equal to 0 is asserted and no data is ready to send to or receive from the host for the number of clock cycles programed in WR72 bits 5-7. Writing a 0 to this bit disables the pre IO_CH_RDY function.

Write Register 75 (4Bh)--Drive Control Register



This register is written by the controller and is used to control both the drive status and the INTRQ and Busy functions. These bits are defined as follows:

BIT 0 = Seek Complete 0

This bit specifies the SEEK COMPLETE status for drive select 0. Writing a 1 to this bit will cause the 82C5059 to indicate SEEK COMPLETE status. Writing a 0 will indicate NO SEEK COMPLETE status. The 82C5059 will set this bit to 1 when the host writes to Register -CS_(0) with A_(2:0) equal to 7 if bit 4 of Host Write Register -CS_(0) with A_(2:0) equal to 6 is a 0.

BIT 1 = Write Fault 0

This bit specifies the WRITE_FAULT status for drive select 0. Writing a 1 to this bit will cause the 82C5059 to indicate WRITE FAULT status. Writing a 0 will signal no WRITE FAULT. The 82C5059 will clear this bit to 0 when the host writes to Register -CS_(0) with A_(2:0) equal to 7 if bit 4 of Host Write Register -CS_(0) with A_(2:0) equal to 6 is a 0.

BIT 2 = Not Ready 0

This bit allows the controller to override the -READY signal for drive select 0. Writing a 1 to this bit will cause the 82C5059 to indicate DRIVE NOT READY status for drive select 0 regardless of the -READY signal. Writing a 0 will allow the -READY signal to indicate DRIVE NOT READY Status. The 82C5059 will clear this bit to 0 when the host writes to Register -CS_(0) with A_(2:0) equal to 7 if bit 4 of Host Write Register -CS_(0) with A_(2:0) equal to 6 is a 0.

BIT 3 = Seek Complete 1

This bit specifies the SEEK COMPLETE status for drive select 1. Writing a 1 to this bit will cause the 82C5059 to indicate SEEK COMPLETE status. Writing a 0 will indicate NO SEEK COMPLETE status. The 82C5059 will set this bit to 1 when the host writes to Register -CS_(0) with A_(2:0) equal to 7 if bit 4 of Host Write Register -CS_(0) with A_(2:0) equal to 6 is a 1.

BIT 4 = Write Fault 1

This bit specifies the WRITE_FAULT status for drive select 1. Writing a 1 to this bit will cause the 82C5059 to indicate WRITE FAULT status. Writing a 0 will signal NO WRITE FAULT. The 82C5059 will clear this bit to 0 when the host writes to Register -CS_(0) with A_(2:0) equal to 7 if Bit 4 of host Write Register -CS_(0) with A_(2:0) equal to 6 is a 1.

BIT 5 = Not Ready 1

This bit allows the controller to override the -READY signal for drive select 1. Writing a 1 to this bit will cause the 82C5059 to indicate DRIVE NOT READY status for drive select 0 regardless of the -READY signal. Writing a 0 will allow the -READY signal to indicate DRIVE NOT READY Status. The 82C5059 will clear this bit to 0 when the host writes to Register -CS_(0) with A_(2:0) equal to 7 if bit 4 of host Write Register -CS_(0) with A_(2:0) equal to 6 is a 1.

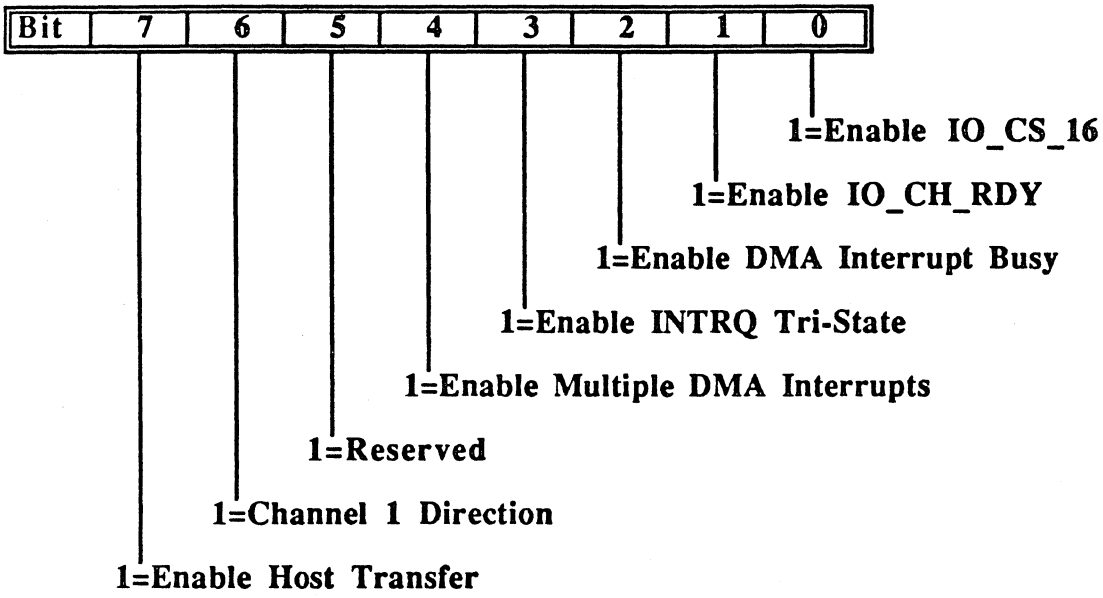
BIT 6 = Set INTRQ & Clear Busy

Writing a 1 to this bit sets the host signal INTRQ and clears the host status BUSY. Writing a 0 to this bit has no effect on the INTRQ or Busy signal.

BIT 7 = Set/Clear Busy

This bit enables or disables the 82C5059 Busy Status on Host writes to Register -CS_(0) with A_(2:0) equal to 7. Writing a 0 to this bit clears Busy. Writing a 1 sets Busy.

Write Register 76 (4Ch)--Host Control Register



This register is written by the controller and is used to control the internal operations of the 82C5059. It is set to 0 at POWER-ON RESET or writing bit 2 of Host Write Register -CS_(1) with A_(2:0) equal to 6 with a 1. The bits are defined as follows:

BIT 0 = Enable -IO_CS_16

This bit enables or disables the assertion of the -IO_CS_16 signal. Writing a 1 to this bit will enable the -IO_CS_16 logic. Writing a 0 to this bit will disable the -IO_CS_16 logic. In this case, the 82C5059 will not assert -IO_CS_16 even if 16 bit data transfers are required. Use caution when disabling -IO_CS_16.

BIT 1 = Enable IO_CH_RDY

This bit enables or disables the de-assertion of the IO_CH_RDY signal. Writing a 1 to this bit will enable the IO_CH_RDY logic. Writing a 0 to this bit will disable the IO_CH_RDY logic. In this case, the 82C5059 will not de-assert IO_CH_RDY even if data is NOT available. Use caution when disabling IO_CH_RDY

BIT 2 = Enable DMA Interrupt Busy

This bit controls if DMA_INTRQ will cause BUSY status. Setting bit 2=1, will enable DMA_INTRQ to cause the 82C5059 BUSY status. Setting bit 2=0, disables the DMA_INTRQ signal. Disabling DMA_INTRQ will not affect the BUSY state.

BIT 3 = Enable INTRQ Tri-State

This bit determines the tri-state function of the INTRQ signal. Writing a 1 to this bit will cause the INTRQ signal to be active only during command execution. The INTRQ signal will tri-state after the last Status Read of the command. If bit (1) of Host Write Register -CS_(1) with A_(2:0) equal to 6 is set to 1, the INTRQ signal will be disabled regardless of the state of this bit. Writing a 0 to this bit will cause the INTRQ signal to operate in the normal mode determined by bit (1) of Host Write Register -CS_(1) with A_(2:0) equal to 6.

BIT 4 = Enable Multiple DMA Interrupts

Writing a 1 to this bit will cause the 82C5059 to assert the INT_DMA (if enabled) but transfers will continue to occur This feature is useful in a multi-sector operation.

BIT 5 = Reserved

This bit is reserved and must be set to 0.

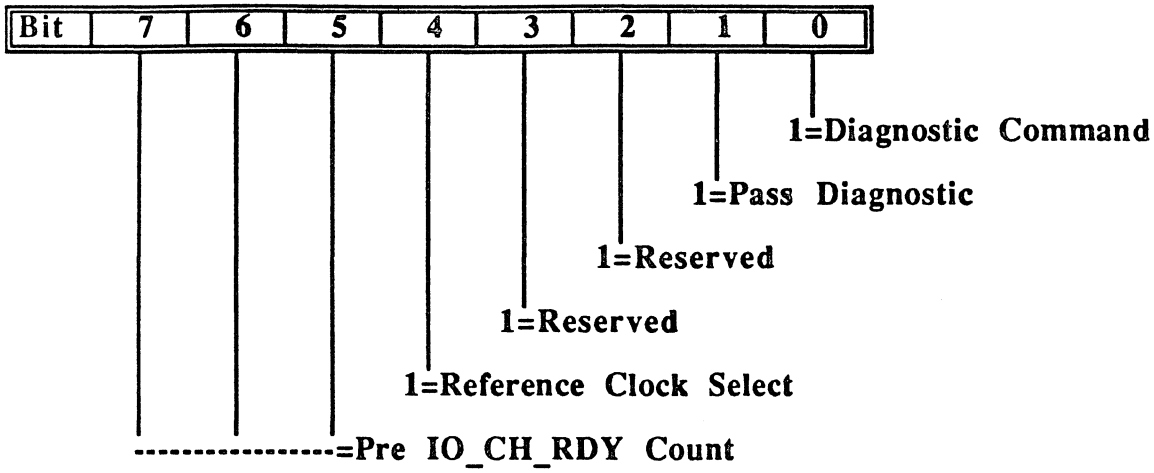
BIT 6 = Channel 1 Direction

This bit determines the direction of data transfers between the controller DMA and the 82C5059. Writing a 1 to this bit will transfer data from the controller DMA RAM to the 82C5059 FIFO. Writing a 0 to this bit will transfer data from the 82C5059 FIFO to the controller DMA RAM.

BIT 7 = Enable Host Transfer

This bit enables data transfers between the 82C5059 and the controller DMA. Writing a 1 to this bit will enable the 82C5059 to issue DMA requests to the controller DMA. When the internal FIFO has 1 byte or word, the DRQ bit will be set in the Host Status Register. At the end of the transfer count, this bit will automatically be reset.

Write Register 77 (4Dh)--Additional Control Register



This register allows control for the drive in diagnostic mode and output signals IO_CH_RDY. It is set to 0 at POWER-ON RESET or writing bit (2) of Host Write Register -CS_(1) with A_(2:0) equal to 6 with a 1. These bits are defined as the following:

BIT 0 = Diagnostic Command

This bit signals that a diagnostic command is in progress. It should be set to a 1 upon decoding a diagnostic command and cleared to 0 at the end of the diagnostic command. This feature is only used in a master/slave configuration.

BIT 1 = Pass Diagnostic

This bit signals that a Slave has passed its diagnostic command. If the 82C5059 is not configured in a master/slave mode, bit 7 of WR40 = 0 or the 82C5059 is configured as a Master, this bit has no function.

BITS 2&3 = Reserved

These bits define the location of the Read/Write Long command bit.

Bit		
0	0	0
1	0	1
2	1	0
3	1	1

BIT 4 = Reference Clock Select

This bit when set to 1 selects the XTAL frequency as a reference for the Pre IO_CH_RDY counter timing. When this bit set to a 0 the XTAL/2 frequency as a reference for the Pre IO_CH_RDY counter timing.

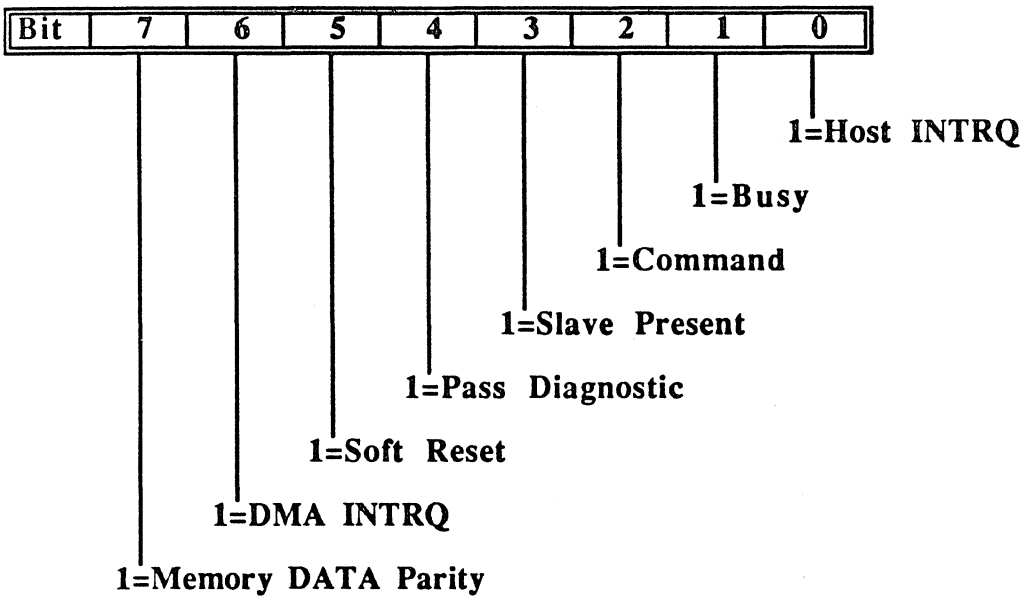
BITS 5-7 = Pre IO_CH_RDY Count

These bits define the number of reference clocks used to hold IO_CH_RDY de-asserted after the assertion of -IO_CS_16. They are set to zero clocks (00) on RESET. The total clocks are defined in the table below:

BIT	7	6	5	Number of Clocks
	0	0	0	Zero Reference Clocks
	0	0	1	One Reference Clocks
	0	1	0	Two Reference Clocks
	0	1	1	Three Reference Clocks
	1	0	0	Four Reference Clocks
	1	0	1	Five Reference Clocks
	1	1	0	Six Reference Clocks
	1	1	1	Seven Reference Clocks

3.2 PC-AT Interface Read Registers

Read Register 64 (40h)-- Interrupt Status Register



BIT 0 = Host INTRQ

This bit contains the status of the host INTRQ status. If this bit is set, INTRQ is asserted. If this bit is cleared, INTRQ is de-asserted.

BIT 1 = Busy

This bit contains the status of the host Busy status. If this bit is set, Busy is asserted. If this bit is cleared, Busy is de-asserted.

BIT 2 = Command

When this status bit is set to 1, a Write to Host Write Register -CS_(0) with A_(2:0) equal to 7 has occurred. This bit is set to 0 by writing the Internal Control Register bit 2 with a 1 or a RESET.

BIT 3 = Slave Present

If the 82C5059 is in the Master mode, this bit is an inverted copy of the -COMMAND input. It is generally used to determine if a Slave drive is present during a diagnostic command.

BIT 4 = Pass Diagnostic

If the 82C5059 is in the Master mode, this bit is an inverted copy of the ~DS_1 input. It is generally used to determine if a slave drive has passed the diagnostic command.

BIT 5 = Soft Reset

When this status bit is set to 1, a Write to Host Write Register-CS_(1) with A_(2:0) equal to 6 bit (2)=1 has occurred. This bit is reset to 0 after reading this register or a RESET_IN.

BIT 6 = DMA Transfer

When this status bit is set to 1 a DMA Interrupt has occurred. This bit is cleared by RESET, a Host Write to -CS_(0) with A_(2:0) equal to >, or a Write to Write Register 76.

BIT 7 = Memory Data Parity

When this status bit is set to 1, a parity error has occurred. This bit is cleared by RESET or after reading this register.

Read Register 65 (41h)--Write Precompensation Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the cylinder at which write precompensation will be applied. The value read must be multiplied by 4 by the firmware. A value of 255 will result in no write precompensation/reduce write current. It is read by the controlier processor only after a command has been written into the Command Register (host).

Read Register 66 (42h)--Sector Count Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the number of sectors to be processed. It is read by the controller processor only after a command has been written into the Command Register (host).

Read Register 67 (43h)--Sector Number Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the starting sector number to be processed. It is read by the controller processor only after a command has been written into the Command Register (host).

Read Register 68 (44h)--Cylinder Low Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

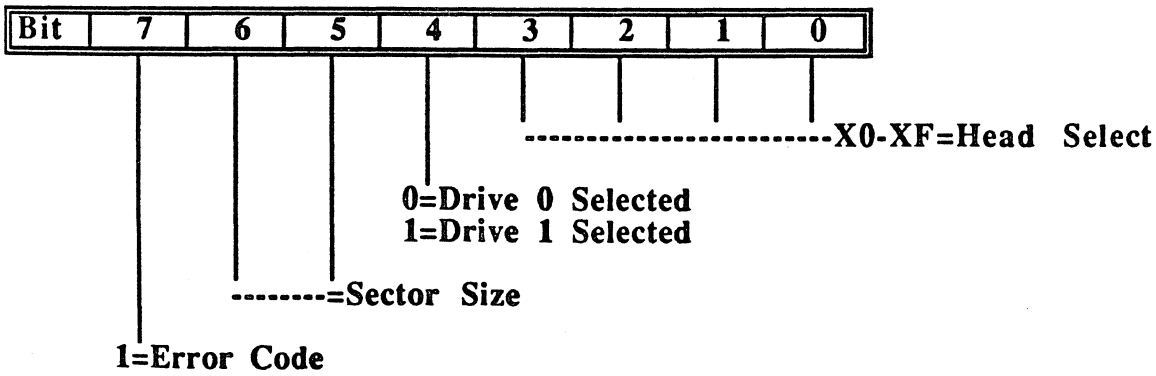
This register contains the starting (least significant byte) cylinder number to be processed. It is read by the controller processor only after a command has been written into the Command Register (host).

Read Register 69 (45h)--Cylinder High Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the starting (most significant byte) cylinder number to be processed. It is read by the controller processor only after a command has been written into the Command Register (host).

Read Register 70 (46h)--Size/Drive/Head Register



This register contains the controller Error Code/Sector Size parameters and the current Drive/Head select. It is read by the controller processor only after a command has been written into the Command Register (host). The bits of this register are defined as the following:

BITS 0-3 = Head Select

These four bits indicate the head to be selected.

BIT 4 = Drive Select

This bit specifies the drive to be selected. If this bit is set to 0, drive 0 is selected. If set to 1, drive 1 is selected.

BITS 5-6 = Sector Size

These bits indicate the sector size to be used as the following table reflects:

BIT	6	5	Sector Size
	0	0	256 Bytes per Sector
	0	1	512 Bytes per Sector
	1	0	1024 Bytes per Sector
	1	1	128 Bytes per Sector

BIT 7 = Drive Select

This bit specifies the error code to be used. If this bit is set to 1, the data field will be appended with an ECC field. If set to 0, the data field will be appended with a CRC field.

Read Register 71 (47h)--Command Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the command to be executed by the controller. It is read only after the -Command signal has been asserted.

2. HOST COMPUTER INTERFACE REGISTERS

The CHIPS 82C5059 contains 9 registers by which the host can communicate with the controller. The register organization described in this document relate to an PC-AT compatible Winchester controller application. However, these registers are general purpose Read/Write Registers and except for some hardware specific bits, can be defined to suit other applications.

Table 3-2 lists the Host Computer Interface Registers. Following these tables is a complete description of these registers.

Table 3-7. Host Computer Interface Registers

Control (Write) Winchester Registers

Write A_(2:0)	Function
-CS_(0) & 0	Data Register (16 bit)
-CS_(0) & 1	Precompensation Register
-CS_(0) & 2	Sector Count Register
-CS_(0) & 3	Sector Number Register
-CS_(0) & 4	Cylinder Low Register
-CS_(0) & 5	Cylinder High Register
-CS_(0) & 6	Size/Drive/Head Register
-CS_(0) & 7	Command Register

Control (Write) Floppy Registers

Write A_(2:0)	Function
-CS_(1) & 6	Host Control Register

Table 3-7 Host Computer Interface Registers (continued)

Status (Read) Winchester Registers

READ A_(2:0)	Function
-CS_(0) & 0	Data Register (16 bit)
-CS_(0) & 1	Error Register
-CS_(0) & 2	Sector Count Register
-CS_(0) & 3	Sector Number Register
-CS_(0) & 4	Cylinder Low Register
-CS_(0) & 5	Cylinder High Register
-CS_(0) & 6	Size/Drive/Head Register
-CS_(0) & 7	Status Register

Control (Read) Floppy Registers

Read A_(2:0)	Function
-CS_(1) & 6	Winchester Secondary Status
-CS_(1) & 7	Head/Select Status

2.1 Host Computer Write Registers

Write Register -CS_(0) & 0--Write Data Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register transfers controller data between the host and the 82C5059. In Word mode, 16 bits of data are transferred requiring -IO_CS_16 to be asserted and possibly de-asserting IO_CH_RDY. In Byte mode, 8 bits of data are transferred leaving-IO_CS_16 de-asserted and IO_CH_RDY asserted.

Write Register -CS_(0) & 1--Write Precompensation Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register determines the cylinder at which write precompensation will be applied. The value written is 1/4 the actual precompensation cylinder. A value of 255 will result in no write precompensation/reduce write current. This register should be written prior to the Command Register being written with a WRITE/FORMAT command. It is set to 32 (128) after a RESET.

Write Register -CS_(0) & 2--Sector Count Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register specifies the number of sectors to be processed. A value of 0 indicates 256 sectors. It should be written prior to the Command Register being written. This register is set to 1 after a RESET.

Write Register -CS_(0) & 3--Sector Number Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register specifies the starting sector number. It should be written prior to the Command Register being written. This register is set to 1 after a RESET.

Write Register -CS_(0) & 4--Cylinder Low Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

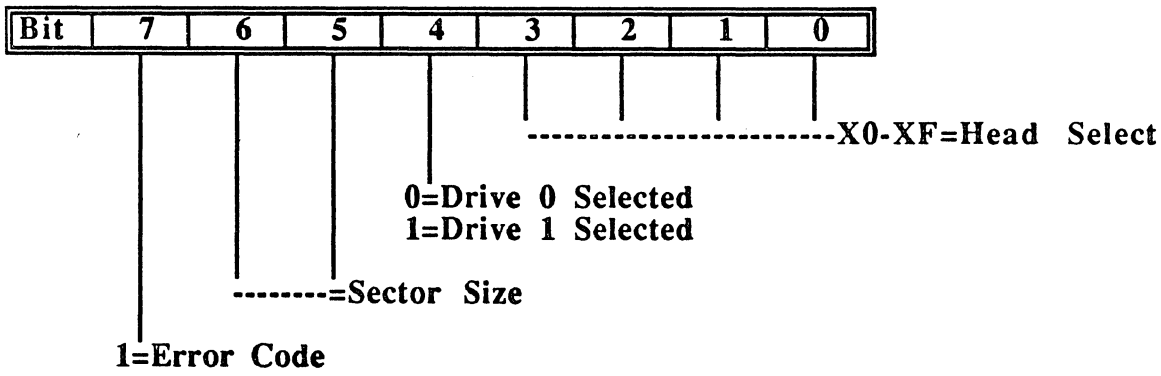
This register specifies the least significant byte of the starting cylinder number. It should be written prior to the Command Register being written. This register is set to 0 after a Reset.

Write Register -CS_(0) & 5--Cylinder High Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register specifies the most significant byte of the starting cylinder number. It should be written prior to the Command Register being written. This register is set to 0 after a Reset.

Write Register -CS_(0) & 6--Size/Drive/Head Register



This register specifies the controller Error Code/Sector Size parameters along with the DRIVE/HEAD select. This register should be written prior to the Command Register being written. It is set to 0 at Power-on Reset or writing bit 2 of Host Write Register -CS_(1) with A_(2:0) equal to 6 with a 1. The bit definitions are:

BITS 0-3 = Head Select

These four bits select the head.

BIT 4 = Drive Select

This bit indicates the selected drive. If this bit is set to a 0, drive zero is selected. If this bit is set to a 1, drive one is selected.

BITS 5-6 = Sector Size

These bits indicate the sector size. The actual sector size is determined with the local microprocessor initializing write registers 6 and 7.

BIT 7 = Error Code

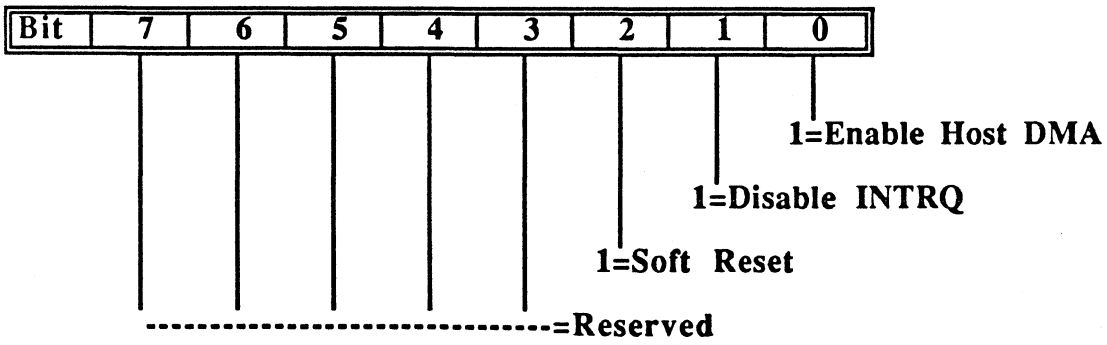
This bit specifies the error code to be selected. If this bit is set, the data field will be appended with an ECC field. If cleared, the data field will be appended with a CRC field.

Write Register -CS_(0) & 7--Command Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register specifies the command to be executed by the controller. It is set to 0 after a Reset. Writing to this register asserts the -Command signal.

Write Register -CS_(1) & 6--Host Control Register



This register allows the host to reset the 82C5059 and enable/disable the INTRQ signal and DREQ (if available). These bits are defined as the following:

BIT 0 = Enable Host DMA

This register has been expanded to include a DMA enable/disable function for Host systems using the 82C5059 DMA mode. The bit definition is as follows:

DMA mode and bit 2 of Microcomputer Write Register XX are set to 1, writing a 1 to this bit will enable the DREQ signal. Writing a 0 to this bit will disable (tri-state) the DREQ signal. If the 82C5059 is not configured in the DMA mode or bit 2 of Microcomputer Write Register is 0 then this bit has no meaning.

BIT 1 = Disable INTRQ

Writing a 0 to this bit enables the 82C5059 INTRQ signal. Writing a 1 to this bit disables (tri-states) the INTRQ signal. Pending interrupts are not affected by tri-stating this signal.

BIT 2 = Soft Reset

Writing a 1 to this bit place the 82C5059 in the BUSY state and resets all internal registers to their reset value. A 0 must be written to this bit for normal operation.

BITS 3-7 = Reserved

Bits 3 to 7 are reserved and must be set to a 0.

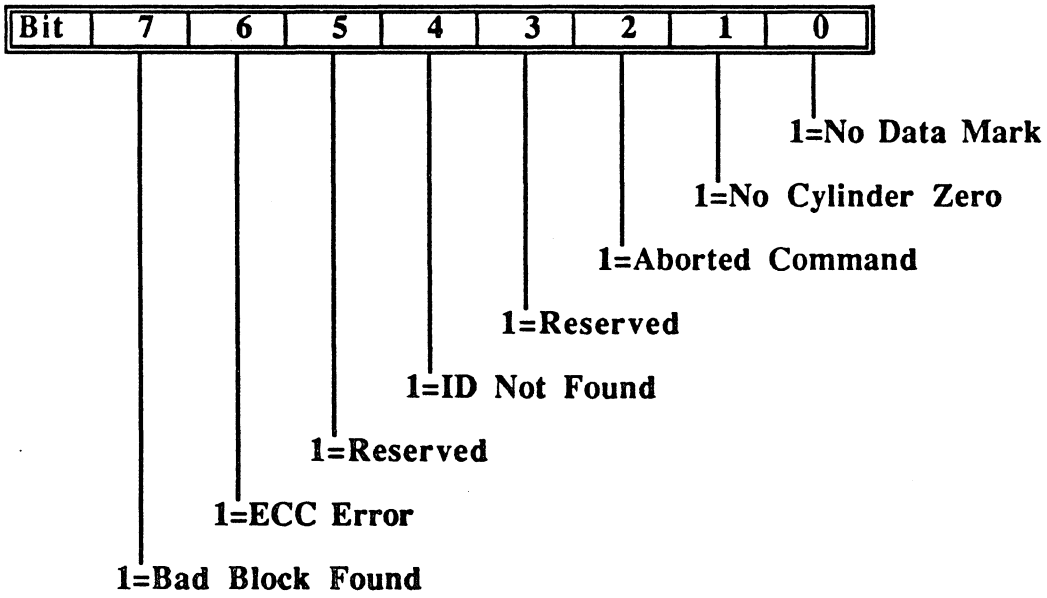
2.2 Host Computer Read Registers

Read Register -CS_(0) & 0--Read Data Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register transfers controller data between the 82C5059 and the host. In Word mode, 16 bits of data are transferred requiring -IO_CS_16 to be asserted and possibly de-asserting IO_CH_RDY. In Byte mode, 8 bits of data are transferred leaving -IO_CS_16 de-asserted and IO_CH_RDY asserted. The 82C5059 allows greater flexibility in controlling -IO_CS_16 and IO_CH_RDY. See Microprocessor Write Register WR63 for programming these signals.

Read Register -CS_(0) & 1--Error Register



This register contains the Error status of the last command executed by the controller. It can only be accessed while the controller is in the Not Busy state. This register is not affected by Reset. These bits are defined as the following:

BIT 0 = No Data Mark

This indicates that the controller was able to locate the sector but was unable to locate the associated data mark.

BIT 1 = No Cylinder Zero

This indicates that during a Recalibration command or if retries are enabled no Cylinder 0 was detected. This error occurs after the controller issues 2048 step pulses toward Cylinder 0 and the selected drive does not respond with the Track 0 signal.

BIT 2 = Aborted Command

The current command issued by the host has been aborted due to an undefined Command Opcode, or a Write Fault/Not Ready condition exist on the selected drive.

BIT 3 = Reserved

Bit 3 is reserved and will be set to 0.

BIT 4 = ID Not Found

This indicates that the controller was able to locate the correct cylinder and head numbers but was unable to locate the correct sector number. An ID CRC error can also generate this error condition.

BIT 5 = Reserved

Bit 5 is reserved and will be a 0.

BIT 6 = ECC Error

This indicates that a non-zero syndrome was detected in a specified data field. If the data error was corrected by ECC, bit 2 of the Status Register will also be set and the command will continue if more sectors are specified. If the data error was **not** corrected by ECC, bit 0 of the Status Register will be set and the command terminated.

BIT 7 = Bad Block Found

This indicates that the specified track has previously been formatted with the Bad Track flag set in the ID field. It is not possible to access data on this track and the command will be terminated.

Read Register -CS_(0) & 2--Sector Count Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the number of sectors to be processed and is decremented as each sector is processed. It can only be accessed while the controller is in the Not Busy state. This register is set to 1 after a Reset.

Read Register -CS_(0) & 3--Sector Number Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the current sector number being processed by the controller. It can only be accessed while the controller is in the Not Busy state. If an error condition exists, this register contains the sector number in error. It is set =1 after a Reset.

Read Register -CS_(0) & 4--Cylinder Low Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the least significant byte of the current cylinder number. It can only be accessed while the controller is in the Not Busy state. If an error condition exists, this register contains the least significant byte of the cylinder number in error. This register is set =0 after a Reset.

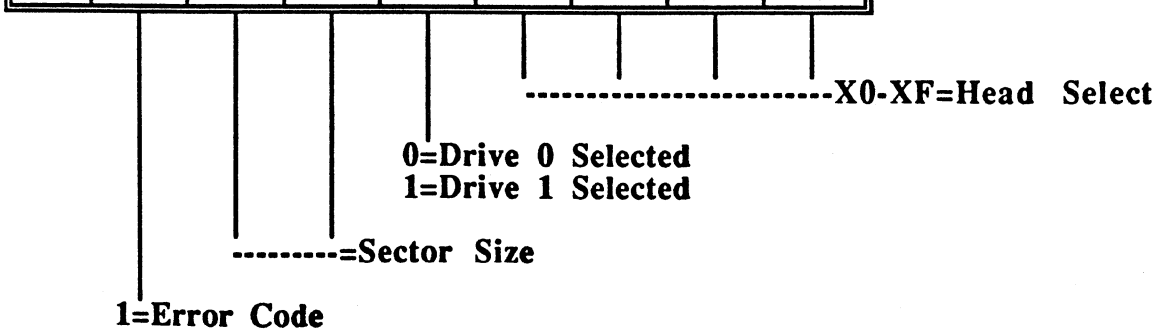
Read Register -CS_(0) & 5--Cylinder High Register

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the most significant byte of the current cylinder number. It can only be accessed while the controller is in the Not Busy state. If an error condition exists, this register contains the most significant byte of the cylinder number in error. This register is set to 0 after a Reset.

Read Register -CS_(0) & 6--Size/Drive/Head Register

Bit	7	6	5	4	3	2	1	0



This register contains the controller Error Code/Sector Size parameters along with the current Drive/Head select. It can only be accessed while the controller is in the Not Busy state. This register is set to 0 after a Reset. These bits are defined as the following:

BITS 0-3 = Head Select

These four bits indicate the selected head.

BIT 4 = Drive Select

This bit reflects the selected drive. If this bit is set to 0, drive 0 is selected. If set to 1, drive 1 is selected.

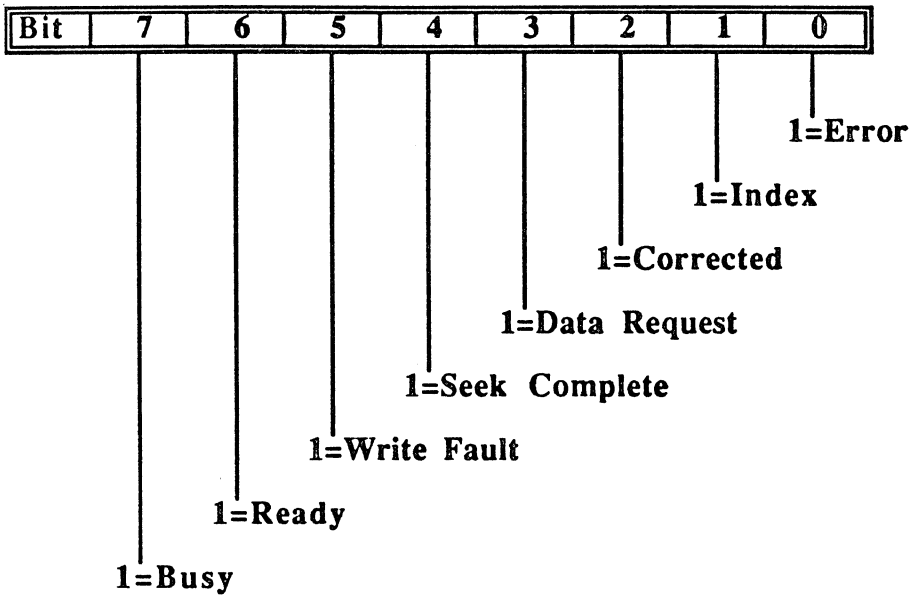
BITS 5-6 = Sector Size

These bits indicate the sector size.

BIT 7 = Error Code

This bit indicates the error code selected. If this bit is set to 1, the data field will be appended with an ECC field. If set to 0, the data field will be appended with a CRC field.

Read Register -CS_(0) & 7--Status Register



This register contains the Controller Drive status. Reading this register de-asserts the INTRQ signal. These bits are defined as follows:

BIT 0 = Error

This bit indicates if an Unrecoverable Error has occurred. If set, an error condition exists and the Status Register must be read to determine the error type.

BIT 1 = Index

This bit is an inverted copy of the -INDEX signal of the selected drive.

BIT 2 = Corrected

This bit indicates if a data error was corrected. If set, an ECC error occurred but was corrected. A corrected ECC error will **not** terminate a multiple sector transfer. If CRC is selected, this bit has no meaning and is set to 0.

BIT 3 = Data Request

This bit indicates that the controller is in a data transfer mode. While this bit is set, the BUSY bit will be cleared and the controller will wait for data to be transferred to or from the host.

BIT 4 = Seek Complete

This bit is a function of WR74 bit 0 or bit 3 based on which drive is selected in the host register -CS_(0) Register 6 bit 4.

BIT 5 = Write Fault

This bit is a function of WR74 bit 1 or bit 4 based on which drive is selected in the host register -CS_(0) Register 6 bit 4.

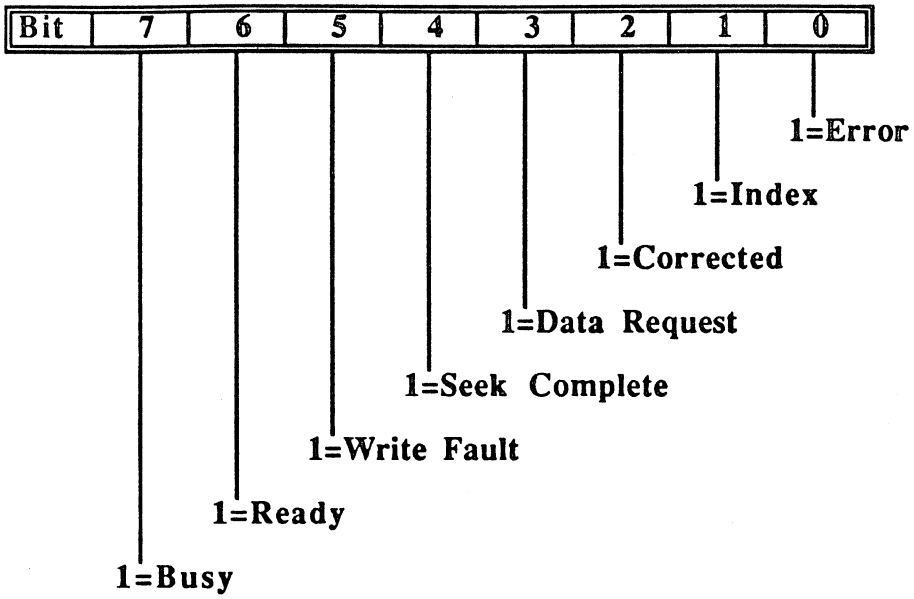
BIT 6 = Ready

This bit is a function of WR74 bit 2 or bit 5 based on which drive is selected in the Host Register -CS_(0) Register 6 bit 4.

BIT 7 = Busy

This bit indicates the state of the controller. If set, the controller is busy executing the specified command and is not in a data transfer state. While set, the Status Register is gated on the bus during any read to the Host Read/Write Registers. Any write to the host Read/Write Registers while this bit is set will be ignored. If cleared, the controller is either in a NOT BUSY or a data transfer state. The DRQ bit will be set if the controller is in the data transfer state.

Read Register -CS_(1) & 6--Winchester Secondary Status Register



This register contains the Controller/Drive status. It is identical to the Status Register at address -CS_(0) with A_(2:0) equal to 7 except that reading this Status Register has no affect on the INTRQ signal. These bits are defined as the following:

BIT 0 = Error

This bit indicates if an unrecoverable error has occurred. If set, an error condition exists and the Status Register must be read to determine the error type.

BIT 1 = Index

This bit is an inverted copy of the -INDEX signal of the selected drive.

BIT 2 = Corrected

This bit indicates if a data transfer was corrected. If set, an ECC error occurred but was corrected. A corrected ECC error will not terminate a multiple sector transfer. If CRC is selected, this bit has no meaning and is set to 0.

BIT 3 = Data Request

This bit indicates that the controller is in a data transfer mode. While this bit is set, the Busy bit will be cleared and the controller will wait for data to be transferred to or from the host.

BIT 4 = Seek Complete

This bit is a function of WR74 bit 0 or bit 3 based on which drive is selected in the Host Register -CS_(0) Register 6 bit 4.

BIT 5 = Write Fault

This bit is a function of WR74 bit 1 or bit 4 based on which drive is selected in the host register -CS_(0) Register 6 bit 4.

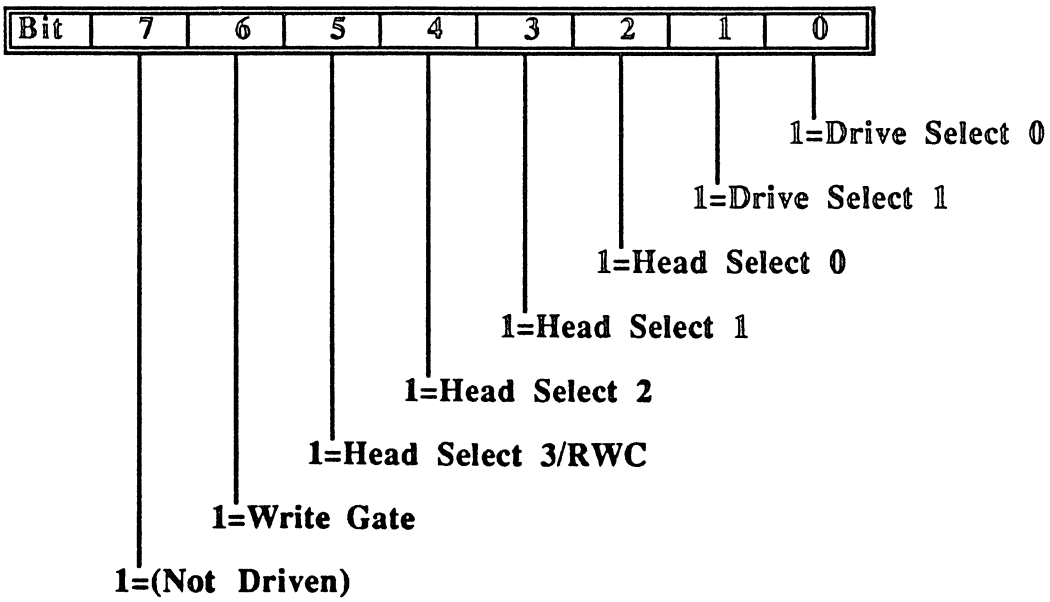
BIT 6 = Ready

This bit is a function of WR74 bit 2 or bit 5 based on which drive is selected in the Host Register -CS_(0) Register 6 bit 4.

BIT 7 = Busy

This bit indicates the state of the controller. If set, the controller is busy executing the specified command and is not in a data transfer state. While set, the Status Register is gated on the bus during any read to the Host Read/Write Registers. Any write to the Host Read/Write Registers while this bit is set will be ignored. If cleared, the controller is either in a NOT BUSY or a data transfer state. The DRQ bit will be set if the controller is in the data transfer state.

Read Register -CS_(1) & 7--Head/Drive Select Status Register



This register contains the Head/Drive Select status. These bits are defined as follows:

BIT 0 = Drive Select 0

This bit indicates the state of Drive Select 0. If set to 0, Drive 0 is selected. If set to 1, Drive 0 is de-selected.

BIT 1 = Drive Select 1

This bit indicates the state of Drive Select 1. If set to 0, Drive 1 is selected. If set to 1, Drive 1 is de-selected.

BIT 2 = Head Select 0

This bit indicates the state of Head Select 0.

BIT 3 = Head Select 1

This bit indicates the state of Head Select 1.

BIT 4 = Head Select 2

This bit indicates the state of Head Select 2.

BIT 5 = Head Select 3/RWC

This bit indicates the state of Head Select 3/RWC.

BIT 6 = Write Gate

This bit indicates the state of the Winchester drive -WRT GATE signal.

BIT 7 = (Not Driven)

This bit is not driven by this device and will always be in a Tri-State condition.

5. FORMAT RAM

The details of the media format for an application depend on the disk drive and some system considerations. The precise definition of the format is required by the 82C5059 both for writing format information on the media and for reading and writing the disk. The 82C5059 provides great flexibility in the definition of the format, supporting a wide variety of drive parameters and system requirements.

Format information is stored in the 82C5059 in an internal RAM viewed as a set of register pairs. Before any commands are issued to access the disk the **parameter RAM** must be loaded by the microprocessor with the format information. The loading must be performed when the controller is initialized, or when the track format is changed.

The parameter RAM is organized as 16 pairs of bytes, each pair consisting of a Value Byte and a Count Byte. The series of byte pairs describes the entire sequence of information recorded on a single track of the drive, beginning at INDEX. For every field on the physical disk track, a corresponding register pair holds the bit pattern for each byte of the field in the Value Byte register--assuming that a certain bit pattern is expected in the bytes of that field--and the length of the field in bytes (i.e., the number of bytes in the field) in the Count Byte Register. Note that only certain fields have expected bit patterns in them; e.g., the ID Sync Field has an expected pattern, the Data Field portion of the data segment does not. As the data sequencer moves from media field to media field, it indexes through the register pairs, using each pair to determine the byte pattern (if applicable) and the number of bytes in each field.

Table 3-6 shows typical register pair values for a soft-sectored MFM ST506 drive using MFM encoding/decoding. **This is intended as an example only.**

See Appendix A for examples of other drive types and formats.

Following the table is a general description of each register pair.

Table 3-8. Example Register Pairs for MFM ST506 Drive

Register Pair	Name	Value	Count	Sequencer State
0	ESDI Sector Gap	00h	01	0
1	Post-Index Gap	4Eh	16	1
2	ID Preamble	00h	13	2
3	ID Sync	A1h	01	3
4	ID Address Mark	FEh	01	4
5	ID Header	00h	04	5
6	ID CRC/ECC	00h	04	6
7	ID Postamble	00h	02	7
8	Data Preamble	00h	13	8
9	Data Sync	A1h	01	9
10	Data Address Mark	F8h	01	A
11	Data Field	E5h	16	B
12	Data CRC/ECC	00h	04	C
13	Data Postamble	00h	02	D
14	Inter-Sector Gap	4Eh	14	E
15	Pre-Index/Sector Gap	4Eh	01	F

Register Pair 0--ESDI Sector Gap

This pair is used only for ESDI type interfaces. It specifies the bit pattern that is expected in the bytes that are placed between sectors, and the number of those bytes.

Register Pair 1--Post-Index Gap

This speed tolerance gap provides space between a write splice (any time WRT GATE is asserted or deasserted) at the end of the track and the first sector's preamble. It also allows for variation in the mechanical detection of the physical drive index. The value used for this field is typically non-zero to prevent confusing it with the Preamble field.

The fields that correspond to the next six register pairs relate to the ID Segment of the disk. They are written once for each sector on a track. The Header portion of the ID Segment contains the Cylinder, Head, and Sector numbers that identify the unique sector.

Register Pair 2--ID Preamble

The ID Preamble field is provided to allow a stream of well controlled data from the disk read channel to be used by the controller PLL to gain frequency and phase synchronization before reading ID data. The Value and Count bytes set for this field are determined by the encoding scheme used and system dynamics. In systems that use MFM encoding, this field generally uses a Value Byte of 00h and a Count Byte of 10-12.

Register Pair 3--ID Sync

For a hard-sectored disk, byte alignment begins with this field. The bytes in this field (usually just one) constitute a bit pattern that enables control circuitry to determine the byte boundaries of the incoming data. The value for this field is normally chosen so that the first bit of this field may be differentiated from the last bit of the preamble. The Count byte for this field is typically 1. Since this field is the first field actively processed by the 82C5059 on read or write commands, its State Number (3) is commonly written to WR25 as the Start State or the Restart State.

For soft-sectored drives, the output pin AM ENABLE is asserted during this field to signal the Encode/Decode circuitry to process Address Mark information. For MFM encoded data, this processing will typically include an illegal (missing) clock scheme used to uniquely define the beginning of ID or Data Segments. For these drives, an illegal MFM pattern of A1h Data/0Ah Clock Byte is very commonly used.

Register Pair 4--ID Address Mark

The ID Address Mark field is required on soft-sectored drives (with the exception of ESDI soft-sectored drives). Its Value is used to differentiate between the ID Segment and the Data Segment. Generally the count is 1.

Register Pair 5--ID Header

The ID Header varies from drive to drive. Its main purpose is to identify or locate the sector within the drive. Typically the Header has two Cylinder Number Bytes, a Head Number Byte, and a Sector Number Byte. The ID Header may also contain flag information for bad track or bad sector recognition.

In the 82C5059, the Header consists of information written into a series of registers by the user firmware. A typical Header consists of four bytes:

Cylinder Address High Byte	(WR20)
Cylinder Address Low Byte	(WR21)
Head Address/Flag Byte	(WR22)
Sector Address Byte	(WR23)

Note: If bit 2 of WR29 is set=0, then only the low nibble of the Head byte is used for the Head Number. The high nibble is then available for flag information. If bit 2 of WR29 is set=1, however, the entire byte contains the Head number, and a fifth byte will contain flag information, which can be read via RR19.

Register Pair 6--ID CRC/ECC

This field contains the CRC or ECC remainder computed for the ID Header if a 1 Field Sync is used (bit 1 of WR29 is cleared), or the ID Address Mark and the ID Header if a 2 Field Sync is used (bit 1 of WR 29 is set). Count should be set to match the polynomial that is used; i.e., Count = 2 for CRC, Count = 6 for 48-bit ECC, etc. The computed CRC or ECC remainder is supplied by the 82C5059 whenever a format-type command writes the ID.

Register Pair 7--ID Postamble

This final field in the sector ID sequence is used to space the beginning of the Data Segment Preamble away from the ID Segment. This allows the write splice from a sector write operation to occur in an area where no recoverable data is present. As was the case for the Post-Index Gap, the Value used for this field is typically non-zero to prevent confusing it with preamble fields.

The fields that correspond to the next six register pairs relate to the Data Segment of the disk. Like the ID Segment, there are Preamble, Sync, Address Mark, CRC/ECC, and Postamble fields. Corresponding to the Header field is the Data field, which is used for actual user data. Note that for a write operation all fields in the Data Segment are rewritten--not just the Data field.

Register Pair 8--Data Preamble

The Data Preamble has the same function in the Data Segment as does the ID Preamble in the ID Segment. Generally, both preambles will be programmed with the same Value and Count bytes.

Register Pair 9--Data Sync

The Data Sync has the same function as the ID Sync. Typically, they use the same Value and Count bytes.

Register Pair 10--Data Address Marker

The Data Address Marker functions much the same as the ID Address Marker. **Note: The Data Address Mark will have a different Value from the ID Address Mark, thus allowing these two fields to be differentiated.**

Register Pair 11--Data Field

Actual user data is written in this field. Note: **The length of this field is the product of the Sub-block Count (WR19) + 1 and Data Count from the format RAM. (Note: This is an exception; the number of bytes in other fields is simply the Count for those fields without multipliers.)** For a Format TRACK or FORMAT SECTOR command, this field is written to with a fill character.

Register Pair 12--Data CRC/ECC

This field contains the CRC or ECC remainder computed for the Data field. Count should be set to match the polynomial that is used; i.e., Count = 2 for CRC, Count = 6 for 48-bit ECC, etc. The computed CRC or ECC remainder is supplied by the 82C5059 whenever the data field is formatted or re-written.

Register Pair 13--Data Postamble

The Data Postamble spaces the write splice at the end of a sector re-write away from the CRC/ECC field. A short gap of one or two bytes is typical.

The final two fields are gaps which, on a soft-sectored disk, space the sectors evenly around the track and provide buffer space for the physical field length changes which occur with variations in both instantaneous and long-term rotation speed.

Register Pair 14--Inter-Sector Gap

This gap provides space between the end of one sector and the beginning of another. The value chosen is typically the same as for other gaps.

Register Pair 15--Pre-Index/Sector Gap

On soft-sectored drives, this last field fills space from the end of the last Sector to the drive Index. The Count field is the number of byte times the sequencer remains Busy and continues formatting after the Index pulse. (Typically the Count is 1.) As with other gaps, the value used for this gap should be chosen so that it is not confused with preamble fields.

INITIALIZATION

The broad flexibility of the 82C5059 requires that various parameter control registers be initialized before commands are issued to access the disk. Once initialized for an application, many of these registers never need to be changed. Typically, the following registers require infrequent initialization:

WR10--Memory Cycle Timing
WR11--CRC/ECC Polynomial Selection
WR18--Index Timeout
WR19--Sub-Block Count
WR27--Bit Ring Start Count
WR28--CRC/ECC Control (most bits)
WR29--Configuration Control
WR67--Arbitration Timing 1
WR68--Arbitration Timing 2
WR69--SCSI Device ID
Media Format Registers (RAM)

Note: Write Registers WRXX are all directly accessible, as described in Chapter 3 (Registers), and that the Media Format Registers (RAM) are indirectly accessed via WR30, WR31, and WR25, as described in the same chapter

ISSUING COMMANDS

1. Command Overview

A specific command is issued by writing WR16 (Sequencer Command Register), but before writing WR16 other parameters specific to that command must be programmed by writing of the appropriate registers. Thus each access to the disk consists of a sequence of register write operations that leads up to issuing the specific command by writing WR16.

The particular sequence of registers written before issuing the specific command varies with each application. The registers commonly written before most commands include:

Memory Controller Registers for data block transfers:
WR00-09

Sequencer Registers:
WR17--Sequencer Loop Count with number of sectors
WR20-23--Header with Cylinder, Head, and Sector
WR25--Sequencer Start/Restart State
(Note: WR25 should be initialized with 33h and does not need to be changed except for a format type command.)
WR26--Sequencer Loop State
(Note: WR26 should be initialized with a 0Eh and does not need to be changed except for a format-type command.)

Access to these registers is discussed in Chapter 3 (Registers). It is reiterated below.

2. How to Issue a Command

Issuing a command is synonymous with writing WR16. (Note: Only certain combinations of writing WR16, as described below, are valid.) To write WR16 (or any other register in the sequence leading up to writing WR16), the processor must put the appropriate register address on the address/data bus (A/D0-7), assert ALE (8051 mode) or -AS (Z8 mode) to latch the address, then with appropriate control signals, transfer the data to the register. (See Chapter 2 for timing details for writing a 82C5059 internal register.)

3. Command Descriptions

Table 4-1 lists all possible command bytes which may be issued to the 82C5059 via the WR16, the Sequencer Command Register. For other values written to WR16, results are undefined.

Table 4-1. Sequencer Command Register

HEX	BITS 7654 3210	COMMAND
00	0000 0000	ABORT
01	0000 0001	NORMAL READ
02	0000 0010	NORMAL WRITE
05	0000 0101	READ ID
06	0000 0110	FORMAT TRACK
09	0000 1001	READ LONG
0A	0000 1010	WRITE LONG
0E	0000 1110	FORMAT TRACK LONG
19	0001 1001	READ SYNDROME LONG
1D	0001 1101	READ ID SYNDROME LONG
21	0010 0001	READ--IGNORE FLAG
22	0010 0010	WRITE--IGNORE FLAG
26	0010 0110	FORMAT SECTOR
29	0010 1001	READ LONG--IGNORE FLAG
2A	0010 1010	WRITE LONG--IGNORE FLAG
39	0011 1001	READ SYNDROME LONG--IGNORE FLAG
41	0100 0001	VERIFY
49	0100 1001	VERIFY LONG
59	0101 1001	VERIFY SYNDROME LONG
61	0110 0001	VERIFY--IGNORE FLAG
69	0110 1001	VERIFY LONG--IGNORE FLAG
79	0111 1001	VERIFY SYNDROME LONG--IGNORE FLAG
81	1000 0001	CHECK DATA CRC/ECC
85	1000 0101	CHECK TRACK FORMAT
A1	1010 0001	CHECK DATA CRC/ECC--IGNORE FLAG

00h ABORT

Issuing an ABORT to the Sequencer Command Register (WR16) when the sequencer is busy will abort the command that is executing. The status (read in Bit 0 or RR16) goes from Busy to Not-Busy. If interrupts are enabled (Bit 7 of WR29 is set), the sequencer interrupt (INTSEQ) will be asserted.

01h NORMAL READ

This is the normal command to read the disk. It is used to transfer one or more blocks of data from the disk to the RAM buffer. The starting disk address for the transfer is taken from WR20 through WR23, and the number of sectors to be transferred is taken from WR17.

02h NORMAL WRITE

This is the normal write to the disk. It is used to transfer one or more blocks of data from the RAM buffer to the disk. Its operation is much the same as the NORMAL READ command except that the direction of data flow is reversed and no data error checking occurs.

05h READ ID

The READ ID command is used for sequentially reading ID segments (ID Header only) from the disk and transferring them to the RAM buffer. The transfer begins with the first ID that is encountered after the command is issued; the number of sectors (ID segments) to be transferred is taken from WR17. The READ ID command is useful for verifying disk addressing errors such as seek positioning and head selection errors. It is also valuable for determining instantaneous disk rotational position. **Note: If this command is used, the firmware should be synchronized to the disk; that is, the firmware must know where it is located on the disk.**

06h FORMAT TRACK

The FORMAT command is used to format a single track on the disk. It may be used for either hard or soft-sectored disks. When the command is issued, the sequencer waits for the next INDEX pulse. On the rising edge of INDEX, the sequencer turns on WRTGATE, and WRTGATE stays on until the Sequencer Loop Count (written via WR17, read via RR25) has counted down to zero. If, as in a normal FORMAT TRACK command, the Sequencer Loop State (written in WR26) is 0Eh (soft sector), WRTGATE is turned off on the next rising edge of INDEX and, if interrupts are enabled (bit 7 or WR29 is set), an interrupt occurs (INTSEQ is asserted). If Enable Write Gate Edge is set (Bit 5 of WR29), then WRTGATE is disabled for 2 bit times preceding each Data Preamble field. The latter feature is an option for some ESDI-type formats.

The Sequencer Loop Count sets the number of sectors on a track; i.e., the number of loops that the sequencer state machine will execute. For each sector on the track, the size of the fields within the sector is determined by the Count Byte for that field in the format RAM. With the exception of the ID Header, ID CRC/ECC, and Data CRC/ECC fields, all fields are determined by the related Value Bytes in the format RAM.

The ID Header field is read by the sequencer from the RAM buffer using DMA Channel 0. It is the responsibility of the firmware to configure DMA Channel 0 properly and to point to a location in the RAM buffer where a table of sequential ID Header fields is located. The sequencer generates the ID CRC/ECC and Data CRC/ECC fields based on the contents of the CRC/ECC polynomial. Selection Register (WR11) and the CRC/ECC Control Register (WR28).

For format commands with Non-ESDI configuration, unlike data read or write commands, the Sequencer Start/Restart Register (WR25) should be loaded with 21h and the Sequencer Loop State Register should be loaded with 0Eh for soft-sectored disks and 0Fh for hard-sectored disks.

09h READ LONG

The READ LONG command is used to transfer one or more blocks of data to the RAM buffer as in the NORMAL READ command except that the Data CRC/ECC field is read as data. This command is sometimes used together with the WRITE LONG command described below to test CRC/ECC operation: a normal sector is written; it is transferred to the RAM buffer, along with its CRC/ECC bytes, using READ LONG; contents are modified in the buffer; then it is written back to the disk using WRITE LONG. This process allows the microprocessor to introduce an error of arbitrary type, length, and location into the data sector for subsequent reading and error detection and recovery.

0Ah WRITE LONG

The WRITE LONG command is used to transfer one or more blocks of data from the external RAM buffer to the disk as in the NORMAL WRITE command except that the CRC/ECC bytes are taken from the RAM buffer instead of from computed values from the sequencer.

0Eh FORMAT TRACK LONG

The FORMAT TRACK LONG command is equivalent to the FORMAT TRACK command except that ID Header and ID CRC/ECC bytes are fetched from the RAM buffer; i.e., ID CRC/ECC bytes are not internally generated by the 82C5059.

19h READ SYNDROME LONG

The READ SYNDROME LONG command is equivalent to the READ LONG command except that CRC/ECC syndrome bytes are transferred to the external RAM buffer instead of the actual CRC/ECC bytes.

Note: The syndrome bytes are computed from the Data portion of the Data Segment and the Data CRC/ECC field. The syndrome bytes may be used to correct bad data.

1Dh READ ID SYNDROME LONG

This command is equivalent to the READ ID command except that the syndrome bytes from reading the ID Segment are also transferred to the external RAM buffer.

21h READ--IGNORE FLAG

The READ--IGNORE FLAG command is equivalent to the NORMAL READ command except it is not aborted by a non-zero flag. (Note: **The non-zero flag would be in the high nibble of byte 3 of the ID Header field if Bit 2 of WR29 is set=0, or it would be in byte 5 of the ID Header if Bit 2 is set.)**

22h WRITE--IGNORE FLAG

This command is equivalent to the NORMAL WRITE command except that it is not aborted by a non-0 flag nibble or byte.

26h FORMAT SECTOR

The FORMAT SECTOR command is used exclusively for hard-sectored disks to format one or more sectors. After the command is issued, the sequencer will start the format on the next SECTOR or INDEX pulse and format for the number of sectors specified in the Sequencer Loop Counter Register (WR17).

It is the responsibility of the microprocessor to issue the command during the sector just before the sector to be formatted. The microprocessor can count the number of sectors since INDEX by polling the Extended Status Register Index and Sector bits (bits 7 and 6 of RR17). This command allows the controller to easily map out bad sectors even after the disk has been formatted and used.

29h READ LONG--IGNORE FLAG
2Ah WRITE LONG--IGNORE FLAG
39h READ SYNDROME LONG--IGNORE FLAG

These commands are equivalent to READ LONG, WRITE LONG, and READ SYNDROME LONG except that they are not aborted by a non-zero flag nibble or byte.

41h VERIFY

A VERIFY command is a convenience for checking data written to disk. A VERIFY command (1) reads data from the disk into the 82C5059; (2) reads data out of the RAM buffer; and (3) performs a byte-by-byte comparison. Unlike the various read commands, this command does not destroy data in the RAM buffer.

49h VERIFY LONG
59h VERIFY SYNDROME LONG
61h VERIFY--IGNORE FLAG
69h VERIFY LONG--IGNORE FLAG
79h VERIFY SYNDROME LONG--IGNORE FLAG

Each of these commands operates like the equivalent READ command except that data is compared as in the VERIFY command.

81h CHECK DATA CRC/ECC

The CHECK DATA CRC/ECC command is equivalent to the NORMAL READ command except that no data is transferred to the RAM buffer. This command is useful as a check of the data and CRC/ECC written on the disk.

85h CHECK TRACK FORMAT

This command performs the same function for the Header field of the ID Segment as the CHECK DATA CRC/ECC command does for the Data portion of the Data Segment.

A1h CHECK DATA CRC/ECC--IGNORE FLAG

This command is equivalent to the CHECK DATA CRC/ECC command except that it is not aborted by a non-zero Flag Byte/Nibble.

Data Transfer

Once the CHIPS 82C5059 has been initialized (including writing the format RAM) and a disk has been formatted (see below), commands can be issued to transfer data.

Note: The Sector Number Register (WR23) gets incremented automatically after each error free block is transferred; thus it is unnecessary to reinitialize it for sequential block transfers.

Part of a command to transfer data consists of searching for a valid ID with the correct Header field.

1. **ID Search.** In non-ESDI mode, after a read/write-type command is issued to the sequencer, RDGATE is asserted. Three bit times after the AMFOUND signal goes active the sequencer first compares the Sync byte found on the disk with the Sync Byte in the format RAM; then it compares the Address Marker found on the disk with the Address Marker in the format RAM. Next the sequencer reads the ID Header, which it latches into the registers RR19-23, and compares the ID Header with the contents of WR20-23.

If the Sync Byte, Address Mark Byte, and the ID Header compare with the expected values, then the sequencer clears the ID Data Compare Error in the Sequencer Status Register (Bit 6 of RR16) and the ID Sync and Marker Error Bit (Bit 5 of RR 16). If the ID Data Compare Error Bit is set=0, the sequencer next checks the Flag Byte (RR19) or the high nibble of the Head/Flag Byte (RR22)--depending on the scheme chosen for storing flag information (see Bit 2 of WR29). If Bit 5 of WR16 is set (to abort on non-zero flag information) and the flag byte or nibble is non-zero, then the command is aborted and the Flag Byte/Nibble Non-Zero Bit in the Extended Sequencer Status Register is set (Bit 3, RR17).

Next, the ID CRC/ECC is read and checked. If it is good, the ID CRC/ECC Bit in the Sequencer Status Register (Bit 4, RR16) is cleared.

If there are any errors in the ID Sector (Sync does not compare, Address Mark does not compare, ID Data does not compare, or CRC/ECC error), the sequencer automatically deasserts RDGATE and loops back to the Start State to retry the desired Sector. The sequencer searches until it finds the valid ID or until it has reached the number of revolutions specified in the Index Timeout Register (WR18).

In ESDI mode, after a read/write-type command is issued to the sequencer, AM ENABLE is asserted. This tells the drive to search for an Address Mark. The drive will respond with AM FOUND on the SECTOR/AMF pin when it detects the Address Mark. The sequencer will deassert the AM ENABLE signal when the drive responds with the AM FOUND function. As the sequencer deasserts AM ENABLE, the drive will deassert AM FOUND, which completes the handshake.

If the drive is in hard-sectored mode and the sequencer is configured for hard-sectored mode, the sequencer still asserts AM ENABLE. This has no effect on the hard-sectored ESDI drive but the drive will still provide a pulse on the SECTOR/AM FOUND pin (interpreted as an AM FOUND).

After the SECTOR/AMF is detected, the sequencer will delay for the State 3 Count, then it will assert RD GATE. After RD GATE is asserted, the sequencer will look for the NRZ IN serial-to-parallel converter (SERDES) to compare with the value in State 4. If this compare doesn't occur within 256 RD_REF_CLK cycles, the sequencer will time-out, deassert RD GATE, and retry the Address Mark search sequence. If the compare does occur, the sequencer will start the internal Byte Clock and compare the first four bytes of the ID with the contents of WR20-WR23.

Note: The value for the ID Sync byte must be shifted three bits from the written Sync value to compensate for the internal delay from the Sync compare function to the desired byte synchronization. The above description assumes the sequencer is configured in Internal Sync mode with "1 Field Sync" in ESDI mode and that ID Sync Timeout is not disabled (Bit 0 of WR 34 not set).

The ID Compare with CRC/ECC check is the same as in a non-ESDI configuration.

2. **Data Transfer.** If the ID search was successful, the RDGATE signal is deasserted, then reasserted to read the data field.

In the External Sync mode (Bit 4 of WR29 is set for non-ESDI type), after the Sync field is detected (AMFOUND from the external data separator goes active), the Data Sync byte from the disk is compared to the value in the format RAM, followed by the comparison of the Address Mark byte. If either of these comparisons fail, then the command is aborted and the Data Sync or Address Mark Error Bit in the Sequencer Status Register is set (Bit 2, RR16).

If AMFOUND is not detected (that is, if the data separator does not detect the Sync field and assert AMFOUND, an input to the 82C5059 within 512 or 32 bit times (see Bit 6 of WR10) after RDGATE is activated), the command is aborted and, if the Enable Data Sync Timeout Bit is set in the CRC/ECC Control Register (Bit 7 or WR28), the Data Sync Field Timeout Bit in the Extended Status Register (Bit 4 of RR17) will be set.

If AMFOUND is detected by the 82C5059 and Data Sync and Data Address Mark fields are valid, the sequencer then uses REQ0 and ACK0 to request the DMA Controller to transfer the data to the buffer memory.

During the data transfer, if the DMA Controller does not respond within one byte time to the sequencer request (REQ0), the Drive Data Over/Under Run Bit is set in the Sequencer Extended Status Register (Bit 0, RR17).

After the data transfer is complete, the data ECC is read and checked. If it is good, the sequencer will increment WR23 (the Sector Register) and decrement WR17 (the Sequencer Loop Count Register). If WR17 is Non-Zero, the sequencer will loop back to the Start State and start the sequencing over again for the next sector in a multi-sector operation.

If the loop count is zero, the sequencer will stop and will clear (RR16 Bit 0=0) and assert the INT SEQ if it is enabled. (Bit 7 of WR29 is set.)

When the command is complete or has aborted, the Sequencer Status will go to not Busy (Bit 0 of RR16 will be cleared). If sequencer interrupts are enabled (Bit 7 of WR29 is set), the INTSEQ line will also go active.

If the ID search was successful, RD GATE is deasserted and reasserted to read the Data field. In Internal Sync mode, the sequencer will (as above) look for the NRZ IN serial-to-parallel converter (SERDES)to compare with the value in State 10. If this compare does not occur within 512 or 32 RD_REF_CLK cycles, the sequencer will time-out and issue a Data Sync Field Timeout (Bit 4 of RR17 set). If the compare is successful, the sequencer will react from this state as it does in non-ESDI mode.

Note: The Value for the Data Sync byte must be shifted three bits from the written Sync Value to compensate for the internal delay from the Sync compare function to the desired byte synchronization.

For data transfer in write mode, if the ID search was successful, the RD GATE signal is deasserted and the WRT GATE signal is asserted. If a "1 Field Sync" has been programmed (Bit 1 of WR29 cleared), then the Data Sync field is written just as it is programmed in the format RAM. If a "2 Field Sync" has been programmed (Bit 1 of WR29 set), then the Data Sync and the Data Address Mark fields are written just as they are programmed in the format RAM. If the sequencer is in ST506/412 mode ("2 Field Sync"), then AM ENABLE is asserted for State 9 (Data Sync field), which tells the Encode/Decode device to insert the illegal pattern violation for the Data Sync field.

From this point on, data is fetched from memory and converted from parallel to serial form and CRC/ECC is calculated for the data. At the end of the data transfer, the CRC/ECC remainder is written out, followed by the postamble as programmed for the Postamble in the Value and Count fields of the format RAM. WRT GATE is then deasserted. From this point on the write operation is complete. For multiple-sector write operations, the ID search would be performed again just as it would for a read operation. Write splices occur at the end of the ID Postamble and beginning of the Data Preamble, and at the end of the Data Postamble and beginning of the Inter-Sector Gap.

Reading Status

As a command is issued to the CHIPS 82C5059, one of the immediate responses is the setting of the Busy Bit (Bit 0) of the Sequencer Status Register (RR16). When the command is completed, the Busy Bit is cleared and an interrupt (INTSEQ) is generated if the interrupt is enabled (Bit 7 of WR29 set). At this point, status related to the command execution is available in the Sequencer Status Register. If the Extended Status Non-Zero Bit (Bit 7) of the Sequencer Status Register is set, then status information is also available in the Extended Sequencer Status Register (RR17).

These registers are accessed, as explained in Chapter 3, by the microprocessor driving the selected I/O addresses for the register onto the A/D0 -7 bus, then generating the address latch, ALE (for 8051 type microprocessor) or -AS (for Z8 type microprocessor).

Error Processing

The 82C5059 performs no error processing explicitly except for ID retries. However, a wide spectrum of its capabilities are valuable in the microprocessor implementation of this phase of controller operation. Among these capabilities are the ability to recover ECC remainders, read sector IDs, etc.

The 82C5059 error detection and correction (EDAC) capability relative to disk data and buffer memory is limited to CRC 16 (error detection only), three computer generated ECC polynomials, and odd parity check/generation for the DMA Buffer RAM data.

In the case of ECC, the 82C5059 generates and checks the serial NRZ data stream for errors. These errors are flagged by a non-zero syndrome. Location and length information is obtained from the syndrome byte(s) returned in case of an error. The 82C5059 does not make corrections by itself. The microprocessor through a specific algorithm will determine:

1. The location of the error.
2. The length of the error.
3. Whether the error length is within correctable range.

It will then make the correction (if length is $\geq$MAX).

The ECC polynomials used by the 82C5059 have associated algorithms available for use. Contact CHIPS Mass Storage Operations Marketing for information concerning this firmware.

Disk Formatting

Three commands are available for formatting disks: FORMAT TRACK, FORMAT TRACK LONG, and FORMAT SECTOR. (Note that FORMAT TRACK and FORMAT TRACK LONG are equivalent except that for the latter, command ID Header and ID CRC/ECC bytes are fetched from the external RAM buffer.) The FORMAT TRACK command can be used for both hard and soft sectored disks, and it is typically used to format an entire track. Formatting begins with the detection of an INDEX pulse, and when used with hard-sectored disks, the SECTOR pulse is used to divide the disk track **n** Sectors, **n** being the number of Sector pulses per track.

The FORMAT SECTOR command is used only with hard-sectored disks. The command can be used to format one or more sectors, as specified by the Sequencer Loop Count (WR17).

For the details of these three commands, see their description under "Issuing Commands" and "Command Descriptions" in this chapter. Note: The size of each field formatted by these commands is determined by its Count byte in the format RAM (see Chapter 3) with the exception of the Data Segment Data field, whose size in bytes is equal to the Count byte in the format RAM times the Sub-Block Count (set by writing WR19). (Note that Sub-Block Count is merely a multiplier for the Count byte in the format RAM, since the Sector Size would be limited to 256 bytes if only the Count byte in the format RAM were used.) Note that all fields will be written during a format operation. The Data field will, of course, be written with fill characters. Thus, before issuing any format-type command, the user firmware must have written the appropriate Value and Count bytes into the format RAM.

APPENDIX A

TRACK FORMAT

The following four tables provide the track format options for MFM Soft Sectored Format, RLL 2,7 Soft Sectored Format, ESDI Soft Sectored Format, and ESDI Hard Sectored Format.

The recommended Sequencer values and byte counts associated with a sequencer state is given in each table.

In addition, diagrams are provided for the Read/Write data sequencer operation on these track formats. The sequencer Start/Restart and Loop End State values are also noted for format, Read and Write commands.

MFM SOFT SECTORED TRACK FORMAT

FORMAT TRACK FUNCTION START/RESTART STATE = 21h LOOP END STATE - OEh

FIELD	POST INDEX GAP	ID PRE-AMBLE	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAP	PRE INDEX GAP
STATE	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	08	0C	01	01	ID-N	04	02	0C	01	01	n	04	02	0E	01(H)
SEQ-VAL	4E	00	A1	FE	00	00	00	00	A1	F8	FILL	00	00	4E	4E

READ SECTOR FUNCITON START/RESTART STATE = 33h LOOP END STATE = OEh

FIELD	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	01	01	ID-N	04	02	SKIP	01	01	n	04	SKIP	SKIP
SEQ-VAL	A1	FE	00	00	00	00	A1	F8	FILL	00	00	4E

WRITE SECTOR FUNCITON START/RESTART STATE = 33h LOOP END STATE = OEh

FIELD	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-E SECTORE GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	01	01	ID-N	04	02	0A	01	01	n	04	02	SKPI
SEQ-VAL	A1	FE	00	00	00	00	A1	F8	FILL	00	00	4E

NOTES: ID-N = ID DATA BYTE
N-U = NOT USED IN THIS COMMAND
FILL = FORMAT FILL BYTE
n = DATA FIELD COUNT

PRM = PARAMETER FROM DRIVE
SKIP = IGNORED = 1
PER ** = MUST INCLUDE SPEED GAP
(H) = HOLD STATE (WAIT FOR SECTOR/INDEX)

Table A-1. MFM SOFT SECTORED FORMAT

Table A-2. RLL 2,7 SOFT SECTORED TRACK FORMAT

RLL 2,7 SOFT SECTORED TRACK FORMAT

FORMAT TRACK FUNCTON — START/RESTART STATE = 21h — LOOP END STATE - 0Eh

FIELD	POST INDEX GAP	ID PRE-AMBLE	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAP	PRE INDEX GAP
STATE	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	0B	0C	01	01	ID-N	02	03	0C	01	01	n	06	03	0E	01(H)
SEQ-VAL	33	FF	62	FE	00	00	33	FF	62	F8	FILL	00	00	33	33

READ SECTOR FUNCTON — START/RESTART STATE = 33h — LOOP END STATE = 0Eh

FIELD	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	01	01	ID-N	02	08	SKIP	01	01	n	06	SKIP	SKIP
SEQ-VAL	62	FE	00	00	33	FF	62	F8	FILL	00	00	33

WRITE SECTOR FUNCTON — START/RESTART STATE = 33h — LOOP END STATE = 0Eh

FIELD	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	01	01	ID-N	02	03	0A	01	01	n	06	03	SKIP
SEQ-VAL	62	FE	00	00	33	FF	62	F8	FILL	00	00	33

NOTES:
ID-N = ID DATA BYTE
N-U = NOT USED IN THIS COMMAND
FILL = FORMAT FILL BYTE
n = DATA FIELD COUNT
PRM = PARAMETER FROM DRIVE
SKIP = IGNORED = 1
PER ** = MUST INCLUDE SPEED GAP
(H) = HOLD STATE (WAIT POR SECTOR/INDEX)

ESDI SOFT SECTORED TRACK FORMAT

FORMAT TRACK FUNCTON START/RESTART STATE = 10h LOOP END STATE - 0Eh

FIELD	POST INDEX GAP	AM ENABL TIME	ID PRE-AMBLE	ID PRE-AMBLE	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER SECTOR GAP	PRE INDEX GAP
STATE	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	PRM	03	PRM-1	01	01	ID-N	02	04	01	PRM	01	n	06	04	PRM**	01(H)
SEQ-VAL	00	00	00	00	C8	00	00	00	00	00	C8	FILL	00	00	00	00

READ SECTOR FUNCTON START/RESTART STATE = 33h LOOP END STATE = 0Eh

FIELD	AMP ID RGAT	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER SECTOR GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	02	01	ID-N	02	02	SKIP	SKIP	01	n	06	SKIP	SKIP
SEQ-VAL	00	19	00	00	00	00	00	19	FILL	00	00	00

WRITE SECTOR FUNCTON START/RESTART STATE = 33h LOOP END STATE = 0Fh

FIELD	AMP ID RGATE	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	WGATE-SAM DELAY	PRE INDEX GAP
STATE	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	02	01	ID-N	02	02	01	PRM	01	n	06	04	0A	00
SEQ-VAL	00	19	00	00	00	00	00	C8	FILL	00	00	00	00

NOTES: ID-N = ID DATA BYTE
N-U = NOT USED IN THIS COMMAND
FILL = FORMAT FILL BYTE
n = DATA FIELD COUNT

PRM = PARAMETER FROM DRIVE
SKIP = IGNORED = 1
PER ** = MUST INCLUDE SPEED GAP
(H) = HOLD STATE (WAIT FOR SECTOR/INDEX)

Table A-3. ESDI SOFT SECTORED TRACK FORMAT

Table A-4. ESDI HARD SECTORED TRACK FORMAT

ESDI HARD SECTORED TRACK FORMAT

FORMAT TRACK FUNCTION START/RESTART STATE = 1Fh LOOP END STATE - 0Fh

FIELD	POST INDEX GAP	AM ENABL TIME	ID PRE-AMBLE	ID PRE-AMBLE	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER SECTOR GAP	PRE INDEX GAP
STATE	F	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	01(H)	PRM	PRM-1	01	01	ID-N	02	04	01	PRM	01	n	06	04	01	01(H)
SEQ-VAL	00	00	00	00	C8	00	00	00	00	00	C8	FILL	00	00	00	00

READ SECTOR FUNCTION START/RESTART STATE = 33h LOOP END STATE = 0Fh

FIELD	AMF TO RGAT	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-E SECTORX GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	PRM	01	ID-N	02	02	SKIP	SKIP	01	n	06	SKIP	SKIP
SEQ-VAL	00	19	00	00	00	00	00	19	FILL	00	00	00-U

WRITE SECTOR FUNCTION START/RESTART STATE = 33h LOOP END STATE = 0Fh

FIELD	AMF TO RGATE	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	WGATE-SAM DELAY	PRE INDEX GAP
STATE	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	PRM	01	ID-N	02	02	01	PRM	01	N	06	04	01	00
SEQ-VAL	00	19	00	00	00	00	00	C8	FILL	00	00	00	00

NOTES:
ID-N = ID DATA BYTE
N-U = NOT USED IN THIS COMMAND
FILL = FORMAT FILL BYTE
n = DATA FIELD COUNT
PRM = PARAMETER FROM DRIVE
SKIP = IGNORED = 1
PER ** = MUST INCLUDE SPEED GAP
(H) = HOLD STATE (WAIT FOR SECTOR/INDEX)

APPENDIX B

FORMAT PARAMETER REGISTER FILE

In order to initialize the Format Parameter Register File, a table must first be setup (typically in ROM) containing the values to be written. Each of the following define byte (DB) directives specify the contents of a value or count. An example for soft sectored ST506/412 Track Format is given in Figure B-1 and Table B-1 is as follows:

```
SEQTBL:  DB    001H    ;; STATE 0 COUNT
         DB    000H    ;; STATE 0 VALUE
         DB    00FH    ;; POST-INDEX BYTE COUNT
         DB    04EH    ;; POST-INDEX BYTE VALUE
         DB    00CH    ;; 10 PREAMBLE BYTE COUNT
         DB    000H    ;; 10 PREAMBLE BYTE VALUE
         DB    001H    ;; ID SYNC BYTE COUNT
         DB    0A1H    ;; ID SYNC BYTE VALUE
         DB    001H    ;; ID MARKER BYTE COUNT
         DB    0FEH    ;; ID MARKER BYTE VALUE
         DB    004H    ;; ID DATA FIELD COUNT
         DB    000H    ;; ID DATA FIELD VALUE (NO CARE)
         DB    004H    ;; ID ECC FIELD COUNT
         DB    000H    ;; ID ECC FIELD VALUE (NO CARE)
         DB    003H    ;; ID POSTAMBLE COUNT
         DB    000H    ;; ID POSTAMBLE BYTE VALUE
         DB    00CH    ;; DATA FIELD PREAMBLE BYTE COUNT
         DB    000H    ;; DATA FIELD PREAMBLE BYTE VALUE
         DB    001H    ;; DATA FIELD SYNC BYTE COUNT
         DB    0A1H    ;; DATA FIELD SYNC BYTE VALUE
         DB    001H    ;; DATA FIELD MARKER BYTE COUNT
         DB    0F8H    ;; DATA FIELD MARKER BYTE VALUE
         DB    004H    ;; DATA FIELD BYTE COUNT
         DB    0E5H    ;; DATA FIELD BYTE VALUE (FORMAT VALUE)
         DB    004H    ;; DATA FIELD ECC BYTE COUNT
         DB    000H    ;; DATA FIELD ECC VALUE (NO CARE)
         DB    003H    ;; DATA FIELD POSTAMBLE COUNT
         DB    000H    ;; DATA FIELD POSTAMBLE VALUE
         DB    017H    ;; INTER-RECORD GAP BYTE COUNT
         DB    04EH    ;; INTER-RECORD GAP BYTE VALUE
         DB    001H    ;; PRE-INDEX GAP BYTE COUNT
         DB    04EH    ;; PRE-INDEX GAP BYTE VALUE
TBLEND:  EQU   $       ;; END OF TABLE
```

Table B-1. Format Parameter Register File for ST506/412 Track Format

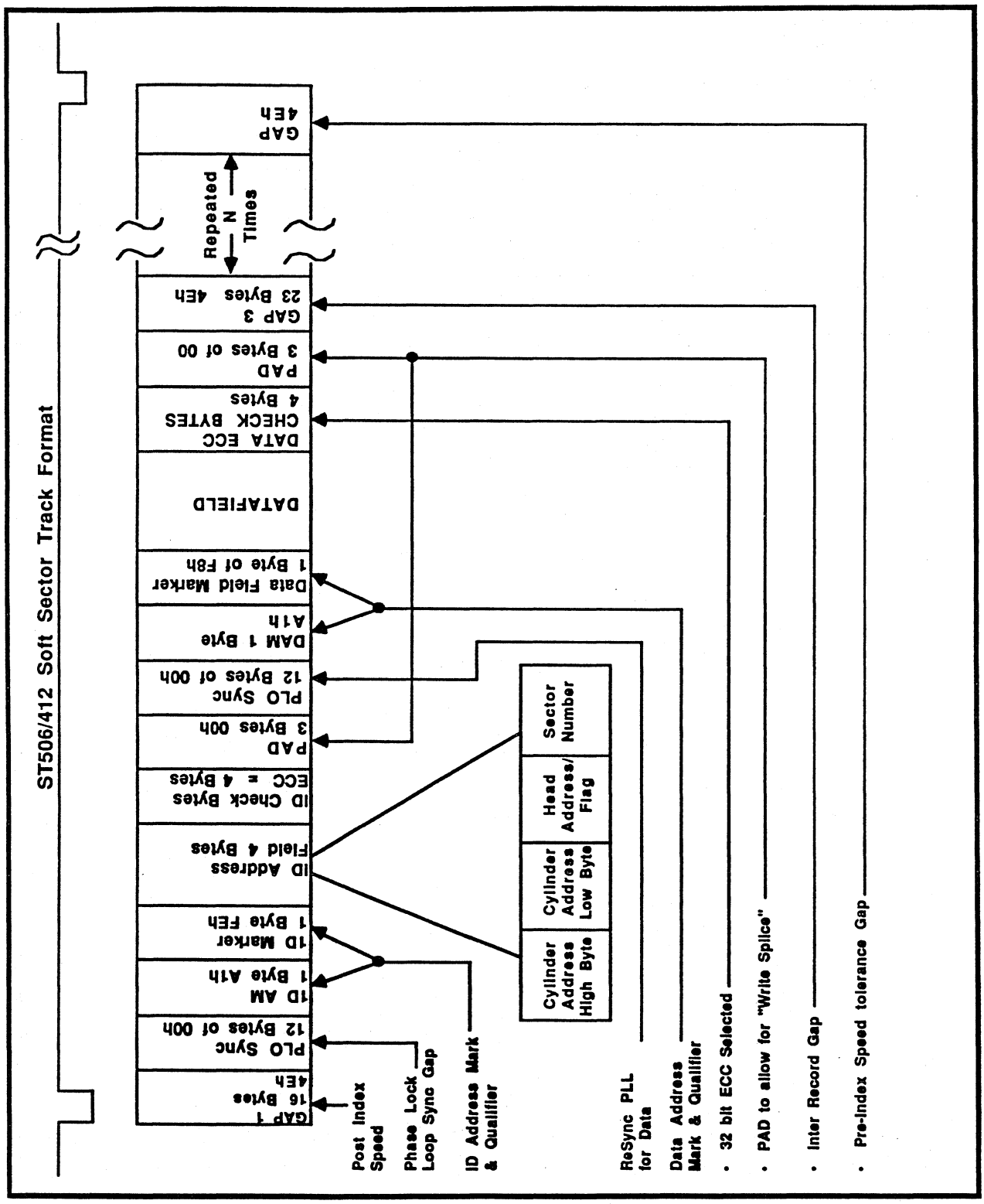


Figure B-1. ST 506/412 Soft Sector Track Format Diagram

APPENDIX C

Table C-1. DRAM From SRAM Pin Conversion (8/16 Bit, 64/128K, 256/512K, 1M)

MEMORY ARRAY CONFIGURATIONS		64K x 8B	64K x 16B	256K x 8 B	256K x 16B	1M x 8B
SRAM PIN FUNCTION	DRAM PIN FUNCITONS	ADDRESS	ADDRESS	ADDRESS	ADDRESS	ADDRESS
MEM_A(0)	MUX_A(0)	0 & 8	———	0 & 8	———	0 & 8
MEM_A(1)	MUX_A(1)	1 & 9	1 & 9	1 & 9	1 & 9	1 & 9
MEM_A(2)	MUX_A(2)	2 & 10	2 & 10	2 & 10	2 & 10	2& 10
MEM_A(3)	MUX_A(3)	3 & 11	3 & 11	3 & 11	3 & 11	3 & 11
MEM_A(4)	MUX_A(4)	4 & 12	4 & 12	4 & 12	4 & 12	4 & 12
MEM_A(5)	MUX_A(5)	5 & 13	5 & 13	5 & 13	5 & 13	5 & 13
MEM_A(6)	MUX_A(6)	6 & 14	6 & 14	6 & 14	6 & 14	6 & 14
MEM_A(7)	MUX_A(7)	7 & 15	7 & 15	7 & 15	7 & 15	7 & 15
MEM_A(8)	MUX_A(8)	———	8 & 16	———	8 & 16	———
MEM_A(9)	MUX_A(A)	———	———	16 & 17	———	16 & 17
MEM_A(10)	MUX_A(B)	———	———	———	17 & 18	———
MEM_A(11)	MUX_A(C)	———	———	———	———	18 & 19
MEM_A(12)	-REFSH	-REFSH	-REFSH	-REFSH	-REFSH	-REFSH
MEM_A(13)	-CAS	-CAS	-CAS	-CAS	-CAS	-CAS
MEM_A(14)	-OE	-OE	-OE	-OE	-OE	-OE
-MEM_CE(0)	-RAS(0)	-RAS	-RAS(0)	-RAS	-RAS(0)	-RAS
-MEM_CE(1)	-RAS(1)	———	-RAS(1)	———	-RAS(1)	———
-MEM_WRT	-WE	-WE	-WE	-WE	-WE	-WE

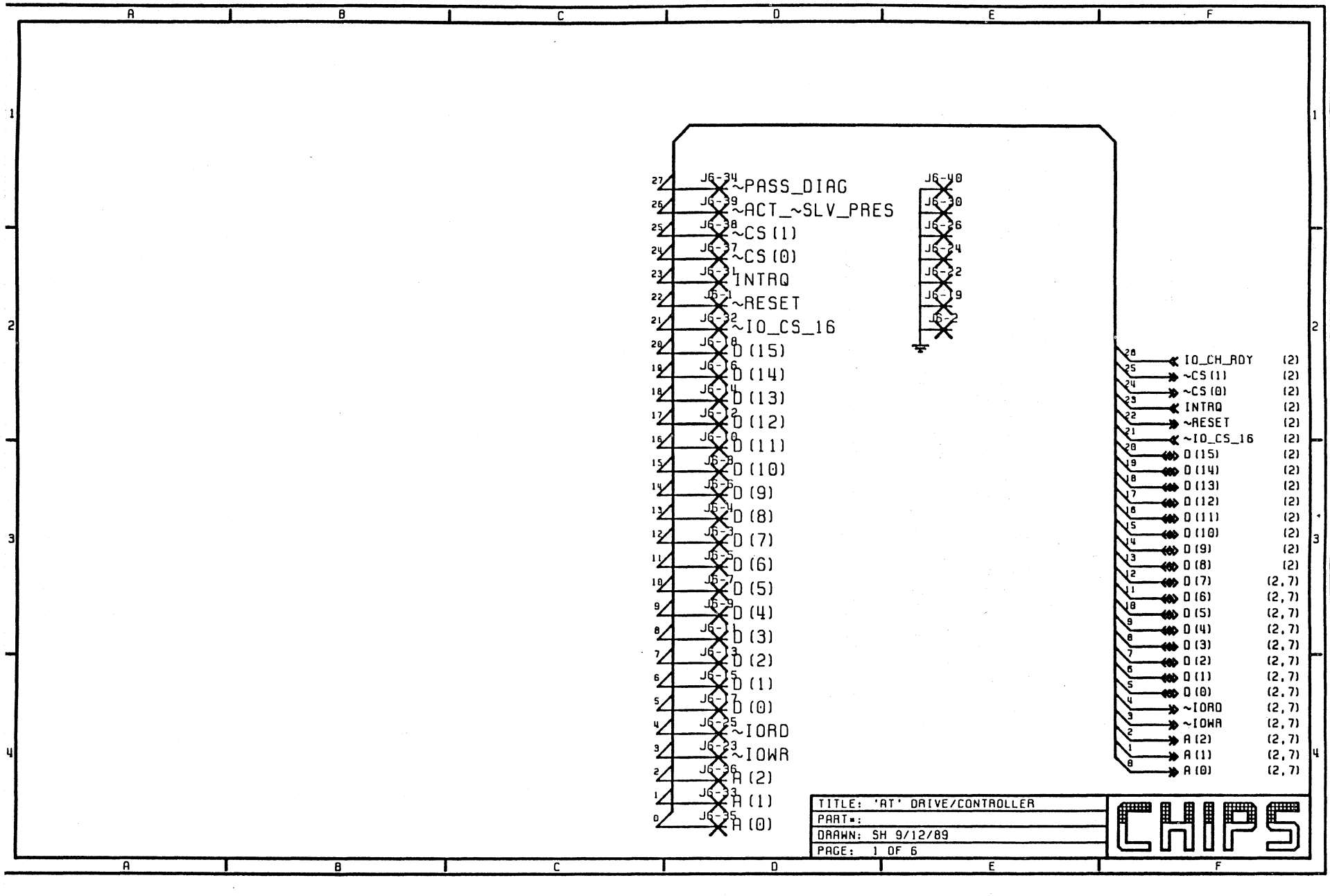
APPENDIX D

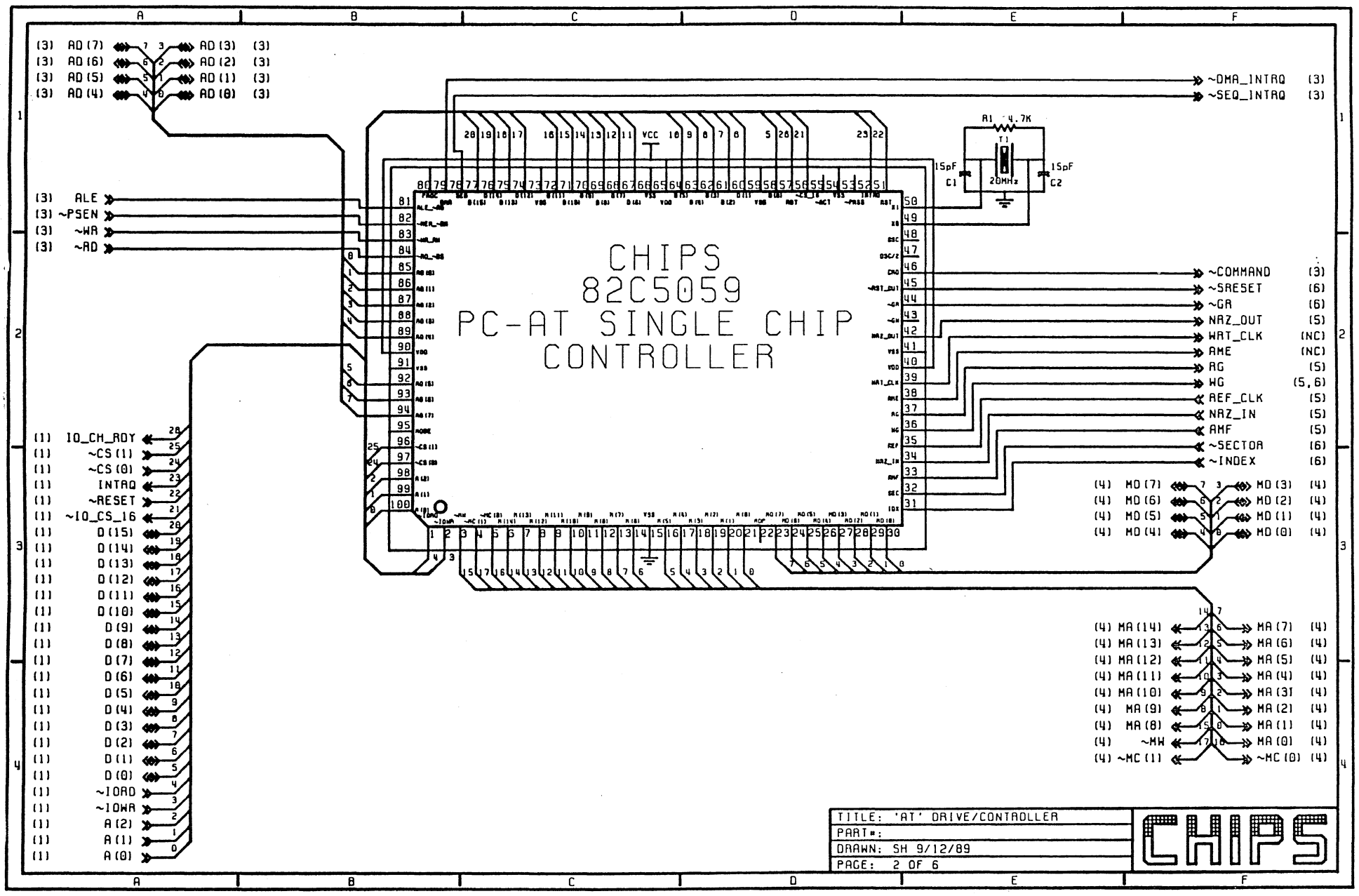
TYPICAL SYSTEM SCHEMATICS

The following five pages are a set of schematics for a typical system configuration using the CHIPS 82C5059 PC-AT Single Chip Controller Solution with a RAM buffer, a CHIPS data separator device , and a microcomputer with a (P)ROM and RAM.

There are three RAM buffer option configurations provided, a 64K x 9 DRAM,256K x 9 DRAM, and 64K x 8 SRAM configuration.

Figures D-1 thru D-6 appear on the following six pages.


J6-34 ~PASS_DIAG
J6-29 ~ACT_~SLV_PRES
J6-28 ~CS(1)
J6-27 ~CS(0)
J6-31 INTRQ
J6-1 ~RESET
J6-32 ~IO_CS_16
J6-18 D(15)
J6-16 D(14)
J6-14 D(13)
J6-12 D(12)
J6-10 D(11)
J6-8 D(10)
J6-6 D(9)
J6-4 D(8)
J6-3 D(7)
J6-5 D(6)
J6-7 D(5)
J6-9 D(4)
J6-11 D(3)
J6-13 D(2)
J6-15 D(1)
J6-17 D(0)
J6-25 ~IORD
J6-23 ~IOWR
J6-36 A(2)
J6-33 A(1)
J6-35 A(0)
J6-40
J6-38
J6-26
J6-24
J6-22
J6-19
J6-2
IO_CH_RDY (2)
~CS(1) (2)
~CS(0) (2)
INTRQ (2)
~RESET (2)
~IO_CS_16 (2)
D(15) (2)
D(14) (2)
D(13) (2)
D(12) (2)
D(11) (2)
D(10) (2)
D(9) (2)
D(8) (2)
D(7) (2,7)
D(6) (2,7)
D(5) (2,7)
D(4) (2,7)
D(3) (2,7)
D(2) (2,7)
D(1) (2,7)
D(0) (2,7)
~IORD (2,7)
~IOWR (2,7)
A(2) (2,7)
A(1) (2,7)
A(0) (2,7)
TITLE: 'AT' DRIVE/CONTROLLER
PART#:
DRAWN: SH 9/12/89
PAGE: 1 OF 6
CHIPS


CHIPS
82C5059
PC-AT SINGLE CHIP
CONTROLLER
A1 4.7K
T1
20MHz
15pF
C1
15pF
C2
VCC
(3) AD(7) AD(3) (3)
(3) AD(6) AD(2) (3)
(3) AD(5) AD(1) (3)
(3) AD(4) AD(0) (3)
(3) ALE
(3) ~PSEN
(3) ~WR
(3) ~RD
~DMA_INTRQ (3)
~SEQ_INTRQ (3)
~COMMAND (3)
~SRESET (6)
~GR (6)
NRZ_OUT (5)
WRT_CLK (NC)
AME (NC)
RG (5)
WG (5,6)
REF_CLK (5)
NRZ_IN (5)
AMF (5)
~SECTOR (6)
~INDEX (6)
(4) MD(7) MD(3) (4)
(4) MD(6) MD(2) (4)
(4) MD(5) MD(1) (4)
(4) MD(4) MD(0) (4)
(4) MA(14) MA(7) (4)
(4) MA(13) MA(6) (4)
(4) MA(12) MA(5) (4)
(4) MA(11) MA(4) (4)
(4) MA(10) MA(3) (4)
(4) MA(9) MA(2) (4)
(4) MA(8) MA(1) (4)
(4) ~MW MA(0) (4)
(4) ~MC(1) ~MC(0) (4)
(1) IO_CH_RDY
(1) ~CS(1)
(1) ~CS(0)
(1) INTRQ
(1) ~RESET
(1) ~IO_CS_16
(1) D(15)
(1) D(14)
(1) D(13)
(1) D(12)
(1) D(11)
(1) D(10)
(1) D(9)
(1) D(8)
(1) D(7)
(1) D(6)
(1) D(5)
(1) D(4)
(1) D(3)
(1) D(2)
(1) D(1)
(1) D(0)
(1) ~IORD
(1) ~IOWR
(1) A(2)
(1) A(1)
(1) A(0)
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PART#:
DRAWN: SH 9/12/89
PAGE: 2 OF 6
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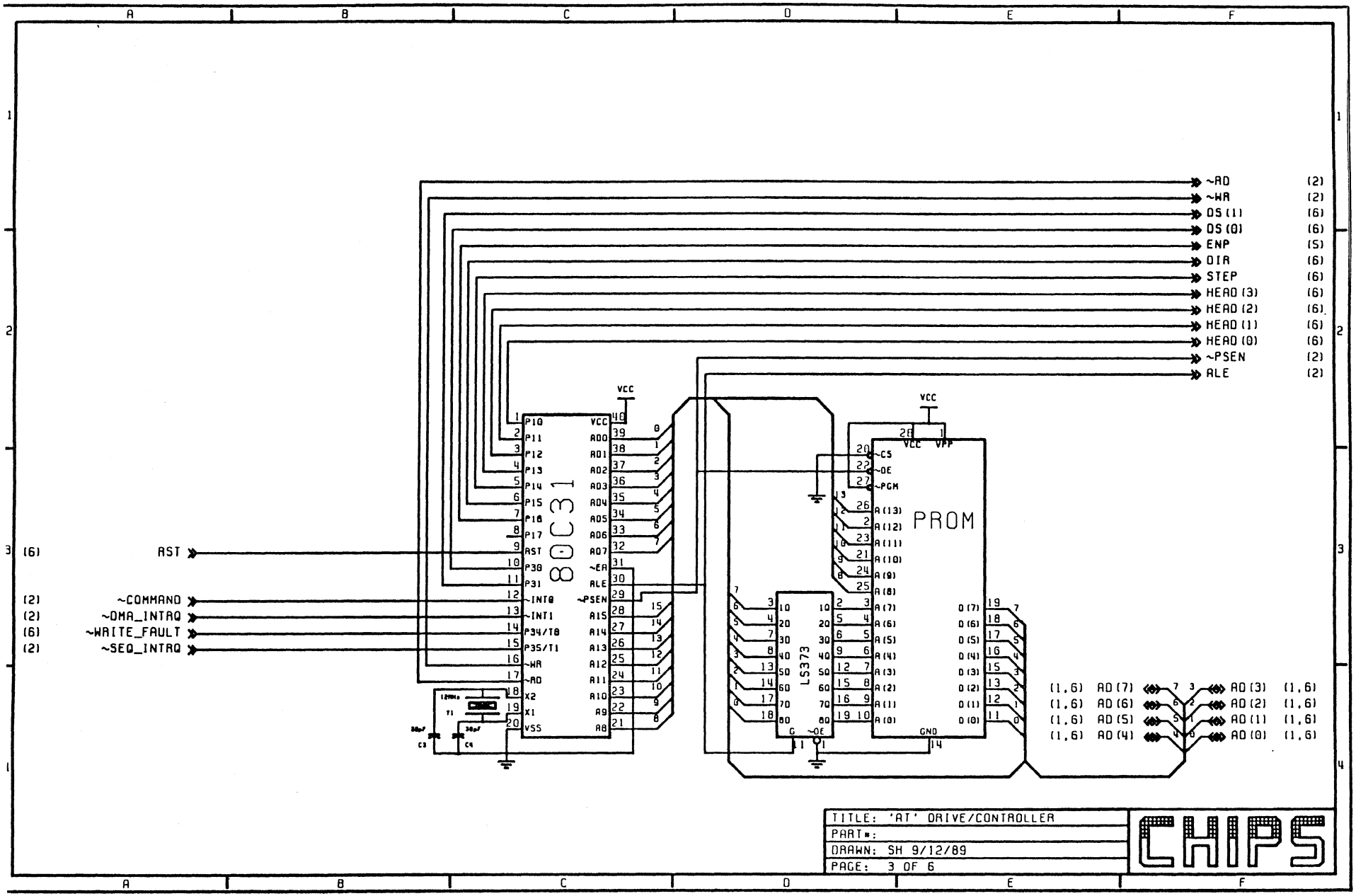
~AD (2)
~WR (2)
DS (1) (6)
DS (0) (6)
ENP (5)
DIR (6)
STEP (6)
HEAD (3) (6)
HEAD (2) (6)
HEAD (1) (6)
HEAD (0) (6)
~PSEN (2)
ALE (2)
(6) RST
(2) ~COMMAND
(2) ~DMA_INTRQ
(6) ~WRITE_FAULT
(2) ~SEQ_INTRQ
VCC
80C31
P10
P11
P12
P13
P14
P15
P16
P17
RST
P30
P31
~INT0
~INT1
P34/T0
P35/T1
~WR
~RD
X2
X1
VSS
VCC
~EA
ALE
~PSEN
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
A15
A14
A13
A12
A11
A10
A9
A8
LS373
~OE
PROM
VCC
VPP
~CS
~OE
~PGM
A(13)
A(12)
A(11)
A(10)
A(9)
A(8)
A(7)
A(6)
A(5)
A(4)
A(3)
A(2)
A(1)
A(0)
D(7)
D(6)
D(5)
D(4)
D(3)
D(2)
D(1)
D(0)
GND
(1,6) AD(7)
(1,6) AD(6)
(1,6) AD(5)
(1,6) AD(4)
AD(3) (1,6)
AD(2) (1,6)
AD(1) (1,6)
AD(0) (1,6)
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PAGE: 3 OF 6
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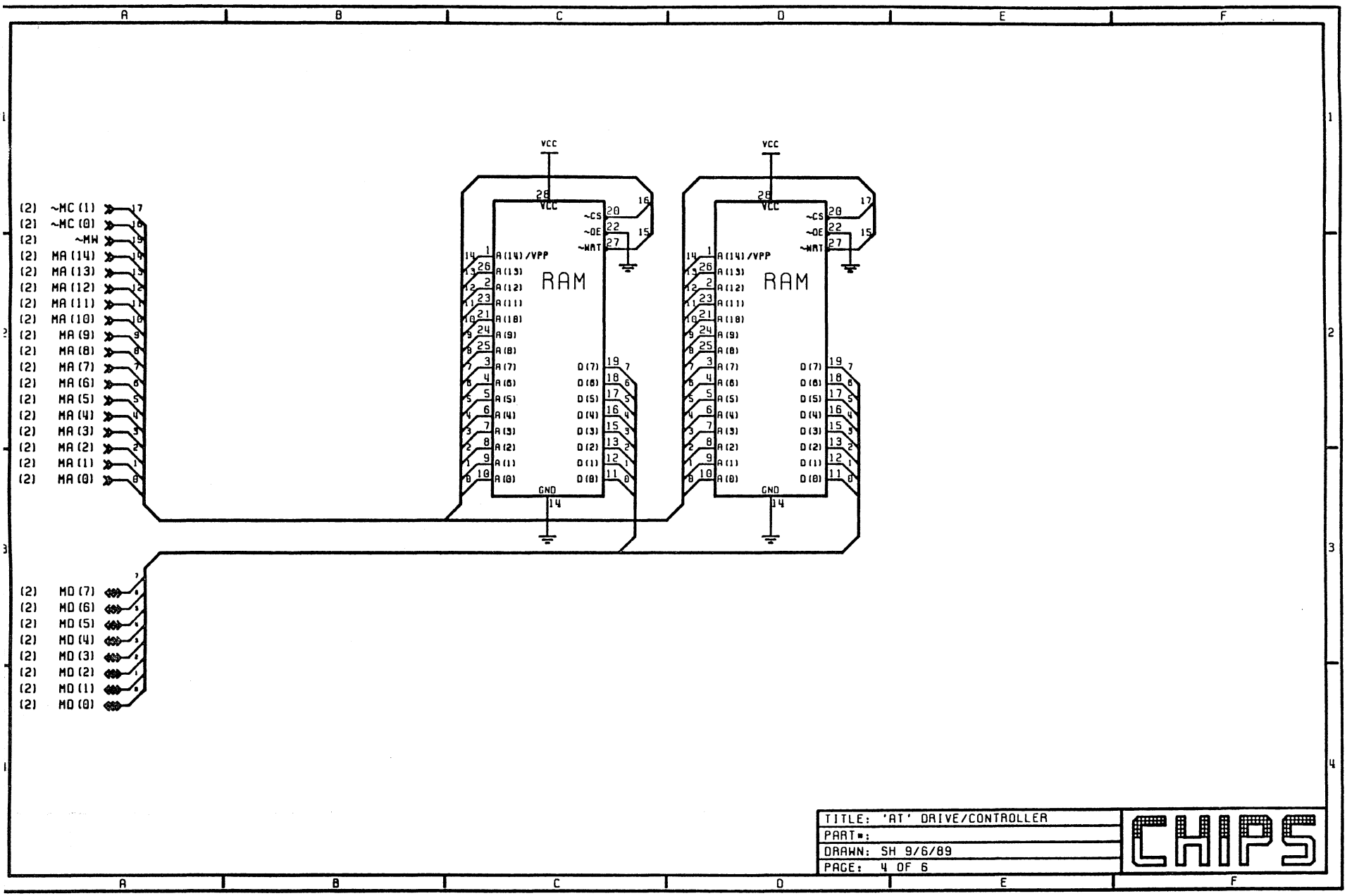
A
B
C
D
E
F
1
2
3
4
(2) ~MC (1)
(2) ~MC (0)
(2) ~MW
(2) MA (14)
(2) MA (13)
(2) MA (12)
(2) MA (11)
(2) MA (10)
(2) MA (9)
(2) MA (8)
(2) MA (7)
(2) MA (6)
(2) MA (5)
(2) MA (4)
(2) MA (3)
(2) MA (2)
(2) MA (1)
(2) MA (0)
(2) MD (7)
(2) MD (6)
(2) MD (5)
(2) MD (4)
(2) MD (3)
(2) MD (2)
(2) MD (1)
(2) MD (0)
VCC
GND
~CS
~OE
~WRT
A (14) /VPP
A (13)
A (12)
A (11)
A (10)
A (9)
A (8)
A (7)
A (6)
A (5)
A (4)
A (3)
A (2)
A (1)
A (0)
D (7)
D (6)
D (5)
D (4)
D (3)
D (2)
D (1)
D (0)
RAM
RAM
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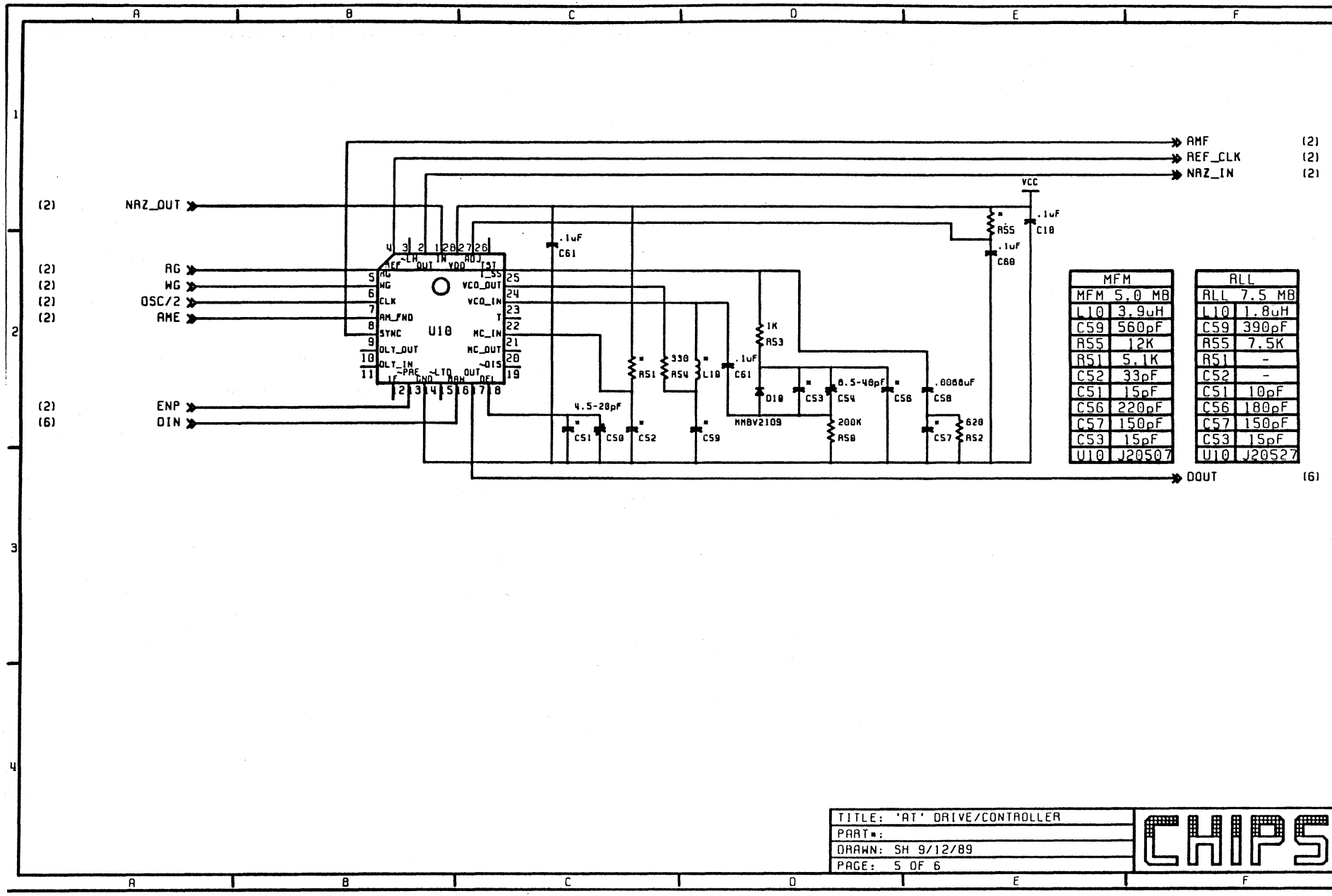

MFM	
MFM 5.0 MB	
L10	3.9uH
C59	560pF
R55	12K
R51	5.1K
C52	33pF
C51	15pF
C56	220pF
C57	150pF
C53	15pF
U10	J20507

RLL	
RLL 7.5 MB	
L10	1.8uH
C59	390pF
R55	7.5K
R51	-
C52	-
C51	10pF
C56	180pF
C57	150pF
C53	15pF
U10	J20527

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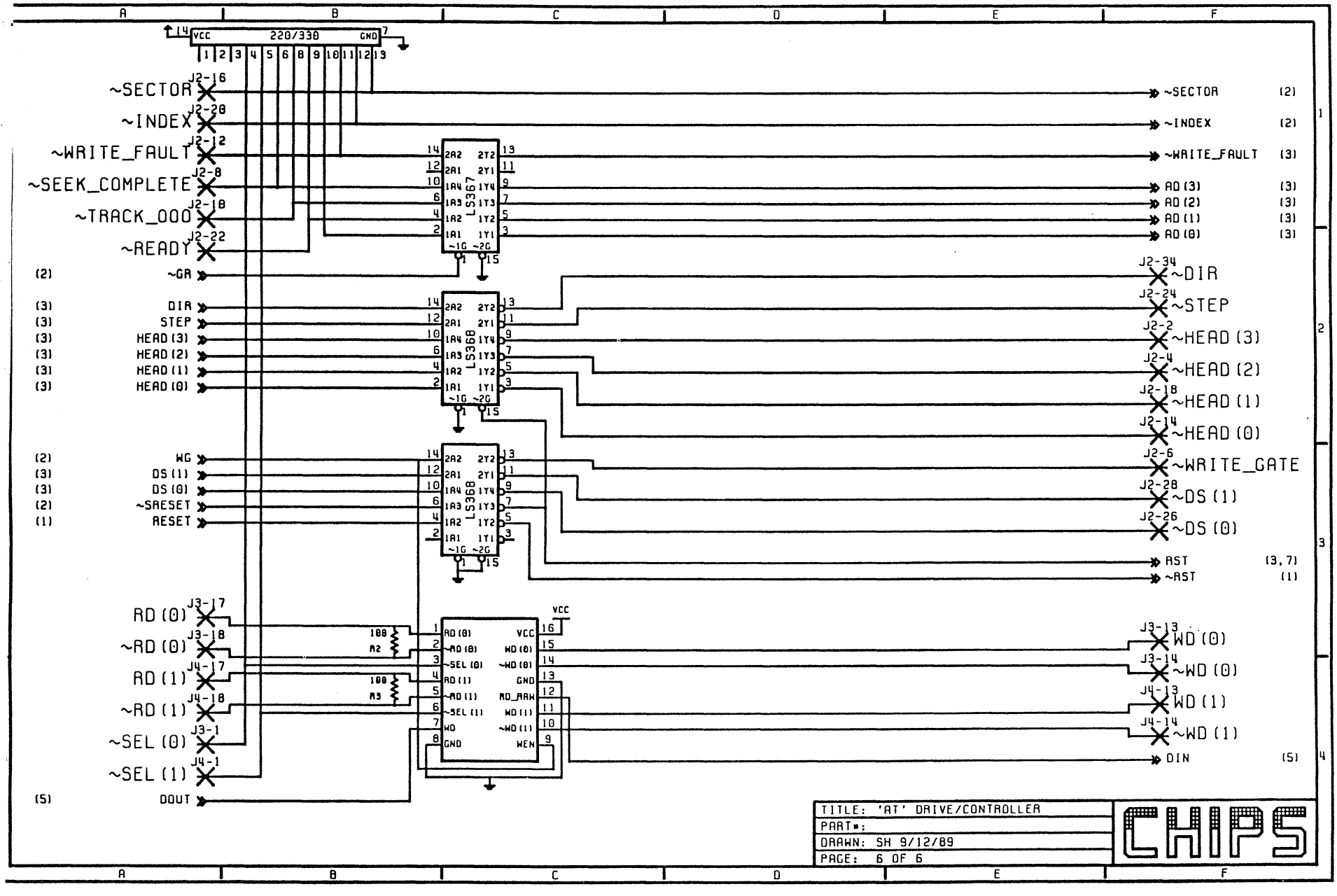
PART#:	
DRAWN: SH 9/12/89	
PAGE: 5 OF 6	CHIPS


VCC
220/330
GND
~SECTOR
~INDEX
~WRITE_FAULT
~SEEK_COMPLETE
~TRACK_000
~READY
~GR
DIR
STEP
HEAD (3)
HEAD (2)
HEAD (1)
HEAD (0)
WG
DS (1)
DS (0)
~SRESET
RESET
RD (0)
~RD (0)
RD (1)
~RD (1)
~SEL (0)
~SEL (1)
DOUT
LS367
LS368
LS368
100
R2
100
R3
~SECTOR (2)
~INDEX (2)
~WRITE_FAULT (3)
AD (3) (3)
AD (2) (3)
AD (1) (3)
AD (0) (3)
~DIR
~STEP
~HEAD (3)
~HEAD (2)
~HEAD (1)
~HEAD (0)
~WRITE_GATE
~DS (1)
~DS (0)
RST (3, 7)
~RST (1)
WD (0)
~WD (0)
WD (1)
~WD (1)
DIN (5)
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PART#:
DRAWN: SH 9/12/89
PAGE: 6 OF 6
CHIPS

APPENDIX E

CRYSTAL CIRCUIT APPLICATION NOTES

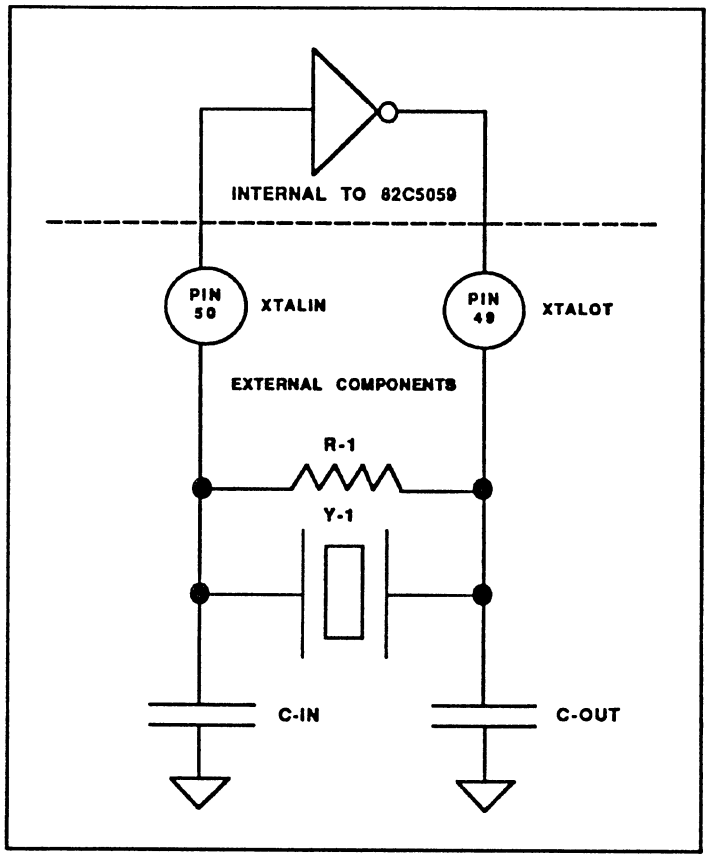

Figure E-1. 82C5059 Crystal Circuit

The crystal Y-1 should be a Series Resonance "AT" cut with an effective series resistance of less than 30 ohms.

For frequenceies less than 24 MHz, a Fundamental Crystal should be used with a R-1 value of 10 Megaohms with a C-IN and C-OUT value of typically 15pF.

For frequencies greater than 24 MHz, a Third Harmonic Crystal should be used with an R-1 value of 4.7 Kohms. The C-IN and C-OUT values are a function of the Crystal used. The most important aspect of the the capacitors are to insure a voltage out swing of at least 3.5 volts. The value of C-IN and C-OUT and their ratio control the gain of the oscillator loop.

As with all analog circuits, printed circuit board layout is very important to minimize both noise and crosstalk. The external components should be located as close as possible to the pins of the device.

A_D	address/data
address	1. a specific location in memory where a unit of data is stored. 2. A disk drive address generally specifies cylinder, head and sector.
address mark	a value used to differentiate between the ID segment and the data segment of the sector.
ANSI	American National Standard for Information Systems.
ASIC	Application Specific Integrated Circuit.
bit	an abbreviation of binary digit, of which there are two possibilities (0 and 1). A bit is the basic data unit of most digital computers. A bit is usually part of a data byte or word, but bits may be used singly to control read logic "on-off" functions.
buffer	a temporary data storage area that compensates for a difference in data transfer rates and /or data processing rates between sender and receiver.
Bus	a length of parallel conductors that forms a major interconnection route between the computer system CPU and its peripheral subsystems.
Byte	a set of binary digits (bits) handled as a unit, usually 8 bits long. One byte is necessary to define an alphanumeric character.
C	centigrade.
CAS	Column Address Strobe. A dynamic RAM input used to store the column address of the RAM matrix.
Channel	a DMA path for access to a memory device.
CMOS	Complementary Metal-Oxide Semiconductor. A technology used in the manufacture of integrated circuits.

CRC	Cyclic Redundancy Check. CRC codes are used for error detection only. Generally, redundancy for these codes is calculated by dividing the data bit stream by a polynomial with binary coefficients which is selected to provide the desired detection capability.
cylinder	a set of disk tracks that are simultaneously under a set of read/write heads. The 3-dimensional storage volume can be accessed with a single head-positioning movement.
data transfer rate	in a disk or tape drive it is the rate at which data is transferred to or from the storage media. It is usually given in thousands of bits per second (kbit/sec.) or millions of bits per second (mbit/sec.).
disk	a flat, circular piece of metal or plastic with a magnetic coating upon which information can be recorded and stored.
DMA	Direct Memory Access.
DRAM	Dynamic Random Access Memory.
ECC	Error Correction Code. Codes used for error detection.
EDAC	Error Detection And Correction.
ESDI	Enhanced Small Device Interface.
FDC	Floppy Disk Controller.
format	in a disk drive, the arrangement of data on a storage media.
head	the electromagnetic device that writes (records), reads (plays back), and erases data on magnetic media.
I/O	input/output.
ID	indentifier.
ID Header	that portion of an ID segment that identifies the cylinder head and sector.
index	usually a mechanical sensor, or an output of a mechanical sensor, on a disk drive to generate one pulse per revolution. It is utilized as a reference point on the track format.

mA	milliamp.
MAX	maximum.
MFM	Modified Frequency Modulation. A method of encoding a digital data signal for recording on magnetic media.
MHz	megahertz.
MIN	minimum.
NRZ	Non-Return to Zero.
ns	nanosecond.
parity	a computer data checking method using an extra bit in which the total number of binary 1's (or 0's) in a byte is always odd or always even; thus, in an odd parity scheme, every byte has eight bits of data and one parity bit. If using odd parity and the number of 1 bits comprising the byte of data is not odd, the 9th or parity bit is set to 1 to create the odd parity. In this way, a byte of data can be checked for accurate transmission by simply counting the bits for an odd parity indication. If the count is ever even, an error has occurred.
PIO	Parallel Input/Output.
PLCC	Plastic Leaded Chip Carrier. The 84-pin version of the 5055B is available in PLCC.
PLL	Phase Lock Loop.
postamble	the field on the track format to position a write splice.
preamble	the field on the track format used by the controller PLL to gain frequency and phase synchronization.
PROM	Programmable Read Only Memory.
QFP	Quad-plastic Flat Package.
RAM	Random Access Memory.
RAS	Row Address Strobe. Dynamic RAM input used to store the row address of the RAM matrix.
read	to access a storage location and obtain previously recorded data.
RLL2,7	Run-Length Limited. An encoding process that repositions data bits and limits the length of a string

	of zero bits in order to compress information being stored on disks.
ROM	Read Only Memory.
RR	Read Register.
SCSI	Small Computer System Interface.
Schmidt trigger input signal	an input device that has hysteresis to prevent a slow rise time or noise on a signal causing a glitch.
sector	one segment of a disk.
SERDES	serial to parallel and parallel to serial converter.
SRAM	Static Random Access Memory.
syndrome	1. A symbol or set of symbols containing information about an error or errors. 2. The remainder of a read long operation used to correct an error in the data field.
TA	temperature ambient.
track	recording path formed when magnetic media moves past a head. Disk tracks are shaped like concentric rings.
transfer count	a counter used to keep track of the number of bytes per sector when reading or writing data.
V	voltage.
VCO	variable control oscillator.
Vdd	drain DC voltage.
Vss	Ground.
WR	write register.
write	to access a storage location and store data on the magnetic surface.
-	a minus sign prefix to a signal name indicates an active low polarity.
+	a plus sign prefix to a signal name indicates an active high polarity.

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