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PROPRIETARY INFORMATION

82C780 MICROCHANNEL™ HARD DISK CONTROLLER
PRELIMINARY SPECIFICATION

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MICROCHANNEL ST506 HARD DISK CONTROLLER

INTRODUCTION

The HDC is a highly integrated VLSI single chip disk controller that provides the read, write, format interface to mass-storage devices while providing the interface to the Microchannel at the other end.

The HDC is capable of achieving one to one sector interleave including track/head switching. It works in conjunction with a local microcontroller, and the Data Seperator to provide Hard Disk Controller functions. This includes DMA, Buffer management, Register file, and micro-channel functions for the PS/2 Hard Disk Controller. The micro-channel interface works in two modes, selectable by a pin on the chip. These are the Normal ST506 mode and the extended mode for ST506-2,7 RLL/ESDI, which will allow support for an on board ROM.The device facilitates achieving 1:1 interleave, at any host transfer rate. The chip operates with a 12 Mhz clock supporting disk data rates upto 15 Mbits/s and host transfer rates upto 5 Mbytes/s.

KEY FEATURES

-LOW POWER CMOS 1.5 u TECHNOLOGY, 144 QFP

-5V SINGLE POWER SUPPLY.

-SUPPORTS 1:1 INTERLEAVE.

-DISK DATA RATES UPTO 15 MBits/Sec.

-SUPPORTS 32-bit & 48-Bit PROGRAMMABLE ECC .

-PROVIDES HARDWARE SUPPORT FOR ERROR CORRECTION.

-SUPPORTS PS/2 ST-506 REGISTER FILE.

-COMPATIBLE TO 8751 & 68HC11 MICRO-CONTROLLER FAMILY.

-INTERRUPT AVAILABLE TO LOCAL CPU.

-DIRECT INTERFACE FOR ST506/ESDI DRIVES

-PROVIDES DUAL BRANCH REGISTERS FOR MINIMUM POLLING BETWEEN COMMANDS.

-SEQUENCER RAM SPACE OF (30 X 4) bytes

-ON BOARD MICROCHANNEL ARBITRATION AND BUS ACQUISITION LOGIC

-ON BOARD POS 102 & 103 REGISTERS.

-PROGRAMMABLE BURST LENGTH.

-PROVIDES ADDRESS GENERATION DURING LOCAL CPU BUFFER ACCESSES WITH OPTIONAL AUTO-INCREMENT CAPABILITIES.

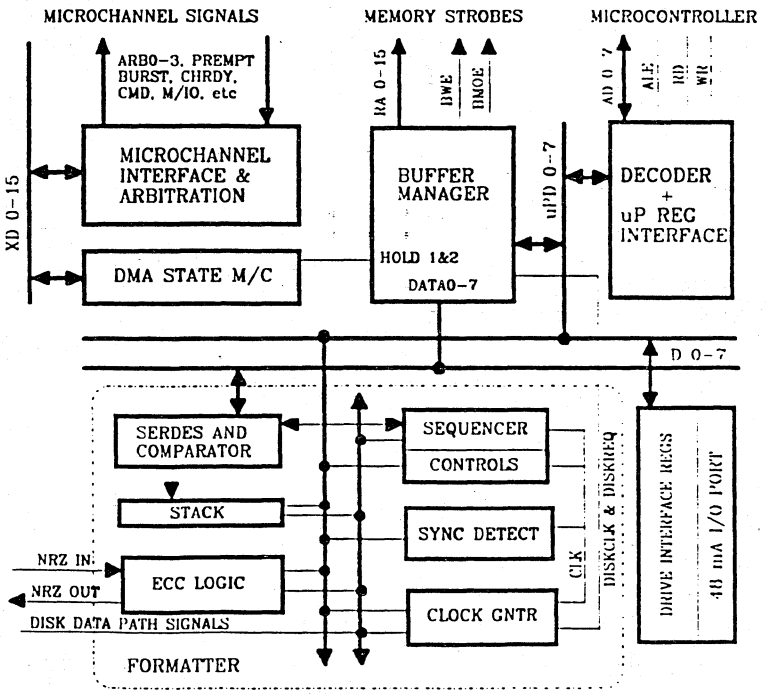
-ADDRESSES UPTO 64K OF BUFFER RAM.

-ON BOARD REGISTER FILE FOR COMMAND AND STATUS.

-SLAVE DMA CONTROLLER SUPPORTS UPTO 5 MBYTES/SEC MICRO-CHANNEL BANDWIDTH

-PROGRAMMABLE CARD ID FUNCTION

INTERNAL BLOCK DIAGRAM OF THE 82C780



FUNCTIONAL DESCRIPTION

The HDC consists of two major functional blocks :

1) Formatter.
2) The Slave DMA/Buffer Controller.

1) FORMATTER

This consists of the following blocks.

- Serializer-Deserializer (SER-DES).
- Sequencer.
- Local Microprocessor Interface Logic.
- Error Detection and Correction Logic (ECC).
- Clock generator.

- Serializer-Deserializer

The SERDES logic de-serializes NRZ data or serializes parallel data into serial NRZ data. This logic also performs the compare functions for the Sync detect, and the ID/Header field.

- Sequencer

The sequencer supports all the sequencing functions needed during disk accesses excluding the Disk Interface controls. It is a WCS based sequencer which is programmed thru the local CPU.

- Local Micro-Processor interface

The local CPU interface logic provides all function enabling the local CPU to read write on-board registers for internal use, generating drive interface signals, and transferring data from the Local Buffer. Optionally local CPU access of the sector buffer will auto increment the pointers. It has dual conditional branch registers to pipe-line the loading of these registers. Provides optional interrupts for local CPU on completion of operation.

- Error Correction and Detection Logic

The 48-bit ECC logic provides the syndromes for data being written into the disk and also checks data during disk reads and if a single, double-burst error is detected within a correction span of 8-bits, it provides the hardware support for easier correction by the local CPU.

- Clock Generator Logic

The Clock Generator Logic provides synchronisation between the sequencer and the slave DMA controller.

2) DMA/BUFFER CONTROLLER

This section consists of the following blocks.

- SLAVE DMA Logic.
- PS/2 Register File.
- RAM Address generation Logic.
- RAM Control Logic.
- Data pipeline
- The BUS ACQUISITION logic.
- The BUS ARBITRATION logic.
- The POS REGISTERS including Card ID Reads.
- ROM SUPPORT

-SLAVE DMA

Slave DMA logic provides the handshake between Buffer Manager and the interface logic which talks to the Microchannel. The DMA logic monitors the state of the PREMPT- line to manage the data path and successfully recover from pre-emptions. An 8-byte deep pipe-line facilitates 8/16 bit data transfers between host and buffer.

-PS/2 REGISTER FILE

PS/2 register file provide logic and the registers for the transfer of status and control information to and from the the Host. These registers are accessible by programmed I/O and are relocatable to a fixed address.

-The following registers are available.

-Control	Host Write
-Status	Host Read CPU Write
-Attention	Host Write CPU Read
-Interrupt Status	Host Read CPU Write

- ADDRESS GENERATION LOGIC

Address Generation Logic consists of two 16-bit pointers externally loadable from the local micro-controller. These pointers manages the host and disk data areas in the buffer. In addition there is a buffer size register that will support a true ring buffer. These pointers increments on the completion of each word/byte transfer from disk to buffer and host to buffer.

- RAM CONTROL LOGIC

Ram Control Logic generates all the strobes needed to read and write from the Buffer Ram, during DMA and CPU access of the Sector buffer.

- DATA PIPE-LINE

Data Pipe-line facilitates the maintenance of high bus transfer rates in both byte and word mode.

- BUS ACQUISTION Logic

The Bus Acquistion Logic provides the PREMPT- and BURST- signals requesting and during a DMA transfer.

- BUS ARBITRATION LOGIC

The Bus Arbitration Logic implements the arbitration protocol set forth by IBM for the Micro-channel. The priority is set by the Arbitration I.D. bits in the POS 103 register.

- THE POS REGISTERS

-The POS 002 register sets various mode on the chip.
-The POS 003 registers which is user writable sets the arbitration level, and burst length for the controller.
-The POS 004 registers is used for Memory address relocation in the Extended mode.
-The CARD ID read-back is enabled from decode POS000 & decode POS 001 and works with the preset registers to provide the 16 bit CARD-ID on the lower 8-bit data-bus byte by byte. This ID bit wii be set by the local CPU on power-up. The external drivers are then enabled to drive the ID on the bus.

-ROM ADDRESSING SUPPORT

This block enables the host read BIOS or other tables from the on the board ROM. It generates the Chip Select, and the output enables.

REGISTER DESCRIPTION

FORMATTER SECTION

REG 49H (Read only)
Drive interface status, a read of the I/O port provided. (LOCAL CPU ACCESSIBLE ONLY)

REG 48H (Write/Read)
Contains the value for driving the I/O port in the output mode, and reads I/O port in input mode.

REG 4AH (Write-only)
Controls the direction for I/O, for register 48H, e.g. REG 4AH Bit 0 controls whether REG48 bit 0 is writable or read only. Consequently, this controls the I/O pin assigned to it. The written value if in output mode will go to the pin.

REG 4C-4D: ECC ERROR LOCATION COUNTER (Read/Write)
16 bit counter from bit 15 to bit 0.

REG 70H: BUFFER DATA: (Read/Write)
The data in this register maps into the sector buffers at the address location set in the hostpointer. The pointers will optionally auto increment after an access is made, to + 1 location.

REG 71H: ECC CONTROL REGISTER. (Write only)
This register sets the controls for ECC, and selects the length of the ECC polynomial.

BIT(0) = Serial ECC input.
BIT(1) = Shift control.
BIT(2) = Disable ECC Feedback.
BIT(3) = Clear ECC.
BIT(4) = Enable Sector Branch.
BIT(5) = Chip reset.
BIT(6) = ECC reset and preset.
BIT(7) = Polynomial Length.

Bit(0): ECC bit 0 is loaded with this bit when Reg 71H Bit(1) and Reg 71H Bit (2) should be set. The Read-gate and Write-gate pin should be inactive and the Read Reference clock (RRC) should be toggling.
Bit(1): When set sends a shift pulse to the ECC registers. The bit is cleared after shift pulse is sent out.
Bit(2): The ECC polynomial registers function as a shift register when this bit is set.

Bit(3): The ECC registers are set /cleared (1/0) depending on polarity of Reg71(6) whenever this bit is set.

Bit(4): This will enable the sequencer to branch on the Sector input whenever this bit is set.

Bit(5): Hardware reset or a write to this register will cause this bit to set, which will be cleared by writing a "zero" into this register.

Bit(6): This when set will cause the polynomial registers to be initialised to "zero", and when reset will cause a initialisation of "one".

Bit(7): When set causes the polynomial length to set to 32-bit ECC mode, otherwise when cleared will select the 48-bit ECC mode.

REG 72H: ECC STATUS (Read only).

This register gives the status on the lower 24 bits of syndrome after a disk read.

BIT(0) = 48/32 bit ECC syndrome (OR of the syndrome bits)
BIT(1) = ---- |
BIT(2) = ---- |
BIT(3) = ---- |
BIT(4) = ---- |---------48/32 BIT ECC SYNDROME.
BIT(5) = ---- |
BIT(6) = ---- |
BIT(7) = ---- |

Bit(0): This bit reflects the 48/32 bit syndrome depeding on the selection. An non-zero syndrome will set this bit.

Bit(1) thru Bit(7): These bits reflect the ECC bits 33 thru 39 for a 48 bit ECC, and ECC bits 17 thru 23 for 32 bit ECC.

REG 72H: POLYNOMIAL (1-8) (Write only)

Each of these bits correspond to the feed-back path being enabled. If Bit 0 (poly bit 1) is set in this register, the output (ECC Bit (47)) will be XORed with the serial data-in which is then XORED with ECC Bit (0) and the result is shifted into ECC Bit(1). These bits represent bit 1 thru 8 of the 48-bit ECC, the ECC bit 8 is the Bit(7) of this register. Set to zeroes, when selecting 32-bit ECC.

REG 73H: ECC STATUS (UPPER 8 bits) (Read only)

This register gives the status on the upper 8 bits <31-24> of the syndrome in the 32 bit mode and <47-40> in the 48-bit mode after a disk read. Bit 47/31 (48/32) corresponds to Bit 7 of the register. Set to 08h when selecting 32-bit ECC.

REG 73H: ECC POLY (9-16) (Write only)

Same function as Write only Register 72H but for 9 thru 16. Represent Bits 9 thru 16 for 48 bit polynomial . MSB is the bit 16 of the 48-bit ECC polynomial.

REG 74H-REG 77 : ECC POLYNOMIAL REGISTERS: (Read/Write)

These registers set up the ECC polynomial.

REGISTER	48-bit ECC (LSB-MSB)	32-bit ECC (LSB-MSB)
74H	Bits 17-24	Bits 1-8
75H	Bits 25-32	Bits 9-16
76H	Bits 33-40	Bits 17-24
77H	Bits 41-47	Bits 25-31

REG 78H: BRANCH ADDRESS REGISTER: (Read/write)

A write to Bit (4 - 0) should consist of the sequencer branch address it will go to, once the conditions is met. The addresses can pre-loaded sequentially for two branches and would be executed in the load sequence. Register 79 bit 3 will contain information related to which branch is being currently executed. Register 7AH bit 3 will enable the dual branch register mode. Default is single branch mode.

REG 79H:SEQUENCER START ADDRESS: (Write)

Any write to this register will start the sequencer. The lower five bits indicates the Sequencer start address.

BIT(0) = -----|
BIT(1) = ---- |
BIT(2) = ---- |-------SEQUENCER START ADDRESS
BIT(3) = ---- |
BIT(4) = ---- |
BIT(5) = ---- Reserved
BIT(6) = ---- Reserved
BIT(7) = ---- (CLEAR disables INT1* and SET enables it)

NOTE: When INT1* is enabled, and sequencer starts, it will become active when the sequencer stops. A read of the status in Reg 79 will reset the INT1*.

REG 79H: FORMATTER STATUS (Read only).

This register gives the status on the FORMATTER. A Read of this register will clear INT1* pin.

BIT(0) = COMPARE EQUAL.
BIT(1) = COMPARE LOW.
BIT(2) = ECC ERROR.
BIT(3) = ECC REVERSE SHIFT IS STOPPED.
BIT(4) = SEQUENCER STOPPED.
BIT(5) = BRANCH IS CURRENTLY ACTIVE.
BIT(6) = DATA TRANSFER.
BIT(7) = ADDRESS MARK ACTIVE.

Bit(0): This bit flags the result of compare between the sequencer ram or the ext. buffer ram and the deserialized data from the disk. The bytes that need to compared are enabled thru the sequecer ram. The flag is valid after all the ECC byte has been read in. If set to one means a good compare. This bit is valid after the previous read till the new sequencer jump is executed.

Bit(1): Same as Bit(0) but a set means the Sequencer /Buffer-ram data is greater than the read data.

Bit(2): Will be set if an ECC error has occured. This bit is valid after the previous read till the new sequencer jump is executed.

Bit(4): When set implies the sequencer has stopped.

Bit(3): The bit is set if the sequencer jumps to address 1F. Will be set after a hardware reset.

Bit(5): The bit is set after the sequencer takes a branch, and is cleared by a read to register 79H.

Bit(6): The bit is set during data transfers to and from the external Buffer memory.

Bit(7): The bit is set during address mark operations i.e. The address mark is written or the sync byte is detected. The bit get cleared whenever the ECC bytes are read and written. The stopped condition clears the bit.

REG 7AH:OPERATION CONTROL STATUS: (Read/Write)

This register indicates the status of the INDEX, SECTOR and NRZ pin. The write to this register controls data-file compares, DISKREQ*, and inhibits data-field carry.

BIT(0) = INDEX DETECT.
BIT(1) = SECTOR DETECTED.
BIT(2) = NRZ DATA IN.
BIT(3) = ENABLE DUAL BRANCH REGISTER MODE.
BIT(4) = SEARCH OPERATION.
BIT(5) = SUPPRESS DATA TRANSFER.
BIT(6) = Reserved
BIT(7) = INHIBIT DATA FIELD CARRY.

Bit(0): If set means a new index pulse has been detected since the last REG 7AH read.

Bit(1): If set means a new sector pulse has been detected since the last REG 7AH read.

Bit(2): A rising edge on the NRZ data during RG active time has been detected since the last REG 7AH read.

Bit(3): This enables the dual branch register option

Bit(4): This bit must be set to enable a search operation where the data-field is compared to the read data.

Bit(5): This bit when set will not defeat disk to buffer transfer. Also during WG active time it will write data from sequencer data field.

Bit(7): This bit when set will inhibit any sequencer jumps after a carry of the field counter. The carry causes this bit to clear. This bit can used to increase the sector size above 256 bytes.

REG 7BH:WAM Control (Read/Write)

This register controls Address Mark writes. A bit set in any location in the register enables the WAM* pin during Format (i.e. WG is on) for the specified bit-time. This indicates the endec to delete clock during address mark writes. Bit time 8 to 1 is selected by bit 7 thru 0 in the preceeding order.

REG 7CH:AMD Control (Read/Write)

This register contains the address mark pattern that causes a sync detect if a match is made during when AMD* pin is active.The register 7FH selects the bits to be compared, all the other bits should be set to zero.

REG 7FH:CLOCK CONTROL AND SYNC COMPARE: (Write)

This register controls bits the sync compare willignore and the frequency of DISKCLK* and DISKREQ*.

BIT(0) = ----|
BIT(1) = ----|-------SYNC DETECT CONTROL.
BIT(2) = ----|
BIT(3) = TRISTATE DISKCLK* AND DISKREQ*.
BIT(4) = RRF/DISKCLK* DIVISOR SELECT
BIT(5) = NOT USED.
BIT(6) = ----|
BIT(7) = ----|------SYSCLK/DISKCLK* DIVISOR SELECT.

Bit(0)thru (2): Sync detect controls. These bits select which bits are compared for sync detect. The three bits are encoded <MSB....LSB> as shown :

000 = Do not Compare.
001 = Compare Bit 7 only.
010 = Compare Bit 7 and 6 .
011 = Compare Bit 7 ,6 and 5
100 = Compare Bit 7, 6 ,5 and 4
101 = Compare Bit 7,6,5,4, and 3
110 = Compare Bit 7,6,5,4,3 and 2
111 = Compare all the bits.

REG 7FH: SEQUENCER STACK

A read to this register gives the value at the top of the stack and pops it.

REG 80H-9BH: (Read/Write)

These sequencer ram addresses controls the next address field and the branch conditions.

BIT(0) = -----|
BIT(1) = -----|
BIT(2) = -----|----NEXT ADDRESS.
BIT(3) = -----|
BIT(4) = -----|
BIT(5) = -----|
BIT(6) = -----|----BRANCH CONDITIONS.
BIT(7) = -----|

REG A0H-BBH: (Read/Write)

These sequencer ram addresses is the control byte and it sets and clears the Disk data control signals.

BIT(0) = DATA TRANSFER.
BIT(1) = COMPARE ENABLE.
BIT(2) = OUTPUT.
BIT(3) = INVALID NRZ BIT.
BIT(4) = STACK ENABLE.
BIT(5) = CRC/ECC SELECT.
BIT(6) = -----|
BIT(7) = -----|----READ/WRITE GATE CONTROL.

REG C0H-DBH: (Read/Write)

These sequencer ram addresses sets the repeat count for the current sequencer word, and the data type.

BIT(0) = -----|
BIT(1) = -----|
BIT(2) = -----|-----FIELD COUNT
BIT(3) = -----|
BIT(4) = -----|
BIT(5) = SEBCRA/ FIELD CNT BIT 5
BIT(6) = ECC/ FIELD CNT 6
BIT(7) = ADDRESS MARK/ FIELD CNT BIT 7

REG E0-FD: (Read/write)

These registers contain the data that are needed for comparison, address mark, ID, and Data Marks.

DMA / BUFFER MANAGER SECTION

Registers are 8751 Accessible

BUFFER SIZE REGISTER (READ/WRITE):
This is an 8 bit register that will be initialized to set the sector buffer size to any size from 512 byte to a maximum of 64 K bytes.

HOST POINTER (READ/WRITE):
This is a 16 bit address register that will be initialized to a starting address by the 8751/8051 for buffer access by the host. The register auto-increments after each access by the host and local CPU. The auto-increment for local CPU can be disabled. The registers are split into an upper and a lower byte. Reset to all zeros.

DISK POINTER (READ/WRITE):
This is a 16 bit address register that is initialized to a starting address by the 8751/8051 for buffer accesses by the formatter. The register auto-increments after each access by the host or the disk.This register is split into upper and a lower byte. Reset to all zeros.

DMA REGISTER: (READ/WRITE):
This register is used by the Slave DMA Control logic for requesting the bus and setting up the direction of transfer. Reset to all zeros.

DMA STOP POINTER (READ/WRITE):
This register controls the byte count for the DMA and is a 16-bit register split into an upper and lower byte, with different addresses.

CARD ID REGISTER:
Written by 8751/8051 after power up to provide card identification to the host. It consists of an upper byte and a lower byte at different addresses for the 8-bit data bus. When the host reads this register the ID is forced on Lower 8-bit bus co-ordinated to the POS 100 and 101 reads. It takes two reads to read the whole word.

BUFFER ACCESSES:
During Buffer Memory accesses from the local CPU the HDC will provide address to the buffer.

REGISTERS ACCESSIBLE BY HOST AND 8751

CONTROL REGISTER:(322/32A) (WRITE ONLY from the HOST)

Pass control information to the controller. The bit definitions are as follows.

Bit 0: DMA/PROGRAMMED I/O.
Bit 1: Interrupt Enable.
Bit 2: 16-bit Mode
Bit 3: Reserved.
Bit 4: Reserved.
Bit 5: 16-bit mode.
Bit 6: Reserved.
Bit 7: Reset.

Bit(0): DMA/PIO This bit when set selects the DMA mode, on the chip for data, and command block transfers. When reset the programmed I/O mode is selected for data and command blocks at address zero of the selected I/O space.

Bit(1): When set this enables the interrupt request pin, IRQ14-, to the host.

Bit(2): When set this bit in conjunction with bit 5 selects the 16-bit mode for data-transfers.

Bit(3): Always set to zero.
Bit(4): Always set to zero.

Bit(5): When set this selects 16-bit mode for data transfers.

Bit(6): Always set to one.

Bit(7): When set resets the adapter. Not self clearing.

STATUS REGISTER:(322/32A) (READ ONLY from HOST)

Sends out completion or controller fault, status to the host. Written by the Local CPU. The bit definitions are as follows. The bit definitions are as follows.

Bit 0: Transfer Enable.
Bit 1: Interrupt Request.
Bit 2: Busy.
Bit 3: Direction.
Bit 4: Data Request.
Bit 5: 16-bit mode.
Bit 6: Reserved.
Bit 7: Reserved.

Bit(0): This bit when set to one indicates data transfers to/from the host in progress. This bit is set and cleared internally during a transfer.

Bit(1): This bit when set indicates an interrupt request to the host.Set by a write to DMA control register (0D) bit 7and cleared by a read of the Interrupt Status Register (324).

Bit(2): This bit when set indicates the adapter is busyand no attempt should be made to write to the attention register till it goes to a zero. The bit is set when the attention register is written into and cleared by writing to DMA Control Register (0D). On power-up this bit will come up as a high till the software clears it.

Bit(3): This bit when set indicates, the adapter set up for a DMA/PIO read to the host. When reset it indicates a DMA/PIO write from the host This bit shows the sense DMA control register (0D) bit (2-3) .

Bit(4): This bit when set indicates a data transfer is being requested to or from host. This bit only used during PIO modes, and the host shall only begin transfer after it sees this bit set. Set by writing a one to bit 5 of the DMA control register. Cleared on termination of DMA.

Bit(5): When set indicates the adapter is in 16-bit mode. When reset indicates an 8-bit mode.

ADAPTER ID : (Read by POS 100 & POS 101 Read).

The Card ID is written by the Local CPU (REG 0B & 0C) to these Registers which is driven to the lower 8-bit Host Data bus by the POS 100 & 101 Reads. Software reset will not clear the card ID register.

ATTENTION REGISTER:(324/32C) (Written from Host)
Passes Command to the controller read by the CPU. The bit definitions are as follows.

Bit 0: Abort.
Bit 1: Reserved.
Bit 2: Drive Select.
Bit 3: Reserved.
Bit 4: Ready.
Bit 5: Sense Summary Block.
Bit 6: Command Specify Block.
Bit 7: Command Control Block.

Bit(0): When set this will cause an command abort and will cause an interrupt to happen after completion of abort sequence. This will force the adapter to re-calibrate whenever a new command is issued, however the command specify block will remain valid.
Bit(2): When set Drive#1 is selected, when cleared it indicates Drive#2 is selected.
Bit(4): When set this will indicate to the adapter that it is ready to process the data transfer portion of the read, write and verify command.
Bit(5): When set this will indicate that current sense summary block can be transferred to the system.
Bit(6): When set this will indicate that command specify block will be transferred from the system.
Bit(7): When set this will indicate that a command control block is ready to be transferred. The adapter will then transfer the block from the system.
Bit(1&3): Always in the zero state.

INTERRUPT STATUS : (324/32C)(Read by the Host)
Passes Interrupt information to the host. Written by the Local CPU. Any read to this register clears the interrupt bit in Adapter Status Register.The bit definitions are as follows.

Bit 0: Equipment Check.
Bit 1: ECC invoked.
Bit 2: Drive Selected.
Bit 3: Reserved.
Bit 4: Reserved.
Bit 5: Command rejected.
Bit 6: Invalid Command.
Bit 7: Terminal Error.

Bit(0): When set it indicates that there has been an internal error on the adapter.
Bit(1): When set this indicates an ECC error has occurred and if set in conjunction with bit (7) it means an irrecoverable error has occurred in the data or ID field.
Bit(2): This bit reflects Attention Register Bit(2), to indicate the current Drive Selected.
Bit(5): This bit when set indicates a command control block is not executable because there is no command specify block relating to it. This bit will be set if a sense summary block command is issued while reset is pending.
Bit(6): This bit when set indicates a invalid command was given to the adapter.
Bit(7): This bit when set indicates a fatal error has occurred on the drive or the controller.

8751--LOCAL CPU ACCESSIBLE REGISTERS

BUFFER SIZE REGISTER: REG 01 (7-0)
This register will be programmed to correspond to the buffer size shown below.

00H = 512 BYTES
01H = 1K BYTES
03H = 2K BYTES
07H = 4K BYTES
0FH = 8K BYTES
1FH = 16K BYTES
3FH = 32K BYTES
7FH = 64K BYTES

HOST-POINTER: REG 02 (7-0)
This register will be loaded with the lower byte of the buffer ram starting address dedicated to the Host transfers. Should be loaded with an even address for the start point.

HOST-POINTER: REG 03 (7-0)
This register will be loaded with the upper byte of the buffer ram starting address dedicated to the Host transfers.

DISK-POINTER: REG 04 (7-0)
This register will be loaded with the lower byte of the buffer RAM starting address dedicated to the DISK transfers.

DISK-POINTER: REG 05 (7-0)
This register will be loaded with the upper byte of the buffer ram starting address dedicated to the DISK transfers.

LOWER HOST STOP-POINTER: REG 06 (7-0)
This register will be loaded with the lower byte of the buffer ram starting address dedicated to the Host transfers.

UPPER HOST STOP-POINTER: REG 07 (7-0)
This register will be loaded with the upper byte of the buffer RAM starting address dedicated to the Host transfers.

WRITE BYTE COUNTER: REG 08 (7-0)
This register will contain the number of bytes to be transferred during DMA or PIO writes. The binary value shall be the required byte count. e.g. FF shall indicate 255 bytes. This in conjunction with REG 0F Bits 5,6,7 forms an eleven bit counter for maximum 2K bytes of transfer.

INTERRUPT STATUS REGISTER: REG 09 (7-0)
This will map into the HOST INTERRUPT STATUS REGISTER.

INTERRUPT CONTROL REGISTER:REG 0A (7-0)
This register when read shows the source of the interrupt, and is cleared by reading and writing back the contents.

Bit(0): When set it means that Interrupt Generated during power up testing and cleared by writing a one to this location.
Bit(1): When set it means the host has written to the attention register, and interrupt is cleared by writing back the contents to this location.
Bit(3): When set it means a host has generated an adapter reset, and interrupt is cleared by writing back the contents to this location.
Bit(5): When set it means the command has been completed by the HOST INTERFACE/BUFFER MANAGER chip, and interrupt is cleared by writing back the contents to this location.
Bits 2, 4, 6, 7 : Reserved

DMA CONTROL REGISTER: REG 0D
This register controls the DMA/PIO operation in conjunction with ADAPTER CONTROL Reg Bit (0).

Bit(0): Reserved
Bit(1): Reserved
Bit(2): When set with bit (3) = zero sets the DMA/PIO transfer direction to Write, by the Host. When set with bit (3) = one toggles from the previous direction. i.e.from write to read or vice versa.
Bit(3): When set with bit (2) = zero sets the DMA/PIO transfer direction to Read by the host. When set with bit (3) = one toggles from the previous direction. i.e. from read to write or vice versa.
Bit(5): Starts the DMA/PIO operation and clears by itself.
Bit(6): Writing a one clears the busy bit in the adapter status register.
Bit (7): Writing a one sets the interrupt request bit in adapter status register. and the IRQ pin if interrupt is enabled.

ATTENTION REGISTER: REG 0E
This register maps the HOST ATTENTION register .

BUFFER MANAGER CONTROL & UPPER BYTE COUNT REGISTER : REG 0F

This register starts the Buffer Manager and setsthe direction of the disk transfer. This register also indicates a completion of DMA/PIO operation. Also includes Bit 8,9,10 of Write byte counter at bit 5,6,7 of this Register.

Bit(1): When set enables auto-increment during REG 70 access.
Bit(2): Read only. This indicates a completion of DMA transfer.
Bit(3): Buffer Manager Start bit. When set turns on the Buffer Manager for a host transfer. Does not have to be re-written once the stopped by completion. Writing into Upper Stop Pointer REG07 clears DMA completion bit and re-starts DMA/PIO. This bit with REG0D bit <3-2> set the host transfer direction.
Bit(4) : This bit when set sets up a disk to buffer operation, and when cleared does a buffer to disk operation. The DISKREQ* initiates the transfer.
Bit (5 to 7): These bits are bits 8,9, and 10 (MSB) of the Write Byte Counter.

PS/2 DRIVE STATUS REGISTERS

These Registers are selected by the Host to read the ST506 Drive Status, or directly monitor the Drive Controls & Faults.

DRIVE STATUS0 (ADDRESS 326/32E) (* alternate address calculated *)

Bit 0: -DRVSEL0
Bit 1: -DRVSEL1
Bit 2: -STEP
Bit 3: -DIRECTION
Bit 4: -HDSEL0
Bit 5: -HDSEL1
Bit 6: -HDSEL2
Bit 7: -HDSEL3

DRIVE STATUS1 (ADDRESS 327/32F)

Bit 0: -INDEX
Bit 1: -TRACK0.
Bit 2: -WRTFLT
Bit 3: -SEEKCMP
Bit 4: -READY
Bit 5: -WRITE GATE
Bit 6: -Reserved - set to 0
Bit 7: -Reserved - set to 0

POS REGISTER DESCRIPTIONS

POS 000 Card Id Lower Byte

POS 001 Card Id Upper Byte

POS 002

Bit 0: Card Enable
Bit 1: Alternate address for IO
Bit 2: Arbitration Method (fairness)
Bit 3: Burst Mode
Bit 4: Reserved
Bit 5: Arbiter Reset
Bit 6: Relocate bios from 0C8000H to new as shown in table for POS 004.
Bit 7: Reserved

Bit(0) = When set enables the Adapter.
Bit(1) = When set, sets the alternate addresses for the Hard-Disk Interface Registers in the HDC.
Bit(2) = When set the Fairness is disabled. i.e. thedevice will be able to compete in the next arbitration, and can therefore HOG the bus. If fairness is enabled the HDC, will not be to compete till the next arbitration cycle.
Bit(3) = When set the HDC will work in the Burst mode, and the Burst length will depend on the programmed value in POS103 bits <7-4>. When cleared will cause it to work in the single burst mode.
Bit(5) = When set this generates an Arbiter Reset.
Bit(6) = When set will relocate to on board ROM to addressshown by POS register 004 bits (2-0).
Bit(4, 6 & 7) = Should be cleared to Zero.

POS 003

Bit 0-3:Arbitration Level
Bit 4-7:Burst Length

Bit(0-3) = This sets the arbitration level from "F" to "0". Where 0 is the highest and F is the lowest priority.During Arbitration Cycle this is ARBITRATION I.D. forced by HDC on to the ARB bus. (ARB00-03)

Bit(4-7) = This sets the burst length of each transfer given by 2 to n -1 i.e.The binary value will indicate one less than length of transfer in words or bytes.

POS 004

This register contains the relocation decodes for the BIOS EPROM.
Bit (0-2) will select the ROM segment address.

B2	B1	B0	ADDRESS RANGE
0	0	0	0C0000-0C3FFF
0	0	1	0C4000-0C7FFF
0	1	0	0C8000-0CBFFF
0	1	1	0CC000-0CFFFF
1	0	0	0D0000-0D3FFF
1	0	1	0D4000-0D7FFF
1	1	0	0D8000-0DBFFF
1	1	1	0DC000-0DFFFF

ADDRESS DECODES FOR PROGRAMMABLE OPTION SELECT (POS) REGISTERS

CDSETUP-(n)	A2	A1	A0	
0	0	0	0	POS 000
0	0	0	1	POS 001
0	0	1	0	POS 002
0	0	1	1	POS 003
1	X	X	X	not selected

TABLE 1. DECODES FOR M/IO- AND S0-, S1-

M/IO-	S0-	S1-	
0	0	0	RESERVED A.
0	0	1	I/O WRITE
0	1	0	I/O READ
0	1	1	RESERVED B.
1	0	0	RESERVED C.
1	0	1	MEMORY WRITE
1	1	0	MEMORY READ
1	1	1	RESERVED D.

PIN DESCRIPTION

Pin numbers are reflected for Seiko 144 pin QFP package

VCC	126, 20, 54, 90	+ 5V SUPPLY
VSS	134, 13, 27, 41, 50, 83, 99, 122	GROUND
NC	1, 2, 3, 37, 71, 72, 106, 107, 108, 109, 143, 144	

PIN-NAME	TYPE	PIN#	DESCRIPTION
MICRO-BUS INTERFACE (8751)			
RD-	I	111	MICRO-CONTROLLER READ
WR-	I	112	MICRO-CONTROLLER WRITE
ALE	I	130	ADDRESS LATCH ENABLE FROM MICROCONTROLLER FOR EXTERNAL REGISTER ACCESS.
AD0	I/O	116	ADDRESS DATA 0-7 MULTIPLEXED U-BUS
AD1	I/O	117	
AD2	I/O	118	
AD3	I/O	119	
AD4	I/O	125	
AD5	I/O	127	
AD6	I/O	128	
AD7	I/O	129	
INT0-	O	114	INTERRUPT TO 8751
INT1-	O	113	INTERRUPT TO 8751
CS1	I	115	CHIP SELECT1 PORT OUTPUT FROM 8751
X1	I	105	CRYSTAL INPUT DRIVING THE OSCILLATOR/CLOCK
X2	I	104	GENERATOR, MAX CLOCK INPUT OF 12 MHZ
CLKOUT	O	103	CLOCK OUTPUT TO MICROCONTROLLER.

PIN-NAME	TYPE	PIN#	DESCRIPTION
BUFFER-MANAGER PINS			
BMOE-	O	91	BUFFER MEMORY OUTPUT ENABLE
BWE-	O	92	BUFFER WRITE ENABLE
RA0	O	78	BUFFER RAM ADDRESS 0 THRU 15
RA1	O	79	
RA2	O	80	
RA3	O	81	
RA4	O	82	
RA5	O	84	
RA6	O	85	
RA7	O	86	
RA8	O	87	
RA9	O	95	
RA10	O	96	
RA11	O	97	
RA12	O	98	
RA13	O	100	
RA14	O	101	
RA15	O	102	
RDATA0	I/O	94	THESE PINS CONTAINS DATA TO BUFFER FROM DISK
RDATA1	I/O	93	AFTER DE-SERIALIZATION DURING READS AND WRITE
RDATA2	I/O	89	DATA FROM BUFFER DURING DISK WRITES.
RDATA3	I/O	88	
RDATA4	I/O	77	
RDATA5	I/O	76	
RDATA6	I/O	75	
RDATA7	I/O	74	
MICRO CHANNEL INTERFACE PINS			
XD15	I/O	9	MICRO-CHANNEL DATA BUS BEFORE THE XCEIVERS
XD14	I/O	10	
XD13	I/O	11	
XD12	I/O	12	
XD11	I/O	14	
XD10	I/O	15	
XD9	I/O	16	
XD8	I/O	17	
XD7	I/O	23	

PIN-NAME	TYPE	PIN#	DESCRIPTION
XD6	I/O	24	
XD5	I/O	25	
XD4	I/O	26	
XD3	I/O	28	
XD2	I/O	29	
XD1	I/O	30	
XD0	I/O	31	
IRQ14-	O	43	INTERRUPT REQUEST TO MICRO-CHANNEL
M/IO-	I	36	STATUS: MEMORY CYCLE ON HOST-BUS IF M/IO
S1-	I	38	HIGH AND I/O CYCLE, IF LOW. DECODES ARE AS
S0-	I	39	ATTACHED IN TABLE 1.
ARB/GNT-	I	40	ARBITRATION CYCLE IF HIGH, BUS-GRANT IF LOW
ARB00	I/O	47	FORCED AND READ BY CHIP TO DETERMINE
ARB01	I/O	46	ARBITRATION STATUS.
ARB02	I/O	45	
ARB03	I/O	44	
PREMPT-	I/O	49	READ TO DETERMINE IF REQUEST IS BEING MADE FOR THE BUS. DRIVEN TO REQUEST BUS .
BURST-	O	48	DRIVEN TO SIGNIFY A DMA BURST IN PROGRESS
ADL-	I	51	ADDRESS LATCH SIGNAL TO INDICATE VALID ADDRESS AND STATUS BITS ON BUS.
CMD-	I	35	DATA-VALID SIGNAL DIFFERENT TIMINGS FOR READS AND WRITES.
14.3MOSC	I	69	SYNCHRONISING CLOCK FROM SYSTEM.
CD CHRDY	O	33	READY OUTPUT FROM CONTROLLER.TO INSERT WAIT STATES FOR SLOWER I/O DEVICES
CDSFDBK-	O	34	CARD SELECTED FEEDBACK, GENERATEDAFTER THE CHIP DETECTS THAT IT HAS BEEN SELECTED.
CHRESET	I	21	RESET FROM HOST
A4	I	57	A4-A11ADDRESS BITS
A5	I	58	
A6	I	59	
A7	I	60	

PIN-NAME	TYPE	PIN#	DESCRIPTION
A8	I	61	
A9	I	62	
A10	I	63	
A11	I	64	
A0	I/O	52	THIS IS A0 BIT
A1	I/O	53	THIS IS A1 BIT
A2	I/O	55	THIS IS THE A2 BIT
A3	I	56	THIS IS THE A3 BIT
A12	I/O	65	A12 THRU A15 ADDRESS BITS
A13	I/O	66	
A14	I/O	67	
A15	I/O	68	
TEST-MODE	I	73	INTERNAL TEST PIN
SBHE-	I	32	SYSTEM BUS HIGH ENABLE (ACTIVE LOW) ENABLES UPPER BYTE
CDDS16-	I	22	DATA-SIZE OF 16-BITS SELECTED
CDSETUP-	I	70	CARD SET UP FOR POS REGISTERS NEEDS TO BE LATCHED
DEN-	O	19	DATA OUTPUT ENABLE TO BUS TRANSCIEVERS
DT/R-	O	18	DATA TRANSFER DIRECTION ENABLE.

DISK DATA CONTROL

INDEX-	I	139	INDEX PULSE FROM THE DRIVE.(active low)
SECTOR-	I	141	SECTOR PULSE FROM HARD-SECTORED DRIVE
READ GATE	O	7	INDICATES A READ OPERATION IS REQUESTED FROM THE DRIVE.
WRITE GATE-	O	42	INDICATES A WRITE OPERATION TO THE DRIVE.

PIN-NAME	TYPE	PIN#	DESCRIPTION
RRF CLOCK	I	8	IT IS THE PRIMARY CLOCK SYNCHRONOUS TO THE NRZ DATA. IT DRIVES THE INTERNAL LOGIC. THIS CLOCK IS RECOVERED FROM INPUT DATA DURING READS OTHERWISE IS OUTPUT LOCAL OSCILLATOR.
NRZ	I/O	5	SERIAL DATA IN/OUT DURING DISK READS/WRITES.
WAM/AMD-	I/O	6	IT TELLS THE WRITE CHANNEL TO WRITE THE ADDRESS MARK DURING WRITES AND AS AN INPUT INDICATES ADDRESS MARK HAS BEEN FOUND DURING READS.

MISCELLANEOUS PINS

READY-	I	140	DRIVE READY INPUT FROM DRIVE.(Active low)
WRTFLT-	I	138	WRITE FAULT INPUT FROM DRIVES (Active low)
TRK0-	I	137	TRACK ZERO INPUT FROM DRIVES(Active low)
SEEKCMP-	I	131	SEEK COMPLETE INPUT FROM DRIVES (Active low)
DRV0SLD-	I	4	DRIVE ZERO SELECTED (Active low)
DRV1SLD-	I	142	DRIVE ONE SELECTED (Active low)
DIRIN-	O	136	DIRECTION OF SEEK IS TO THE INNER TRACKS (A low)
DSEL0-	O	133	SELECT DRIVE ZERO (Active low)
DSEL1-	O	135	SELECT DRIVE ONE (Active low)
STEP-	O	132	STEP SIGNAL TO THE DRIVE HEAD (Active low)
HDSL0-	O	124	HEAD SELECT LINE ZERO (Active low)
HDSL1-	O	123	HEAD SELECT LINE ONE (Active low)
HDSL2-	O	121	HEAD SELECT LINE TWO (Active low)
HDSL3-	O	120	HEAD SELECT LINE THREE (Active low)
EXTSTAT	I	110	SELECT EXTERNAL STATUS REGISTER

82C780 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	VCC		7.0	V
INPUT VOLTAGE	VI	-0.5	5.5	V
OUTPUT VOLTAGE	VO	-0.5	5.5	V
OPERATING TEMPRETURE	TOP	-25	85	DEG. C
STORAGE TEMPRETURE	TSTG	-40	125	DEG. C

NOTE: Permanent device damage may occur if Absolute Max Ratings are exceeded. Functional operations should be restricted to the conditions described under Operating Conditions.

82C780 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	VCC	4.75	5.25	V
AMBIENT TEMPRETURE	TA	0	70	DEG C

82C780 DC CHARACTERISTICS:

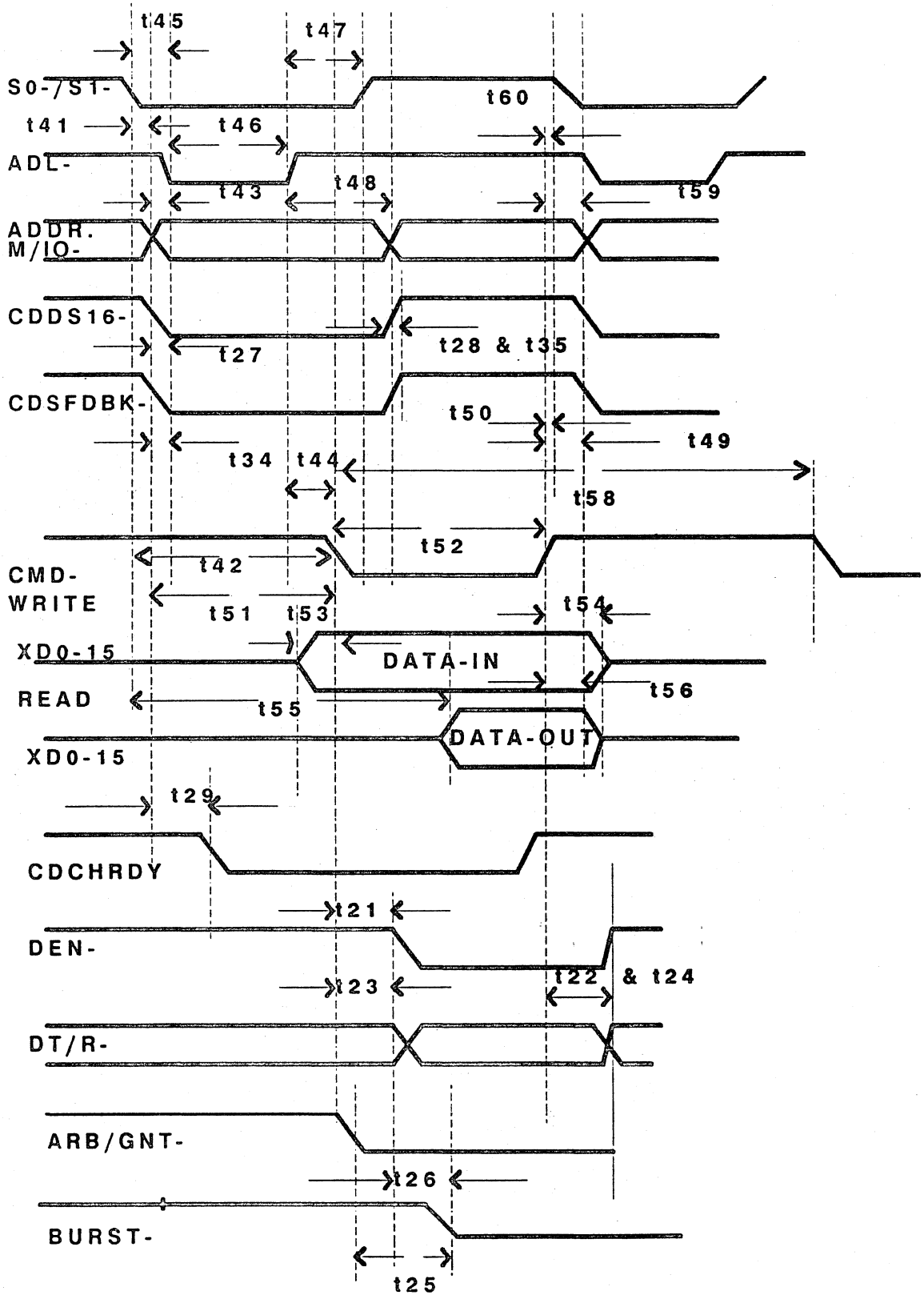
PARAMETER	SYMBOL	MIN	MAX	UNITS
POWER SUPPLY CURRENT	ICC		50MA	
INPUT LOW VOLTAGE	VIL	-0.50	.8	V
INPUT HIGH VOLTAGE	VIH	2.0	VCC+0.5	V
OUTPUT LOW VOLTAGE	VOL	0.4		V
OUTPUT HIGH VOLTAGE	VOH	2.4		V
INPUT LEAKAGE CURRENT For Vin=0 to VCC	IIL	-10	10	UA
OUTPUT TRISTATE LEAKAGE CURRENT for VO=0 to VCC	IOL	-10	10	UA

Note: IOL = 4ma for all pins except PREMPT-,BURST-,ARB00, ARB01,ARB03,ARB04, and IRQ14-. For these pins IOL = 24 ma., and ST506 drive interface pins HDSL0- THRU HDSL3-, DSEL0-,DESL1-,DIRIN,STEP-, DRV0SD-,DRV1SD- and WRITE-GATE-.which are rated at 48 ma at 0.5V

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS
INPUT CAPACITANCE FOR fC = 1MHZ	CIN		10	PF
OUTPUT CAPACITANCES	COUT		35	PF
I/O CAPACITANCES	CI/O		35	PF

MICROCHANNEL TIMINGS



MICROCHANNEL TIMINGS: (ta=0 DEG C TO 70 DEG C VCC=5v +/-5%, Cl=35pf for all outputs except microchannel interface pins, PREMPT-,BURST-,ARB00 thru ARB03 which are rated at 240pf max and CDCHRDY,CDSFDBK-,CDDS16- at 85pf)

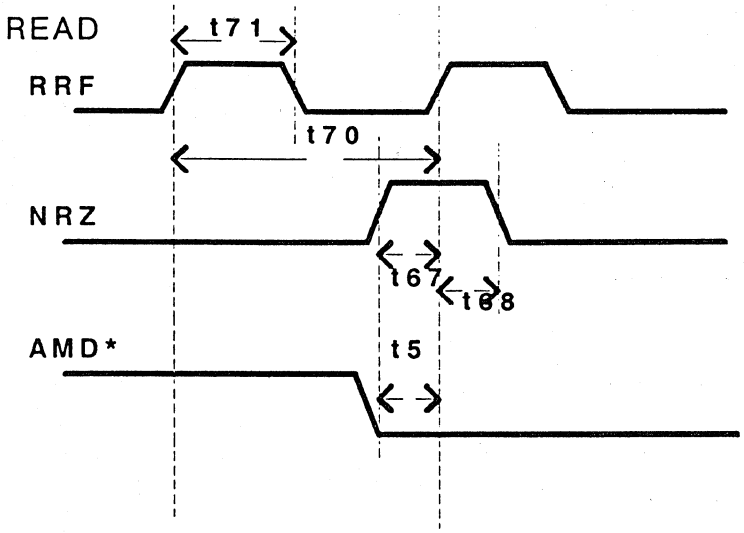
tImings	description	min	max
t21	CMD- V to DT/R- V	-	35
t22	CMD- ^ to DT/R- ^	-	25
t23	CMD- v to DEN- v	-	35
t24	CMD- ^ to DEN- ^	-	25
t25	ARBGNT- to BURST- V	-	25
t26	CMD- to BURST- ^	-	35
t27	M/IO- to CDDS16- v	-	30
t28	M/IO- to CDDS16- ^	-	25
t29	M/IO- to CDCHRDY	-	35
t33	CMD- to CDCHRDY	-	20
t34	M/IO- to CDSFDBK- ^	-	35
t35	M/IO- to CDSFDBK- v	-	30
t36	ARBGNT- to ARBxx	-	60

MICROCHANNEL TIMINGS:

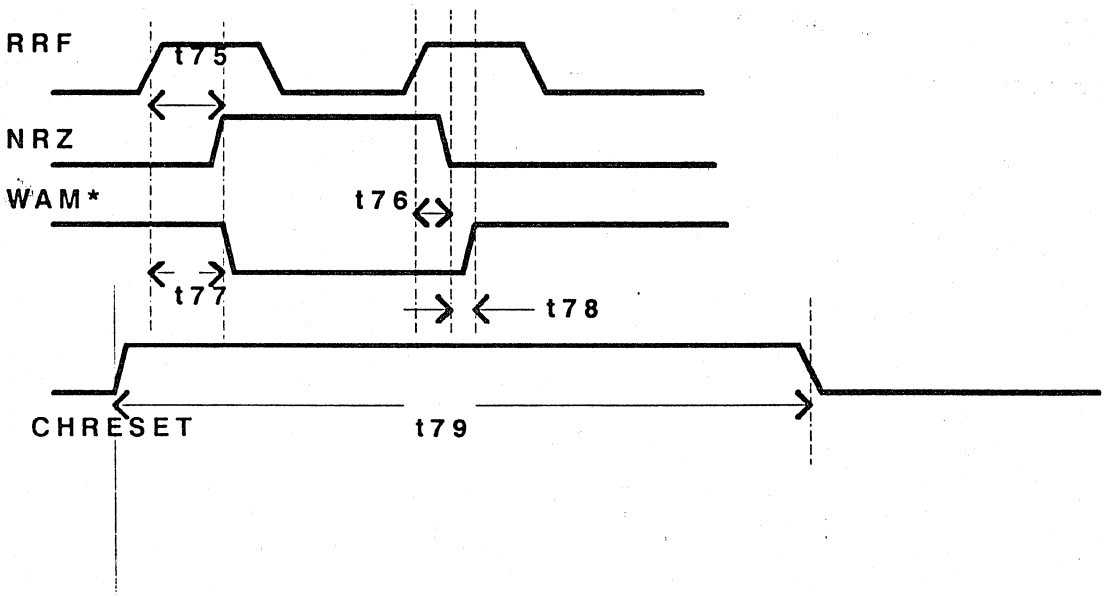
timing	Description	min	max
t41	STATUS ACTIVE FROM ADDRESS M/IO- VALID	10	-
t42	CMD- ACTIVE FROM STATUS ACTIVE	55	-
t43	ADL- ACTIVE FROM ADDRESS M/IO- VALID	45	-
t44	ADL- ACTIVE CMD- ACTIVE	40	-
t45	ADL- ACTIVE FROM STATUS ACTIVE	12	-
t46	ADL- PULSE WIDTH	40	-
t47	STATUS HOLD FROM ADL- INACTIVE	25	-
t48	ADDRESS M/IO- HOLD FROM ADL- INACTIVE	25	-
t49	ADDRESS M/IO- HOLD FROM CMD- INACTIVE	30	-
t50	STATUS HOLD FROM CMD- ACTIVE	30	-
t51	CMD- ACTIVE FROM ADDRESS VALID	85	-
t52	CMD- PULSE WIDTH	90	-
t53	WRITE DATA SETUP TO CMD- ACTIVE	0	-
t54	WRITE DATA HOLD FROM CMD- INACTIVE	30	-

t55	STATUS TO READ DATA VALID	-	125
t56	READ DATA HOLD FROM CMD-INACTIVE	0	-
t57	CMD- ACTIVE TO NEXT CMD- ACTIVE	190	-
t58	CMD- INACTIVE TO NEXT ACTIVE	80	-
t59	CMD- INACTIVE TO NEXT ADL- ACTIVE	40	-
t60	NEXT STATUS ACTIVE CMD- INACTIVE	-	20

DISK DATA TIMINGS.



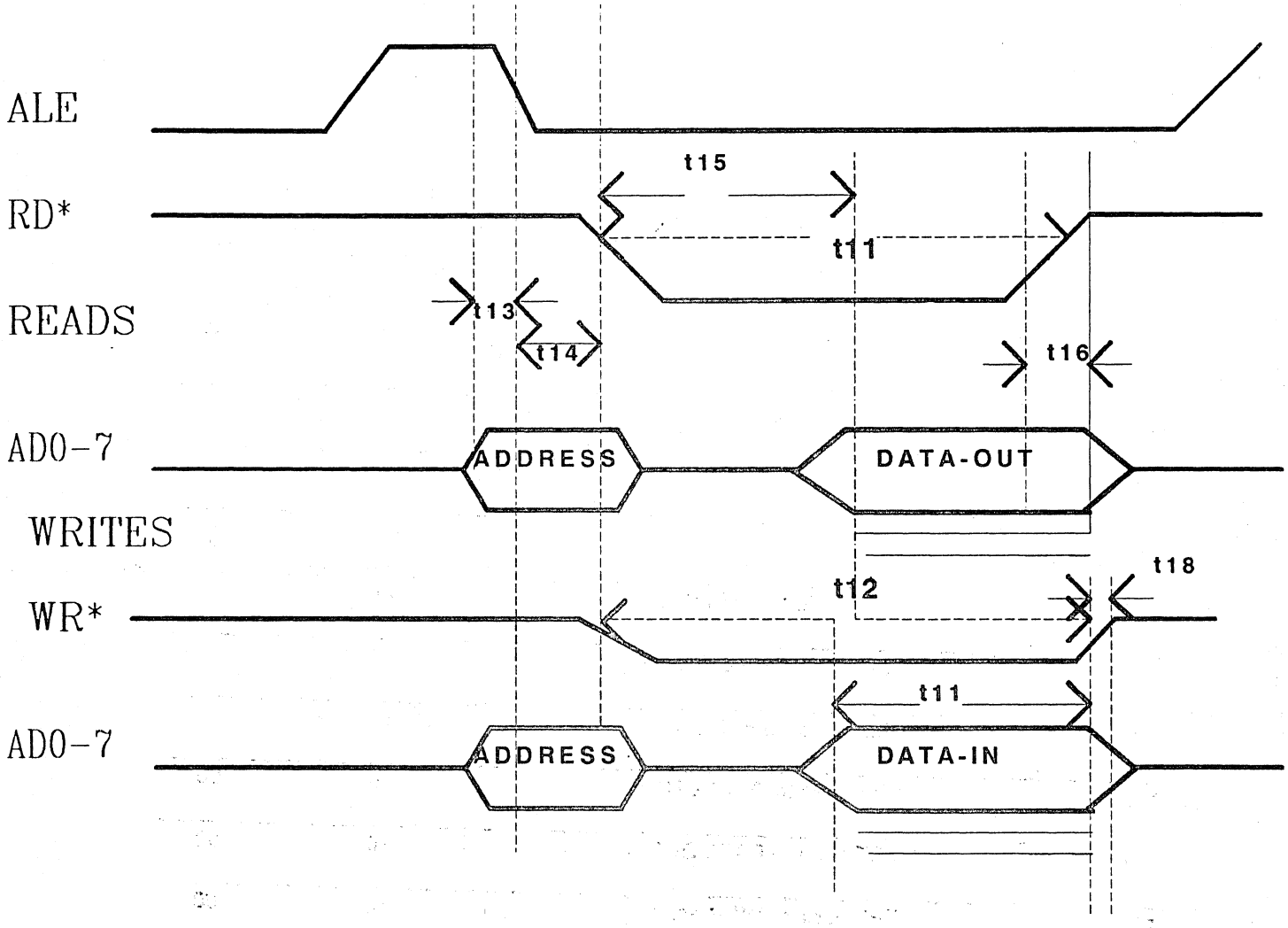
WRITES



DISK TIMINGS:

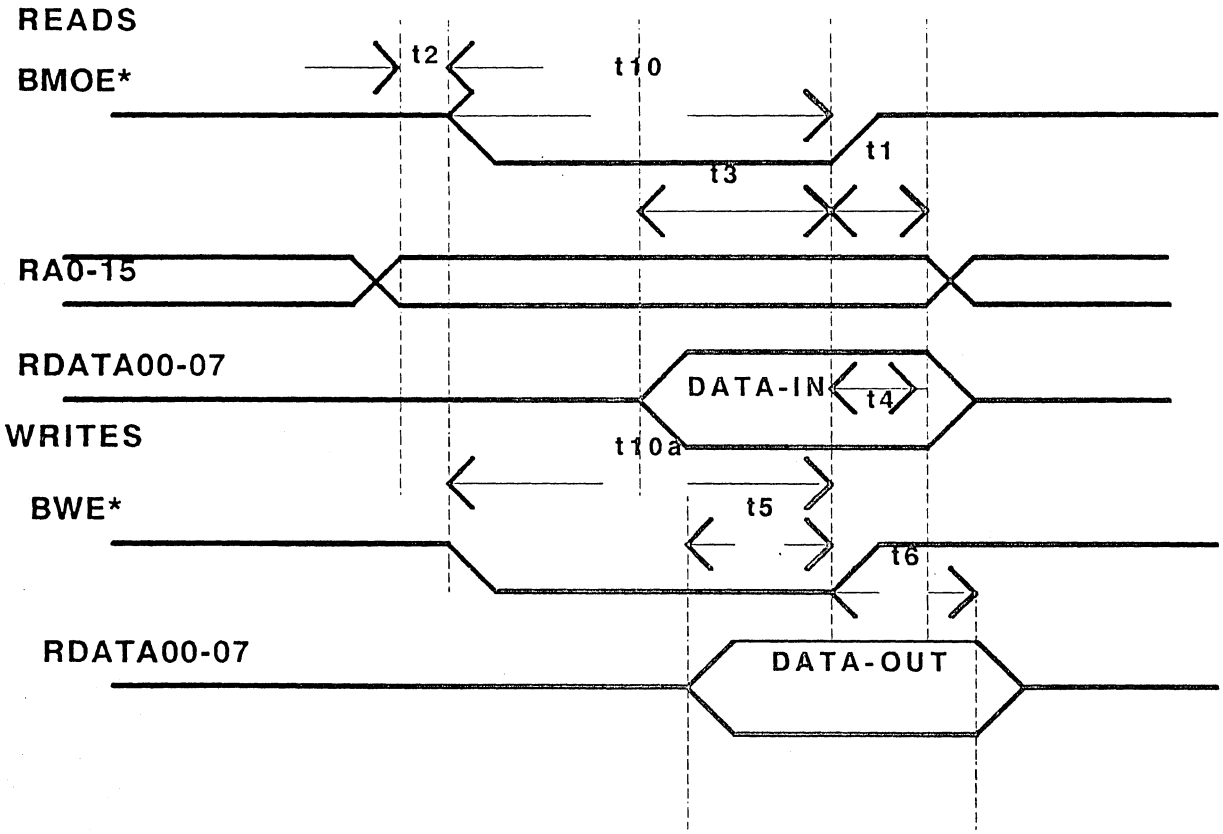
timings	Description	min	max
t65	RRF period	100	7500
t66	RRF period/2	38	-
t67	RRF fall time	-	10
t68	RRF rise time	-	10
t69	DATA valid to RRF edge	18	-
t70	RRF edge to Data Switching	44	-
t71	AMD- Valid to RRF edge	18	-
t75	RRF edge to DATA-OUT HI	10	90
t76	RRF edge to DATA-OUT LO	10	90
t77	RRF edge to WAM active	10	60
t78	RRF edge WAM inactive	10	60
t79	CHRESET length	3X t65	-

LOCAL MICROPROCESSOR INTERFACE TIMINGS



TIMING	DESCRIPTION	MIN (ns)	MAX (ns)
t11	RD* pulse width	250	-
t12	WR* pulse width	250	-
t13	Address setup to ALE V	15	-
t14	Address hold to ALE V	5	
t15	RD* V to Data valid	-	60
t16	RD* ^ to Data invalid	2	-
t17	WR* ^ Data setup	-	50
t18	WR* ^ Data hold	5	-

BUFFER MANAGER TIMINGS



TIMING	DESCRIPTION	MIN(ns)	MAX(ns)
t1	BMOE*^ TO ADDRESS INVALID	5	-
t2	ADDRESS SET-UP TO BMOE* V	50	-
t3	RDATAXX TO BMOE* ^ SET-UP	25	-
t4	RDATAXX TO BMOE* ^ HOLD	5	-
t5	RDATAXX TO BWE* ^ SET-UP	60	90
t6	RDATAXX TO BWE* ^ HOLD	10	-
t10	BMOE* PULSE-WIDTH	50	1000 **
t10A	BWE* PULSE-WIDTH	50	1000 **

** note: Parameters t10 and t10a are depedent on the Read Reference Clock and System Clock frequency. The divide ratio selected in the Register for the System Clock (During Writes, and Disk idle time) and the RRF clock (Read Data-field time), will detemine the pulse widths t10 and t10a.

If RRF or SYSCLK Frequency= F1 and n is divide ratio:

t10 and t10a PULSE WIDTHS = F1/n/2