



**CS8245 VGA CHIPSET 82C441 VGA CONTROLLER
 82A442 BUS INTERFACE**

- **Compatible to:**
 - 1) IBM PS/2™ Video Graphics Array (VGA)
 - 2) IBM Enhanced Graphics Adapter™
 - 3) IBM Color Graphics™ Adapter
 - 4) IBM Monochrome™ Adapter
 - 5) Hercules™ Adapters
- **Supports the following monitors:**
 - 1) IBM PS/2™ Analog displays
 - 2) IBM EGA™, CGA™ and Monochrome monitors
 - 3) Multifrequency Monitors (NEC Multi-sync™, Sony Multiscan™ and compatibles)

- **VGA solution for PC add-in cards can be implemented using 14 standard components, including 256 Kbytes of display memory and Color Palette/DACs.**
- **Hardware support for context switching in windowing and multi-tasking environments.**
- **Smart Auto-Emulation adjusts automatically to display mode required by application software.**

The 82C441 Graphics Controller and 82A442 Bus Interface offer a complete, highly integrated solution for implementing an IBM Video Graphics Array compatible controller, with backward compatibility to EGA, CGA, IBM Monochrome, and Hercules modes. A complete VGA, with backward compatibility can be implemented using a total of 14 off-the-shelf components, including 256K bytes of display memory and color palette and D/A converters for analog displays.

82C441 Graphics Controller

The 82C441 is a single-chip graphics controller which supports all the display modes of the IBM's VGA. The 82C441 includes support logic and registers for supporting the IBM's new VGA modes.

The 82C441 is packaged in an 84-pin PLCC or optional 100-pin PFP.

82A442 Bus Interface

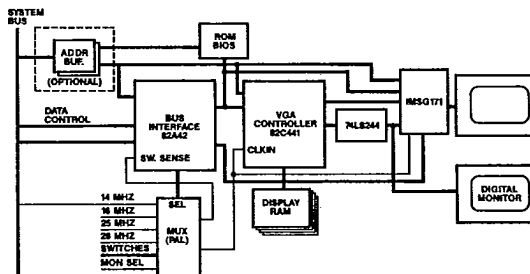
The 82A442 Bus Interface provides bus interface, memory select and I/O select logic functions. This includes all the logic to interface to the Inmos G171 (and compatible palette) color palette/DAC. The 82A442 is a bipolar device and is packaged in a 68 pin PLCC.

Backward Compatibility/Smart Auto-Emulation

The 82C441 supports backward compatibility on-chip to EGA, CGA, IBM Monochrome and Hercules modes. It also supports Smart Auto-Emulation which automatically adjusts to the graphics mode required by the application software. The 82C441 provides enhanced performance to CGA modes by allowing CGA text to be displayed in EGA/VGA resolution.

Hardware Support for Context Switching

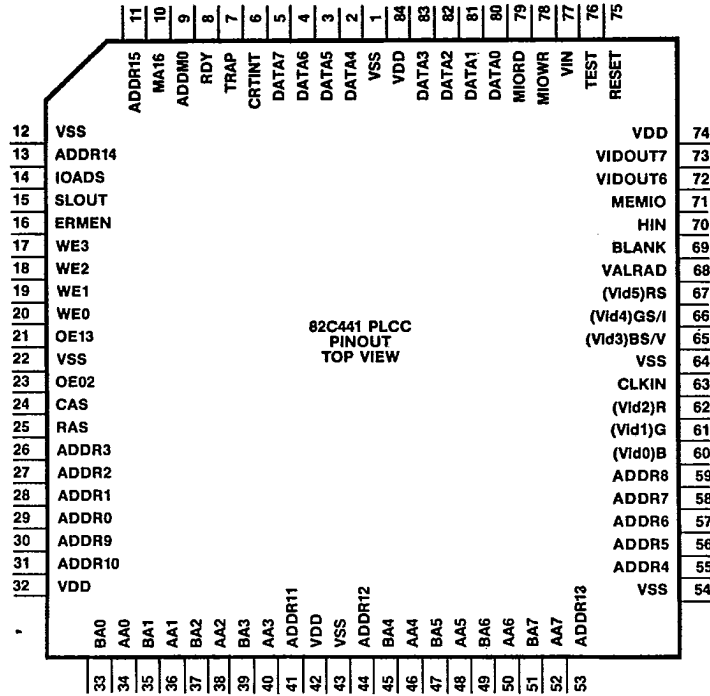
For support of multitasking and windowing environments, the entire state of the 82C441/82A442 (registers and latches in the 82C441/82A442) is readable and writable. This feature is compatible to IBM's VGA.

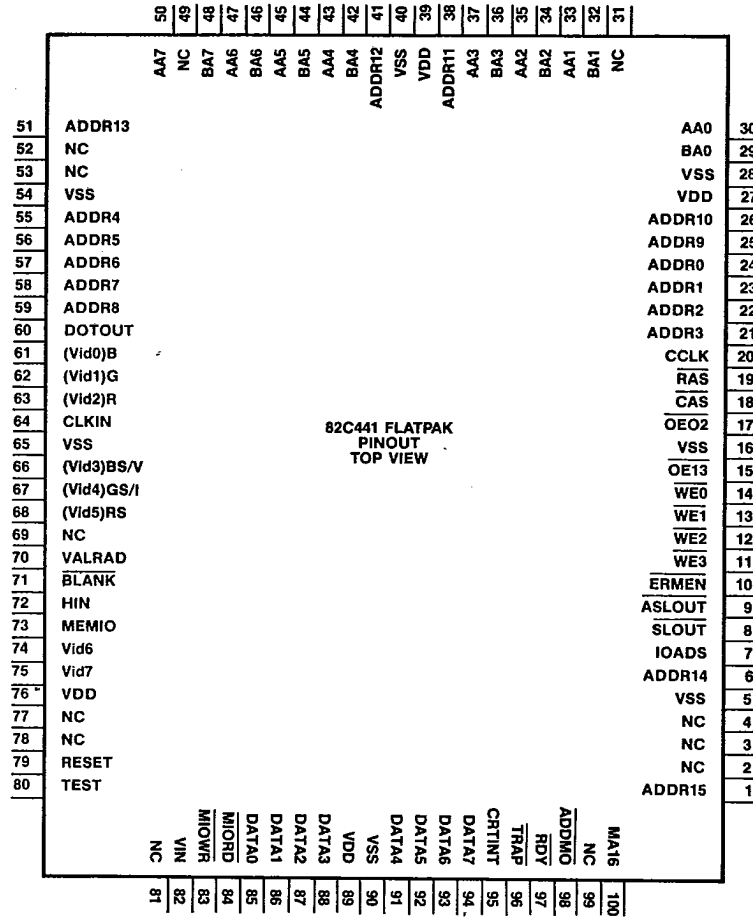


82C441/82A442 VGA Implementation

CHIPS

T-52-33-03





**82C441 Pin Description**

Pin No PLCC	Pin No. Flatpak	Pin Type	Symbol	Description
29	24	I	ADDR0	SYSTEM ADDRESS bits 0-15. These bits are used for addressing the display memory.
28	23	I	ADDR1	
27	22	I	ADDR2	
26	21	I	ADDR3	
55	55	I	ADDR4	
56	56	I	ADDR5	
57	57	I	ADDR6	
58	58	I	ADDR7	
59	59	I	ADDR8	
30	25	I	ADDR9	
31	26	I	ADDR10	
41	38	I	ADDR11	
44	41	I	ADDR12	
53	51	I	ADDR13	
13	6	I	ADDR14	
11	1	I	ADDR15	
80	85	I/O	DATA0	SYSTEM DATA BUS bits 0-7. These bits are used to transfer data to and from the CPU data bus. These are open drain outputs and must have external pull up resistors.
81	86	I/O	DATA1	
82	87	I/O	DATA2	
83	88	I/O	DATA3	
2	91	I/O	DATA4	
3	92	I/O	DATA5	
4	93	I/O	DATA6	
5	94	I/O	DATA7	
10	100	I	MA16	Buffered MA16 input from the 82A442; derived from the CPU address.
63	64	I	CLKIN	DOT CLOCK INPUT. CLKIN is the clock input from the external clock select multiplexer.
9	98	I	ADD \overline{M} 0	Active Low Decoded input (from the 82A442) for the three upper system address bus bits to address the display memory at locations AXXX and BXXX. Low when A19-A17 = 101.
79	84	I	MIORD	MEMORY I/O READ. MIORD is an active low input from 82A442 for memory or I/O read operations.
78	83	I	MIOWR	MEMORY-I/O WRITE. MIOWR is an active low input from 82A442 for all memory or I/O write operations.
71	73	I	MEMIO	MEMORY I/O. MEMIO is a control signal from the 82A442: 0 = memory; 1 = I/O.



82C441 Pin Description (Continued)

Pin No PLCC	Pin No. Flatpak	Pin Type	Symbol	Description
75	79	I	RESET	<p>RESET is an active high input from the system bus used to reset the CRT Controller Registers as follows:</p> <ol style="list-style-type: none"> It initializes the horizontal and vertical polarity control to logical 0. Mode Register bits 4 and 7 are reset. All counters in the CRT Controller Registers are reset. Hercules configuration switch (I/O address 3BF) bits 0 and 1 are reset. <p>All other control registers remain unchanged. RESET must be active for at least 64 dot clocks.</p>
14	7	I	IOADS	I/O ADDRESS. IOADS selects the I/O address to the CRT Controller. 0 = 2XX, 1 = 3XX.
76	80	I	TEST	TEST = 0 sets the vertical retrace counter to the complement of the contents of the Vertical Retrace Start Register (CR10) at the end of the current scan line. TEST = 1 allows normal operation.
60	61	O	(Vid0)B	<p>R, G, B, RS, GS/I, BS/V are the six outputs that drive the monochrome or color monitor. R, G, and B are the Red, Green and Blue signals, respectively. The RS, GS/I, and BS/V are the Secondary Red, Secondary Green/Intensity, Secondary Blue/Monochrome Video (display) signals. These six signals can also drive the six inputs of the color palette (IMSG 171) in analog mode.</p>
61	62	O	(Vid1)G	
62	63	O	(Vid2)R	
65	66	O	(Vid3)BS/V	
66	67	O	(Vid4)GS/I	
67	68	O	(Vid5)RS	
72	74	O	Vid6	<p>Vid6, Vid7 are the upper 2 video bits of the 8 bit video bus. These 2 bits combined with the above six video bits drive the eight video inputs of the color palette to produce 256 colors in analog mode.</p>
73	75	O	Vid7	
70	72	O	HIN	HORIZONTAL SYNC OUTPUT. HIN is active high if horizontal polarity bit (bit 6 of the Miscellaneous Output Register (I/O address 3C2)) is low. It is active low if the horizontal polarity bit is high.
77	82	O	VIN	VERTICAL SYNC OUTPUT. VIN is active high if the vertical polarity bit (bit 7 of the Miscellaneous Output Register (I/O address 3C2)) is low. It is active low if the vertical polarity bit is high.
69	71	O	BLANK	BLANK is a programmable output for blanking the screen during retrace periods.

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82C441 Pin Description (Continued)

Pin No PLCC	Pin No. Flatpak	Pin Type	Symbol	Description
15	8	O	SLOUT	ATTRIBUTE SHIFT LOAD. SLOUT is an active low output on the features connector (pin 9). It is used internally by the Attributes Controller in text mode to load parallel data coming in from the display memory.
6	95	O	CRTINT	CRT INTERRUPT. CRTINT is an active high output signal to the system bus pin IRQ2 (IRQ9), used to signal the CPU that the CRT needs attention. CRTINT is enabled by bit 5 of the Vertical Retrace End Register. It can be cleared by programming bit 4 of the Vertical Retrace End Register to 0. When not active, the CRTINT output is in a tri-state condition.
8	97	O	RDY	READY. RDY is an active low output used by the 82C441 to indicate to the CPU that a data transfer will be completed. RDY becomes inactive as soon as a memory read or a memory write operation is completed. When a read or write operation is completed, the RDY output goes high for one dot clock period, and then goes tri-state. RDY can directly drive the I/OCHRDY on the I/O bus.
7	96	I/O	TRAP	This pin is active low and is used to inform an external processor that some assistance is needed in the Hercules or CGA emulation modes. This pin can directly drive the IOCHCHK line on the PC bus. An external pull up resistor must be provided on this pin.
34	30	O	AA0	Multiplexed data/address bus AA0-7 for memory planes 0 and 1.
36	33	O	AA1	
38	35	O	AA2	
40	37	O	AA3	
46	43	O	AA4	
48	45	O	AA5	
50	47	O	AA6	
52	50	O	AA7	
25	19	O	RAS	ROW ADDRESS STROBE. RAS is an active low signal to the display memory. At the falling edge of RAS, the row address is present on the AA and BA busses.
24	18	O	CAS	COLUMN ADDRESS STROBE. CAS is an active low signal to the display memory. At the falling edge of CAS, the column address is present on the AA and BA busses.



82C441 Pin Description (Continued)

Pin No PLCC	Pin No. Flatpak	Pin Type	Symbol	Description
23	17	O	$\overline{OE02}$	OUTPUT ENABLE PLANES 0 AND 2. OE02 is an active low signal which causes plane 0 and plane 2 data to be read by the 82C441. Plane 0 data is read over the AA bus and plane 2 data is read over the BA bus.
21	15	O	$\overline{OE13}$	OUTPUT ENABLE PLANES 1 AND 3. OE13 is an active low signal which causes plane 1 and plane 3 data to be read by the 82C441. Plane 1 data is read over the AA bus and plane 3 data is read over the BA bus.
20	14	O	$\overline{WE0}$	WRITE ENABLE PLANE 0. WE0 is an active low write enable to display memory plane 0 for memory write operations.
19	13	O	$\overline{WE1}$	WRITE ENABLE PLANE 1. WE1 is an active low write enable to display memory plane 1 for memory write operations.
18	12	O	$\overline{WE2}$	WRITE ENABLE PLANE 2. WE2 is an active low write enable to display memory plane 2 for memory write operations.
17	11	O	$\overline{WE3}$	WRITE ENABLE PLANE 3. WE3 is an active low write enable to display memory plane 3 for memory write operations.
33	29	O	BA0	Multiplexed data/address bus BA0-7 for memory planes 2 and 3.
35	32	O	BA1	
37	34	O	BA2	
39	36	O	BA3	
45	42	O	BA4	
47	44	O	BA5	
49	46	O	BA6	
51	48	O	BA7	
16	10	O	\overline{ERMEN}	EARLY MEMORY ENABLE. ERMEN goes low three or five dot clocks before the time slot for a CPU to memory read or write access.



82C441 Pin Description (Continued)

Pin No PLCC	Pin No. Flatpak	Pin Type	Symbol	Description																	
68	70	O	VALRAD	VALID READ ADDRESS. VALRAD is active high when bit 1 (enable RAM) of the Miscellaneous Output Register (I/O address 3C2) is high and one of the following conditions is true: <table border="1"> <thead> <tr> <th colspan="2">Bits*</th> <th rowspan="2">Valid Address Ranges</th> </tr> <tr> <th>3</th> <th>2</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>A0000h-BFFFFh</td> </tr> <tr> <td>0</td> <td>1</td> <td>A0000h-AFFFFh</td> </tr> <tr> <td>1</td> <td>0</td> <td>B0000h-B7FFFh/BFFFFh</td> </tr> <tr> <td>1</td> <td>1</td> <td>B8000h-BFFFFh</td> </tr> </tbody> </table>	Bits*		Valid Address Ranges	3	2	0	0	A0000h-BFFFFh	0	1	A0000h-AFFFFh	1	0	B0000h-B7FFFh/BFFFFh	1	1	B8000h-BFFFFh
Bits*		Valid Address Ranges																			
3	2																				
0	0	A0000h-BFFFFh																			
0	1	A0000h-AFFFFh																			
1	0	B0000h-B7FFFh/BFFFFh																			
1	1	B8000h-BFFFFh																			
—	60	O	DOTOUT	Dot Clock output																	
—	20	O	CCLK	Character Clock Output																	
—	9	O	ASLOUT	ASLOUT is used to load the alphanumeric display memory data into the Attributes controller.																	
12	90	P	Vss																		
22	5	P	Vss																		
—	16	P	Vss																		
43	28	P	Vss																		
54	54	P	Vss																		
64	65	P	Vss																		
1	40	P	Vss																		
32	27	P	Vdd																		
42	39	P	Vdd																		
74	76	P	Vdd																		
84	89	P	Vdd																		

* Bits 3 and 2 are D3 and D2 of the register GR6 in graphics controller.

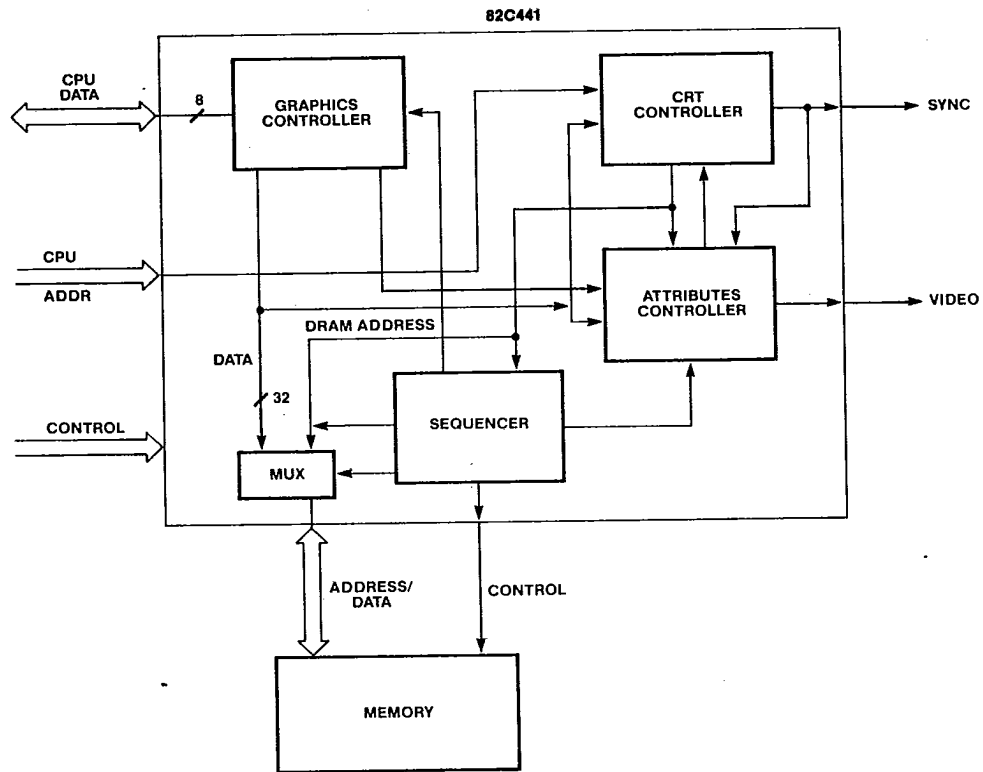


Figure 1. Video Graphics Array

82C441 Functional Description

The 82C441/82A442 offers a complete solution for implementing a VGA/MCGA/EGA/CGA/MDA/HERCULES compatible graphics system. Mode initialization is supported at the BIOS level. This allows the applications software to be portable. The pixel updating operations are supported at the Register level. All EGA functions are supported by the 82C441 Single Chip Video Graphics Array directly in hardware at the register level. CS8245 is more EGA compatible than IBM's VGA. The VGA display memory of 256 Kbytes is supported using 8 64k*4 DRAM chips. Additionally, the 82C441 supports more CPU bandwidth.

For support of multitasking environments and context switching, the *entire state* of the 82C441/82A442 (registers and latches in the 82C441/82A442) is readable and writable. This feature is 100% compatible to IBM's VGA.

The 82A442 is a bus interface companion chip to interface the 82C441 to the 8 bit PC(XT/AT) bus. The 82A442 Bus Interface Chip integrates all the external logic required around the 82C441 to implement a VGA/EGA/CGA/MDA/Hercules compatible graphics subsystem. The 82A442 internally decodes all memory and I/O (normal and alternate) addresses used by each of the graphics subsystems. Total chip count for a VGA compatible solution using the CS8245 chip set is **14 chips**.

The 82C441/82A442 directly interface to an external Inmos G171 color palette (or compatible) and D/A converter. Like the VGA, this is capable of displaying resolutions upto 640*480 (16 Colors) and upto 256 colors (320*200) from the external palette of 256 thousand (or 16 million) colors. The 82C441 can also be used with the SharpScan EGA™ 82C437 to display resolutions up to 1200*800 in 4 colors. With the use of external palette any four colors out of 256,000 can be displayed in the high resolution SharpScan mode.

The 82C441 is an integration of four different modules. The four modules are:

- a) **Graphics Controller** — The Graphics Controller interfaces the 8 bit CPU data bus to four planes of display memory. It supports different types of pixel/data mappings for read and write operations.
- b) **Sequencer** — The Sequencer generates all the timing signals for the 82C441 and the memory control signals for the display memory.
- c) **Attributes Controller** — The Attributes Controller generates the video data stream from the font pattern and attribute code in the text mode. Additionally, the Attributes Controller provides a 16/64 color palette (in both the text and graphics modes).
- d) **CRT Controller** — The CRT Controller generates all the sync and timing signals for the monitor and also generates the multiplexed display memory row and column addresses for display refresh and CPU access to display memory.

Graphics Controller

The Graphics Controller is responsible for directing data from the display memory to the Attributes Controller and the CPU. The Graphics Controller operates in two basic modes: Text (Alphanumeric) and Graphics. In the Text Mode, the Graphics Controller fetches the character code and attribute byte from memory, it then fetches the appropriate byte of the character font from the memory based character font table. The font pattern and the attribute byte are then sent to the Attributes Controller. In the Graphics Mode, the Graphics Controller, fetches data for 8 pixels (4 bits/pixel) or 4 pixels (8 bits/pixel) from display memory and then serially sends each pixel data to the Attributes Controller.



The Graphics Controller formats the data for use in various compatible modes. The Graphics Controller also provides color comparators which can be used in color painting and filling operations. Data can be written to the display memory planes in 32 bit words to expedite fast color presetting of the display areas on the monitor. Logical functions on the chip allow for manipulation of the data before being written to the display memory, allowing the user to implement features such as transparency and overlaying.

The Graphics Controller has two major sections, Graphics A and Graphics B. The Graphics A section normally writes to the display memory planes 0 and 1, and the

Graphics B section normally writes to the memory planes 2 and 3. The following description will refer to these two sections as Graphics A and Graphics B.

Graphics Controller Registers

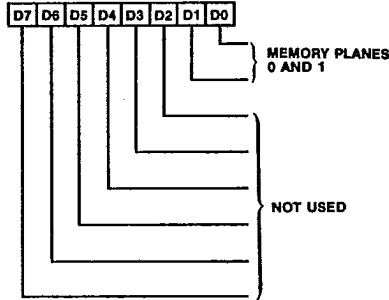
Most Graphics Controller registers are located at two byte addresses in the CPU I/O space. The registers are accessed by first writing a pointer to the actual data register into the Graphics Address Register and then accessing the Graphics Data Register. The Graphics Address Register is located at I/O address 3CEh, and the Graphics Data Registers are all located at I/O address 3CFh. The following table describes the Graphics Registers:

Register Number	Register Name	Address Pointer	Address
—	Graphics A Position	—	3CCh
—	Graphics B Position	—	3CAh
—	Graphics Address	—	3CEh
GR0	Set/Reset	00	3CFh
GR1	Enable Set/Reset	01	3CFh
GR2	Color Compare	02	3CFh
GR3	Data Rotate	03	3CFh
GR4	Read Map Select	04	3CFh
GR5	Graphics Mode	05	3CFh
GR6	Miscellaneous	06	3CFh
GR7	Color Don't Care	07	3CFh
GR8	Bit Mask	08	3CFh
GRF7	Graphics Control Register	F7h	3CFh
GRF8	Processor Latch 0	F8h	3CFh
GRF9	Processor Latch 1	F9h	3CFh
GRFA	Processor Latch 2	FAh	3CFh
GRFB	Processor Latch 3	FBh	3CFh

Register Description

GRAPHICS A POSITION REGISTER:

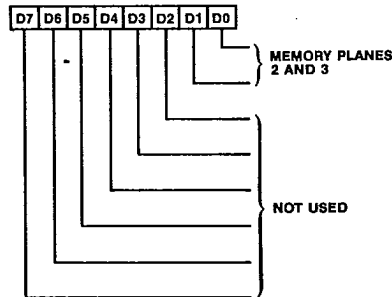
Read-Write Register
I/O Address: 3CCh



The Graphics A Position Register selects the CPU data bus signals and directs them to/from display memory planes 0 and 1. This register should normally be programmed to 00h to select D0 and D1 for display memory planes 0 and 1 respectively.

GRAPHICS B POSITION REGISTER:

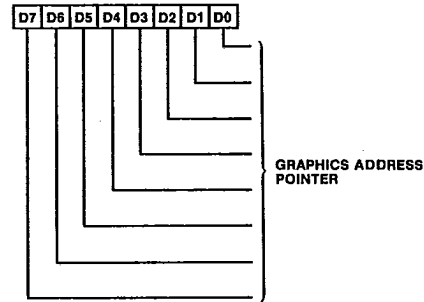
Read-Write Register
I/O Address: 3CAh



The Graphics B Position Register selects the CPU data bus signals and directs them to/from display memory planes 2 and 3. This register should normally be programmed to 01h to select D2 and D3 for display memory planes 2 and 3 respectively.

GRAPHICS ADDRESS REGISTER:

Read-Write Register
I/O Address: 3CEh

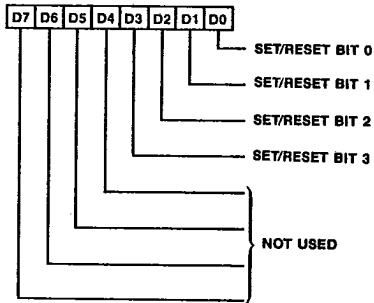


The Graphics Address Register is used to point to other registers in the Graphics Controller. The four least significant bits determine the register which will be pointed to in the next register write operation. If the Graphics Position Registers A and B are programmed with 0 and 1 respectively, then data bus signals D0, D1 correspond to the planes 0 and 1, while D2, D3 correspond to the planes 2 and 3 of the display memory.

When this register is read, D5, D6 and D7 are always '1'. D4 is '1' if D5, D6 and D7 were written as 1. D4 is '0' if D5, D6 or D7 were written as '0'.

SET/RESET REGISTER (GR0)

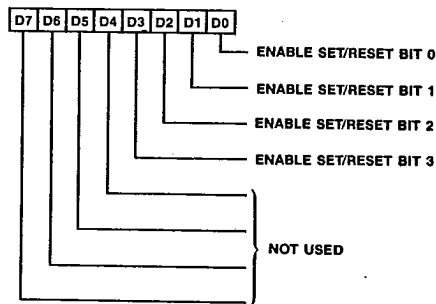
Read-Write Register
I/O Address: 3CFh
Address Pointer: 00



When the Graphics Mode Register selects write mode 0, and the Set/Reset mode is enabled through the Enable Set/Reset Register, bit 0 of this register is written to the entire addressed byte in display memory plane 0. Similarly bits 1, 2 and 3 determine the data to be written into display memory planes 1, 2 and 3 respectively.

ENABLE SET/RESET REGISTER (GR1)

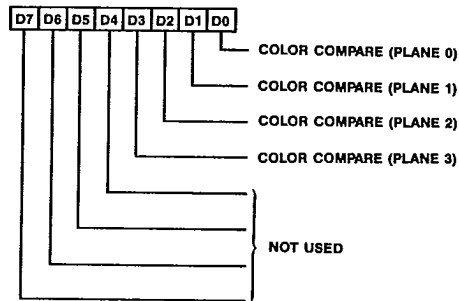
Read-Write Register
I/O Address: 3CFh
Address Pointer: 01



The Enable Set/Reset Register works in conjunction with the Set/Reset Register. If the Graphics Mode Register is programmed to write mode 0, and Set/Reset is enabled (=1), then the contents of the Set/Reset Register determine the data to be written to the respective display memory planes. If write mode 0 is selected and Set/Reset is not enabled (=0) on a plane, the plane is written with the data from the CPU data bus.

COLOR COMPARE REGISTER (GR2)

Read-Write Register
I/O Address: 3CFh
Address Pointer: 02



If the Graphics Mode Register is set to Read Mode 1, each bit of data read from the display memory planes 0-3 is compared to bits D0 through D3 programmed in the Color Compare Register and the Color Don't Care Register. A match between the memory data and the Color Compare Register (for the bits as specified in the Color Don't Care Register) results in a logical 1 being output on the corresponding data bus bit. Following is an example to illustrate the mechanism:

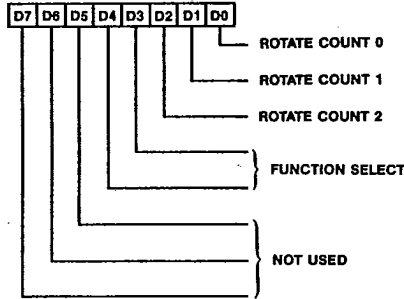
If Color Compare Register = 0011, Color Don't Care = 1111, and:

- Plane 0 has data = 11111111
- Plane 1 has data = 00000001
- Plane 2 has data = 11111110
- Plane 3 has data = 00000000

then the data bus D7-D0 will have 00000001, indicating that a match occurred on the bit D0 only.

DATA ROTATE REGISTER (GR3)

Read-Write Register
I/O Address: 3CFh
Address Pointer: 03



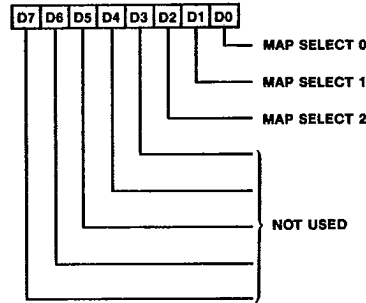
The Data Rotate Register is used to perform a rotate function on the data written by the CPU. If the Graphics Mode Register is programmed for write mode 0, then the value in the Rotate Count Field represents the number of bits the CPU data will be rotated (right) during the CPU write cycles. The CPU data bits are first rotated and then subject to the logical operation as specified in the Function Select Field.

The Function Select bits allow the contents of the processor latches (loaded on a previous Read Cycle) to operate logically upon the CPU data being written into the VGA memory. The bits operate as follows:

D4	D3	
0	0	No change to the Data
0	1	Logical 'AND' between Data and latched data.
1	0	Logical 'OR' between Data and latched data.
1	1	Logical 'XOR' between Data and latched data.

READ MAP SELECT REGISTER (GR4)

Read-Write Register
I/O Address: 3CFh; Address Pointer: 04

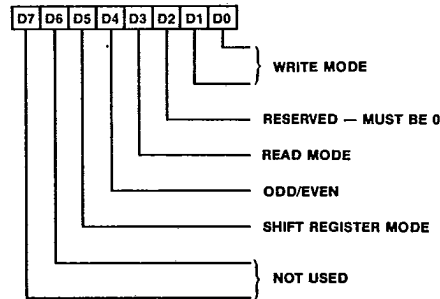


The contents of the Read Map Select Register represent the memory plane from which the CPU reads the data in read mode 0. This register does not effect the read operation performed through the Color Compare Register (read mode 1). The four memory maps are selected as follows:

D2	D1	D0	
0	0	0	Map 0
0	0	1	Map 1
0	1	0	Map 2
0	1	1	Map 3

GRAPHICS MODE REGISTER (GR5)

Read-Write Register
I/O Address: 3CFh; Address Pointer: 05



The function of the bits is as follows:

Write Mode (D0, D1) — Figure 2

D1 D0

0 0 Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.

0 1 Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.

1 0 All planes (0-3) in the addressed byte are set to the value of data bus (D0-D3). The data bits are treated as the color value to be written into the eight pixels in the addressed byte. For example, memory plane 0 is set to the value of data bit D0, memory plane 1 is set to the value of data bus bit D1, etc. Individual pixels (all planes) in the addressed byte can be prevented from being updated by appropriately programming the Bit Mask Register.

1 1 Illegal

The operations specified above also work in conjunction with the Function Select options available through Data Rotate Register.

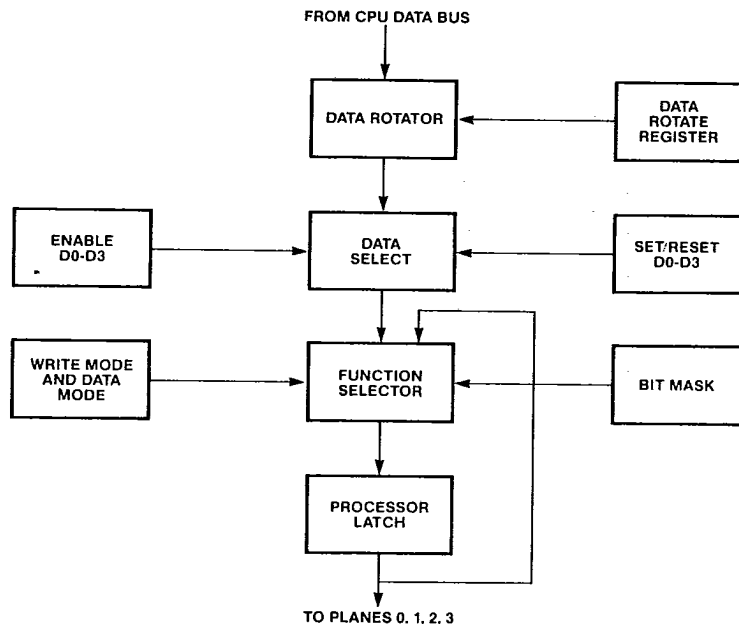


Fig. 2

Read Mode (D3) — Figure 3

D3	
0	When D3 = 0, the CPU reads the data from one of the display memory planes. The exact plane is selected through the Read Map Select Register.
1	When D3 = 1, the CPU reads the result of the logical comparison between the four display memory planes data and the contents of the Color Compare and Color Don't Care Registers.

Odd/Even (D4)

D4 = 1 will put the Graphics Controller in the Odd/Even addressing mode. In this mode, even CPU addresses access planes 0 and 2 while odd CPU addresses access planes 1 and 3. This option is useful for IBM Color Graphics Adapter compatible memory organization. The value of this bit should be the complement of the value programmed in D2 of the Sequencer Memory Mode Register.

Shift Register (D5)

The data bits in the memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7, respectively. When D5 = 1, the data in the 4 serial shift registers is formatted as follows:

MSB	LSB	Output to:
M1D0 M1D2 M1D4 M1D6 M0D0 M0D2 M0D4 M0D6	Bit0	
M1D1 M1D3 M1D5 M1D7 M0D1 M0D3 M0D5 M0D7	Bit1	
M3D0 M3D2 M3D4 M3D6 M2D0 M2D2 M2D4 M2D6	Bit2	
M3D1 M3D3 M3D5 M3D7 M2D1 M2D3 M2D5 M2D7	Bit3	

The Least Significant Bit (LSB) is shifted out first. The first two registers correspond to the Graphics A shift registers, while the following two correspond to the Graphics B shift registers. This is normally used for CGA compatible 320x200, 4 color graphics mode.

When D5 = 0, then M0D7-M0D0, M1D7-M1D0, M2D7-M2D0 and M3D7-M3D0 are shifted out with the bit D7 going out first in all cases.

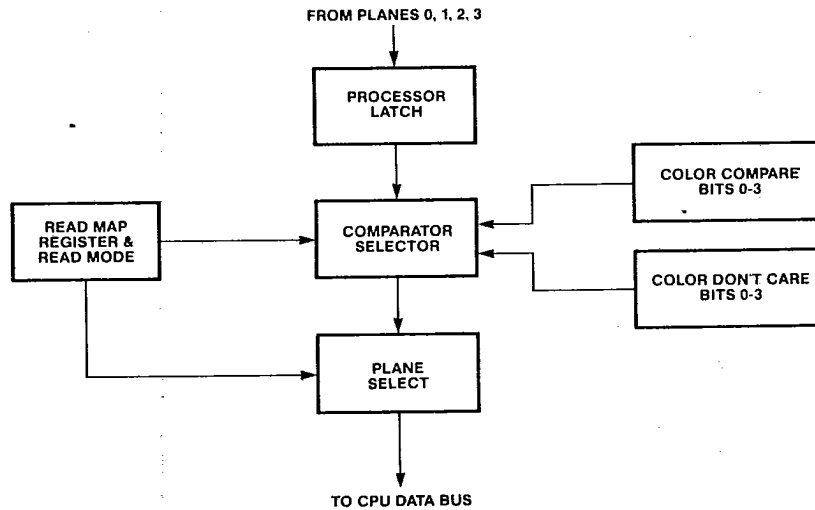


Fig. 3

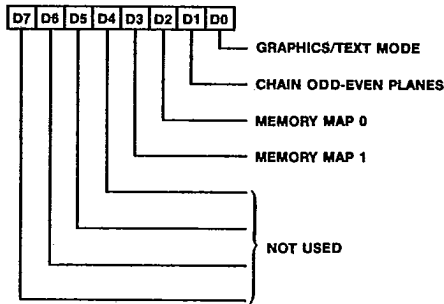
MSB
 LSB Output to:

MOD0 MOD1 MOD2 MOD3 MOD4 MOD5 MOD6 MOD7 BI10
 M1D0 M1D1 M1D2 M1D3 M1D4 M1D5 M1D6 M1D7 BI11
 M2D0 M2D1 M2D2 M2D3 M2D4 M2D5 M2D6 M2D7 BI12
 M3D0 M3D1 M3D2 M3D3 M3D4 M3D5 M3D6 M3D7 BI13

Refer to Graphics Control Register (GRF7) for the shift register format for 8 bits/pixel.

MISCELLANEOUS REGISTER (GR6)

Read-Write Register
 I/O Address: 3CFh
 Address Pointer: 06



Graphics/Text Mode

D0 = 1 selects the graphics mode. D0 = 0 selects the text mode.

Chain Odd-Even Planes

When D1 = 1, the CPU address bit A0 is replaced by a higher order address bit. The contents of A0 determine which memory plane is selected. A '0' selects planes 0 and 2, and a '1' selects planes 1 and 3. This mode can be used to have a 128 kbyte long display buffer with 2 bits/pixel (SharpScan™ graphics mode)

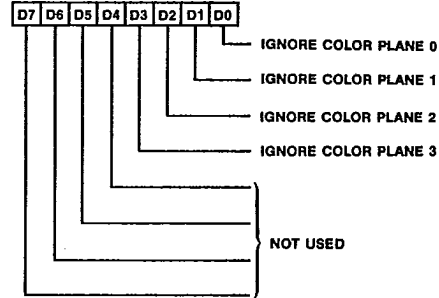
Memory Maps 0 and 1

These bits control the mapping of the display memory buffers into the CPU address space.

D3	D2	
0	0	Address A0000h-BFFFFh
0	1	Address A0000h-AFFFFh
1	0	Address B0000h-B7FFFh/BFFFFh-used in Hercules emulation
1	1	Address B8000h-BFFFFh-used in CGA emulation

COLOR DON'T CARE REGISTER (GR7)

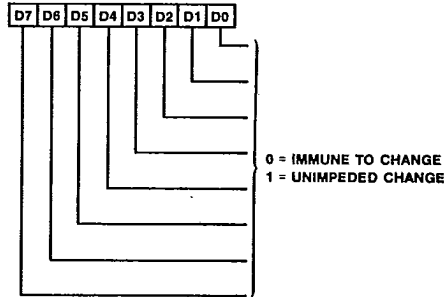
Read-Write Register
 I/O Address: 3CFh
 Address Pointer: 07



Any bit in the Color Don't Care Register that is set to 0 indicates that the corresponding bit in the Color Compare Register is a don't care in read mode 1. Any bit set to 1 enables the corresponding bit in the Color Compare Register.

BIT MASK REGISTER (GR8)

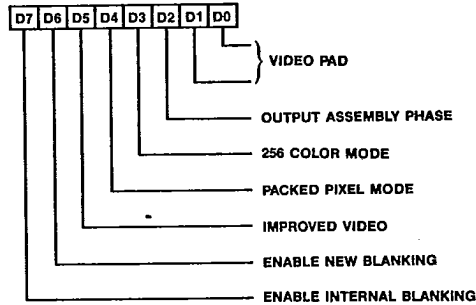
Read-Write Register
 I/O Address: 3CFh
 Address Pointer: 08



Any bit programmed to 0 in the Bit Mask Register causes the corresponding bit in each of the four memory planes to be immune to change. The data written into these memory bits is the data stored in the corresponding bits of the processor latches on the chip. Any bit programmed to 1 allows unrestricted manipulation of the corresponding bit in each of the four memory planes. The bit mask is applicable to any data written by the CPU, including rotate, logical functions (AND, OR, XOR), Set/Reset and No Change. **The data to be preserved using the bit mask must be latched by reading the addressed byte.** In order to execute a proper read-modify-write cycle into memory, each byte must first be read, the Bit Mask Register set and the new data is then written. The bit mask applies to all the four planes simultaneously.

GRAPHICS CONTROL REGISTER (GRF7)

Read-Write Register
I/O Address: 3CFh
Address Pointer: F7h



Video Pad Bits 0 and 1 (D0, D1)

These bits determine the state of video output pins Vid6 and Vid7 respectively when the 82C441 is not in the 256 color mode.

Output Assembly Phase (D2)

This bit determines the mapping of the two four bit nibbles into the two halves of a 8 bit pixel. When 0 the first nibble is the upper half, when 1 the first nibble is the lower half of the 8 bit pixel.

Enable 256 Color Mode (D3)

This bit is used in conjunction with the bit D4 of this register. When '0', one 4 bit pixel (expanded to 6 bits through the internal palette) is output on the 6 lower video out pins every dot clock. The upper 2 video outputs—Vid6 and Vid7 output the predefined Video Pad bits (D0,D1). When the 256 color bit is '1', two 4 bit nibbles are internally assembled and 1 eight bit pixel is output on the video out pins every 2 dot clocks. Each 4 bit nibble comes out of the shift registers every dot clock and go through the attribute (internal palette) controller. The upper 2 bits of the palette outputs are ignored. The two nibbles are then assembled according to the output assembly phase bit (D2) and are output as an eight bit value on the video output pins. The internal palette must be programmed for pass through condition to use the 256 color (8 bits/pixel mode).

Packed Pixel Mode (D4)

When 0, the display memory is organized in the planer mode similar to the EGA memory organization. When 1, a new CPU address mapping and shift register formatting for the 16 and 256 color packed pixel mode is enabled. The 4 shift registers are formatted as follows in the packed pixel mode:

		SHIFT DIRECTION-							
		MSB		LSB					
M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit 0	
M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit 1	
M3D2	M3D6	M2D2	M2D6	M1D2	M1D6	M0D2	M0D6	Bit 2	
M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit 3	

Enable Improved Video (D5)

When 0, video outputs are not resynchronized to dot clock. When 1, all the video outputs are resynchronized to the dot clock. This bit also controls the polarity of the BLANK signal. When D5 is '0', the BLANK is an active high signal. When D5 is '1', the BLANK is an active low signal. This bit should be set to a '1' when an external color palette (Inmos G171 or compatible) is used to drive the analog monitor.

Enable New Blanking (D6)

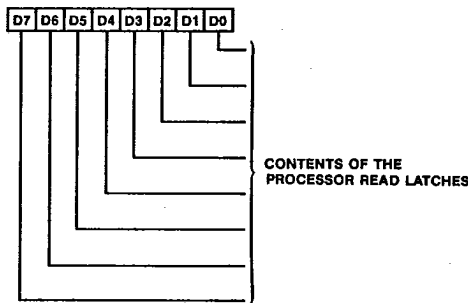
When D6 is '0', the internal blanking signal is similar to IBM's EGA. When D6 is '1', the internal blanking is delayed by 7 dot clocks. This allows proper centering of the screen.

Enable Internal Blanking (D7)

When D7 is '0', the external blanking is similar to IBM's EGA. When '1', the external blanking is same as the internal blanking. This bit should be set to '1' when external color palette/DAC is used.

PROCESSOR LATCH REGISTERS (GRF8-GRFB)

Read Only Register
I/O Address: 3CFh
Address Pointer: F8h-FBh



There are four byte-wide latches inside the 82C441. These latches are set whenever the CPU reads the display memory. The contents of these latches are subsequently used for the logical operations in the CPU write cycles. In order to completely determine the context of the 82C441, these latches can be read by the CPU as four byte-wide registers in the Graphics Controller address space. The registers at offset F8h-FBh reflect the contents of the latches for planes 0-3 respectively. In order to restore the processor latches, the CPU should first transfer the old contents of the processor latches to some address in memory and then read the same address.

Sequencer

The Sequencer generates memory timings for the display RAMs and the character clock for controlling the regenerative memory fetches. The Sequencer provides control signals for other modules in the 82C441. It also allows the CPU to access memory during active display intervals by inserting dedicated CPU memory cycles. Figures 4, 5, 6 and 7 illustrate various memory cycles for different configurations. As shown in the figures, the memory cycle selection allows different screen resolutions. The Sequencer also protects the entire memory from being altered, by selectively masking out planes through the configurable Mask Register. Figure 8 shows the memory control signals for the four memory planes.

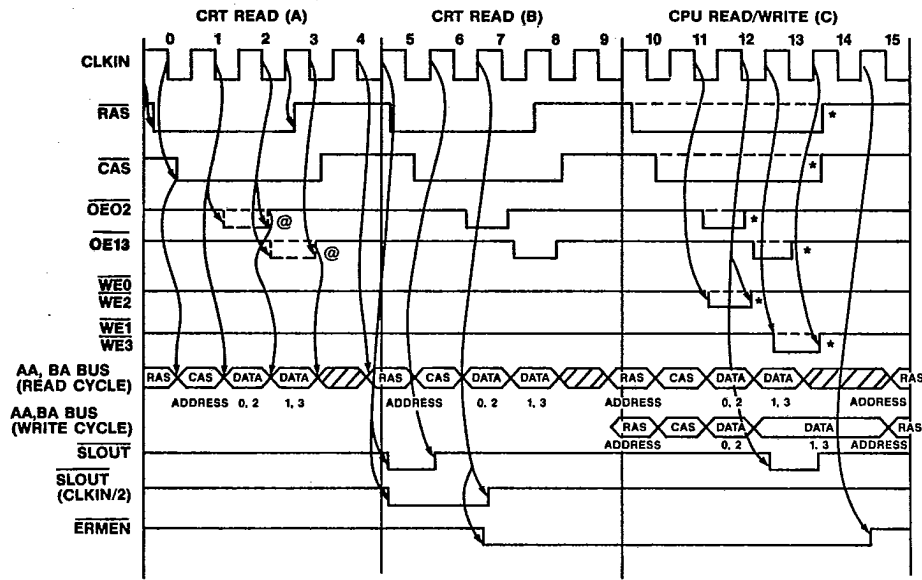
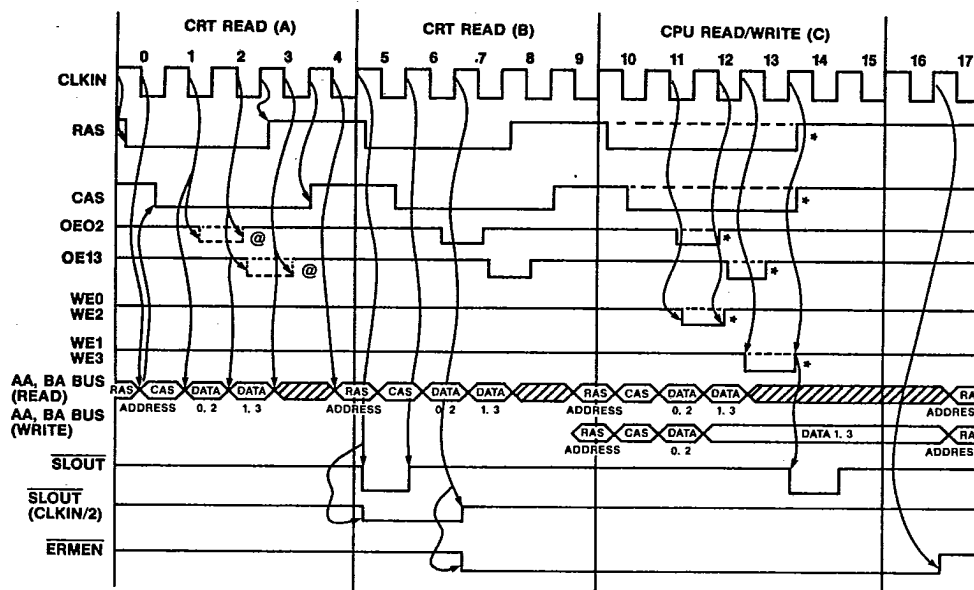
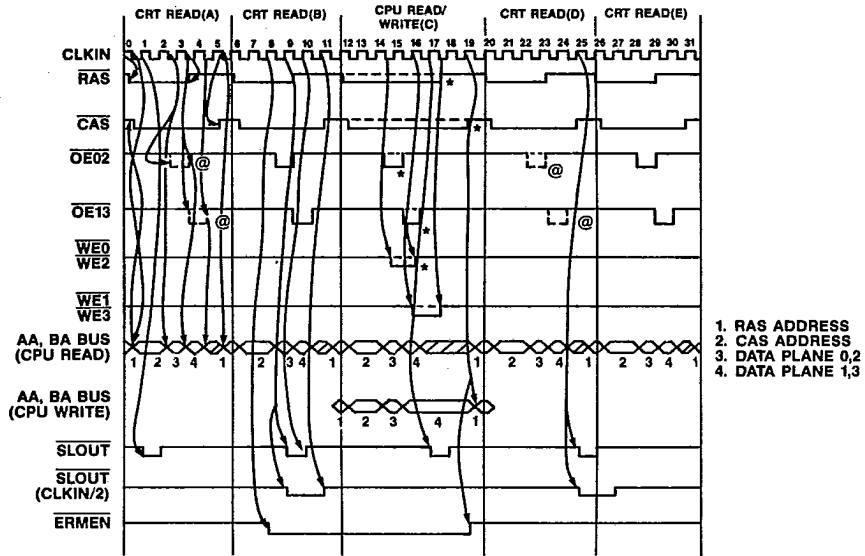


Figure 4. Memory Cycle Division for High CPU Bandwidth Mode (SR1-D4 = 0), 8 Dots/Character



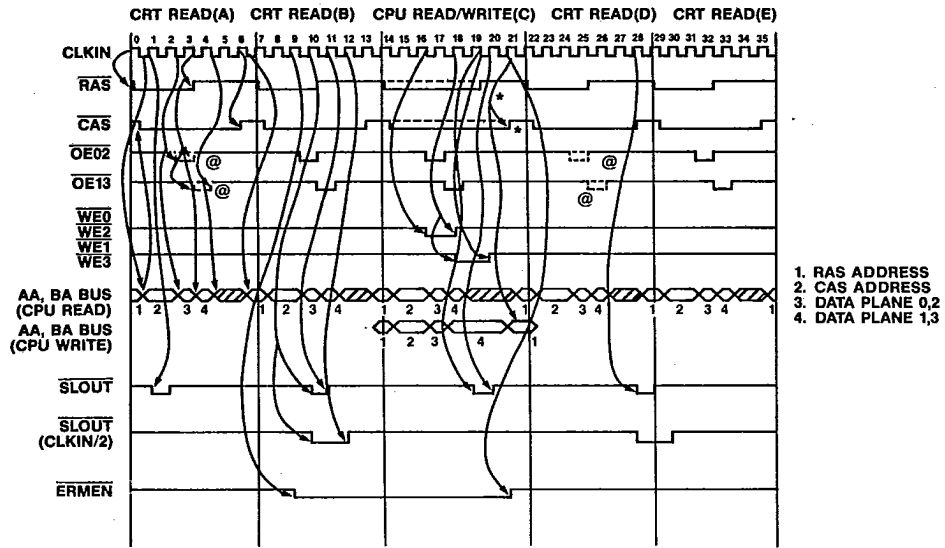
@ NOEX ACTIVE DURING CRT READ CYCLE A ONLY FOR HIGH CRT BANDWIDTH MODE (SR1-D1=0)
 + ONLY FOR CPU-MEMORY RD/WR CYCLES

Figure 5. Memory Cycle Division for High CPU Bandwidth Mode (SR1-D4 = 0), 9 Dots/Character



@ NOEX ACTIVE DURING CRT READ CYCLES A AND D ONLY FOR HIGH CRT BANDWIDTH MODE (SR1-D1=0)
 * ONLY ACTIVE FOR VALID CPU-MEMORY READ/WRITE CYCLES

Figure 6. Memory Cycle Division for Low CPU Bandwidth Mode (SR1-D4 = 1), 8 Dots/Character



@ NOEX ACTIVE DURING CRT READ CYCLES A AND D ONLY FOR HIGH CRT BANDWIDTH MODE (SR1-D1=0)
 * ONLY ACTIVE FOR VALID CPU-MEMORY READ/WRITE CYCLES

Figure 7. Memory Cycle Division for Low CPU Bandwidth Mode (SR1-D4 = 1), 9 Dots/Character

Sequencer Registers

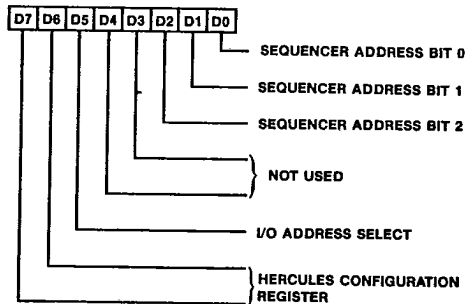
The Sequencer Registers are all located at two byte addresses in the CPU I/O space. The registers are accessed by first writing a pointer to the actual data register into the Sequencer Address Register and then accessing the Sequencer Data Register. The Sequencer Address Register is located at I/O address 3C4h. The Sequencer Data Registers are all located at I/O address 3C5h. The following table describes the Sequencer Registers:

Register Number	Register Name	Address Pointer	Address
SR0	Address Reset	00	3C4h
SR1	Sequencer Clocking Mode	01	3C5h
SR2	Plane Mask (Map Mask)	02	3C5h
SR3	Character Map Select	03	3C5h
SR4	Sequencer Memory Mode	04	3C5h

Sequencer Register Description

ADDRESS REGISTER

Read-Write Register
I/O Address: 3C4h



The Address Register is a three bit write-only register. When loaded with a binary value (pointer), it points to the data register where data is to be written.

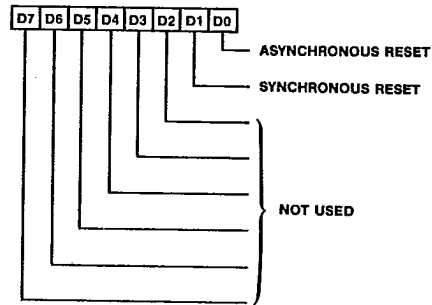
D5 is a secondary read location for the I/O address select bit of the Miscellaneous Output Register (I/O address 3C2h).

D6 and D7 are the read locations for the Hercules Configuration Register (bits D0 and D1 at I/O address 3BFh).

RESET REGISTER (SR0)

Read-Write Register

I/O Address: 3C5h; Address Pointer: 00



Asynchronous Reset

D0 = 0 causes the Sequencer to clear asynchronously and halt. It also places all the outputs (except R, G, B, RS, GS/I, BS/V) in a high impedance state. D0 = 1 causes the Sequencer to run unless D1 = 0 (Synchronous Reset). Asynchronous Reset can cause data loss in the dynamic display RAMs.

Synchronous Reset

D1 = 0 causes the Sequencer to clear synchronously and halt. D1 = 1 causes the Sequencer to run unless D0 (Asynchronous Reset) is cleared to zero. Synchronous reset for a short duration will preserve the data in the memory.

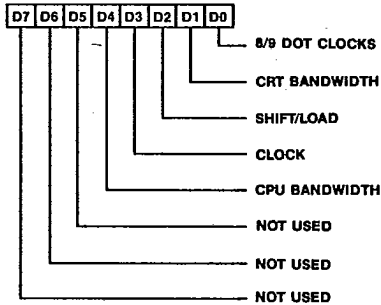
Before changing the Clocking Mode Register, the Sequencer should be reset with this bit. This will preserve the memory contents.

Both the Reset bits must be a logical 1 to allow the Sequencer to operate.



SEQUENCER CLOCKING MODE REGISTER (SR1)

Read-Write Register
I/O Address: 3C5h; Address Pointer: 01



The description for the individual bit fields is as follows:

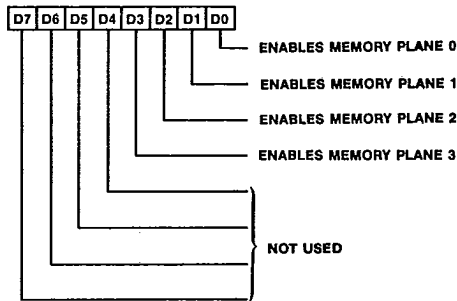
- D0** 8/9 Dot Clocks: D0 = 0 causes the Sequencer to generate character clocks which are 9 dots wide. D0 = 1 causes the Sequencer to generate character clocks which are 8 dots wide.
- D1** CRT Bandwidth: D1 = 1 makes CRT memory accesses for the low resolution modes (horizontal resolution of 320 pixels). D1 = 0 must be programmed for all higher resolution modes (horizontal resolution of 640 or 720 pixels).
- D2** Shift/Load: D2 = 0 causes the display serializers in the Graphics Controller to be reloaded every character clock. D2 = 1 causes the display serializers to be reloaded every other character clock. This mode is useful when 16 bits are fetched every memory cycle and chained together in the shift registers. This bit is only set for APA (all-points-addressable) graphics modes.
- D3** Dot Clock: D3 = 0 selects the Sequencer master clock input to be output on the Dot Clock output pin. D3 = 1 causes the master clock to be divided by 2 to generate the dot clock. As the Dot Clock is the primary clock used by the

82C441, all other timings will be stretched as they are derived from the Dot Clock. Dot Clock divided by 2 is used for 320 x 200 4 colors and 16 colors modes and 360 x 400 16 color mode.

- D4** CPU Bandwidth: D4 = 0 allows two CPU accesses into display memory for every four CRTC accesses. This effectively doubles the memory bandwidth available to the CPU. This high speed mode can be used for video clocks up to 20 MHz. Therefore at normal EGA operation (16 Mhz video clock), the CPU can update the screen at up to twice the normal speed. At higher video rates, D4 must be set to one, resulting in the normal EGA mode of one CPU memory access for every four CRTC memory accesses. CPU Bandwidth is independent of the CRT Bandwidth (bit D1) of this register.

PLANE MASK REGISTER (MAP MASK REGISTER SR2)

Read-Write Register
I/O Address: 3C5h
Address Pointer: 02

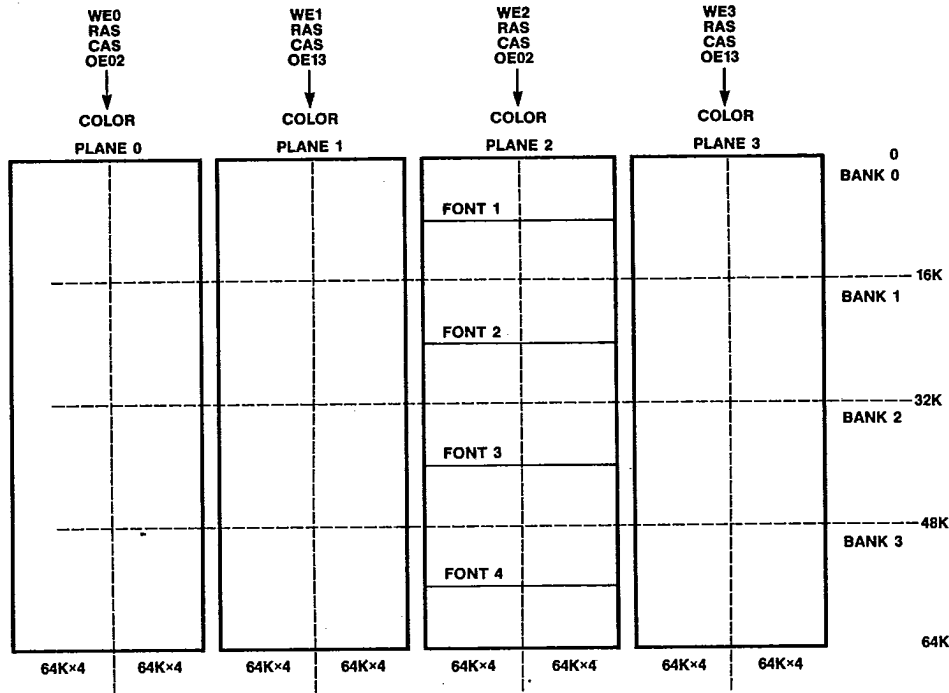


The Plane Mask Register is also referred to in some cases as Map Mask Register. A logical 1 in any of the bits 0 through 3 enables the CPU to write to the corresponding memory planes 0 through 3. A logical 0 in any of the bits disables the CPU to write to the corresponding memory planes by suppressing the WE signal to that memory plane. When this

register is loaded with 0FH, the CPU can perform a 32-bit write operation in one memory cycle. This substantially reduces the CPU overhead in the CPU in graphics drawing and filling operations.

When odd/even modes are selected (by clearing bit 2 of the Sequencer Memory Mode Register) planes 0, 1 and planes 2, 3 should have the same plane mask value.

In Graphics modes, each pixel consists of four bits. Planes 0-3 contain one bit each from the four bit pixel information. In the Text mode, plane 0 contains the character codes, plane 1 contains the corresponding attribute byte, plane 2 contains the character font (up to four fonts can be stored in plane 2) and plane 3 is not used. Figure 8 represents the memory organization in the two modes.



IN GRAPHICS MODE: PLANES 0-3 CONTAIN 1 BIT EACH OF A 4 BIT PIXEL. A TOTAL OF 64K PIXELS CAN BE STORED IN MEMORY IN THIS MODE.

IN THE ALPHANUMERIC MODE: PLANE 0 HAS ADDRESS DATA PLANE 2 HAS CHARACTER FONT PLANE 1 HAS ATTRIBUTE DATA PLANE 3 NOT USED

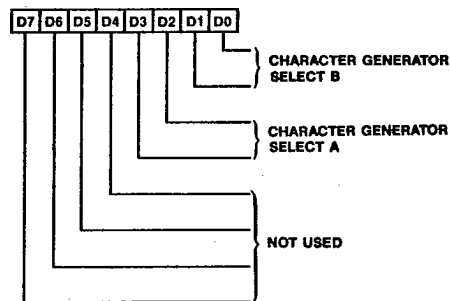
EACH FONT SUPPORTS 256 CHARACTERS UP TO 32 SCAN LINES HIGH AND REQUIRES 8K BYTES OF MEMORY. THE FONT IS RESIDENT IN THE UPPER 8K BYTE POSITION OF EVERY 16K BYTE BLOCK OF PLANE 2.

Figure 8: VGA Display Memory Organization



CHARACTER MAP SELECT REGISTER (SR3)

Read-Write Register
I/O Address: 3C5h
Address Pointer: 03



The 82C441 supports 2 out of 4 fonts in the text mode.

Character Generator Select B

D1-D0 select the font used to generate text characters when attribute bit 3 is 0 (display memory bit M1D3) according to the following table:

D1	D0	Character Generator	Table Location
0	0	0	First 8K of Plane 2 Bank 0
0	1	1	First 8K of Plane 2 Bank 1
1	0	2	First 8K of Plane 2 Bank 2
1	1	3	First 8K of Plane 2 Bank 3

Character Generator Select A

D3-D2 select the font used to generate text characters when attribute bit 3 is a 1, according to the following table:

D3	D2	Character Generator	Table Location
0	0	0	First 8K of Plane 2 Bank 0
0	1	1	First 8K of Plane 2 Bank 1
1	0	2	First 8K of Plane 2 Bank 2
1	1	3	First 8K of Plane 2 Bank 3

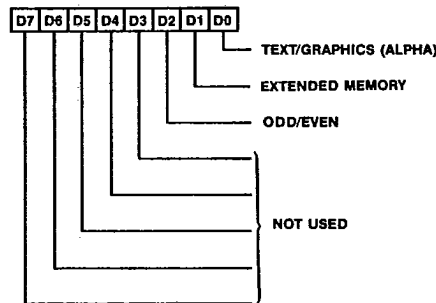
In text modes, bit 3 of the attribute bit D3 normally turns the foreground intensity on or off. This bit may be redefined to be a switch between character sets. This function is enabled when there is a difference in the values

of Character Map Select A and Character Map Select B bits. Whenever the two values are the same, the character select function is disabled and attribute bit D3 turns the foreground intensity on or off.

Asynchronous Reset (Reset Register bit 0) clears the Character Map Select Register to 0. This should only be done during a system reset.

SEQUENCER MEMORY MODE REGISTER (SR4)

Read-Write Register
I/O Address: 3C5h
Address Pointer: 04



Text/Graphics (D0)

D0 = 0 indicates that a graphics mode is active. This forces the same address on the multiplexed memory address bus AAx and BAx.

D0 = 1 indicates that the text mode is active and forces the display buffer address on memory address bus AAx and the character font address on memory address bus BAx.

Extended Memory (D1)

In VGA/EGA modes this bit must be programmed to 1. The 82C441 does not support 16k*4 DRAMs. Only 64k*4 DRAMs are supported, for 256 Kbytes of display memory. In CGA/Hercules modes this bit must be programmed to 0. In CGA mode, the memory is restricted to 16 Kbytes while in the Monochrome (Hercules) Text mode the memory is restricted to 4 Kbytes.

Odd/Even (D2)

D2 = 0 puts the Sequencer in the Odd/Even addressing mode. In this mode, even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for IBM Color Graphics Adapter (text and graphics mode) compatible memory organization. The value of this bit should be the complement of the value programmed in D4 of the Graphics Controller Mode Register (GR5).

Attribute Controller

The Attribute Controller provides a palette of 16 colors selectable from a possible 64, each one of which may be specified separately. Six color outputs, Red (R), Green (G), Blue (B), Secondary Red (RS), Secondary Green/Intensity (GS/I) and Secondary Blue/Monochrome (BS/V) are available as outputs. The Attribute Controller also controls blinking and underline operations.

The Attribute Controller formats data from the display memory for display on the screen. It also provides the horizontal pixel panning capability in both text and graphics modes.

In the text mode, the attribute bits are decoded to select one of the 16 color palette registers. The color palette, which consists of 16 registers, each 6-bit wide, can be loaded with any color combination. Thus it is possible to display the characters in any one of the 16 colors out of a possible of 64 (6-bit wide registers).

In the graphics mode, the color information is stored in the display memory as a 1, 2, 4 or 8 bits per pixel. In the first three cases, the pixel bit pattern is used to select one of the 2, 4 or 16 color registers. The six bit content of the respective color register determines the color on the screen for each individual pixel.

In the 256 color mode (8 bits/pixel), external color palette is used to generate the colors on the screen. **The internal palette must be programmed for pass through condition to use the 256 colors.** The external color palette/DAC (G171) can also be used for 1, 2 or 4 bits/pixel.

Attribute Controller Registers

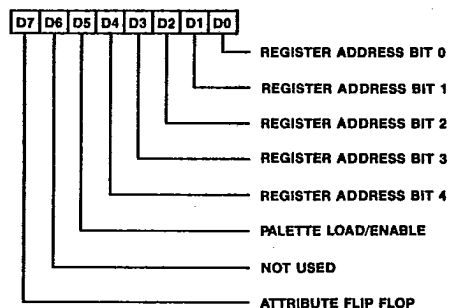
The Attributes Controller registers are all located at a single byte address in the CPU I/O space for the Write operations. The registers are accessed by first writing a pointer to the actual data register into the Attributes Address Register and then accessing the Attributes Data Register. Both the Attributes Address and Data Registers are located at I/O address 3C0h. Both registers can also be accessed at I/O address 3C1h for write operations. An internal flip-flop controls the selection of the Attributes Address and Data Registers. To select the Address Register, an IO Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Address Register has been loaded by an IO Write to address 3C0h, this flip-flop toggles, and the 82C441 is ready to have a Data Register (pointed to by the Address Register) loaded. Every IO Write to address 3C0h toggles this flip-flop. **For Read operations, the Address register is located at I/O address 3C0h and the data register is located at 3C1h.** The state of the attribute flip flop is not returned while reading the data registers. The following table describes the Attribute Registers:

Register Number	Register Name	Address Pointer	Address Writes	Address Reads
-	Address Register	-	3C0h	3C0h
AR0-ARF	Palette Registers	00h-0Fh	3C0h	3C1h
AR10	Attribute Mode Control	10h	3C0h	3C1h
AR11	Overscan Color	11h	3C0h	3C1h
AR12	Color Plane Enable	12h	3C0h	3C1h
AR13	Horizontal Pixel Panning	13h	3C0h	3C1h



ATTRIBUTES ADDRESS REGISTER

Read-Write Register
I/O Address: 3C0h



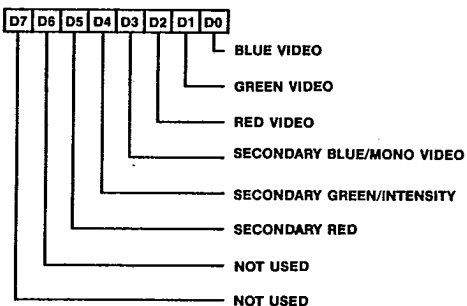
D0-D4 are used to point to the internal data registers in the Attribute Controller.

D5 = 0 disables the internal color palette and video to allow access to the color registers. D5 = 1 enables the video and normal palette function of color translation. This bit must be 0 to load the palette registers (AR0-ARF). After the palette registers have been loaded, this bit must be set to 1 to enable the video data.

D7 indicates the current state of the Attributes flip flop that toggles between the Attributes Address and Data Registers. D7 = 0 when the Attributes Address Register is read and D7 = 1 when any of the Attributes Data Registers is read. This bit is a read only bit. To set this bit to a desired value, you need to reset the flip-flop as described earlier and then it can be toggled to the desired state.

PALETTE REGISTERS (AR0-ARF)

Read-Write Registers
I/O Address: 3C0h : Writes, 3C1h: Reads;
Address Pointer: 00-0Fh

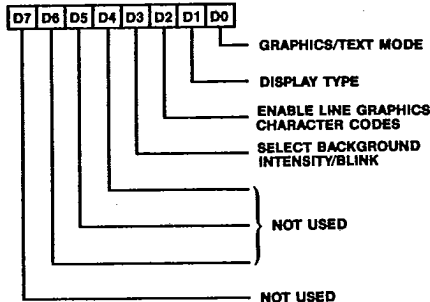


These six bit registers allow a dynamic mapping between the text attribute or graphic color input and the display color on the CRT screen. The six bits, D0-D5 are output as B, G, R, BS, GS/I, and RS/V respectively. A logical 1 in a bit selects the corresponding color for that bit while a 0 de-selects it. The maximum number of possible displayable colors is 64 for monitors with six color inputs. Monitors with 3 color inputs allow a maximum of eight displayable colors, while monitors which also have an intensity input allow a maximum of sixteen displayable colors. **The above description applies to monitors with digital inputs.** The external color palette/DAC is not used to drive the digital monitors.

For analog monitors, the above six video bits are used to drive the external palette (G171 or compatible). The analog R, G and B outputs of the color palette then drive the monitor to produce 16 or 256 colors from a maximum 256K colors. The palette registers in the attribute controller should be programmed for a pass through condition for 256 colors mode.

ATTRIBUTE MODE CONTROL REGISTER (AR10)

Read-Write Register
 I/O Address: 3C0h: Writes, 3C1h: Reads;
 Address Pointer: 10h



Graphics/Text Mode (D0)

D0 = 0 selects text mode. D0=1 selects graphics mode.

Monochrome/Color Display (D1)

D1 = 0 selects color display attributes. D1=1 selects IBM Monochrome display attributes.

Enable Line Graphics Character Codes (D2)

D2 = 0 makes the ninth dot the same as the background. D2 = 1 enables the special line graphics character codes. When this bit is set, it forces the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes for the VGA/MDA are C0H through DFH. The ninth dot is zero (off) for all other characters.

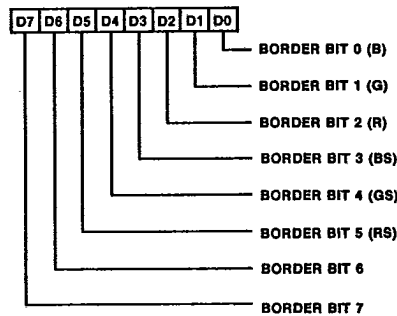
Enable Blink/Select Background Intensity (D3)

D3 = 0 selects the background intensity for the attribute input. D3 = 1 enables the blink attribute in text and graphics modes. The blinking counter operates off the Vertical Sync signal. It divides the VRTC period by 32. For text and graphics modes, the blink is ON for 16 VRTC periods and OFF for 16 VRTC periods. In text mode, the blink affect displays the character for 16 frames and blanks the screen for 16 frames. In the graphics mode,

when blink is activated, the most significant color bit (bit 3) for each pixel is inverted alternately, thus allowing two different colors to be displayed for 16 CRT frames each. When the CURSOR is displayed in the text mode, the 'characters' are blinked at the rate of 16 frames ON and 16 frames OFF. The CURSOR, however, is blinked at a rate of ON for 8 frames and OFF for 8 frames.

OVERSCAN COLOR REGISTER (AR11)

Read-Write Register
 I/O Address: 3C0h: Writes, 3C1h: Reads;
 Address Pointer: 11h

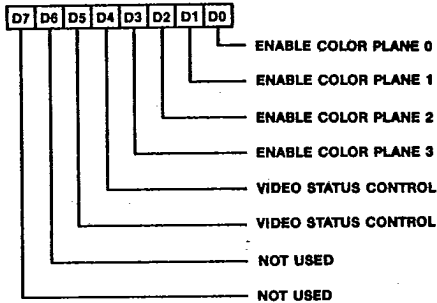


Overscan Color

This eight-bit register defines the overscan or border color displayed on the CRT screen. For monochrome displays, this register should be cleared to logical 0. A logical 1 selects the corresponding color. The border color is displayed in the interval after Display Enable End and before Blank Start and between Blank End and Display Enable Start (the beginning).

COLOR PLANE ENABLE REGISTER (AR12)

Read-Write Register
I/O Address: 3C0h: Writes, 3C1h: Reads;
Address Pointer: 12h



Enable Color Plane (D0-D3):

A logical 1 in any of the bits D0-D3 enables the respective color bits for each pixel. If any bit is set to zero, the corresponding bit of the pixel data from memory is forced to zero before accessing the palette.

Display Status MUX (D4-D5):

Bits D4 and D5 select two of the six primary outputs (V0-V5) to the CRT screen. The output color combinations available on the status bits are listed in the following table:

COLOR PLANE ENABLE REGISTER		VGA STATUS REGISTER 1 OUTPUTS	
D5	D4	Bit5	Bit4
0	0	Red	Blue
0	1	Secondary Red	Secondary Green
1	0	Secondary Blue	Green
1	1	Not Used	Not Used

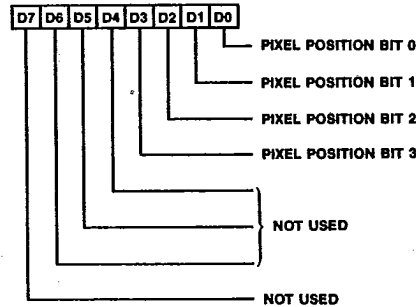
This capability can be used to run diagnostics on the color sub-system card.

D4 = 1 will also:

- Tri-state the color monitor outputs, R, G, B, RS, GS/I and BS/V and,
- Clear the cursor blink counter. D4 must be cleared to logical 0 for the cursor blink counter to function.

HORIZONTAL PIXEL PANNING REGISTER (AR13)

Read-Write Register
I/O Address: 3C0h: Writes, 3C1h: Reads;
Address Pointer: 13h



Horizontal Pixel (Pel) Panning

Bits D0-D3 select the number of pixels to shift the display data horizontally to the left. Pixel panning is available in both text and graphics modes. In monochrome text mode the output can be shifted a maximum of 9 pixels, whereas in all other modes a maximum shift of 8 pixels is possible. The Start Address Register specifies the byte of the upper left corner of the screen display, and pixel panning gives pixel resolution to the left end of the display. In the 256 color mode, this register **must** always have even values.

CRT Controller

The CRT Controller provides the synchronization signals for the display monitor. The CRT Controller contains various CPU accessible I/O registers, that allow flexible configuration options. These options include user configurable horizontal and vertical timings and polarity, cursor type and position, horizontal scan lines, and several other display related characteristics. The CRT controller also provides split screen capability and soft scrolling.



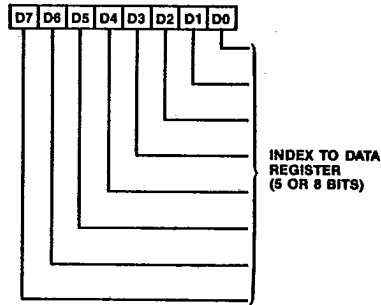
CRT Controller Registers

Register Address Number	Register Name	Pointer	Address
—	Address Register	—	3B4h/3D4h
CR0	Horizontal Total	00	3B5h/3D5h
CR1	Horizontal Display End	01	3B5h/3D5h
CR2	Start Horizontal Blanking	02	3B5h/3D5h
CR3	End Horizontal Blanking	03	3B5h/3D5h
CR4	Start Horizontal Retrace Pulse	04	3B5h/3D5h
CR5	End Horizontal Retrace Pulse	05	3B5h/3D5h
CR6	Vertical Total	06	3B5h/3D5h
CR7	CRT Controller Overflow	07	3B5h/3D5h
CR8	Preset Row Scan	08	3B5h/3D5h
CR9	Maximum Scan Line	09	3B5h/3D5h
CRA	Cursor Start Scan Line	0Ah	3B5h/3D5h
CRB	Cursor End Scan Line	0Bh	3B5h/3D5h
CRC	Start Address High	0Ch	3B5h/3D5h
CRD	Start Address Low	0Dh	3B5h/3D5h
CRE	Cursor Location High	0Eh	3B5h/3D5h
CRF	Cursor Location Low	0Fh	3B5h/3D5h
CR10	Vertical Retrace Start	10h	3B5h/3D5h
CR11	Vertical Retrace End	11h	3B5h/3D5h
CR12	Vertical Display Enable End	12h	3B5h/3D5h
CR13	Offset	13h	3B5h/3D5h
CR14	Underline Location	14h	3B5h/3D5h
CR15	Start Vertical Blanking	15h	3B5h/3D5h
CR16	End Vertical Blanking	16h	3B5h/3D5h
CR17	CRT Mode Control	17h	3B5h/3D5h
CR18	Line Compare	18h	3B5h/3D5h
CRF7	Tag Register 0 ²	F7h	3B5h/3D5h
CRF8	Tag Register 1 ²	F8h	3B5h/3D5h
CRF9	400 Line Register ²	F9h	3B5h/3D5h
CRFA	Temporary Storage 0 ^{1,2}	FAh	3B5h/3D5h
CRFB	Temporary Storage 1 ^{1,2}	FBh	3B5h/3D5h
CRFC	Temporary Storage 2 ^{1,2}	FCh	3B5h/3D5h
CRFD	Temporary Storage 3 ^{1,2}	FDh	3B5h/3D5h
CRFE	Temporary Storage 4 ^{1,2}	FEh	3B5h/3D5h
CRFF	Emulation Mode Register ²	FFh	3B5h/3D5h

(1—in 82A442, 2—used in CRTC Extended Mode only)



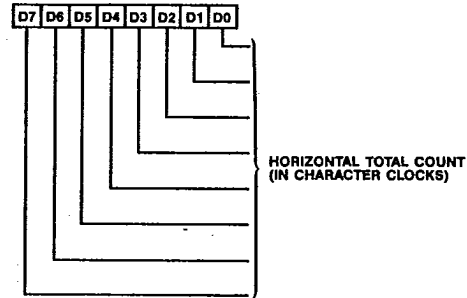
ADDRESS REGISTER
Read-Write Register
I/O Address: 3B4h/3D4h



The CRT Controller Registers are all located at two byte addresses in the CPU I/O space. The registers are accessed by first writing an pointer to the actual data register into the CRT Controller Address Register and then accessing the CRT Controller Data Register. The Address Register is located at I/O address 3B4h/3D4h. The data registers are all located at I/O address 3B5h/3D5h. The exact address 3Bx/3Dx is selected thorough bit D0 of the Misc. Output Register (I/O ADD.3C2h).

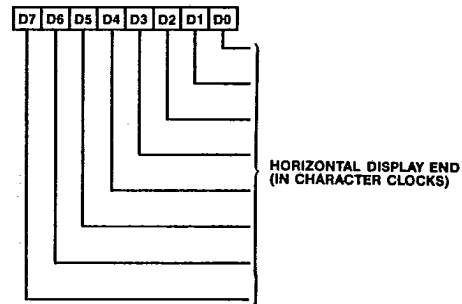
The Address Register is normally a 5 bit register with the upper 3 bits being ignored. When the CRTC Extended Mode Registers are enabled through register CR17, all 8 bits of the Address Register are used to point to the appropriate data register. When this register is read, D6 and D7 are always '1'. D5 is '1' if D6 and D7 were written as 1. D5 is '0' if D6 or D7 were written as 0.

HORIZONTAL TOTAL REGISTER (CR0)
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 00h



The Horizontal Total Register defines the total number of characters in a horizontal scan line, including the retrace time. This defines the horizontal sweep rate. The character clock is derived from the dot clock as defined by the Sequencer Clocking Mode Register. The actual number of character clocks per horizontal scan is two more than the value programmed in this register.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR1)
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 01h

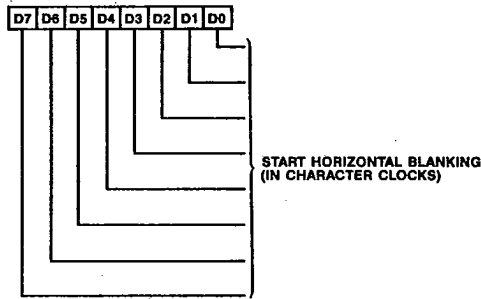




The Horizontal Display Enable End Register defines the number of characters to be displayed per horizontal line. The actual characters displayed per horizontal line is one more than the contents of this register.

START HORIZONTAL BLANKING REGISTER (CR2)

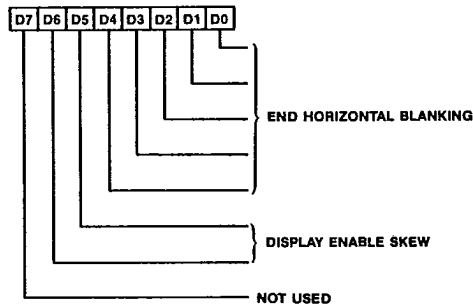
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 02h



The contents of the Start Horizontal Blanking Register define the time when the horizontal blanking will start. The register is defined in terms of the number of horizontal character clocks. The period between horizontal display enable end and horizontal blanking start is the right side border on the screen.

END HORIZONTAL BLANKING REGISTER (CR3)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 03h



The contents of the End Horizontal Blanking Register define the time when the horizontal blanking will terminate. The register is defined in terms of the number of character clocks.

D0-D4 End Horizontal Blanking: The horizontal blanking signal width, W, is determined as follows:

Value in Start Blanking Register + W = 5-bit value to be programmed in End Horizontal Blanking Register.

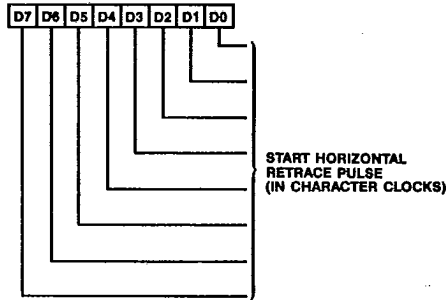
The five least significant bits of the horizontal character counter are compared with the contents of this register. When a match occurs, the horizontal blanking pulse becomes inactive. Note that the five bits of this register limit the length of the blanking pulse to 31 character clocks.

D5-D6 Display Enable Skew Control: Prior to displaying data on the screen, the 82C441 has to fetch the character and attribute code, then access the character generator font and finally read the Pixel Panning Register in the Attributes Controller. Each one of these accesses require the display enable signal to be skewed by one character clock to allow for synchronization with the horizontal and vertical retrace pulses. The display enable skew bits in this register allow for this skew. The skew can be programmed from 0-3 character clocks as follows:

		Skew in character clocks	
D6	D5		
0	0	0	
0	1	1	
1	0	2	
1	1	3	

START HORIZONTAL RETRACE PULSE REGISTER (CR4)

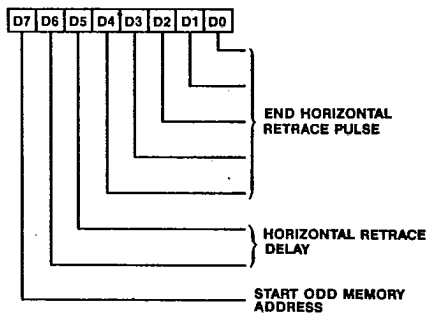
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 04h



The Start Horizontal Retrace Pulse Register defines the character position at which the Horizontal Retrace Pulse becomes active. It is used to center the monitor screen horizontally. The value in the register is the character count at which the Horizontal Retrace Pulse becomes active.

END HORIZONTAL RETRACE PULSE REGISTER (CR5)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 05h



The contents of the End Horizontal Retrace Register define the character count at which the Horizontal Retrace Pulse becomes inactive.

D0-D4 End Horizontal Retrace: The horizontal retrace signal becomes inactive after the character count becomes equal to the count in these bits. The width, W, of the retrace signal (in character clocks) is determined as follows:

Value in Horizontal Retrace Start Register + W = 5-bit result to be programmed in End Horizontal Retrace Register.

The five least significant bits of the horizontal character counter are compared to the contents of this register. When a match occurs, the horizontal retrace pulse becomes inactive. Note that the 5 bit register limits the length of the retrace signal to 31 character clocks maximum.

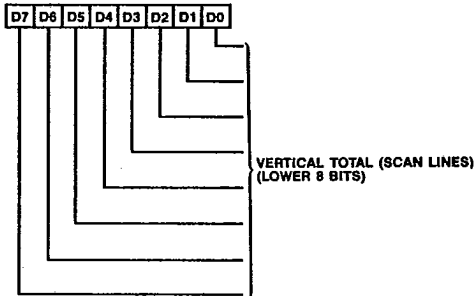
D5-D6 Horizontal Retrace Delay: The skew of the horizontal retrace signal is controlled by these bits. For some monitors, it is necessary to provide a horizontal retrace signal that takes up the entire blanking period. The horizontal retrace signal also triggers some internal timings on the falling edge of the signal. To ensure that the signals are latched properly, the retrace signal is started before the end of the display enable signal. It is then skewed several character clocks to provide the proper screen centering.

		Skew in character clocks
D6	D5	
0	0	0
0	1	1
1	0	2
1	1	3

D7 Start Odd/Even Memory Address:
 This bit determines the CRT memory address after a horizontal retrace. D7 = 0 selects an even address, and D7 = 1 selects an odd address. In most cases this bit should be set to '0'. The bit is useful in applications where horizontal pixel panning is required.

VERTICAL TOTAL REGISTER (CR6)

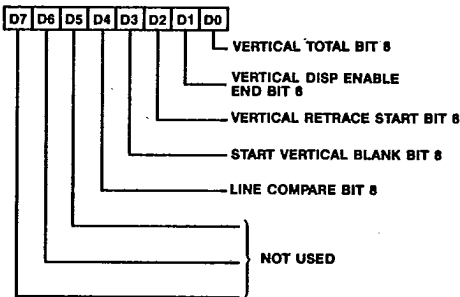
Read-Write Register
 I/O Address: 3B5h/3D5h
 Address Pointer: 06h



The Vertical Total Register contains the 8 low order bits of a 9 bit register. The ninth bit is located in the CRT Controller Overflow Register. The Vertical Total Register defines the total number of scan lines (horizontal retrace periods) per frame.

CRT CONTROLLER OVERFLOW REGISTER (CR7)

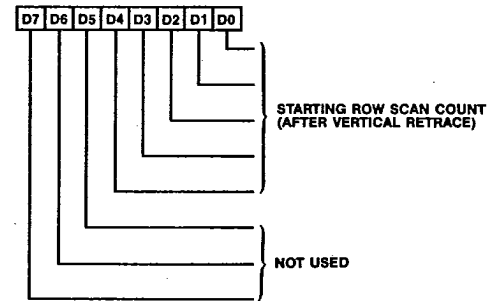
Read-Write Register
 I/O Address: 3B5h/3D5h
 Address Pointer: 07h



The CRT Controller Overflow Register contains the ninth bit (D8) of Vertical Total, Vertical Retrace Start, Start Vertical Blanking and Line Compare Registers.

PRESET ROW SCAN REGISTER (CR8)

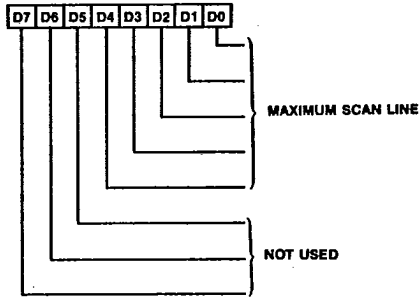
Read-Write Register
 I/O Address: 3B5h/3D5h
 Address Pointer: 08h



D0-D4 of the Preset Row Scan Register specify the starting row scan count after a vertical retrace. Each horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count, which is programmed through register CR9. This register is used for soft scrolling in text modes and in the Hercules Graphics or CGA graphics modes.

MAXIMUM SCAN LINE REGISTER (CR9)

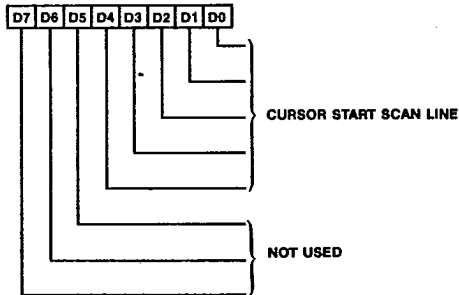
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 09h



The contents of the Maximum Scan Line Register specifies the number of scan lines per character row. This actual number of scan lines per row is the contents of this register plus one.

CURSOR START SCAN LINE REGISTER (CRA)

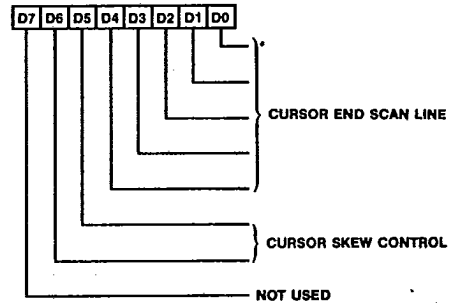
Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: 0Ah



The Cursor Start Register defines the scan line within a character row where the cursor block is to begin. The first scan line for the cursor is the contents of this register.

CURSOR END SCAN LINE REGISTER (CRB)

Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 0Bh



The Cursor End Register defines the scan line within a character row where the cursor block is to end. It also controls the cursor skew as described below:

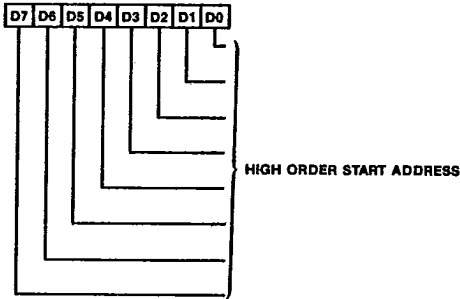
D0-D4 the last scan line for the block cursor is the contents of this field minus one.

D5-D6 The cursor skew is controlled by these two bits. The bits control the skew as follows:

D6	D5	Skew
0	0	Zero character skew
0	1	One character skew
1	0	Two character skew
1	1	Three character skew

START ADDRESS HIGH REGISTER (CRC)

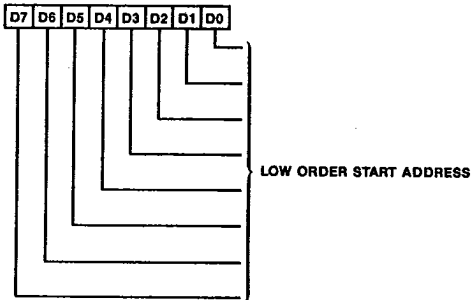
Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 0Ch



The Start Address is a 16-bit value which specifies the first word address in the display buffer for the screen refresh process. This display buffer address is mapped to the upper left corner of the screen. The Start Address High Register contains 8 high order bits of the address, while the Start Address Low Register specifies the other 8 low order bits. Byte resolution on this address can be achieved through the Extended Mode Register (CRF9-bit D1).

START ADDRESS LOW REGISTER (CRD)

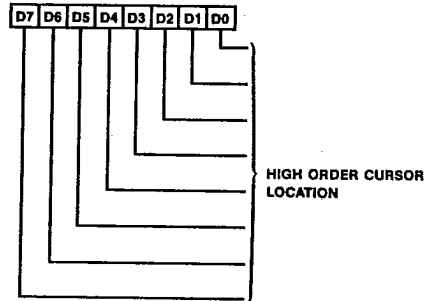
Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 0Dh



The Start Address Low Register contains the 8 low order bits of the Start Address (word address).

CURSOR LOCATION HIGH REGISTER (CRE)

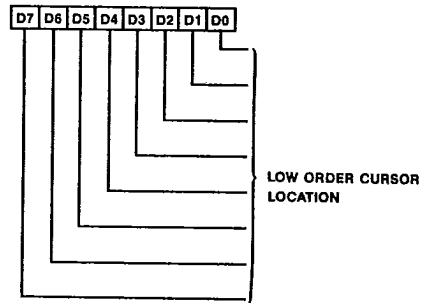
Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 0Eh



The Cursor Location address is a 16-bit value. The 8 high order bits are programmed in the Cursor Location High Register. The other 8 low order bits are programmed in the Cursor Location Low Register. The 16-bit word address defines the memory address for the character which should have the cursor super-imposed on it.

CURSOR LOCATION LOW REGISTER (CRF)

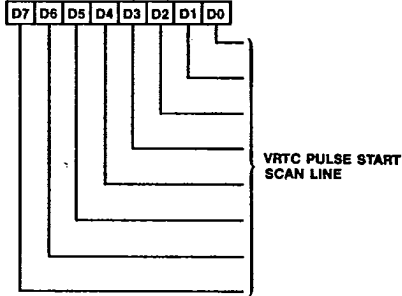
Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 0Fh



In conjunction with the Cursor Location High Register, the Cursor Location Low Register defines the low order 8 bits of the cursor location.

VERTICAL RETRACE START REGISTER (CR10)

Read-Write Register.
I/O Address: 3B5h/3D5h;
Address Pointer: 10h



The Vertical Retrace Start Register is a 9-bit address which defines the scan line position of the VRTC pulse. The low order 8 bits are programmed through this register, while the high order ninth bit is programmed through the Overflow Register, CR7.

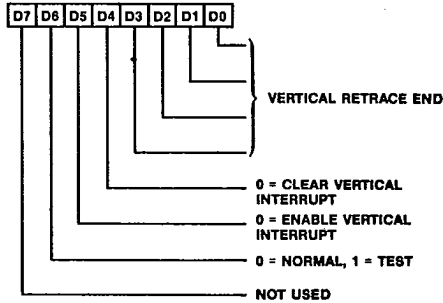
compared with the four least significant bits of the scan line counter. When the four counter bits are equal to the contents in this register, the vertical retrace is terminated. The maximum retrace pulse width can only be 15 scan lines. The width, W, of the vertical retrace pulse can be determined as follows:

Value of Start Vertical Retrace Register + W = Four bit value to be programmed into the End Vertical Retrace Register.

- D4 Clear Vertical Interrupt: This bit is used to clear the vertical interrupt generated on the CRTINT output. A logical 0 will clear the interrupt.
- D5 Enable Vertical Interrupt: A logical 0 will enable the vertical interrupt of the CRT Controller.
- D6 Test: For normal operation this bit must be set to logical 0.

VERTICAL RETRACE END REGISTER (CR11)

Read-Write Register.
I/O Address: 3B5h/3D5h;
Address Pointer: 11h

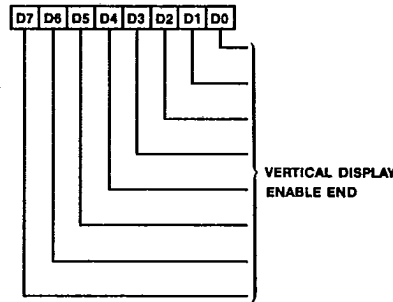


The Vertical Retrace End Register performs multiple functions, as described below:

- D3-D0 Vertical Retrace End: These four bits specify the scan line count at which the vertical retrace output pulse becomes inactive. The four bits are

VERTICAL DISPLAY ENABLE END REGISTER (CR12)

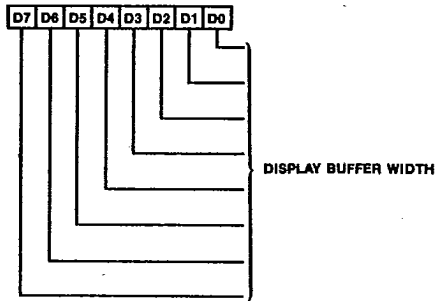
Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 12h



The Vertical Display Enable End Register defines 8 bits of the 9-bits address which specifies the scan line position where the display on the screen ends. The ninth bit is located in the Overflow Register CR7.

OFFSET REGISTER (CR13)

Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 13h



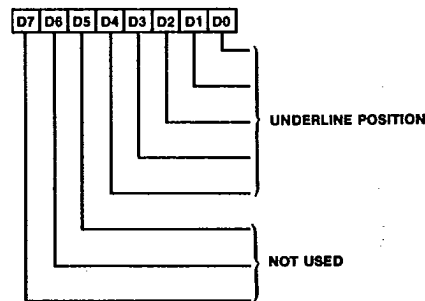
The Offset Register contents define the width of the Display Buffer currently used. This register is used to compute the memory starting address for the next display row (or scan line in graphics modes). The byte starting address of the next display row is computed as follows:

Byte Start Address for next row = Byte Start Address for current row + K • Contents of Offset Register (where K = 2 in Byte Mode and K = 4 in Word Mode).

The byte or word mode for the memory address counter is selected by the CRT Mode Control Register CR17, bit 6. In the CRT Extended Mode, the 400 Line Register (CRF9) bit D2 allows byte/word resolution to the Display Buffer Width.

UNDERLINE LOCATION REGISTER (CR14)

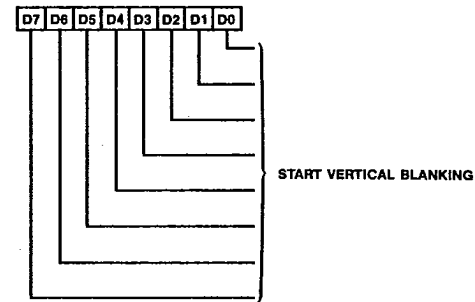
Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 14h



The Underline Location Register specifies the scan line within a character row at which the underline will appear for underlined characters. The value in the register should be one less than the desired scan line number.

START VERTICAL BLANKING REGISTER (CR15)

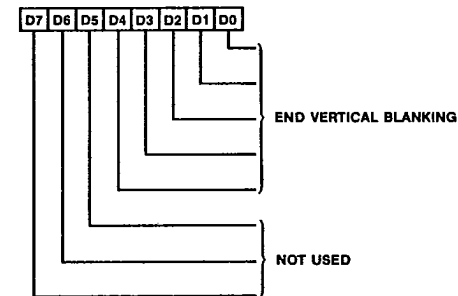
Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 15h



The Start Vertical Blanking Register contains the low order 8 bits of the scan line count at which vertical blanking becomes effective. The ninth bit is located in the Overflow Register CR7.

END VERTICAL BLANKING REGISTER (CR16)

Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 16h

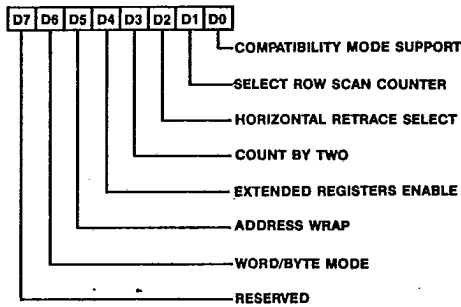


The End Vertical Blanking Register specifies the scan line count at which vertical blanking becomes inactive. The vertical blanking width, W, is determined as follows:

Value of Start Vertical Register + W = 5-bit value to be programmed into the End Vertical Blanking Register.

The five least significant bits of the result are programmed into this register. When the five least significant bits of the horizontal scan line counter are equal to the value in this register, Vertical Blanking is terminated. Note that the maximum width of the vertical blanking is limited to 31 scan lines.

CRT MODE CONTROL REGISTER (CR17)
 Read-Write Register
 I/O Address: 3B5h/3D5h;
 Address Pointer: 17h



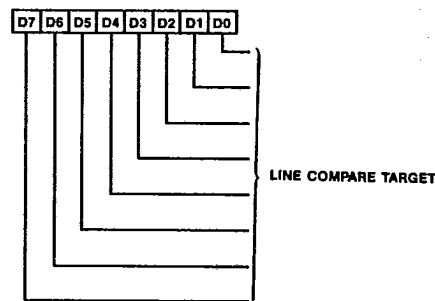
CRT Mode Control Register is a multi-function register, with each bit defining a different option. Following is a description of these bits:

- D0 Compatibility Mode Support: This bit allows compatibility with the IBM CGA 2 bank graphics mode. When D0 = 0, the character row scan line counter bit 0 is substituted for memory address bit 13 during active display time. When D0 = 1, no such substitution takes place.
- D1 Select Row Scan Counter: This bit allows compatibility with the Hercules graphics card and with any other 4-bank graphics system. When D1 = 0, the row scan line counter bit 1 is substituted for memory address bit 14 during active display time. When D1 = 1, no such substitution takes place.
- D2 Horizontal Retrace Select: This bit controls the vertical resolution capability of the CRT Controller. The vertical counter has a maximum resolution of 512 scan lines as defined by the Vertical Total Register. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, then the vertical resolution is doubled to 1024 horizontal scan lines. D2=0 selects the horizontal retrace clock, and D2=1 selects the horizontal retrace clock divided by 2.

- D3** **Count By Two:** This bit selects the character clock as the clock input or character clock divided by 2 as the character clock. This bit defines whether the contents of the Offset Register are a memory or a double word value. When D3 = 0, the memory address counter is clocked by the character clock input. When D3 = 1, the memory address is clocked by the character clock input divided by 2. This bit is also used to create either a byte or word refresh address for the display memory.
- D4** **Extended Register Enable:** D4 = 0 is the default on reset. In this case the 82C441 behaves exactly as an VGA. When D4 = 1, then all the Extended Mode Registers in the 82C441 become enabled. These registers are used for compatibility with CGA/MDA/Hercules graphics card and to save/restore the context of the 82C441. All extended register functionality is gated with this bit. The extended registers can always be read or written regardless of this bit.
- D5** **Address Wrap:** Since the 82C441 does not support 64 Kbytes of display memory (it requires 256 Kbytes), this bit must always be one for all VGA/EGA modes. In the CGA mode, this bit must be set to 0.
- D6** **Word Mode or Byte Mode:** When D6 = 0, Word Mode is selected. This mode causes the display memory address counter bits to shift down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output. D6 = 1 selects the Byte mode.
- D7** **Reserved Bit.** This bit should be set to '1' for proper operation of the chip.

LINE COMPARE REGISTER (CR18)

Read-Write Register
I/O Address: 3B5h/3D5h;
Address Pointer: 18hH



The Line Compare Register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address generator is cleared to 0. The display buffer address generator then sequentially addresses the display buffer starting at address 0. Each subsequent row address is generated by the addition of Offset Register contents.

This feature allows a given area on the screen to be immune to scrolling. The scrolling operation utilizes the Start Address High and Low Registers, and the split screen screen capability will allow scrolling through some areas of the screen while the remaining screen remains immune to it.

The CRT Controller provides all the timing and control signals for the display monitor. Figure 9 shows a graphic illustration of how the contents of these registers control the display screen. The horizontal blanking signal is controlled by the contents of CR2 and CR3 registers. Similarly, the contents of CR15 and CR16 determine the location and length of the vertical blanking signal. The screen blanking signal BLANK is a logical 'OR' of HBLANK and VBLANK as programmed in the respective registers. The horizontal retrace

start location and width are controlled by the contents of CR4 and CR5 registers, while the vertical retrace start location and width are controlled by the CR10 and CR11 registers. CR0 controls the total number of characters in the horizontal scan interval, including the

retrace time. The total number of scan lines on one raster are determined by the vertical total register CR6. CR1 and CR12 define the effective display area on the screen by specifying the horizontal and vertical display enable positions, respectively.

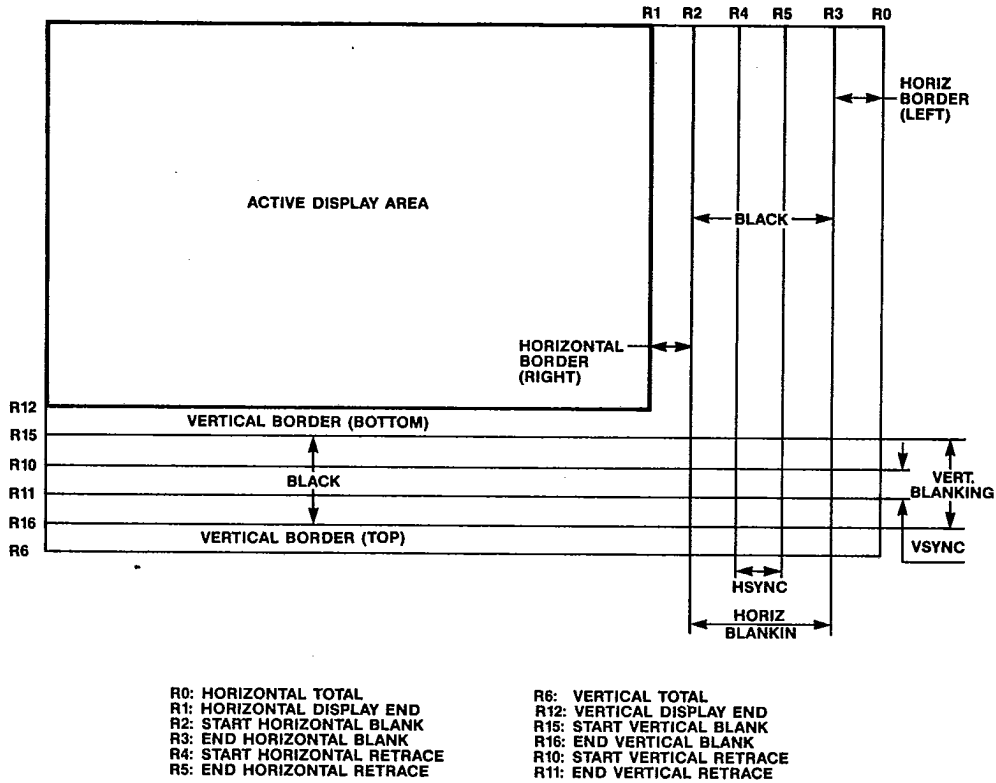


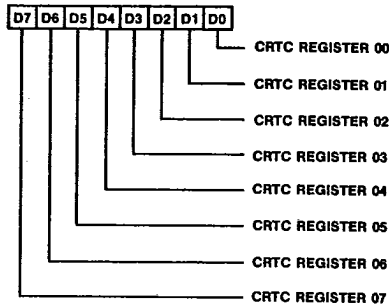
Figure 9: Raster Parameters

CRTC EXTENDED REGISTERS

The CRTC Extended Registers are located in the CRT Controller address space (Address Pointer at 3B4h/3D4h and Data Register at 3B5h/3D5h). These registers are functional only after bit D4 of the CR17 Register is set.

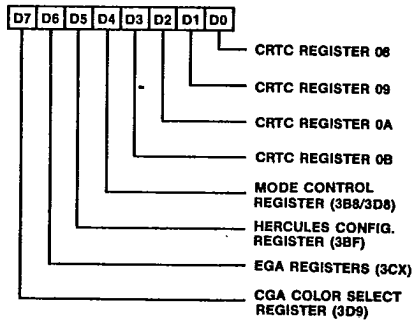
TAG REGISTER 0 (CRF7)

Read-Clear Register
I/O Address: 3B5h/3D5h;
Address Pointer: F7h



TAG REGISTER 1 (CRF8)

Read-Clear Register
I/O Address: 3B5h/3D5h;
Address Pointer: F8h

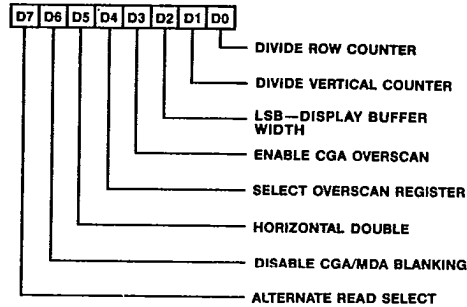


Tag Registers 0 and 1 are located at offset 0F7h (Tag Register 0) and 0F8h (Tag Register 1) in the CRT Controller. They can be accessed by first writing 0F7h/0F8h in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h).

A bit in these registers is set whenever the corresponding register is written into. When traps are enabled, then any bit set in the two Tag Registers will cause a trap. When emulation is in progress, then the emulation software can read these registers to determine which register access caused the trap resulting in the emulation software being invoked. Reading these registers clears the registers, serving as a trap acknowledge.

400 LINE REGISTER (CRF9)

Read-Write Register
I/O Address: 3B5h/3D5h
Address Pointer: F9h



The 400 Line Register is located at offset 0F9h in the CRT Controller. This register can be accessed by first writing 0F9h in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h).

The description for the individual bit fields is as follows:

- D0** Divide Row Counter: D0 = 0 causes the scan line (in a row) counter to be incremented every scan line. D0 = 1 causes this counter to be incremented every two scan lines. This bit when set to '1', causes the display memory to be scanned twice for each scan line. This bit should be set to '1' when it is desired to run 200 scan line software on a 400 line monitor. Power-on reset clears this bit.



- D1 **Divide Vertical Counter:** D1 = 0 causes the vertical counters to be incremented every scan line. D1 = 1 causes the vertical timing counters to be incremented every two scan lines. This bit should be set to 1 when it is desired to double each scan line (running 200 scan line software on a 400 scan line monitor). Power-on reset clears this bit.

- D2 **LSB-Display Buffer Width:** This is the complement of the least significant bit for the Display Buffer Width (CRTC Offset Register CR13). This allows byte resolution on the Display Buffer Width.

- D3 **Enable CGA Overscan:** D3 = 0 disables the CGA overscan (border) feature provided bits D3 and D2 of Emulation Mode Register (CRFF) are both 1. This is useful when running CGA software on a 21.8 KHz monitor, when it may be desirable to disable the borders. D3 = 1 enables the border. This bit is effective only in 80 column text mode.

- D4 **Select Overscan Register:** D4 = 0 selects the CGA Color Select Register (hardware palette) as the source for the border color. D4 = 1 selects the Attribute Controller Overscan Color Register as the source for the border color. This bit is ignored in the VGA/EGA mode.

- D5 **Horizontal Double:** D5 = 0 causes the CRTC to generate a 640*200 display when programmed for a 320*200 display. D5 = 1 generates a 320*200 display. When emulating the 640*200 CGA mode, it is easier to algorithmically translate the 6845 parameters to EGA CRTC parameters in the 320*200 mode. Setting this bit to 0 results in a 640*200 display. This bit is used only when emulating 640*200*1 CGA graphics mode. For all other modes, this bit must be programmed high.

- D6 **Disable CGA/MDA Blanking:** D6 = 1, disables the functionality of the Display Blanking feature of the CGA and MDA Mode Control Registers—bit D3 of MDA CRT Control Register (I/O address 3B8h) and bit D3 of CGA Mode Control Register (I/O address 3D8h). D6 = 0 enables this functionality.

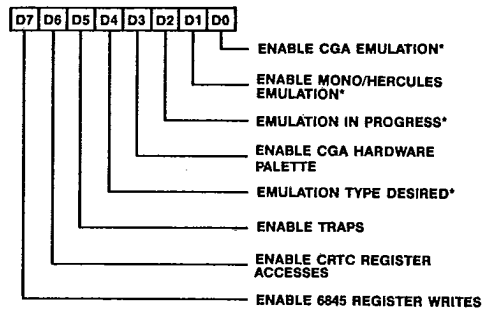
- D7 **Alternate Read Select:** D7 = 0 returns the contents of the Feature control Register (I/O Address 3BAh/3DAh) and Miscellaneous output Register when reading CRTC Registers CRE and CRF respectively. D7 = 1 returns the contents of the Cursor Location High and Low Registers when reading CRTC Registers CRE and CRF respectively. On reset, this bit is set to 1.

Temporary Storage Registers

There are five byte wide temporary storage read-write registers in the 82A442. These registers are located at offset 0FAh-0FEh in the CRTC Controller data register space. These registers can be accessed by first writing 0FAh/0FBh/0FCh/0FDh/0FEh in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h). These registers can be used as working registers.

EMULATION MODE REGISTER (CRFF)

Read-Write Register
 I/O Address: 3B5h/3D5h;
 Address Pointer: FFh



* (82C441 AND 82A442)

The Emulation Mode Register is located at offset 0FFh in the CRT Controller. This register can be accessed by first writing 0FFh in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h).

The description for the individual bit fields is as follows:

D0 Enable CGA Emulation: This bit determines if CGA Emulation is to be enabled (=1) or disabled (=0). This bit should be '1' to enable writing to the CGA Color Select Register (I/O Add.3D9h).

D1 Enable Mono/Hercules Emulation: This bit determines if Monochrome/Hercules Emulation is to be enabled (=1) or disabled (=0). (See page 43)

To automatically allow switching between VGA/EGA, CGA and Hercules emulation modes, CRFF bits D0 and D1 must be set as follows.

Switching between D1 D0 modes		
0	0	Lock into VGA mode only.
0	1	Allow auto-emulation between VGA and CGA mode only.
1	0	Allow auto-emulation between VGA and Hercules modes only.
1	1	Allow auto-emulation between VGA, CGA and Hercules modes.

D2 Emulation in Progress: This bit determines if the 82C441 is currently in the CGA or Hercules emulation mode (=1) or in the normal VGA mode (=0). This bit must be set while CGA/MDA/Hercules emulation is in progress.

D3 Enable CGA Hardware Palette: A one in this bit selects the CGA Color Select Register (at I/O address 3D9h) to generate the colors to be displayed. A zero in this bit causes colors to be selected from the EGA Attribute Controller Palette. When this bit is set to 1, then TAG Register 1 bit 7 (CGA Color Select Register is disabled).

D4 Emulation Type: This is a read only bit that indicates what type of emulation is desired by the application software. If CGA emulation is enabled (D0 of this register) then any access to I/O address 3D8h will cause this bit to be set to zero indicating that CGA emulation is desired. If Mono/Hercules emulation is enabled (D1 of this register) then any access to I/O address 3B8h causes this bit to be set to one indicating that Monochrome/Hercules emulation is desired.

D5 Enable Traps: A one in this bit generates a trap indicating processor support required for emulation whenever emulation is enabled and software desires a change in mode. A zero in this bit disables the traps

A trap is generated under any one of the following conditions:

- a) Write to I/O address 3BFh when Emulation Mode Register bit D1 = 1 (Hercules emulation enabled and access to Hercules Configuration Register).
- b) Write to I/O address 3B8h when Emulation Mode Register bit D1 = 1 and bit D2 = 0 (Currently in VGA mode, Hercules emulation enabled and access to Hercules Mode Control Register).
- c) Write to I/O address 3B8h when Emulation Mode Register bit D1 = 1, bit D2 = 1 and bit D4 = 0 (Currently emulating CGA and access to Hercules Mode Control Register).



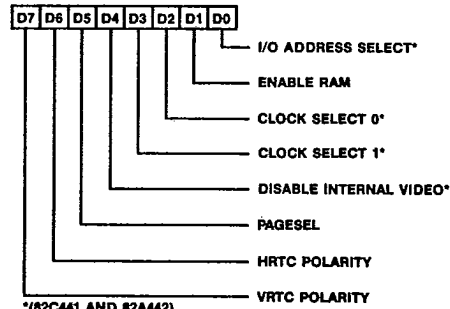
- d) Write to I/O address 3B8h when Emulation Mode Register bit D1 = 1, bit D2 = 1, bit D4 = 1, Hercules Mode Control Register bit D3 = 1 and bit D1 toggles (currently emulating Hercules, video enabled and switch between text and graphics modes).
 - e) Write to I/O address 3D8h when Emulation Mode Register bit D0 = 1 and bit D2 = 0 (Currently in VGA mode, CGA emulation enabled and access to CGA Mode Control Register).
 - f) Write to I/O address 3D8h when Emulation Mode Register bit D0 = 1, bit D2 = 1 and bit D4 = 1 (Currently emulating Hercules and access to CGA Mode Control Register).
 - g) Write to I/O address 3D8h when Emulation Mode Register bit D0 = 1, bit D2 = 1, bit D4 = 0, CGA Mode Control Register bit D3 = 1 and any one of bits D0, D1, D2 or D4 change state (currently emulating CGA, video enabled and mode switch).
 - h) Write to I/O address 3D9 when Emulation Mode Register bit D0 = 1 and bit D3 = 0 (CGA emulation enabled, CGA hardware palette disabled and access to CGA Color Select Register).
 - i) Write to any one of I/O addresses 3C0h, 3C2h, 3C4h, 3C5h, 3CAh, 3CCh, 3CEh or 3CFh when Emulation Mode Register bit D2 = 1 (currently emulating Hercules or CGA and access to any VGA only register).
 - j) Write to I/O address 3B5h when Emulation Mode Register bit D7 = 1, Misc. Output Register bit D0 = 0 and CRTC Address Register = 00 through 0Bh (emulating Hercules/CGA and access to the Hercules 6845 Data Register).
 - k) Write to I/O address 3D5h when Emulation Mode Register bit D7 = 1, Misc. Output Register bit D0 = 1 and CRTC Address Register = 00 through 0Bh (emulating Hercules/CGA and access to the CGA 6845 Data Register).
- D6** Enable CRTC Registers: A one in this bit causes data writes to I/O address 3B5h/3D5h to be directed to the CRT Controller Registers. For data read operation at I/O address 3B5h/3D5h, D6 = 1 reads the CRTC registers and D6 = 0 reads the 6845 registers.
- D7** Enable 6845 Registers: A one in this bit causes data writes to I/O address 3B5h/3D5h to be directed to the 6845 registers. Simultaneously setting D6 and D7 = 1 causes both the CRTC and 6845 registers to be written.

Other VGA Registers

Register Name	Address
Miscellaneous Output	3C2h
Feature Control Register	3BAh/3DAh
Input Status Register 0	3C2h
Input Status Register 1	3BAh/3DAh

MISCELLANEOUS OUTPUT REGISTER

Read/Write Register
I/O Address: 3C2h



The Miscellaneous Output Register is normally a write only register. It can be read by setting the alternate read select bit in the 400 Line Register (CRF9 bit D7 = 0) and then reading CRTC Data Register at offset 0Fh. This register performs the following functions:

D0 This bit maps the CRT Controller address and data registers into the 3Bxh/3Dxh address space. This bit defaults to 0 on reset and is present in both the 82C441 and 82A442. Setting this bit to 0 or 1 maps the registers as follows:

Register Name	I/O Address for D0=0 D0=1
CRTC Address Register (82C441/82A442)	3B4h 3D4h
CRTC Data Register (82C441/82A442)	3B5h 3D5h
Feature Control Register (82C441/82A442)	3BAh 3DAh
Input Status Register I (82C441/82A442)	3BAh 3DAh

D1 D1 = 0 prevents the CPU from accessing the VGA display memory. D1 = 1 allows such accesses.

D2-D3 D2-D3 bits are output on the CLKSEL0 and CLKSEL1 pins on the 82A442. Typically these are used to externally select the clock source for the 82C441. These bits are present in the 82C441 so that this register can be read correctly.

D4 Disable Internal Video. This bit is used in the 82A442. It is also present in the 82C441 so that this register can be read correctly.

D5 If the display memory is chained to get 128Kbytes and only 64 Kbytes are available in the CPU space, then this bit maps upper and lower 64k of display memory into the CPU address space A0000h - AFFFFh as follows:

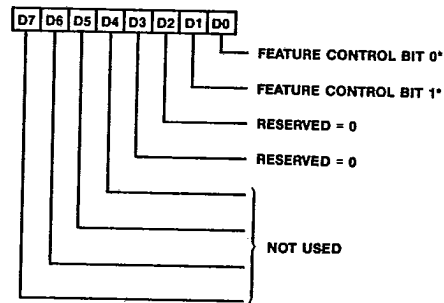
D5 = 1 Lower Display page (64K) is mapped into the CPU space.
D5 = 0 Upper Display page (64K) is mapped into the CPU space.

D6 D6 selects the polarity for the Horizontal Sync pulse.
0 Positive horizontal sync pulse
1 Negative horizontal sync pulse

D7 D7 selects the polarity for the Vertical Sync pulse.
0 Positive vertical sync pulse
1 Negative vertical sync pulse

FEATURE CONTROL REGISTER

Read/Write Register
I/O Address: 3BAh/3DAh



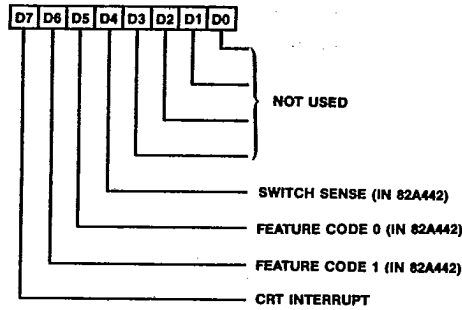
*(82C441 AND 82A442)

The Feature Control Register exists in both the 82C441 and the 82A442. This is normally a write only register in the 82A442. It can be read (in the 82C441) by setting the alternate read select bit in the 400 Line Register (CRF9 bit D7 = 0) and then reading CRTC Data Register at offset 0Eh. Feature Control Bits 0 and 1 from this register are also output on 82A442 output pins FCOUT0 and FCOUT1 respectively. These pins are typically used to drive the EGA Feature Connector.



INPUT STATUS REGISTER 0

Read Only Register
I/O Address: 3C2h



Parts of the Input Status Register 0 exist in both the 82C441 and the 82A442. The data path to the CPU from the 82C441 always goes through the 82A442. When the CPU reads this register, the 82A442 reformats the status data put out by the 82C441 and passes the final status to the CPU.

Switch Sense (D4 — in 82A442)

This bit returns the current status of the 82A442 input pin SWITCH to the CPU. Typically, the CPU scans the state of the DIP switches and the monitor type on the VGA board through this bit.

Feature Code 0 and 1 (D5-D6 — in 82A442)

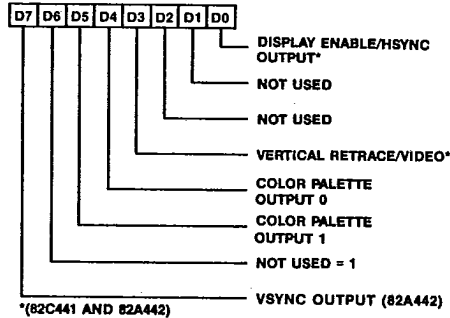
These two bits return the current status of the 82A442 input pins FEATIN0 and FEATIN1 respectively. These bits are typically used to read the status information from the EGA Board Feature Connector.

CRT Interrupt (D7)

D7 is a reflection of the CRTINT output from the 82C441. This bit is 1 if the CRTINT pin is high. CRTINT is enabled through bit D5 of CR11. Once CRTINT goes active, it can only be reset through bit D4 of CR11.

**INPUT STATUS REGISTER 1
(CGA/HERCULES STATUS REGISTER)**

Read Only Register
I/O Address: 3BAh/3DAh



Parts of the Input Status Register 1 exist in both the 82C441 and the 82A442. The data path to the CPU from the 82C441 always goes through the 82A442. When the CPU reads this register, depending on the current emulation mode, the 82A442 reformats the status data output by the 82C441 and passes the final status to the CPU.

Display Enable/HSYNC Output (D0)

In VGA/EGA and CGA modes, D0 is an active low Display Enable signal generated by the 82C441. A logical 0 indicates the active display interval. This bit is returned high during the horizontal and vertical retrace interval. In Hercules emulation mode this bit is driven by the 82A442 and it indicates the current level of the 82C441 Horizontal Sync signal, HIN.

Vertical Retrace/Video (D3)

In VGA/EGA mode, D3 is an active high vertical retrace signal, which is functionally the same as the active high Vertical Sync output (VIN) from the 82C441 (the polarity of this bit is always positive). In CGA emulation mode, D3 is driven by the 82A442 and is same as the Vertical Sync output from the 82C441. In Hercules emulation mode D3 is driven by the 82A442 and it indicates the current status of the Video (Secondary Blue) signal from the 82C441.

Color Palette Output (D4, D5)

D4 and D5 are two bits of the six bit video output from the color palette. Two of these 6 bits can be selectively read by the CPU through bits D4 and D5 of Input Status Register 1. The two output signals to be multiplexed are determined by the contents of the Attributes Color Plane Enable Register (AR12). These bits are valid only in the VGA mode. In the CGA and Hercules modes, the 82A442 always drives these bits high.

Vertical Sync Output (D7)

This bit is valid only in the Hercules emulation mode. In this mode, D7 indicates the current level of the 82C441 Vertical Sync signal (to the monitor). In the VGA and CGA modes, this bit is always high.

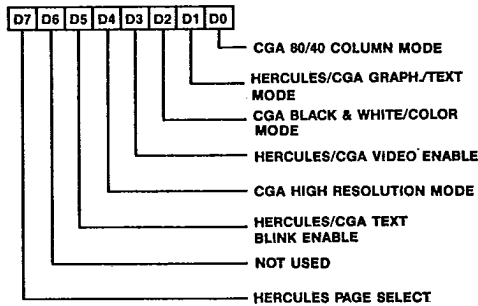
Backward Compatibility Registers

To complete the register description, there are some additional registers in the 82C441/82A442. These registers are:

I/O Address	Register
3B8h/3D8h	Hercules/CGA Mode Control Register (in 82C441)
3D9h	CGA Color Select Register (in 82C441)
3BFh	Hercules Configuration Register (in 82C441)

HERCULES/CGA MODE CONTROL REGISTER

Read/Write Register
I/O Address: 3B8h/3D8h



All the bits in the Hercules/CGA Mode Control Register are effective only when emulation is in progress (CRFF bit D2 = 1). When CGA emulation is in progress (Emulation Mode Register bit D0 = 1), then this register functions as the CGA Mode Register and is located at I/O address 3D8h. When Hercules emulation is in progress (Misc. Output Register bit D0 = 0), then this register functions as the Hercules Mode Register and is located at I/O address 3B8h.

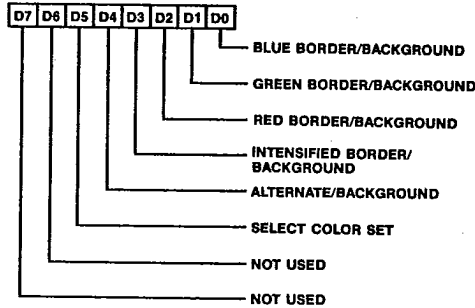
- D0 CGA 80/40 Column Mode: This bit is effective only when CGA emulation is in progress. D0 = 0 selects 40 column CGA text mode. D0 = 1 selects 80 column CGA text mode.
- D1 Hercules/CGA Graphics/Text Mode: D1 = 0 selects the text mode and D1 = 1 selects the graphics mode. This is effective for both CGA and Hercules emulation modes.
- D2 CGA Black & White/Color Mode: This bit is effective only when CGA emulation is in progress. D2 = 1 selects CGA Black & White mode, D2 = 0 selects CGA color mode.
- D3 Hercules/CGA Video Enable: D3 = 1 enables the video signals. D3 = 0 blanks the screen. This is effective for both CGA and Hercules emulation modes.
- D4 CGA High Resolution Mode: This bit is effective only when CGA emulation is in progress. D4 = 0 selects the 320*200 CGA graphics mode, D4 = 1 selects 640*200 CGA graphics mode.
- D5 Hercules/CGA Text Blink Enable: D5 = 1 enables the character blink attribute. D5 = 0 disables the character blink feature and the blink attribute bit is used to control background intensity. This is effective for both CGA and Hercules emulation modes.



D7 Hercules Page Select: This bit is effective only when Hercules emulation is in progress. D7 = 0 selects the lower part of memory (address B0000h onwards) in the Hercules Graphics Mode. D7 = 1 selects the upper part of the memory (address B8000h onwards).

CGA COLOR SELECT REGISTER

Read/Write Register
I/O Address: 3D9h



This registers serves as the CGA hardware palette register. D0 of Register CRFF should be '1' to program this register. This register is effective only when emulation is in progress (CRFF bit D2 = 1). This register can be disabled through the Emulation Mode Register (CRFF bit D3 = 0).

D0 Blue Border/Background: Selects blue border in 40*25 CGA text mode. Selects blue background in CGA 320*200 graphics mode. Selects blue foreground in CGA 640*200 graphics mode.

D1 Green Border/Background: Selects green border in 40*25 CGA text mode. Selects green background in CGA 320*200 graphics mode. Selects green foreground in CGA 640*200 graphics mode.

D2 Red Border/Background: Selects red border in 40*25 CGA text mode. Selects red background in CGA 320*200 graphics mode. Selects red foreground in CGA 640*200 graphics mode.

D3 Intensified Border/Background: Selects Intensified border in 40*25 CGA text mode. Selects Intensified background in CGA 320*200 graphics mode. Selects Intensified foreground in CGA 640*200 graphics mode.

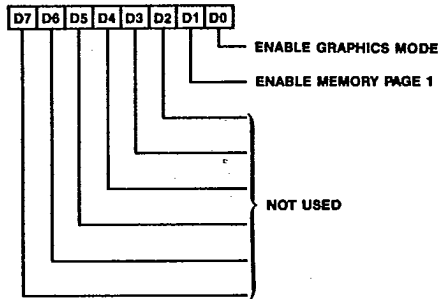
D4 Alternate/Background: Selects alternate intensified colors in CGA graphics mode. Selects background colors in CGA text modes.

D5 Select Color Set: Selects colors in CGA 320*200 graphics mode. The colors are generated as follows:

D5	Pixel		Color
	Bit 1	Bit 0	
0	0	0	Background (= D0-D3)
0	0	1	Green
0	1	0	Red
0	1	1	Brown
1	0	0	Background (= D0-D3)
1	0	1	Cyan
1	1	0	Magenta
1	1	1	White



HERCULES CONFIGURATION REGISTER
Read/Write Register
I/O Address: 3BFh



The Hercules Configuration Register is effective only when Hercules emulation is in progress (CRFF bit D2 = 1) and Misc Output Register bit D0 = 0. Bits D0 and D1 are read at bits D6 and D7 respectively in the Sequencer Address Register (I/O Address 3C4h).

D0 Enable Graphics Mode: D0 = 0 locks the 82C441 in the Hercules/MDA text mode. In this mode, the CPU has access to memory only in the address range B0000h-B0FFFh.

D1 Enable Memory Page 1: D0 = 0 prevents the setting of Page Select bit (D7 in Hercules Mode Control Register). This also restricts memory usage to address B0000h-B7FFFh. D0 = 1 allows setting of the Page Select bit and enables the use of the upper part of the display memory (address B8000h-BFFFFh).

Memory Address Generation

The 82C441 serves as a DRAM controller for the 256 Kbytes of display memory required by the VGA. The 82C441 is responsible for DRAM refresh, fetching of display data (text and graphics mode) from the display memory, and controlling CPU accesses to the display memory. All the DRAM control signals are generated by the 82C441. The 82C441 interfaces to the DRAMs using a multiplexed row address/column address/databus. When the

82C441 accesses the display memory to fetch data to transfer to the screen, the DRAM addresses are generated as required by an internal 16 bit memory address counter (MA0-MA15). All DRAM refreshes are done during the horizontal blanking period. The refresh is done by reading the display memory. The refresh addresses are generated by an internal refresh counter. For CPU accesses to display memory, the 82C441 generates the DRAM row and column addresses as required by the CPU (A0-A16).

The DRAM row/column addresses are generated as follows:

ROW ADDRESSES FOR CPU ACCESS

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0	
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
A7	A6	A5	A4	A3	A2	A1	A0	No Chaining
A7	A6	A5	A4	A3	A2	A1	A16	Chained & CDSEL0,1=00
A7	A6	A5	A4	A3	A2	A1	PAGESL	Chained & CDSEL0,1=01
								10,11

COLUMN ADDRESSES FOR CPU ACCESS

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
A15	A8	A13	A12	A11	A10	A9	A14

ROW ADDRESSES FOR CRT ACCESSES (GRAPHICS MODE)

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

COLUMN ADDRESSES FOR CRT ACCESSES (GRAPHICS MODE)

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
MA15	MA8	MA13	MA12	MA11	MA10	MA9	MA14

ROW ADDRESSES FOR CRT ACCESSES (TEXT MODE)

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
CC2	CC1	CC0	RS4	RS3	RS2	RS1	RS0



COLUMN ADDRESSES FOR CRT ACCESSES (TEXT MODE)

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
MA15	MA8	MA13	MA12	MA11	MA10	MA9	MA14
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
FS1	CC3	0	CC7	CC6	CC5	CC4	FS0

DRAM ADDRESSES IN PACKED PIXEL MODE

ROW ADDRESSES FOR CPU ACCESS

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0

A7	A6	A5	A4	A3	A2	A15	A14
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COLUMN ADDRESSES FOR CPU ACCESS

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0

A15	A8	A13	A12	A11	A10	A9	A14
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ROW ADDRESSES FOR CRT ACCESS

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0

MA5	MA4	MA3	MA2	MA1	MA0	MA13	MA12
-----	-----	-----	-----	-----	-----	------	------

COLUMN ADDRESSES FOR CRT ACCESS

AA7	AA6	AA5	AA4	AA3	AA2	AA1	AA0
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0

MA13	MA6	MA11	MA10	MA9	MA8	MA7	MA12
------	-----	------	------	-----	-----	-----	------

AAx—Multiplexed Memory Address Bus A on 82C441
 BAx—Multiplexed Memory Address Bus B on 82C441
 RSx—Character Row Scan Line Counter Outputs
 FSx—Font Select Codes as programmed in the Sequencer
 MAx—Memory Address/Refresh Counter Outputs
 CCx—Character Code

Display Memory Refresh

The 82C441 automatically generates control signals to refresh the display memory. The refresh is performed during the horizontal blanking period. There is an internal eight bit refresh row address counter in the 82C441. Every horizontal blanking period, this counter is used to generate six read cycles with incrementing row addresses. The user should always program the horizontal parameters in the CRT Controller, so that six refresh cycles per horizontal blanking period is sufficient to meet the refresh specs for the DRAMs being used.

Split Screen

The CRT Controller is capable of displaying split screens. Figure 10 shows a split screen display. The two screens, Screen 1 and Screen 2, are created by properly setting the Memory Address Registers (CRC and CRD) and the Line Compare Register (CR18). The CRC and

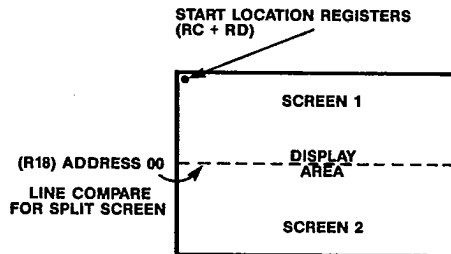


Figure 10. Split Screen Display

CRD register contents specify the memory address for the first pixel to be displayed on the active screen. The start address for Screen 1 in figure 10 is determined by the contents of the registers CRC and CRD. Split screens are created with the use of Line Compare Register CR18. The internal display memory address counter is cleared when the absolute scan line counter reaches the value equal to the contents of CR18. Thus Screen 2 in figure 10 starts at display memory address 0000H. The linear address generator addresses the display buffer sequentially starting at 0000H. Each subsequent row address is determined by the Offset Register contents as described earlier under register description.

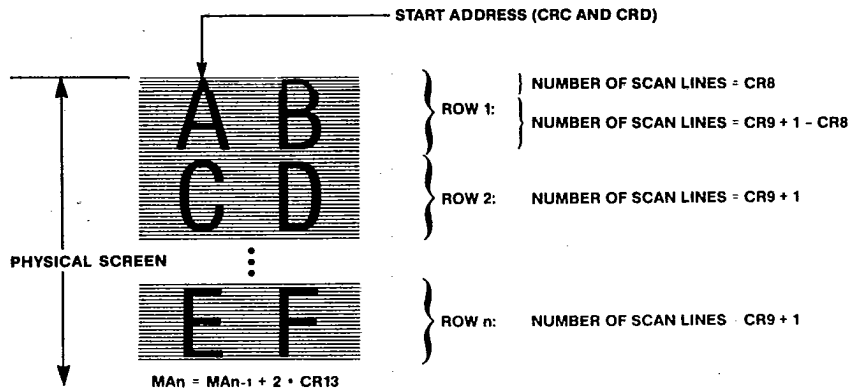
Soft Scroll

The CRT Controller offers soft scrolling capability by pre-setting a value in the Preset Scan Register, CR8. Figure 11 shows a typical example of how this can be achieved. As described in the CRT Controller section, the Start Address Registers CRC and CRD define the address of the first pixel that is displayed on the screen.

In the text mode, the start address is the address of the first character which will be displayed in the first row. The Preset Scan Row Register defines the top scan line for the first character row on the screen. By incrementing CR8, the screen will appear to scroll upwards one scan line at a time. When CR8 becomes equal to CR9 (maximum scan line),

then CR8 should be reset to 0 and the Start Address Registers (CRC and CRD) should be updated to start with the next character row.

The Preset Scan Register should be set to zero for graphics modes. In this mode the vertical scrolling can be controlled by updating the Start Address Registers only.



CR8 = PRESET ROW SCAN
 CR9 = MAXIMUM NUMBER OF SCAN LINES/CHARACTER ROW
 CRC, CRD = DISPLAY BUFFER START ADDRESS
 CR13 = DISPLAY BUFFER WIDTH (OFFSET)
 MA_n = MEMORY ADDRESS FOR FIRST CHARACTER IN THE nth ROW

Figure 11. Soft Scrolling with 82C441; Increment CR8 To Move The Screen Up By One Scan Line



Cursor Control

The height of the CURSOR is programmable through registers CRA and CRB. The memory address of the CURSOR is programmable

through registers CRE and CRF. Figure 12 shows how the CURSOR height is controlled by setting the horizontal scan line equal to the contents of CRA and CRB registers.

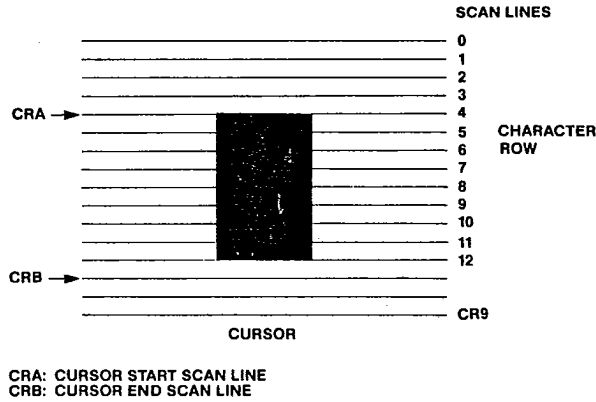


Figure 12. CRT Cursor Control

Vertical Interrupt

The 82C441 generates an interrupt at the end of a vertical display. The Vertical Display End Register CR12 controls the time when the interrupt becomes active, if the interrupt enable bit was cleared in the Vertical Retrace End Register CR11. The interrupt can be used by the CPU to update the 82C441 during the vertical blanking interval.

CGA/MDA/Hercules Compatibility

Compatibility with the CGA, MDA and Hercules display subsystems is required to be compatible with older software that does not support VGA or EGA. There are two levels of compatibility:

- a) Compatibility at memory interface and higher level mode selections,
- b) Compatibility at direct register level

The 82C441/82A442 allow compatibility at both levels described above.

The memory interfaces required are:

CGA 40 Column Text Mode	16 Kbytes at address B8000h
CGA 80 Column Text Mode	16 Kbytes at address B8000h
CGA 160*100 Graphics Mode	16 Kbytes at address B8000h
CGA 320*200 Graphics Mode	16 Kbytes at address B8000h
CGA 640*200 Graphics Mode	2 scan bank format 16 Kbytes at address B8000h
MDA/Hercules Text Mode	4 Kbytes at address B0000h
Hercules Graphics Mode-Half	32 Kbytes at address B0000h
Hercules Graphics Mode-Full	64 Kbytes at address B0000h 4 scan bank format

The 82C441 supports text mode memory organizations required by the CGA and the Monochrome/Hercules boards.

From a software point of view, the accesses that the software makes to the hardware can be categorized as follows (in order of frequency of occurrences):

- a) software access to display memory - this is done to update the character codes and attributes in the text mode and to set the pixel pattern in the graphics modes.
- b) software access to certain hardware registers, these include the CGA Color Select Register (at I/O address 3D9h), the Status Register, the 6845 Cursor Position Registers (Registers 0an45 Start Address Registers (Registers 0Ch and 0Dh).
- c) software access to the other hardware registers, including the mode registers and the video timing (6845 internal) registers.

The 82C441/82A442 provide a direct hardware interface to the software at levels a) and b) described above. Software accesses to the registers at level c) described above are very infrequent. Typically most accesses to these registers is done through the BIOS and the BIOS on the display board should program the VGA registers properly to correspond to the CGA/MDA/Hercules display modes. In the event of some software that directly accesses these registers, the 82C441/82A442 require some assistance from the CPU.

Any software that is configured to run with a CGA/MDA/Hercules board that programs registers on the video boards directly, accesses the registers at I/O addresses 3B8/3D8h Mode Register, 3BFh-Hercules Configuration Register, 3B4/3D4h-6845 Index Register and 3B5/3D5h-6845 Data Register.

The 6845 Index Register is present in hardware on the 82C441. The VGA CRT Controller registers are mapped to the same address space as the 6845 registers. Of the 18 registers in the 6845, 7 have a direct one to one correspondence with the registers on the VGA CRT Controller (Registers 0Ch-11h). The other registers on the 6845 however do not have a one to one correspondence with the VGA CRT Controller registers.

The CPU has to in this case transform the register contents of the 6845 registers and write them into the VGA CRT Controller. To assist in the transform process, the 82C441 has an alternate bank of 11 registers corresponding to 6845 Data Registers 0-08h, 0Ah and 0Bh. These registers are called 6845 Registers. In the emulation mode all CPU accesses to I/O address 3B5h/3D5h (6845/CRTC Data Register) are directed to the CRT Controller Register or the 6845 registers (or both) depending on the contents of the Emulation Mode Register in the 82C441. Whenever a 6845 register is written into, a trap to the CPU is generated in the form of a Non Maskable Interrupt. The Emulation Mode Register also enables or disables such traps. On a write to a 6845 register, a bit is also set in one of two Tag Register in the 82C441. There is one bit in the Tag Registers for each of the 6845 registers, Mode Control Registers and the unique VGAonly Registers. On receipt of an NMI, the CPU should first read the TAG Registers which will indicate which register access generated the trap and requires emulation help. This can also be used to automatically switch from one emulation mode to another emulation mode or to the normal VGA mode. If none of the bits in the Tag Registers are set, it means that the NMI was not generated by the video board but by some other source (eg parity error). The CPU should then be directed to the old NMI handling routine. The emulation software when loaded, redirects the PC NMI vector to point to the emulation software. The old NMI vector can be stored in temporary storage registers in the 82A442 allowing for a safe way to store the old NMI vector.

Traps to the CPU can also be selectively enabled on accesses to the CGA/MDA/Hercules Mode Registers, the CGA Color Palette and the unique VGAonly Registers. Thus it is possible to let the board automatically detect if software wants to use an VGA/CGA/MDA/Hercules modes on the board. It is also possible to disable all the emulation and lock the board in the 100% VGA mode. One advantage of using the NMI to trap CPU accesses to the 6845 is to allow CGA text mode emulation on the enhanced 350 scan line monitor. In this case although the software selects a 200 scan line display, the emulation software can still cause higher quality character to appear on the screen.

6845 Registers

Index Register

0	bits 6-0 of Horizontal Total Register
1	bits 6-0 of Horizontal Displayed Register
2	bits 4-0 of Horizontal Sync Position Register
3	bits 7-0 of Horizontal Sync Width Register
4	bits 6-0 of Vertical Total Register
5	bits 4-0 of Vertical Total Adjust Register
6	bits 6-0 of Vertical Displayed Register
7	bits 6-0 of Vertical Sync Position Register
8	bits 5, 4, 1 and 0 of Interlace Mode Register
Ah	bits 6-0 of Cursor Start Register
Bh	bits 4-0 of Cursor End Register

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Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	-	7.0	V
Input Voltage	V_I	-0.5	$V_{DD} + 0.5$	V
Output Voltage	V_O	-0.5	$V_{DD} + 0.5$	V
Operating Temperature	T_{OP}	-25	85	C
Storage Temperature	T_{STG}	-40	125	C

82C441 Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	4.75	5.25	V
Ambient Temperature	T_A	-40	70	°C

82C441 DC Characteristics

Parameter	Symbol	Min	Max	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage $I_{OL1} = 2mA^1$ $I_{OL2} = 4mA^2$ $I_{OL3} = 8mA^3$ $I_{OL4} = 4mA^4$	V_{OL}		0.45	V
Output High Voltage $I_{OH1} = 2mA^1$ $I_{OH2} = 4mA^2$ $I_{OH3} = 8mA^3$	V_{OH}	3.5		V
Input Leakage Current	I_{IL}	-100	+100	μA
Power Supply Current @ 25 MHz CLKIN, 0C	I_{CC}		100	mA
Output High Impedance Leakage $0.45 < V_{PIN} < V_{DD}$	I_{OZ}	-100	+100	μA

NOTES:

- 2 mA source and sink drive on pins ERMEN, CDSEL0-1, CCLK, DOTCLK, VALRAD
- 4 mA source and sink drive on pins SLOUT, WE0-3, OE02, OE13, AA0-7, BA0-7, R, G, B, RS, BS/V, GS/I
- 8 mA source and sink drive on pins CAS, RAS, BLANK, HIN, VIN, CRTINT, TRAP, RDY
- 4 mA sink drive only (open drain) on pins DATA0-7



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82C441 AC Timing Characteristics

($T_A = 0C - 70C$, $V_{DD} = 5V \pm 5\%$)

CLKIN Timings

Parameter	Symbol	Min(ns)
CLKIN Period	t_c	33
CLKIN High time	t_{ch}	$t_c/2-5\%$
CLKIN Low time	t_{cl}	$t_c/2-5\%$

Video Timings

Parameter	Symbol	Min(ns)	Max(ns)
VIN, BLANK delay from CLKIN	t_{vin}		150
HIN delay from CLKIN	t_{hin}		150
Video delay from CLKIN @	t_{vid}	5	30
SLOUT delay from CLKIN	t_{vid}	5	40

Other Timings

Parameter	Symbol	Min(ns)	Max(ns)
RESET Pulse Width	t20		$64t_c^*$

* In CLKIN/2 mode, t20 must be 128 t_c minimum.

@ $t_{vid} = \frac{\text{Min(ns)} \quad \text{Max(ns)}}{- 5 \quad 20}$

When bit D5 of GRF7 is set to '1'.

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I/O Bus Timings

Parameter	Symbol	Min(ns)	Max(ns)
MIORD, MIOWR Pulse Width	t1	100	
MIORD, MIOWR to RDY Low delay	t2		50
Address setup to MIOWR (I/O Write)	t3	80	
Address hold from MIOWR (I/O Write)	t4	80	
Address setup to MIORD (I/O Read)	t3	20	
Address hold from MIORD (I/O Read)	t4	20	
Memory Address setup to MIORD, MIOWR	t3	20	
MIORD, MIOWR hold from RDY (Memory)	t4a	0	
Trap delay from MIORD, MIOWR	t5		150
MEMIO setup to MIORD, MIOWR	t6	20	
MEMIO hold from MIORD, MIOWR	t7	5	
I/O Write Data setup to MIOWR	t8	45	
I/O Write Data hold from MIOWR	t9	60	
I/O Read Data delay from MIORD	t10		150
I/O Write Data hold from MIORD	t11	5	100
RDY high time	t12	0.5t _c	
Memory Read Data setup to RDY	t13	1.5t _c	
Memory Read Data hold from MIORD	t14	20	
Memory Write Data setup to RDY	t15	6t _c	
Memory Write Data hold from RDY	t16	-1.5t _c	
VALRAD delay from Address	t17		60
CDSEL0, 1 delay from MIOWR	t18		200
RDY width	t21	6t _c	42t _c

DRAM Timings High CPU Bandwidth Mode

Parameter	Symbol	8 dot mode		9 dot mode	
		Min(ns)	Max(ns)	Min(ns)	Max(ns)
Read/Write Cycle time (read)	t_{rc}	$5t_c$	—	$5t_c$	—
RAS Pulse Width (read)	t_{ras}	$3t_c - 8$	—	$3t_c$	—
Read/Write Cycle time (write)	t_{rc}	$6t_c$	—	$8t_c$	—
RAS Pulse Width (write)	t_{ras}	$4t_c - 8$	—	$4t_c$	—
Column Address Hold from RAS	t_{ar}	$1.5t_c + 10$	—	$1.5t_c + 10$	—
RAS precharge	t_{rp}	$2t_c - 2$	—	$2t_c - 2$	—
CAS to RAS precharge	t_{crp}	$t_c + 1$	—	$t_c + 1$	—
CAS hold from RAS	t_{csh}	$4t_c - 5$	—	$4t_c - 5$	—
RAS to CAS delay	t_{rcd}	$0.5t_c + 4$	—	$0.5t_c + 4$	—
RAS hold from CAS	t_{rsh}	$2.5t_c - 28$	—	$2.5t_c - 28$	—
CAS Precharge	t_{cpn}	$1.5t_c + 7$	—	$1.5t_c + 7$	—
CAS Pulse Width	t_{cas}	$3.5t_c - 23$	—	$3.5t_c - 23$	—
Row Address Setup to RAS	t_{asr}	$0.5t_c - 11$	—	$0.5t_c - 11$	—
Column Address setup to CAS	t_{asc}	1	—	1	—
Row Address hold from RAS	t_{rah}	$0.5t_c$	—	$0.5t_c$	—
Column Address hold from CAS	t_{cah}	t_c	—	t_c	—
Data Access time from OE	t_{oea}	—	$t_c - 10$	—	$t_c - 10$
Data Access time from CAS	t_{cac}	—	$2t_c - 26$	—	$2t_c - 26$
Data Access time from RAS	t_{rac}	—	$2.5t_c - 3$	—	$2.5t_c - 3$
WE Pulse Width	t_{wp}	$t_c - 7$	—	$t_c - 7$	—
Write Data Setup to WE	t_{ds}	0	—	0	—
Write Data Hold from WE	t_{dh}	$t_c - 5$	—	$t_c - 5$	—
Write Data Hold from RAS	t_{dhr}	$2.5t_c - 10$	—	$2.5t_c - 10$	—
WE hold from CAS	t_{wch}	$2t_c - 7$	—	$2t_c - 7$	—
WE hold from RAS	t_{wcr}	$2.5t_c + 2$	—	$2.5t_c + 2$	—
WE lead to RAS	t_{rwl}	$t_c - 11$			
WE lead to CAS	t_{cwl}	$t_c - 6$			

**DRAM Timings Low CPU Bandwidth Mode**

Parameter	Symbol	8 dot mode		9 dot mode	
		Min(ns)	Max(ns)	Min(ns)	Max(ns)
Read/Write Cycle time (read)	t_{rc}	$6t_c$	—	$7t_c$	—
RAS Pulse Width (read)	t_{ras}	$3.5t_c - 1$	—	$4.5t_c - 1$	—
Read/Write Cycle time (write)	t_{rc}	$8t_c$	—	$8t_c$	—
RAS Pulse Width (write)	t_{ras}	$5.5t_c - 1$	—	$5.5t_c - 1$	—
Column Address Hold from RAS	t_{ar}	$2.5t_c + 8$	—	$2.5t_c + 8$	—
RAS precharge	t_{rp}	$2.5t_c - 2$	—	$2.5t_c - 2$	—
CAS to RAS precharge	t_{crp}	$t_c + 1$	—	$t_c + 1$	—
CAS hold from RAS	t_{csh}	$5t_c - 5$	—	$5t_c - 5$	—
RAS to CAS delay	t_{rcd}	$0.5t_c + 7$	—	$0.5t_c + 7$	—
RAS hold from CAS	t_{rsh}	$3t_c - 8$	—	$3t_c - 8$	—
CAS Precharge	t_{cpn}	$1.5t_c + 6$	—	$1.5t_c + 6$	—
CAS Pulse Width	t_{cas}	$4.5t_c - 13$	—	$4.5t_c - 13$	—
Row Address Setup to RAS	t_{asr}	$0.5t_c - 11$	—	$0.5t_c - 11$	—
Column Address setup to CAS	t_{asc}	1	—	1	—
Row Address hold from RAS	t_{rah}	$0.5t_c$	—	$0.5t_c$	—
Column Address hold from CAS	t_{cah}	$2t_c$	—	$2t_c$	—
Data Access time from OE	t_{oea}		$t_c - 6$		$t_c - 6$
Data Access time from CAS	t_{cac}		$2t_c - 10$		$2t_c - 10$
Data Access time from RAS	t_{rac}		$3.5t_c - 6$		$3.5t_c - 6$
WE Pulse Width	t_{wp}	$1.5t_c - 15$	—	$1.5t_c - 15$	—
Write Data Setup to WE	t_{ds}	0	—	0	—
Write Data Hold from WE	t_{dh}	$t_c - 2$	—	$t_c - 2$	—
Write Data Hold from RAS	t_{dhr}	$2.5t_c + 3$	—	$2.5t_c + 3$	—
WE hold from CAS	t_{wch}	$3.5t_c - 14$	—	$3.5t_c - 14$	—
WE hold from RAS	t_{wcr}	$4t_c - 4$	—	$4t_c - 4$	—
WE lead to RAS	t_{rwl}	$1.5t_c - 3$			
WE lead to CAS	t_{owl}	$2.5t_c - 8$			



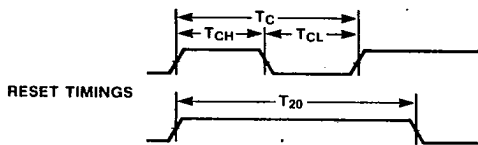
Compatibility with DRAMs

RAS access time	Maximum CLKIN frequency for	
	High CPU Bandwidth Mode	Low CPU Bandwidth Mode
150ns	16.5MHz	20MHz
120ns	20MHz	27MHz
100ns	21.5MHz	30MHz

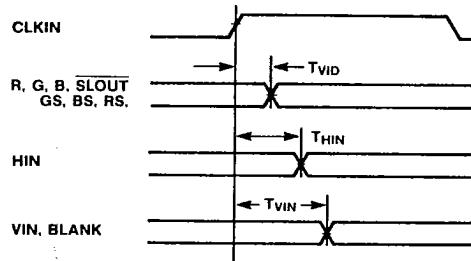
DRAM refresh Interval (ms) = $43000 / (V_r \cdot V_l)$
 V_r = Vertical Refresh Rate
 V_l = Total Number of lines/frame (including retrace)

82C441 Timing Diagrams

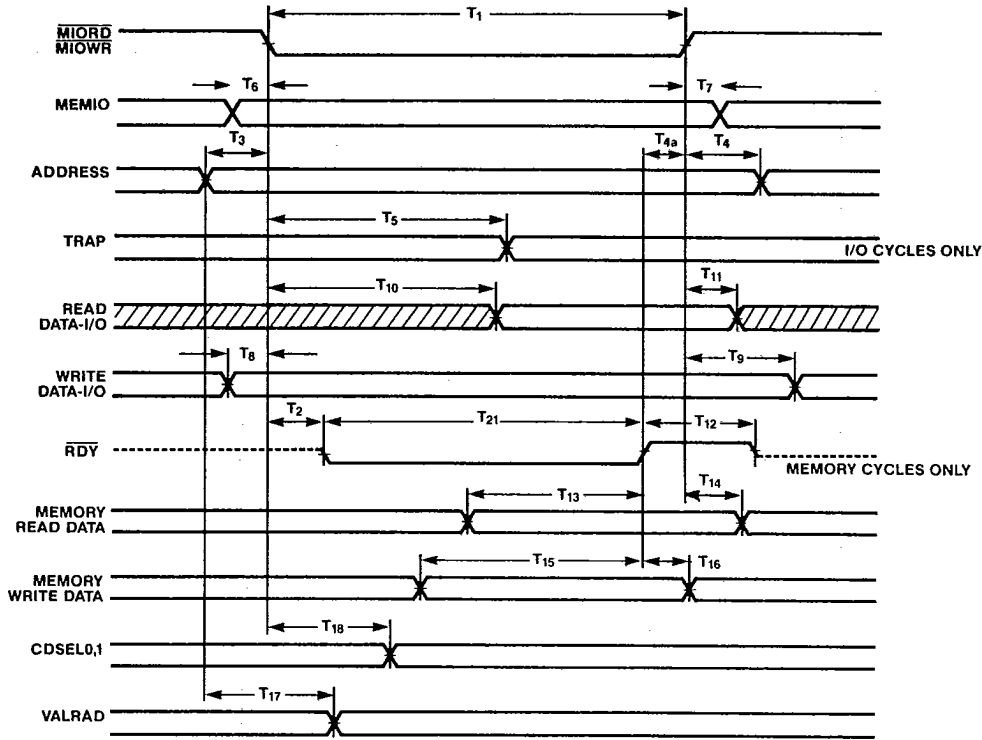
CLKIN TIMINGS



VIDEO TIMINGS



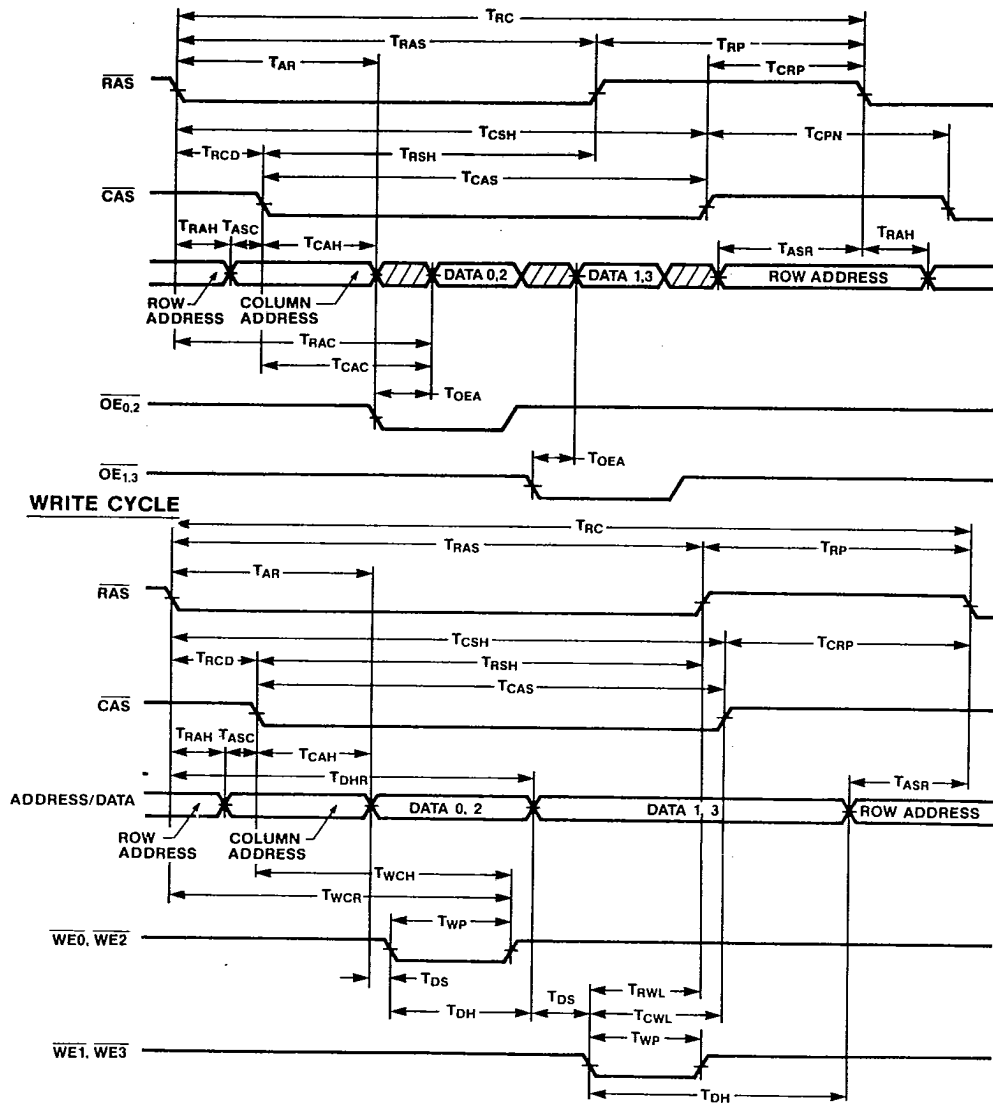
I/O BUS TIMINGS

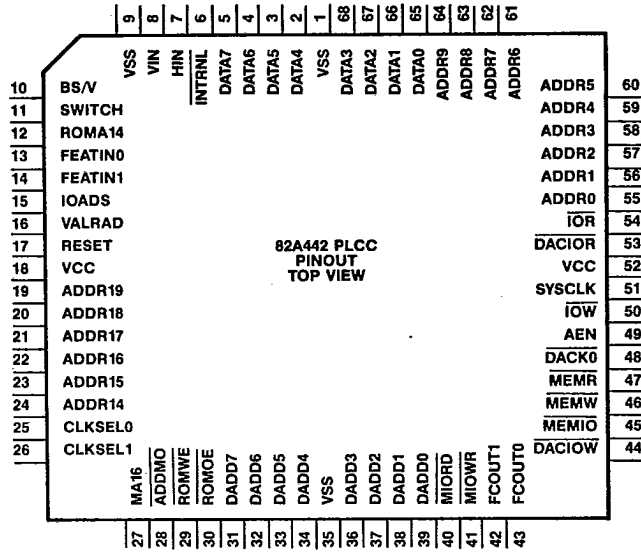




READ CYCLE

DRAM TIMINGS





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82A442 Pin Description

Pin No.	Pin Type	Symbol	Description
55	I	ADDR0	SYSTEM ADDRESS bits 0-9 and 14-19. These bits are used for addressing the display memory and I/O operations. ADDR0-ADDR9 are I/O and memory addresses. ADDR14-ADDR19 are memory addresses only.
56	I	ADDR1	
57	I	ADDR2	
58	I	ADDR3	
59	I	ADDR4	
60	I	ADDR5	
61	I	ADDR6	
62	I	ADDR7	
63	I	ADDR8	
64	I	ADDR9	
24	I	ADDR14	SYSTEM DATA BUS bits 0-7. These bits are used to transfer data to and from the CPU data bus.
23	I	ADDR15	
22	I	ADDR16	
21	I	ADDR17	
20	I	ADDR18	
19	I	ADDR19	
65	I/O	DATA0	
66	I/O	DATA1	
67	I/O	DATA2	
68	I/O	DATA3	
2	I/O	DATA4	
3	I/O	DATA5	
4	I/O	DATA6	
5	I/O	DATA7	
47	I	MEMR	MEMORY READ. MEMR is an active low input from the system bus. It is used by the CPU to read display memory and the VGA BIOS ROM in conjunction with the 82C441.
46	I	MEMW	MEMORY WRITE. MEMW is an active low input from the system bus. It is used to write into the display memory and the VGA BIOS ROM in conjunction with the 82C441.
54	I	IOR	I/O READ. IOR is an active low signal from the system bus. It is used to read the 82C441 and 82A442 registers.
50	I	IOW	I/O WRITE. IOW is an active low signal from the system bus. It is used to write to the 82C441 and 82A442 registers.
48	I	DACK0	DMA ACKNOWLEDGE. DACK0 is an active low input from the system bus used to acknowledge DMA requests. It disables all memory read and memory write operations (MEMR and MEMW) to the 82C441 and 82A442.
49	I	AEN	ADDRESS ENABLE. AEN is an input from the system bus used to disable devices from the I/O channel to allow DMA transfers to take place.

82A442 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
17	I	RESET	RESET is an active high input from the system bus used to reset the Miscellaneous Output Register (I/O address 3C2h), the Feature Control Register (I/O address 3BAh/3DAh) and the Emulation Mode Register (I/O address 3B5h/3D5h).
51	I	SYSCLK	SYSTEM CLOCK. SYSCLK is the I/O bus clock and is used to synchronize IOW.
53	O	DACIOR	DAC I/O READ. DACIOR is an active low signal for reading the color palette/DAC - G171 (or compatible). This signal is asserted low for I/O reads at address 3c6h, 3c8h and 3c9h.
44	O	DACIOW	DAC I/O WRITE. DACIOW is an active low signal for writing to the color palette/DAC - G171 (or compatible). This signal is asserted low for I/O writes at 3c6h, 3c7h, 3c8h and 3c9h.
12	O	ROMA14	ROM A14 ADDRESS. ROMA14 is used to configure 27256 EPROM in paged mode with two 16Kbytes pages. This pin should be connected to A14 pin of the 27256 if the 27256 is to be configured in paged mode. This pin reflects the state of the data bit D0 when any address in the range C0000-C3fff is written. The page number is written on the data bit D0.
13	I	FEATIN0	FEATURE CODE 0 and FEATURE CODE 1 are inputs from the feature connector (pins 19 and 17, respectively) and can be read in the VGA mode as bits 5 and 6 in the Input Status Register 0 (I/O address 3C2h).
14	I	FEATIN1	
43	O	FCOUT0	FEATURE CONTROL 0, FEATURE CONTROL 1. FCOUT0 and FCOUT1 are bits 0 and 1 of the Feature Control Register (I/O address 3BAh/3DAh). FCOUT0 and FCOUT1 go to pins 20 and 21 of the Feature Connector.
42	O	FCOUT1	
11	I	SWITCH	SWITCH is a multiplexed input from a 4-position external configuration DIP-switch. In the VGA mode, the state of this input can be read as the switch sense bit (bit 4 of the Input Status Register 0 - I/O address 3C2h). CLKSEL0 and CLKSEL1 pins (bits 2 and 3 of the Miscellaneous Output Register - I/O address 3C2h) determines which switch is read.
7	I	HIN	HORIZONTAL RETRACE INPUT. HIN is an input from the 82C441. This input is used in Hercules mode to generate bit 0 of the Hercules Status Register (I/O address 3BAh).
10	I	BS/V	SECONDARY BLUE/MONOCHROME VIDEO. BS/V input on the 82A442 is normally the BS/V output from the 82C441. This input is used to generate bit 3 of the CRT Status Register in Hercules mode (I/O address 3BAh).

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82A442 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
39	I/O	DADD0	Local data bus for memory or I/O data between the 82C441, 82A442 and the BIOS ROM.
38	I/O	DADD1	
37	I/O	DADD2	
36	I/O	DADD3	
34	I/O	DADD4	
33	I/O	DADD5	
32	I/O	DADD6	
31	I/O	DADD7	
29	O	ROMWE	BIOS ROM WRITE ENABLE. ROMWE is active low for memory writes at address C0000h-C3FFFh. This output can be used to select the active page in Page Select ROMs (27513).
30	O	ROMOE	BIOS ROM OUTPUT ENABLE. ROMOE is active low for memory reads at address C0000h-C3FFFh.
27	O	MA16	Buffered system address bus bit A16.
28	O	ADDM0	Address Decode. Decoded output for three upper system address bus bits to address the display memory at locations AXXXX and BXXXX. This output is low when A19-A17 = 101.
40	O	MIORD	MEMORY-I/O READ. MIORD is active low for memory or I/O read operations. MIORD is active whenever MEMR or IOR is active.
41	O	MIOWR	MEMORY-I/O WRITE. MIOWR is active low for all memory or I/O write operations. MIOWR is active whenever MEMW or IOW is active.
45	O	MEMIO	MEMORY-I/O. MEMIO is a control signal, low for memory (MEMR or MEMW), high for I/O (IOR or IOW).
25	O	CLKSEL0	CLOCK SELECT 0 AND 1. CLKSEL0 and CLKSEL1 are bits 2 and 3 or the Miscellaneous Output Register (I/O address 3C2h). These bits are used as select inputs into an external multiplexer to select the configuration switch bits and the clock source.
26	O	CLKSEL1	
15	I	IOADS	I/O ADDRESS. IOADS selects the I/O address to the CRT Controller. 0 = 2XXh, 1 = 3XXh.
16	I	VALRAD	VALID READ ADDRESS. VALRAD, generated by the 82C441, allows the 82A442 to drive the system data bus during a memory read cycle (MEMR).
6	O	INTERNL	INTERNAL SELECT. INTERNL is bit 4 of the Miscellaneous Output Register (I/O address 3C2h). It is an active low signal which enables the 82C441 outputs (R, G, B, RS, GS/I, BS/V, HIN, VIN) through an external buffer to the monitor. It is also an output to the feature connector (pin 27).

82A442 Functional Description

The 82A442 integrates the bus drivers, decode logic and other external logic that is required to implement a complete VGA/EGA/CGA/Hercules compatible display subsystem around the 82C441.

The functionality of the 82A442 can be classified as follows:

- a) Decodes memory addresses and control signals.
- b) Serves as a data transceiver between the I/O bus and the 82C441, display memory and VGA BIOS.
- c) Provides temporary storage locations.
- d) Feature Connector interface logic.
- e) Includes parts of some registers on the VGA/CGA/Hercules display subsystems.
- f) Includes complete interface for Inmos G171 color palette/DAC (or compatible).

Memory Address and Control Decode

The 82A442 generates a memory address select signal (ADDM0) for the 82C441. This signal is active low for all memory accesses in the address space A0000h-BFFFFh. The 82A442 also generates Output Enable and Write Enable signals for the BIOS ROM in the address range C0000h-C3FFFh. The ROMOE signal is low for all read accesses to this address space. The ROMWE signal is low for all write accesses to this address space. The ROMWE signal allows the use of page select ROMs like 27513 on the VGA board.

82A442 also includes logic to use a 27256 EPROM in a paged configuration of two pages of 16Kbytes each. Both pages occupy the same address space 0C000h to 0C3FFFh. To allow this 82A442 provides an output signal called ROMA14. This pin should be connected to A14 pin of the 27256 if the EPROM is to be configured in the paged mode (ROMWE should not be used in this case). To switch the active page, the CPU needs to write to any address in the 0C000h-0C3FFFh range.

The 82C441 uses the same control pins (MIORD & MIOWR) for memory and I/O accesses. The 82A442 generates MIORD,

MIOWR and MEMIO signals from the I/O bus control signals.

Data Transceiver Function

The 82A442 also serves as a bidirectional transceiver for data transfer between the CPU (I/O bus) and the display memory, BIOS ROM and 82C441. When the CPU needs to write to the display subsystem, the 82A442 passes the data through to the local data bus in the display subsystem. When the CPU reads from the display subsystem, the 82A442 handles the data transfer in two ways:

- a) If the data is to come from a register (or register bit) that exists in the 82A442, the 82A442 drives those specific bits onto the I/O bus data bus.
- b) For all other read cycles (memory, other register and register bits), the 82A442 transfers the data from the local data bus through to the I/O bus. In this case, the local data bus is driven by the BIOS ROM or the 82C441 or the palette (G171).

Temporary Storage Registers

There are five byte wide temporary storage read-write registers in the 82A442. These registers are located at offset 0FAh-0FEh in the CRT Controller data register space. These registers can be accessed by first writing 0FAh/0FBh/0FCh/0FDh/0FEh in the CRTC Address Register (I/O address 3B4h/3D4h) and then accessing the CRTC Data Register (I/O address 3B5h/3D5h). These registers can be used as working registers.

Feature Connector Interface Logic

The VGA/EGA has the facility to interface to an external video system. This interface is through the Feature Connector. The external video system, can take the Sync signals and video data stream from the 82C441. It can also accept a composite signal through an external port. This external video system, can then either drive a composite video signal or also drive a standard RGB monitor through the VGA. The Feature Connector interface

logic consists of the Feature Control outputs, Feature Code inputs and a control signal to select between internal and external video source.

The CPU can pass control and status information to the external video system through the Feature Control Register. Feature Control Bits 0 and 1 from this register are output on 82A442 output pins FCOU0 and FCOU1 respectively. These pins are usually connected to the Feature Connector.

The Feature Connector can also pass information to the CPU. This is done through two pins FEATIN0 and FEATIN1 on the 82A442. The CPU can read the state of these two pins through Input Status Register 0 at I/O address 3C2h.

Select Video Source

The Video and Sync outputs to the monitor can come from two sources. The 82C441 could drive the monitor or the Feature Connector SharpScan could drive the monitor. The internal video stream or the Feature Connector SharpScan video stream is selected through the Disable Internal Video bit in the Miscellaneous Output Register at I/O address 3C2h. This bit controls the state of the INTERNL output pin on the 82A442. The INTERNL output is typically used to enable a tri-state buffer that isolates the monitor from the 82C441. If the feature connector is to drive the monitor, then the Disable Internal Video bit must be programmed to 1.

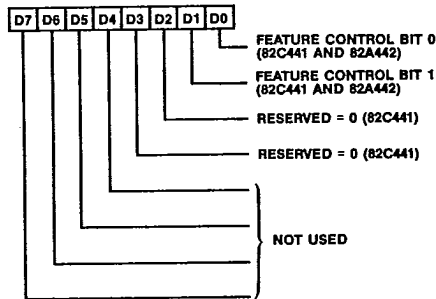
82A442 Registers

There are several registers (or parts of registers) in the 82A442. These are:

Register	Address
Bits D0, D1 of Feature Control Register	3BAh/3DAh
Bits D0, D1, D2 of Emulation Mode Register (Pointer = FFh)	3B5h/3D5h
Bits D0, D2, D3, D4 of Miscellaneous Output Register	3C2h
Bits D4, D5, D6 of Input Status Register 0	3C2h
Bits D0 and D3 of Input Status Register 1	3BA/3DAh
Bits D1, D2, D3 of CGA Status Register	3DAh
Bits D0, D3, D7 of Hercules Status Register	3BAh
Temporary Storage Registers 0-4 (Pointer = FAh-FEh)	3B5h/3D5h
DAC State Register	3C7h

FEATURE CONTROL REGISTER

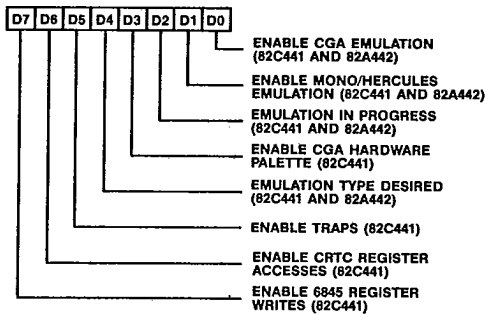
Write Only Register
I/O Address: 3BAh/3DAh



The Feature Control Register exists in both the 82C441 and the 82A442. In the 82A442 this is a write only register and only bits 0 and 1 are implemented. These bits are also present in the 82C441. When this register is read, the 82C441 drives the local data bus and the 82A442 transfers the contents of the local data bus to the CPU. Feature Control Bits 0 and 1 from this register are output on output pins FCOU0 and FCOU1 respectively. These bits can be used to transfer status information to the Feature Connector. On reset, bits D0 and D1 of this register default to 0.

EMULATION MODE REGISTER (CRFF)

Write Only Register
I/O Address: 3B5h/3D5h;
Address Pointer: FFh



The Emulation Mode Register exists in both the 82C441 and the 82A442. This register is located at offset 0FFh in the CRT Controller register space. In the 82A442 this is a write only register and only bits 0,1 and 2 are implemented. These bits are also present in the 82C441. When this register is read, the 82C441 drives the local data bus and the 82A442 transfers the contents of the local data bus to the CPU.

D0 Enable CGA Emulation: This bit determines if CGA Emulation is to be enabled (=1) or disabled (=0). On reset, this bit defaults to 0.

D1 Enable Mono/Hercules Emulation: This bit determines if Monochrome/Hercules Emulation is to be enabled (=1) or disabled (=0). On reset, this bit defaults to 0.

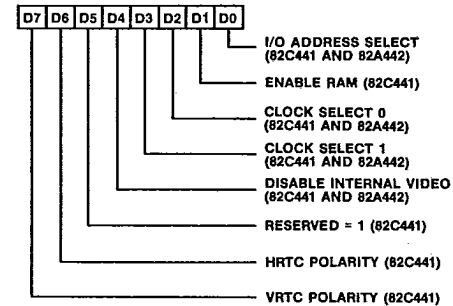
D2 Emulation in Progress: This bit determines if the 82C441/82A442 is currently in the CGA or Hercules emulation mode (=1) or in the normal VGA mode (=0). This bit must be set while CGA/MDA/ Hercules emulation is in progress. On reset, this bit defaults to 0.

D4 Emulation Type: This bit is set when software desires an automatic emulation mode switch. D4 = 0 and CGA emulation enabled means that the software desires CGA emulation. D4 = 1 and Hercules emulation enabled means that the software desires Hercules emulation. On reset, this bit is undefined.

The format for the Input Status Register 1 (CGA/Hercules Status Register) is determined according to these bits.

MISCELLANEOUS OUTPUT REGISTER

Write Only Register
I/O Address: 3C2h



The Miscellaneous output Register exists in both the 82C441 and the 82A442. This register is located at I/O address 3C2h. In the 82A442, this is a write only register and only bits 0, 2, 3, and 4 are implemented. These bits are also present in the 82C441. When this register is read, the 82C441 drives the local data bus and the 82A442 transfers the contents of the local data bus to the CPU.

D0 I/O Address Select. This bit maps the CRT Controller address and data registers into the 3Bxh/3Dxh address space. This bit defaults to 0 on reset and is present in both the 82C441 and 82A442. Setting this bit to 0 or 1 maps the registers as follows:

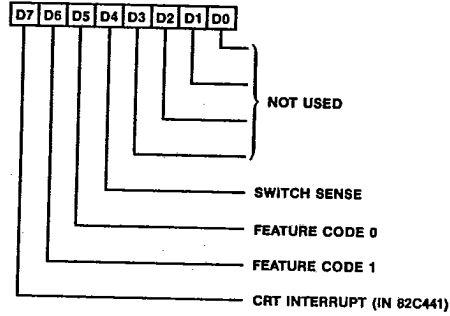
Register Name	I/O Address for	
	D0 = 0	D0 = 1
CRTC Address Register	3B4h	3D4h
CRTC Data Register	3B5h	3D5h
Feature Control Register	3BAh	3DAh
Input Status Register 1	3BAh	3DAh

D2-D3 D2-D3 bits are output on the CLKSEL0 and CLKSEL1 pins on the 82A442. Typically these are used to externally select the clock source for the 82C441. On reset, these bits default to 0.

D4 Disable Internal Video. This bit is output on the INTERNL pin on the 82A442. The INTERNL output is used to select the 82C441 video data stream or an external video data stream to the monitor. On reset, this bit defaults to 0.

INPUT STATUS REGISTER 0

Read Only Register
I/O Address: 3C2h



The Input Status Register 0 exists in both the 82C441 and the 82A442. This register is located at I/O address 3C2h. In the 82A442, this is a read-only register and only bits 4, 5, and 7 are implemented. When this register is read in the VGA mode, the 82C441 drives the local data bus bit 7 and the 82A442 drives the other bits. In the CGA and Hercules modes, this register returns undefined values when read.

Switch Sense (D4)

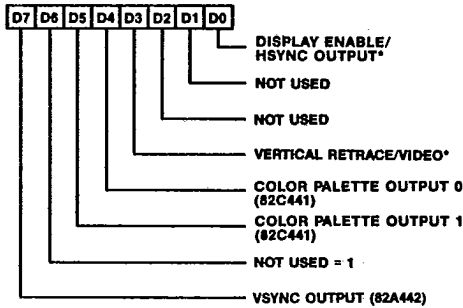
This bit returns the current status of the 82A442 input pin 'SWITCH' to the CPU. The CPU scans the state of the DIP switches on the VGA board through this bit.

Feature Code 0 and 1 (D5-D6)

These two bits return the current status of the 82A442 input pins FEATIN0 and FEATIN1 respectively. These bits are used to read the status information from the VGA Board Feature Connector.

**INPUT STATUS REGISTER 1
(CGA/HERCULES STATUS REGISTER)**

Read Only Register
I/O Address: 3BAh/3DAh



*(82C441 AND 82A442)

The Input Status Register 1 exists in both the 82C441 and the 82A442. This register changes address and format in the VGA, CGA and Hercules modes. In VGA mode this register is located at I/O address 3BAh/3DAh. In CGA mode this register is located at I/O address 3DAh. In Hercules mode this register is located at I/O address 3BAh. When this register is read, the 82C441 and 82A442 drive different bits in the three modes as follows:

- VGA mode 82C441 drives bits 0,3,4,5 bits
 1,2,6 and 7 are high
- CGA mode 82C441 drives bit 0 82A442
 drives bit 3 bits 1,2,4,5,6 and 7
 are high
- Hercules 82A442 drives bits 0 and 3 bits
mode 1,2,4,5,6 and 7 are high

Display Enable/HSYNC Output (D0)

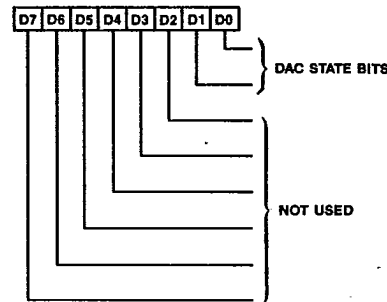
In VGA and CGA modes, D0 is an active low Display Enable signal generated by the 82C441. A logical 0 indicates the active display interval. This bit is returned high during the horizontal and vertical retrace interval. In Hercules emulation mode this bit is driven by the 82A442 and it indicates the current level of the 82A442 HIN input.

Vertical Retrace/Video (D3)

In VGA mode, D3 is an active high vertical retrace signal, which is functionally the same as the active high Vertical Sync output from the 82C441 (the polarity of this bit is always positive). In CGA emulation mode, D3 is driven by the 82A442 and is the complement of the VIN input on the 82A442. In Hercules emulation mode D3 is driven by the 82A442 and it indicates the current state of the BS/V input on the 82A442.

DAC STATE REGISTER

Read Only Register
I/O Address: 3C7h



Bits D0 and D1 are '0' if the Palette DAC is in the "Write" state (last Write to the palette was at 3C8h). Bits D0 and D1 are '1' if the Palette DAC is in "Read" state (last Write to the palette was at 37h).

CHIPS

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Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25	85	C
Storage Temperature	T_{STG}	-40	125	C

82A442 Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A442 DC Characteristics

Parameter	Symbol	Min	Max	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage $I_{OL1} = 10mA^1$ $I_{OL2} = 24mA^2$	V_{OL}		0.5	V
Output High Voltage $I_{OH} = 3.3mA$	V_{OH}	2.4		V
Input Leakage Current	I_{IL}	-200	+200	μA
Power Supply Current	I_{CC}		250	mA
Output High Impedence Leakage $0.45 < V_{PIN} < V_{CC}$	I_{OZ}	-300	+120	μA

NOTES:

- $I_{OL} = 10mA$ on all pins except DATA0-7
- $I_{OL} = 24mA$ on DATA0-7



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82A442 AC Characteristics(T_A = 0°C-70°C, V_{CC} = 5V ±5%)**Timings**

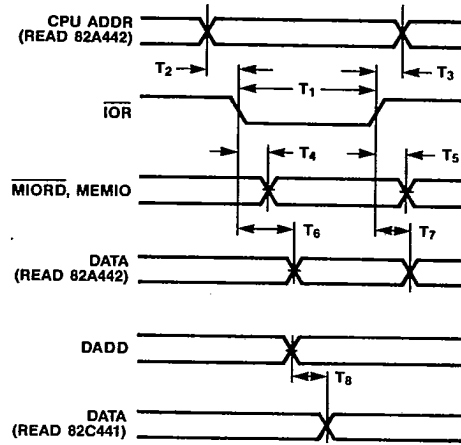
Parameter	Symbol	Min(ns)	Max(ns)
System Clock Period	T _C	80	
I _{OR} Pulse Width	T ₁	T _C	
Address setup (82A442 register access)	T ₂	20	
Address hold (82A442 register access)	T ₃	0	
Control active delay	T ₄		25
Control inactive delay	T ₅		23
I/O Read Data delay (82A442 register)	T ₆		45
I/O Read Data hold (82A442 register)	T ₇	10	30
Propagation delay (DATA-DADD, DADD-DATA)	T ₈		25
I _{OW} Setup to System Clock	T ₉ *	10	
I _{OW} Pulse Width (Short Write)	T ₁₀		2T _C
I _{OW} Pulse Width (Long Write)	T ₁₀	2T _C	
M _{IOWR} active delay (I/O write)	T ₁₁ *		31
M _{IOWR} inactive delay (Short I/O write)	T ₁₂ *		28
M _{IOWR} inactive delay (Long I/O write)	T ₁₂		34
I/O Write Data setup (82A442 register)	T ₁₃	10	
I/O Write Data hold (82A442 register)	T ₁₄	20	
Register Output delay (long write)	T ₁₆		45
Register Output delay (short write)	T ₁₆		40
VALRAD setup (display memory access)	T ₂₀	5	
Address setup (ROM access)	T ₂₀	20	
VALRAD hold (display memory access)	T ₂₁	0	
Address hold (ROM access)	T ₂₁	0	
Control active delay (memory access)	T ₂₂		26
Control inactive delay (memory access)	T ₂₃		20
ADD _{M0} delay	T ₂₄		26
MA ₁₆ delay	T ₂₄		20

NOTE:

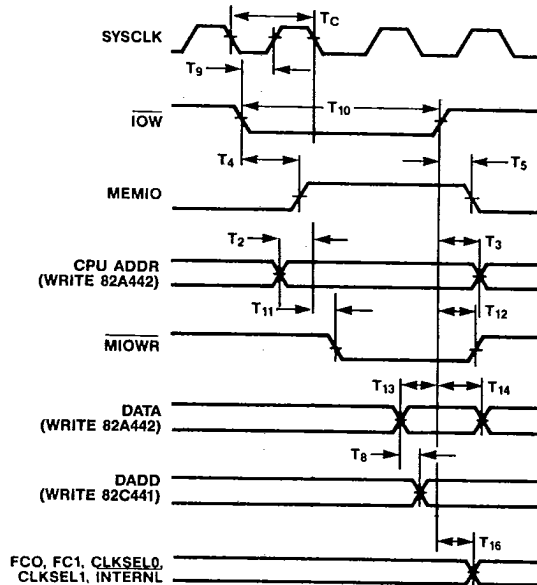
* T₉, T₁₁ and T₁₂ (long write) are specified on both rising and falling edges of SYSCLK. M_{IOWR} stays active for a maximum of 1½ SYSCLKs starting at any of the edges of the SYSCLK.

82A442 Timing Diagrams

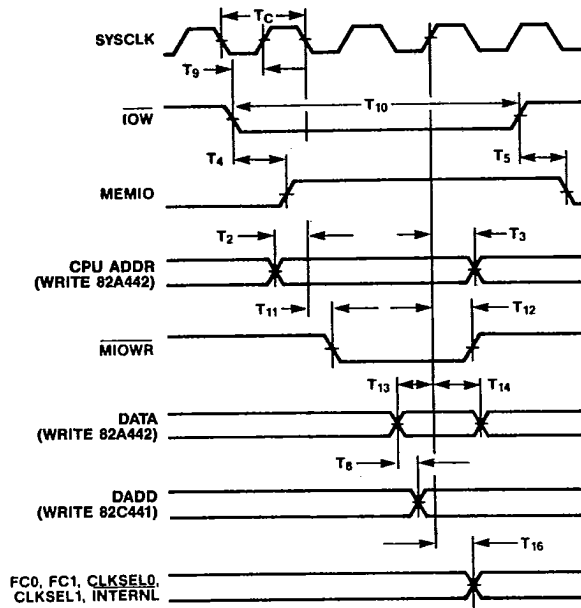
CPU—IO READ ACCESS



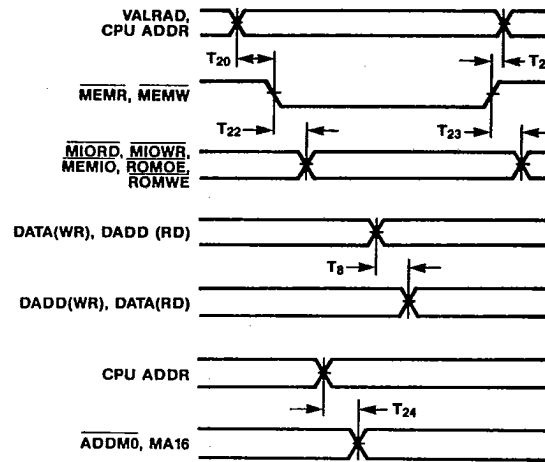
CPU—IO WRITE ACCESS (SHORT WRITE)



CPU—IO WRITE ACCESS (LONG WRITE)



CPU—MEMORY ACCESS



Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L (pF)	R_1 (Ω)	R_L (Ω)	SW_1	SW_2
Propagation Delay Time	Totem pole	t_{PLH}	50	—	1.0K Ω	OFF	ON
	3-state	t_{PHL}					
Propagation Delay Time	Bidirectional						
	Open drain or Open Collector	t_{PLH}	50	0.5K	—	ON	OFF
Disable Time	3-state	t_{PLZ}	5	0.5K	1.0K	ON	OFF
	Bidirectional	t_{PHZ}					
Enable Time	3-state	t_{PZL}	50	0.5K	1.0K	ON	ON
	Bidirectional	t_{PZH}					

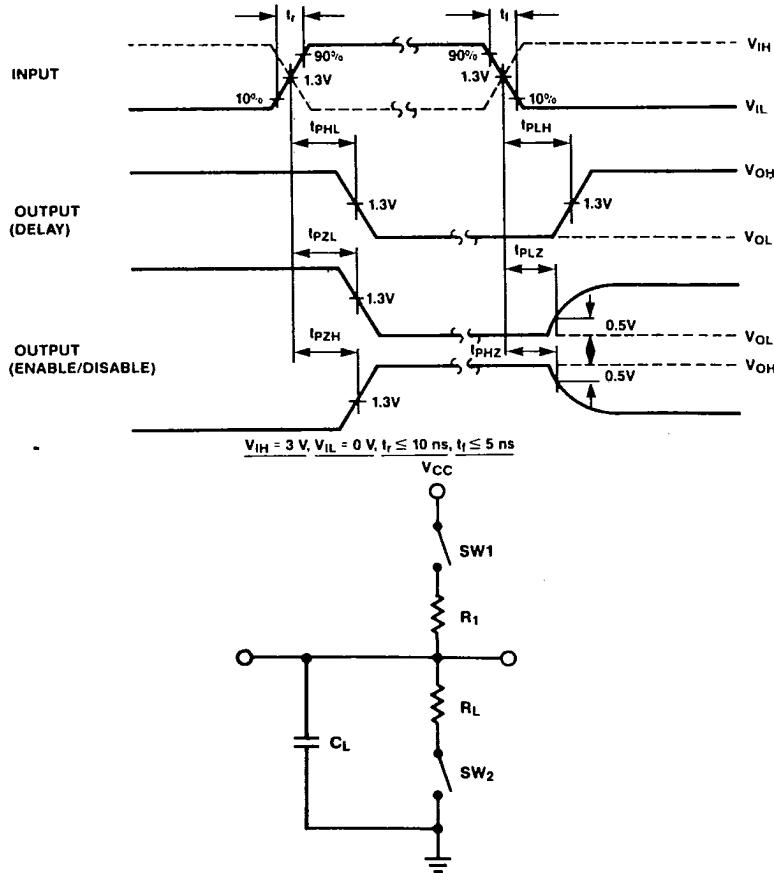
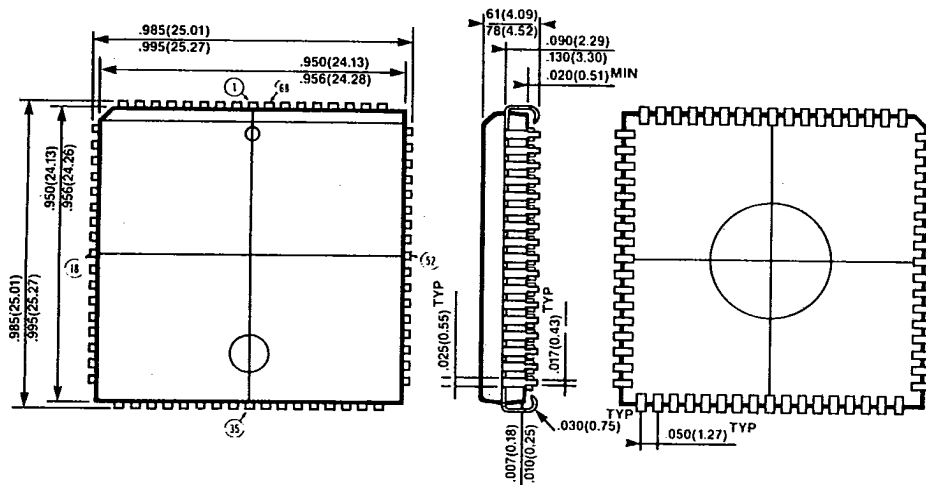
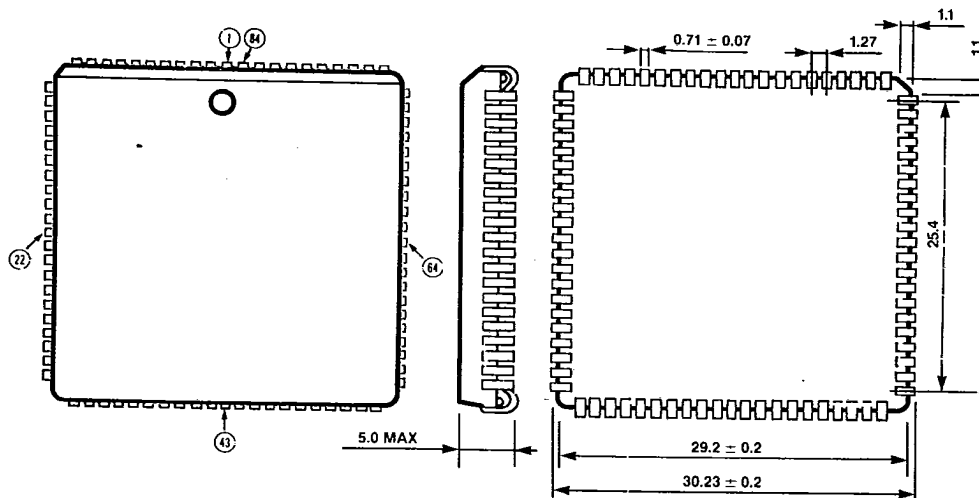


Figure 13. Load Circuit and AC Characteristics Measurement Waveform

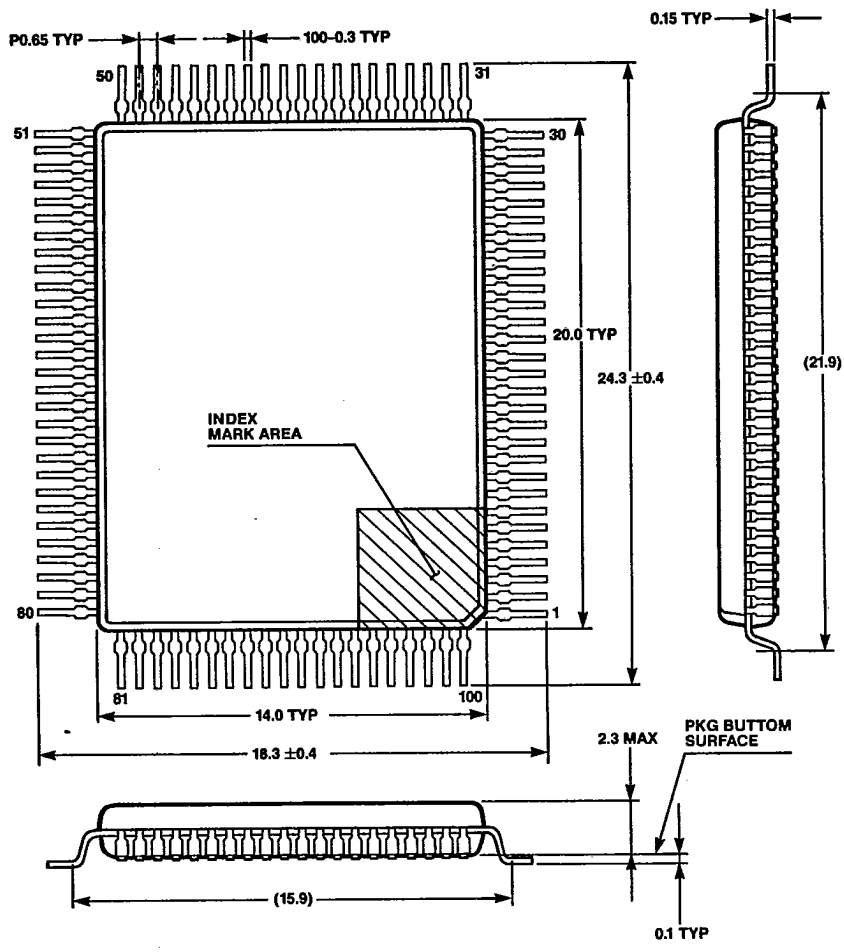
68-PIN PLASTIC LEADED CHIP CARRIER



84-PIN PLASTIC LEADED CHIP CARRIER



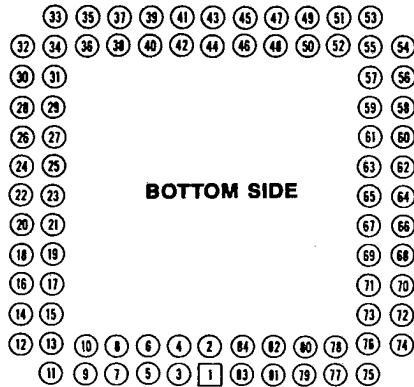
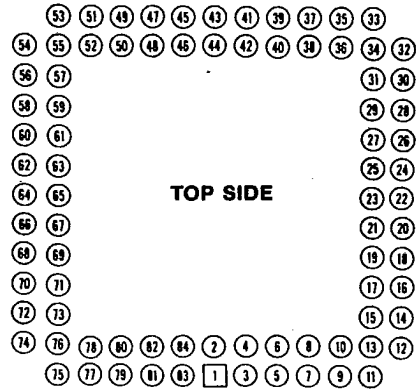
100-PIN PLASTIC FLAT PACKAGE





T-52-33-03

84-PIN PLCC SOCKET



68-PIN PLCC SOCKET

