CIRRUS LOGIC®

CL-GD542X

Preliminary Data Book

True Color VGA Family		
CL-GD5429	–	Memory-Mapped I/O VGA GUI Accelerator with Local Bus
CL-GD5428	–	Enhanced VGA GUI Accelerator with Local Bus
CL-GD5426	–	VGA GUI Accelerator with Local Bus
CL-GD5425	–	True Color VGA Controller with TV Output
CL-GD5424	–	True Color VGA with Local Bus
CL-GD5422	–	True Color VGA
CL-GD5420	–	Super VGA

FEATURES

- **32-bit GUI acceleration (CL-GD5426/'28/'29)**
  - — BitBLT (Bit block transfer) engine
  - — Color expansion for 8- or 16-bit pixels
- **16/32-bit CPU interface**
  - — VESA® VL-Bus™ (up to 50 MHz)
  - — ISA bus (12.5 MHz)
  - — Zero-wait-state write cycles
- **Resolutions up to 1280 × 1024**
  - — 1024 × 768 × 256 colors, non-interlaced
  - — 800 × 600 × 64K colors, non-interlaced
  - — 640 × 480 × 16M colors, non-interlaced
  - — 1280 × 1024 × 256 colors, interlaced
  - — 1024 × 768 × 64K colors, interlaced
- **Programmable dual-clock synthesizer**
  - — Pixel clock programmable up to 86 MHz
  - — Memory clock programmable up to 60 MHz
- **Integrated 24-bit true-color RAMDAC**
- **'Green PC' power-saving features**
  - — VESA® DPMS (Display Power Management Signal)
  - — Internal DAC with programmable power-down mode
  - — Static monitor sync signals
- **Support for multimedia applications**
  - — 3-3-2 RGB DAC modes for video playback (CL-GD5425/'28/'29)
  - — Support of VAFC (VESA® advanced feature connector) baseline for video overlay (CL-GD5425/'29)
- **100% hardware- and BIOS-compatible with IBM® VGA display standards**

(cont.)

OVERVIEW

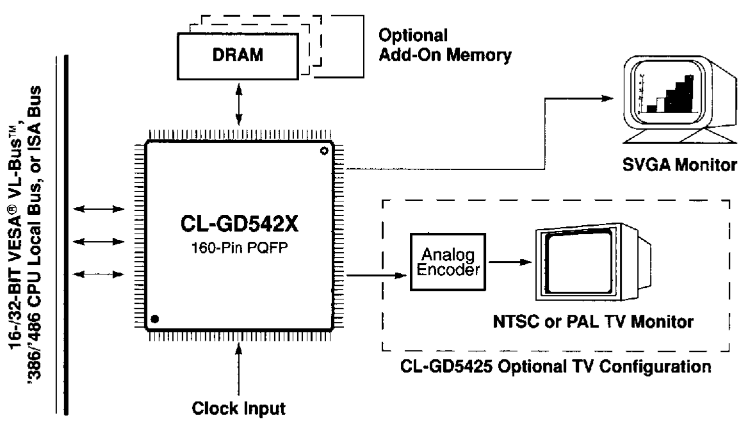
The CL-GD542X family of true-color VGA controllers offers an extensive range of industry-leading features and functionality for IBM®-compatible personal computers.

Ideally suited to highly integrated systems, CL-GD542X devices require no external support other than display memory and a crystal frequency reference. CL-GD542X devices are 100% hardware- and BIOS-compatible with IBM VGA standards, and connect directly to an ISA or local bus, allowing a minimum adapter solution.

Operating at dot clock rates programmable up to 86 MHz, CL-GD542X devices support standard and VESA® high-resolution and extended modes. The internal palette DAC may be configured as an industry-standard RAMDAC to provide a palette of 256K colors, or true-color displays of 32K, 64K, and 16.8 million colors.

(cont.)

System Block Diagram



OVERVIEW (cont.)

The internal dual-frequency synthesizer requires a single crystal or reference for all supported screen resolutions, as well as all standard display memory speeds and formats. The CL-GD542X devices implement all control and data registers according to current VGA standards. They also implement all standard data path and manipulation functions, providing complete hardware compatibility.

In addition, the CL-GD542X devices support extended registers and capabilities to provide functional and performance enhancements beyond standard VGA.

CL-GD542X devices support ISA or 32-bit VESA VL-Bus interfaces in all operations, including I/O and memory operations in planar modes. The write cycles to memory are optimized with zero-wait-state capability. Sixteen-/thirty-two-bit local bus interfacing can be achieved for '386SX, '386DX, and '486 microprocessors as well as VESA VL-Bus. The CL-GD5426/'28/'29 also offer BitBLT operation for GUI acceleration.

The CL-GD542X family also includes many power-saving ('Green PC') features, including an internal DAC with programmable power-down mode, sync signals that can be individually disabled (static levels), and internal clocks programmable to low frequencies for nearly static operation.

Software Support

Software Drivers	Resolution Supported[a]	No. of Colors
Microsoft® Windows® 95 *CL-GD5425*	640 × 480, 800 × 600, 1024 × 768	256
	640 × 480, 800 × 600	32,768
	640 × 480	16.8 million
Microsoft® Intel® DCI *CL-GD5425*	640 × 480, 800 × 600, 102 4 × 768	256
	640 × 480, 800 × 600	65,536
	640 × 480	16.8 million
Microsoft® Windows® v3.X *CL-GD5425*	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16
	640 × 480, 800 × 600,1024 × 768, 1280 × 1024	256
	640 × 480, 800 × 600, 1024 × 768	65,536
	640 × 480	16.8 million
Microsoft® Windows NT™ v1.X	640 × 480, 800 × 600, 1024 × 768	16 and 256
OS/2® v2.0, v2.1	800 × 600, 1024, × 768	16 [b]
	640 × 480, 800 × 600, 1024, × 768	256 [b]
AutoCAD® v11, v12, Autoshade® v2.0, w/ Renderman, 3D Studio™ v1,v2	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16
	640 × 480, 800 × 600,1024 × 768, 1280 × 1024	256
	640 × 480, 800 × 600, 1024 × 768	65,536
	640 × 480	16.8 million
GEM™ v3.X	800 × 600, 1024 × 768	16
Ventura Publisher® v2, v3	800 × 600, 1024 × 768	16
Lotus® 1-2-3® v2.X,	132 × 25, 132 × 43 (text)	16
	800 × 600	16
Lotus® 1-2-3® v3.X	132 × 25, 132 × 43 (text)	16
	800 × 600, 1024 × 768	16
Microsoft® Word v5.X	132 × 25, 132 × 43 (text)	16
	800 × 600, 1024 × 768	16
WordPerfect® v5.0	800 × 600	16
WordPerfect® v5.1	132 × 25, 132 × 43 (text)	16
	800 × 600, 1024 × 768	16
WordStar® v5.5–v7.0	800 × 600, 1024 × 768	16

[a] Not all monitors support all resolutions; 640 × 480 drivers will run on PS/2®,-type monitors. Extended resolutions are dependent upon monitor type and VGA system implementation.

[b] OS/2® v2.0 requires a v2.0 Corrective Service Pack for 256 .

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CL-GD5425 Highlights
True Color VGA Controller with TV Output

FEATURES

- **True color VGA controller with TV output**
  - — Scaling fits full VGA display into TV viewing area while maintaining proper aspect ratio
  - — Flicker-filter reduces interlaced artifacts associated with computer-generated graphic images
- **Glueless interface to popular TV encoders**
- **Multimedia support**
  - — Video overlay of 16-bit RGB, 16-bit YCrCb
  - — 8-bit feature connector
  - — 16-bit VAFC (VESA® advanced feature connector)
  - — GENLOCK support
- **Graphics acceleration features:**
  - — Color expansion reduces host bus traffic
  - — 64 × 64 hardware cursor
  - — Display memory linear addressing
- **Flexible 16-bit host interface**
  - — VESA® VL-Bus™ (up to 50 MHz)
  - — ISA bus
- **Flexible 32-bit display memory interface**
  - — Supports 256K ×4, ×8, ×16 DRAMs
  - — 512-Kbyte or 1-Mbyte memory capacity
- **Integrated 24-bit DAC**
  - — VGA resolution up to 1024 × 768, 256 colors
  - — NTSC resolution up to 640 × 480, 64K colors, scaled with flicker filter
  - — PAL resolution up to 640 × 480, 64K colors with flicker filter

OVERVIEW

The CL-GD5425 integrates a Super VGA controller, dual-frequency synthesizer, true-color palette DAC, and TV processing support into a single device.

A member of the industry-standard CL-GD542X family of true color VGA controllers, the CL-GD5425 is fully backed by software and design support.

The CL-GD5425 provides NTSC/PAL timing for standard VGA display modes, as well as the following extended resolutions:

Extended Resolutions for TV Output

Resolution	No. of Colors	Memory
640 × 480	256	512 Kbyte
640 × 480	64K	1 Mbyte
640 × 400	64K	512 Kbyte

The CL-GD5425 provides integrated scaling, flicker reduction, and a glueless encoder interface that delivers high-quality TV display at the lowest possible cost without the need for additional frame or line stores.

The programmable flicker-reduction function reduces interlaced artifacts inherent in computer-generated images displayed on interlaced TV monitors. The degree of filtering is selectable by the end-user.

The CL-GD5425 is 100% hardware- and BIOS-compatible with VGA standards, and connects directly to the VESA® VL-Bus™ or ISA bus. A single DRAM, two frequency references, and an economical analog encoder are added to make a complete set-top graphics system.

CL-GD542X ADVANTAGES

Unique Features	Benefits
Cost Effectiveness —	
■ Glueless interface to as few as one DRAM, built-in true-color palette DAC and dual-frequency synthesizer	❐ Minimizes chip count and board space; enables a cost-effective solution.
■ Interface to ×4, ×8, ×16 DRAMs	❐ Allows design flexibility for use of appropriate type and amount of memory.
High Performance —	
■ 16-bit VESA® VL-Bus™ and local bus interface	❐ Increases system throughput.
■ Hardware BitBLT for Windows® (CL-GD5425/'26/'28/'29)	❐ Accelerates GUI applications such as Microsoft® Windows® and similar applications.
■ 32-bit-wide DRAM interface	❐ Eliminates display-memory bottleneck.
■ Maximizes fast-page mode access to display-memory DRAMs	❐ Improves CPU performance by accessing maximum bandwidth available from DRAM display memory.
■ Host access to DRAMs through advanced write buffers	❐ Provides faster host access for writes to display memory.
■ 15-, 16-, or 24-bit true-color palette DAC	❐ Provides high- and true-color display for photo-realistic images; 32K, 64K, or 16.8 million colors displayed simultaneously on screen for lifelike images.
Multimedia —	
■ 3-3-2 RGB DAC modes for video playback (CL-GD5425/'28/'29)	❐ Enables high-resolution playback for live video applications.
■ NTSC or PAL output (CL-GD5425)	❐ Allows TV viewing of PC games and applications.
■ Overlay and 'color key', and GENLOCK support	❐ Allows 16-bit per pixel interfacing through the VESA® connector for multimedia applications.
Compatibility —	
■ Compatible with VGA and VESA® standards	❐ Ensures compatibility with installed base of systems and software.
■ Drivers supplied at various resolutions for Windows® 3.1, Windows® 95™, and other key applications	❐ Provides a 'ready-to-go' solution that minimizes the need for additional driver development.
■ Connects directly to multifrequency analog monitors	❐ Drives all PC-industry-standard, high-resolution monitors to ensure compatibility.

BIOS SUPPORT

- **Fully IBM® VGA-compatible BIOS**
- **Relocatable, 32 Kbytes with VESA® VL-Bus™ local bus support**
- **VBE (VESA® BIOS extensions) support in ROM**
- **Support for DPMS (display power management signaling) in ROM**

UTILITIES

- **Graphics and video diagnostics test**
- **Windows® and DOS utilities**
- **Video mode configuration utility — CLMODE**
- **Set resolution in Windows® utility — WINMODE**
- **Configurable system integration for OEMs — OEMSI**

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CL-GD542X Family Features

Features	'GD5420	'GD5422	'GD5424	'GD5425	'GD5426	'GD5428	'GD5429
Performance							
VESA® VL-Bus™ and Direct 80386 or 80486 CPU interface			✓	✓	✓	✓	✓
BitBLT engine					✓	Enhanced	MM I/O
Zero-wait-state operation	✓	✓	✓	✓	✓	✓	✓
Maximum display memory	1 Mbyte	1 Mbyte	1 Mbyte	1 Mbyte	2 Mbytes	2 Mbytes	2 Mbytes
Display memory interface	16-bit	32-bit	32-bit	32-bit	32-bit	32-bit	32-bit
Hardware cursor (in pixels)	up to 32×32	up to 64×64	up to 64×64	up to 64×64	up to 64×64	up to 64×64	up to 64×64
Maximum dot clock frequency	75 MHz	80 MHz	80 MHz	80 MHz	80 MHz	80 MHz	86 MHz
Maximum MCLK frequency	50 MHz	50 MHz	50 MHz	60 MHz	50 MHz	50 MHz	60 MHz
High integration							
Integrated palette DAC and dual-frequency synthesizer	✓	✓	✓	✓	✓	✓	✓
Motherboard VGA solution with only two ICs	✓	✓	✓	Plus Encoder	✓	✓	✓
Built-in port for VESA® feature connector	✓	✓	✓	✓	✓	✓	✓
Built-in ISA (up to 12.5 MHz) bus support	✓	✓	✓	✓	✓	✓	✓
Built-in TV output support				✓			
Flexibility							
Support for x4-, x8-, and x16-bit-wide DRAMs	✓	✓	✓	✓	✓	✓	✓
8- or 16-bit host bus I/O and memory interface	✓	✓	✓	✓	✓	✓	✓
8-bit gray and 3-3-2 RGB DAC modes				✓		✓	✓
CCIR 601 YCrCb mode				✓			
General							
100% hardware- and BIOS-compatible with IBM® VGA display standards	✓	✓	✓	✓	✓	✓	✓
'Green PC' compliant	✓	✓	✓	✓	✓	✓	✓
132-column text mode support	✓	✓	✓	✓	✓	✓	✓
46E8 or 3C3 sleep mechanism		✓	✓	✓	✓	✓	✓
Video overlay and 'color key' support		✓	✓	✓	✓	✓	✓
VESA® VAFC™ base support (for video overlay)				✓			✓
Low-power CMOS, 160-pin package	✓	✓	✓	✓	✓	✓	✓
Screen resolution and colors							
640×480	up to 256	up to 16M	up to 16M	up to 16M	up to 16M	up to 16M	up to 16M
800×600	up to 256	up to 64K	up to 64K	up to 64K	up to 64K	up to 64K	up to 64K
1024×768 (interlaced)	up to 256	up to 256	up to 256	up to 256	up to 256	up to 64K	up to 64K
1024×768 (non-interlaced)	up to 256	up to 256	up to 256	up to 256	up to 256	up to 256	up to 256
1280×1024 (interlaced)		up to 16	up to 16	up to 16	up to 256	up to 256	up to 256

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Revision History

The following are the differences between the July 1994 and May 1995 versions of this data book:

- The CL-GD5425 device and all pertinent information regarding it has been added.
- The BIOS timing diagrams have been updated.

CONVENTIONS

This section lists conventions used in this data book. 'CL-GD542X' represents CL-GD5420, CL-GD5422, CL-GD5424, CL-GD5425, CL-GD5426, CL-GD5428, and CL-GD5429, the six members of the True Color VGA controller family.

Abbreviations

Units of measure	Symbol
degree Celsius	°C
hertz (cycle per second)	Hz
kilobyte (1,024 bytes)	Kbyte
kilohertz	kHz
kilohm	kΩ
megabyte (1,048,576 bytes)	Mbyte
megahertz (1,000 kilohertz)	MHz
microfarad	µF
microsecond (1,000 nanoseconds)	µs
milliampere	mA
millisecond (1,000 microseconds)	ms
nanosecond	ns
picovolt	pV

The use of 'tbd' indicates values that are 'to be determined', 'n/a' designates 'not available', and 'n/c' indicates a pin that is a 'no connect'.

Acronyms

The following table lists acronyms used in this data book.

Acronym	Definition
AC	alternating current
BIOS	basic input/output system
BitBLT	bit boundary block transfer
CAD	computer-aided design
CAS	column address strobe
CLUT	color lookup table
CMOS	complementary metal-oxide semiconductor
CRT	cathode ray tube
DAC	digital-to-analog converter
DC	direct current

Acronym	Definition *(cont.)*
DPMS	display power management signaling
DRAM	dynamic random-access memory
EEPROM	electrically erasable/programmable read-only memory
EISA	extended industry standard architecture
EPROM	electrically programmable read-only memory
FIFO	first in/first out
HI-Z	high-impedance
HSYNC/VSYNC	horizontal/vertical synchronization
ISA	industry standard architecture
LSB	least-significant bit
LUT	lookup table
MD	memory data
MSB	most-significant bit
PCI	peripheral component interconnect
PQFP	plastic quad-flat pack
RAM	random-access memory
RAS	row address strobe
RGB	red, green, blue
ROPs	raster operations
R/W	read/write
SC	serial clock
TSR	terminate and stay resident
TTL	transistor-transistor logic
VAFC	VESA® advance feature connector
VESA®	Video Electronics Standards Association
VGA	video graphics array
VRAM	video random-access memory

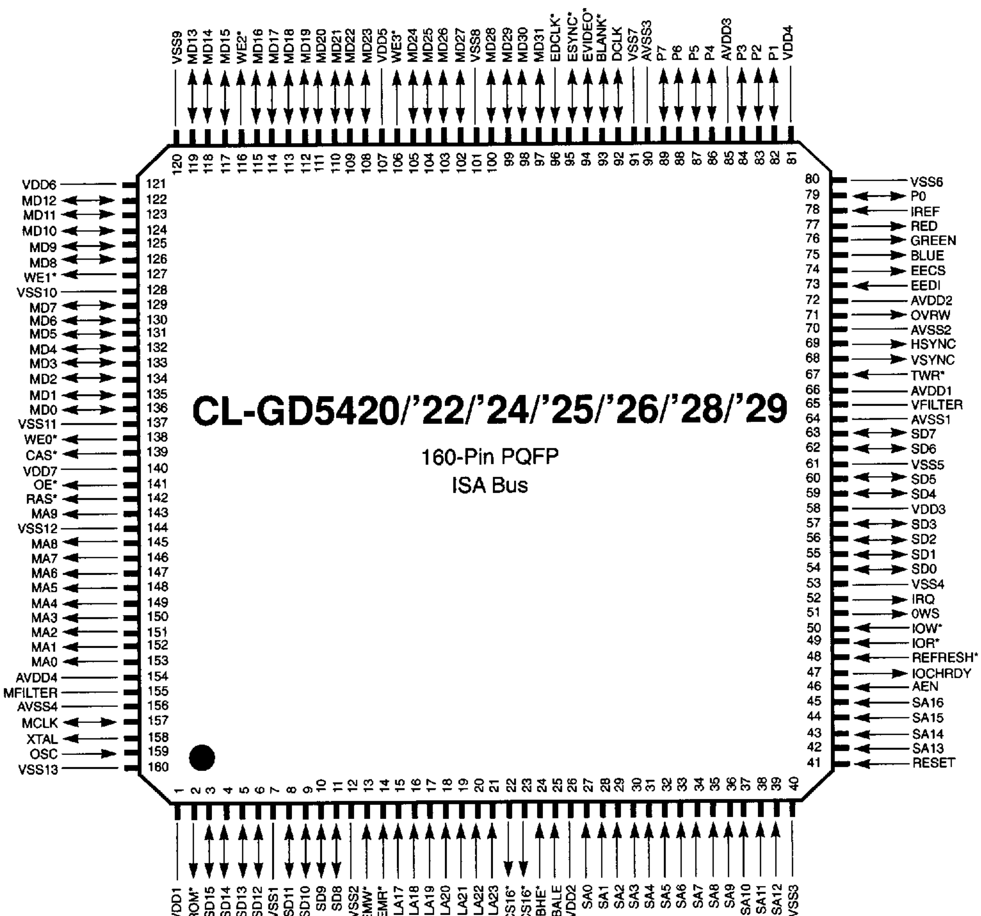
Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase and a lowercase 'h' is appended to them (for example, '14h', '3A7h', and 'C000h' are hexadecimal numbers). Numbers not indicated by an 'h' are decimal.

1. PIN INFORMATION

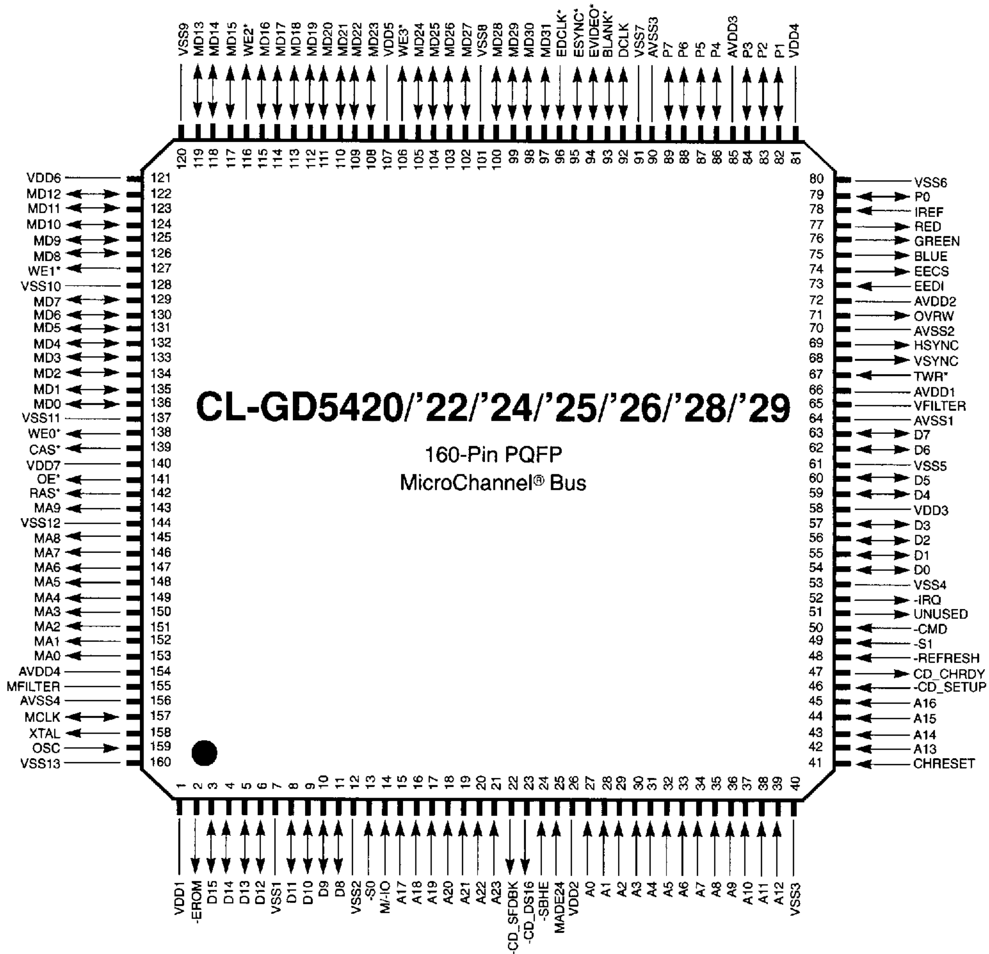
The CL-GD542X family of VGA controllers is available in a 160-pin quad flat pack device configuration, shown below.

1.1 Pin Diagram (ISA Bus)



NOTE: WE1*, WE0*, MD[15:0], and OVRW are reserved on CL-GD5420.

1.2 Pin Diagram (MicroChannel® Bus)



NOTES:

1) WE1*, WE0*, MD[15:0], and OVRW are reserved on CL-GD5420.
2) '-' indicates active-low on the MicroChannel bus.

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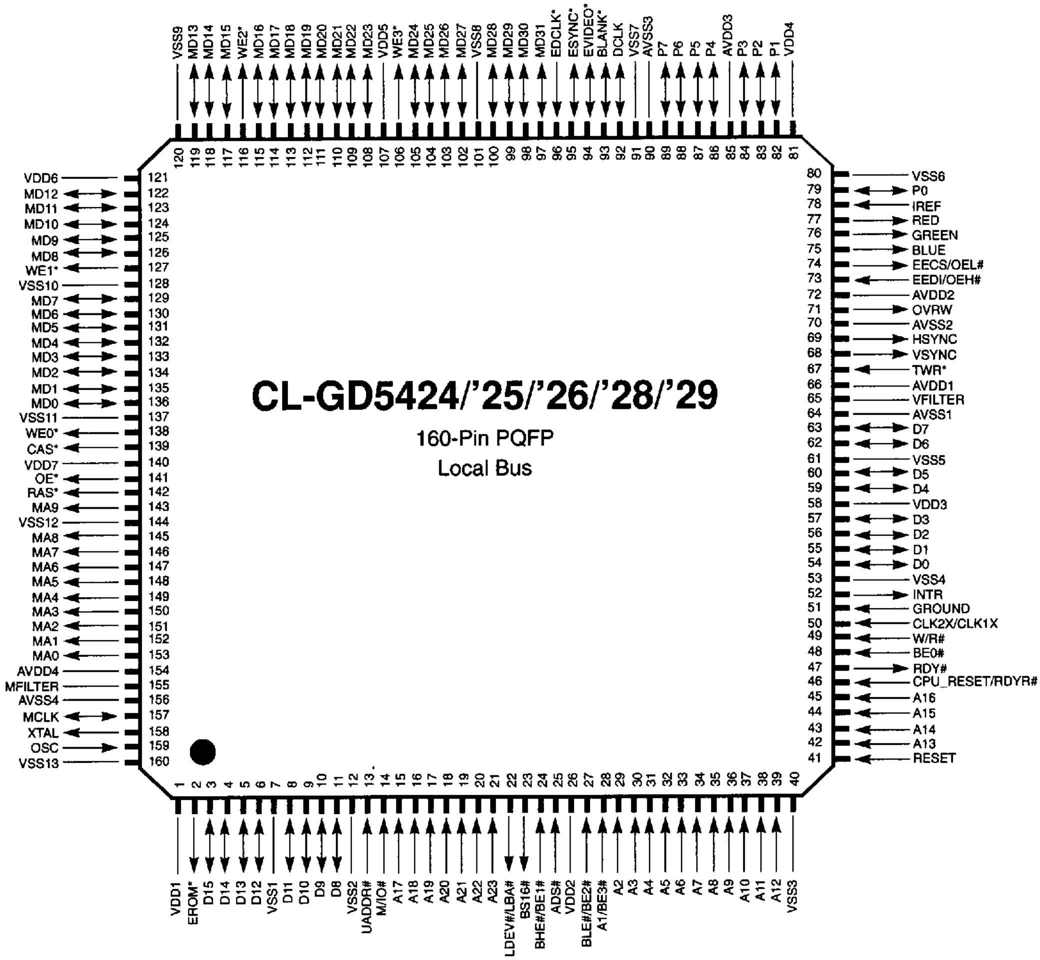
1.3 Pin Diagram (Local Bus)



1.4 Pin Summary

The following abbreviations are used for pin types in the following tables: (I) indicates input; (O) indicates output; (I/O) indicates input or output depending on how the device is configured and programmed

Table 1-1. Host Interface — ISA/MicroChannel®

Pin Number	Pin Type	Pull-up[a]	I_{OH}[b] (mA)	I_{OL}(mA)	Load (pF)	ISA	MicroChannel®
21	I	•				LA23	A23
20	I	•				LA22	A22
19	I	•				LA21	A21
18	I	•				LA20	A20
17	I	•				LA19	A19
16	I	•				LA18	A18
15	I	•				LA17	A17
45	I					SA16	A16
44	I					SA15	A15
43	I					SA14	A14
42	I					SA13	A13
39	I					SA12	A12
38	I					SA11	A11
37	I					SA10	A10
36	I					SA9	A9
35	I					SA8	A8
34	I					SA7	A7
33	I					SA6	A6
32	I					SA5	A5
31	I					SA4	A4
30	I					SA3	A3
29	I					SA2	A2
28	I					SA1	A1
27	I					SA0	A0
3	I/O	•	–3	12	240	SD15	D15
4	I/O	•	–3	12	240	SD14	D14
5	I/O	•	–3	12	240	SD13	D13
6	I/O	•	–3	12	240	SD12	D12
8	I/O	•	–3	12	240	SD11	D11
9	I/O	•	–3	12	240	SD10	D10
10	I/O	•	–3	12	240	SD9	D9
11	I/O	•	–3	12	240	SD8	D8
63	I/O		–3	12	240	SD7	D7
62	I/O		–3	12	240	SD6	D6
60	I/O		–3	12	240	SD5	D5
59	I/O		–3	12	240	SD4	D4
57	I/O		–3	12	240	SD3	D3
56	I/O		–3	12	240	SD2	D2

Table 1-1. Host Interface — ISA/MicroChannel® *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH}[b] (mA)	I_{OL}(mA)	Load (pF)	ISA	MicroChannel®
55	I/O		–3	12	240	SD1	D1
54	I/O		–3	12	240	SD0	D0
24	I	•				SBHE*	–SBHE
25	I					BALE	MADE24
46	I					AEN	–CD_SETUP
49	I					IOR*	–S1
50	I					IOW*	–CMD
14	I					MEMR*	M/–IO
13	I					MEMW*	–S0
41	I	•				RESET	CHRESET
48	I					REFRESH*	–REFRESH
47	O		–3	20	200	IOCHRDY	CD_CHRDY
22	O		–3	20	200	IOCS16*	–CD_SFDBK
23	O		–3	20	200	MCS16*	–CD_DS16
51	O		(OC)	20	200	0WS	(unused)
52	O		–3	20	200	IRQ	–IRQ

[a] • indicates the presence of a 250 kΩ, ± 50 % pull-up resistor.

[b] Data pads nominally rated at –3 mA I_{OH} will sink –15 mA at V_{OH} = 2.0 V.

Table 1-2. Host Interface — Local Bus (CL-GD5424/'25/'26/'28/'29 only)

Pin Number	Pin Type	Pull-up[a]	I_{OH}[b] (mA)	I_{OL} (mA)	Load (pF)	'386SX	'386DX	'486	VESA® VL-Bus™
21	I	•				A23	A23	A23	A23
20	I	•				A22	A22	A22	A22
19	I	•				A21	A21	A21	A21
18	I	•				A20	A20	A20	A20
17	I	•				A19	A19	A19	A19
16	I	•				A18	A18	A18	A18
15	I	•				A17	A17	A17	A17
45	I					A16	A16	A16	A16
44	I					A15	A15	A15	A15
43	I					A14	A14	A14	A14
42	I					A13	A13	A13	A13
39	I					A12	A12	A12	A12
38	I					A11	A11	A11	A11
37	I					A10	A10	A10	A10
36	I					A9	A9	A9	A9
35	I					A8	A8	A8	A8
34	I					A7	A7	A7	A7
33	I					A6	A6	A6	A6

Table 1-2. Host Interface — Local Bus (CL-GD5424/'25/'26/'28/'29 only) *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH}[b] (mA)	I_{OL} (mA)	Load (pF)	'386SX	'386DX	'486	VESA® VL-Bus™
32	I					A5	A5	A5	A5
31	I					A4	A4	A4	A4
30	I					A3	A3	A3	A3
29	I					A2	A2	A2	A2
28	I					A1	BE3#	BE3#	BE3#
27	I					BLE#	BE2#	BE2#	BE2#
3	I/O	•	–3	12	240	D15	D15	D15	D15
4	I/O	•	–3	12	240	D14	D14	D14	D14
5	I/O	•	–3	12	240	D13	D13	D13	D13
6	I/O	•	–3	12	240	D12	D12	D12	D12
8	I/O	•	–3	12	240	D11	D11	D11	D11
9	I/O	•	–3	12	240	D10	D10	D10	D10
10	I/O	•	–3	12	240	D9	D9	D9	D9
11	I/O	•	–3	12	240	D8	D8	D8	D8
63	I/O		–3	12	240	D7	D7	D7	D7
62	I/O		–3	12	240	D6	D6	D6	D6
60	I/O		–3	12	240	D5	D5	D5	D5
59	I/O		–3	12	240	D4	D4	D4	D4
57	I/O		–3	12	240	D3	D3	D3	D3
56	I/O		–3	12	240	D2	D2	D2	D2
55	I/O		–3	12	240	D1	D1	D1	D1
54	I/O		–3	12	240	D0	D0	D0	D0
24	I	•				BHE#	BE1#	BE1#	BE1#
25	I					ADS#	ADS#	ADS#	LADS#
46	I					CPU–Reset	CPU–Reset	CPU–Reset	RDYRTN#
49	I					W/R#	W/R#	W/R#	W/R#
50	I					CLK2X	CLK2X	CLK1X	LCLK
14	I					M/IO#	M/IO#	M/IO#	M/IO#
13	I					(unused)	UADDR#	UADDR#	UADDR#
41	I	•				RESET	RESET	RESET	RESET
48	I					(unused)	BE0#	BE0#	BE0#
47	O		–3	20	200	READY#	READY#	RDY#	RDY#
22	O		–3	20	200	LBA#	LBA#	LBA#	LDEV#
23	O		–3	20	200	(unused)	BS16#	BS16#	LDS16#
51	I		(OC)	20	200	GROUND	GROUND	GROUND	GROUND
52	O		–3	20	200	INTR	INTR	INTR	INTR

[a] • indicates the presence of a 250 kΩ, ± 50 % pull-up resistor.

[b] Data pads nominally rated at –3 mA I_{OH} will sink –15 mA at V_{OH} = 2.0 V.

Table 1-3. Synthesizer Interface

Pin Number	Pin Type	Pull-up	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
159	I					OSC
158	Analog Out/TTL In *(CL-GD5425 only)*					XTAL
155	Analog					MFILTER
65	Analog					VFILTER
157	I/O		–12	12	20	MCLK

Table 1-4. Video Interface

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
68	I/O		–12	–12	50	VSYNC
69	I/O		–12	–12	50	HSYNC
93	I/O		–12	12	50	BLANK*
89	I/O		–12	12	50	P7
88	I/O		–12	12	50	P6
87	I/O		–12	12	50	P5
86	I/O		–12	12	50	P4
84	I/O		–12	12	50	P3
83	I/O		–12	12	50	P2
82	I/O		–12	12	50	P1
79	I/O		–12	12	50	P0
92	I/O		–12	12	50	DCLK
95	I/O	•				ESYNC*
94	I/O	•				EVIDEO*
96	I	•				EDCLK*
77	Analog Out					RED
76	Analog Out					GREEN
75	Analog Out					BLUE
78	Analog In					IREF

[a] • indicates the presence of a 250 kΩ, ± 50% pull-up resistor.

Table 1-5. Display Memory Interface

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
142	O		–8	12	50	RAS*
139	O		–12	12	50	CAS*[b]
141	O		–12	12	50	OE*[c]
106	O		–12	12	50	WE3*[d]
116	O		–12	12	50	WE2*
127	O		–12	12	50	WE1*[e]
138	O		–12	12	50	WE0*[e]
143	O		–12	12	50	MA9
145	O		–12	12	50	MA8
146	O		–12	12	50	MA7
147	O		–12	12	50	MA6
148	O		–12	12	50	MA5
149	O		–12	12	50	MA4
150	O		–12	12	50	MA3
151	O		–12	12	50	MA2
152	O		–12	12	50	MA1
153	O		–12	12	50	MA0
97	I/O	•	–12	12	50	MD31
98	I/O	•	–12	12	50	MD30
99	I/O	•	–12	12	50	MD29
100	I/O	•	–12	12	50	MD28
102	I/O	•	–12	12	50	MD27
103	I/O	•	–12	12	50	MD26
104	I/O	•	–12	12	50	MD25
105	I/O	•	–12	12	50	MD24
108	I/O	•	–12	12	50	MD23
109	I/O	•	–12	12	50	MD22
110	I/O	•	–12	12	50	MD21

Table 1-5. Display Memory Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
111	I/O	•	–12	12	50	MD20
112	I/O	•	–12	12	50	MD19
113	I/O	•	–12	12	50	MD18
114	I/O	•	–12	12	50	MD17
115	I/O	•	–12	12	50	MD16
117	I/O	•	–12	12	50	MD15[e]
118	I/O	•	–12	12	50	MD14[e]
119	I/O	•	–12	12	50	MD13[e]
122	I/O	•	–12	12	50	MD12[e]
123	I/O	•	–12	12	50	MD11[e]
124	I/O	•	–12	12	50	MD10[e]
125	I/O	•	–12	12	50	MD9[e]
126	I/O	•	–12	12	50	MD8[e]
129	I/O	•	–12	12	50	MD7[e]
130	I/O	•	–12	12	50	MD6[e]
131	I/O	•	–12	12	50	MD5[e]
132	I/O	•	–12	12	50	MD4[e]
133	I/O	•	–12	12	50	MD3[e]
134	I/O	•	–12	12	50	MD2[e]
135	I/O	•	–12	12	50	MD1[e]
136	I/O	•	–12	12	50	MD0[e]

a • indicates the presence of a 250 kΩ, ± 50 % pull-up resistor.
b CAS* is redefined as WE* for multiple-CAS* 256K × 16 DRAMs for the CL-GD5422/'24/'25/'26/'28/'29.
c OE* is redefined as RAS1* for 2-Mbyte display memory configurations for the CL-GD5426/'28/'29 only.
d WE*[3:0] are redefined as CAS*[3:0] for multiple-CAS* 256K × 16 DRAMs for the CL-GD5422/'24/'25/'26/'28/'29.
e WE1*, WE0, MD[15:0] are reserved on the CL-GD5420.

Table 1-6. Miscellaneous Pins

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
74	Out		–12	12	35	EECS[b]
73	In					EEDI[c]
2	Out		–12	12	35	EROM*
71	Out		–12	12	35	OVRW[d]
67	In					TWR*

a • indicates the presence of a 250 kΩ, ± 50 % pull–up resistor.

b EECS is redefined as OEL# when the CL-GD5424/'25/'26/'28/'29 (only) is configured for '486, VESA VL-Bus, or local bus operation.

c EEDI is redefined as OEH# when the CL-GD5424/'25/'26/'28/'29 (only) is configured for '486, VESA VL-Bus, or local bus operation.

d OVRW is reserved on the CL-GD5420.

Table 1-7. Power and Ground

Pin Number	Pin Type	Pull-up	I_{OH}	I_{OL}	Load (pF)	Name	Note
140	Power					VDD7	Digital
121	Power					VDD6	Digital
107	Power					VDD5	Digital
81	Power					VDD4	Digital
58	Power					VDD3	Digital
26	Power					VDD2	Digital
1	Power					VDD1	Digital
160	Ground					VSS13	Digital
144	Ground					VSS12	Digital
137	Ground					VSS11	Digital
128	Ground					VSS10	Digital
120	Ground					VSS9	Digital
101	Ground					VSS8	Digital
91	Ground					VSS7	Digital
80	Ground					VSS6	Digital
61	Ground					VSS5	Digital
53	Ground					VSS4	Digital
40	Ground					VSS3	Digital
12	Ground					VSS2	Digital
7	Ground					VSS1	Digital
66	Power					AVDD1	VCLK
64	Ground					AVSS1	VCLK
154	Power					AVDD4	MCLK
156	Ground					AVSS4	MCLK
85	Power					AVDD3	DAC
72	Power					AVDD2	DAC
90	Ground					AVSS3	DAC
70	Ground					AVSS2	DAC

2. DETAILED PIN DESCRIPTIONS

The following abbreviations are used for pin types in the following sections: (I) indicates input; (O) indicates output; (I/O) indicates a bidirectional signal; (TS) indicates three-state; (OC) indicates open collector.

2.1 Host Interface — ISA Bus Mode

Name	Type	Description
LA[23:17]	I	**ADDRESS [23:17]:** These inputs, in conjunction with SA[16:0], are used to select the resource to be accessed during memory operations. These address bits are latched with the falling edge of BALE.
SA[16:0]	I	**ADDRESS [16:0]:** These inputs, in conjunction with LA[23:17], are used to select the resource to be accessed during any memory or I/O operation. These address bits must remain valid throughout the cycle.
SD[15:8]	TS	**SYSTEM DATA [15:8]:** These bidirectional pins are used to transfer data during 16-bit memory or I/O operations. These pins can be directly connected to the corresponding ISA bus pins. These pads have pull-up resistors to guarantee a valid input level when not connected.
SD[7:0]	TS	**SYSTEM DATA [7:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. These pins can be directly connected to the corresponding ISA bus pins.
SBHE*	I	**SYSTEM BYTE HIGH ENABLE:** This input is used in conjunction with A[0] to determine the width and alignment of a data transfer. SBHE* and A[0] are decoded as shown in Table 2-1:

Table 2-1. SBHE/A0 Decoding

SBHE*	A0	Function
0	0	16-bit Transfer
0	1	Upper-byte Transfer
1	0	Lower-byte Transfer
1	1	Lower-byte Transfer *(on odd address)*

Name	Type	Description
BALE	I	**BUS ADDRESS LATCH ENABLE:** This active-high input is used to latch LA[23:17] on the high-to-low transition.
AEN	I	**ADDRESS ENABLE:** If this input is high, it indicates that the current cycle is a DMA cycle. In this case, the CL-GD542X will not respond to I/O cycles. There is no effect on memory cycles.

2.1 Host Interface — ISA Bus Mode *(cont.)*

Name	Type	Description
IOR*	I	**I/O READ:** This active-low input is used to indicate that an I/O read is occurring. If the address on SA[15:0] is within the range of the CL-GD542X, it will respond by placing the contents of the appropriate register on the System Data bus.
IOW*	I	**I/O WRITE:** This active-low input is used to indicate that an I/O write is occurring. If the address on SA[15:0] is within the range of the CL-GD542X, it will respond by transferring the contents of the System Data bus into the appropriate register. The transfer will occur on the trailing (rising) edge of this signal. A list of I/O addresses that the CL-GD542X will respond appears in Section 5 on page 49. When a 16-bit I/O write is done, the address specified is typically the Index register for one of the VGA groups. The index should appear on SD[7:0] and the data should appear on SD[15:8].
MEMR*	I	**MEMORY READ:** This active-low input is used to indicate that a memory read is occurring. If linear addressing is being used, this pin must be connected to ISA signal MEMR*. If linear addressing is not being used, this pin must be connected to ISA signal SMEMR*. The CL-GD542X decodes A[23:15] to determine if a display memory read is occurring. If so, data is placed on the System Data pins according to the read mode and the contents of display memory. The CL-GD542X decodes A[23:15] to determine if a BIOS read is occurring. If so, the CL-GD542X makes EROM* active for the duration of MEMR*.
MEMW*	I	**MEMORY WRITE:** This active-low input is used to indicate that a memory write is occurring. If linear addressing is being used, this pin must be connected to ISA signal MEMW*. If linear addressing is not being used, this pin must be connected to ISA signal SMEMW*. The CL-GD542X decodes A[23:15] to determine if a display memory write is occurring. If so, data is written into display memory according to the write mode and the data on SD[15:0]. The data are latched in the CL-GD542X on the rising edge of this signal, and are actually transferred to display memory later.
RESET	I	**RESET:** This active-high signal is used to initialize the CL-GD542X to a known state. The trailing (falling) edge of this input loads the Configuration register CF[14:0] with the data on MD[30:16], determined by internal pull-up resistors and (optional) external pull-down resistors.
REFRESH*	I	**REFRESH*:** This active-low signal indicates that a DRAM refresh is occurring. The CL-GD542X ignores memory read operations occurring when REFRESH* is active since it controls the refresh of display memory.

2.1 Host Interface — ISA Bus Mode *(cont.)*

Name	Type	Description
IOCHRDY	TS	**I/O CHANNEL READY:** When driven low, this output indicates that additional wait states are to be inserted into the current display memory read or write cycle. This output is never driven low during I/O cycles or BIOS reads. During a display memory read cycle, this signal is always driven low as soon as MEMR* goes active. When the data are ready to be placed on the System Data bus, this signal is driven high. It remains high until MEMR* goes inactive; it then goes high impedance. During a display memory write cycle, this signal is driven high as soon as MEMW* goes active if there is space in the Write Buffer. If there is no space in the Write Buffer, this signal is driven low as soon as MEMW* goes active and remains low until there is space. Once there is space in the Write Buffer, this signal is driven high. It will remain high until MEMW* goes inactive; it then goes high-impedance.
IOCS16*	OC	**I/O CHIP SELECT 16*:** This open-collector output is driven low to indicate that the CL-GD542X can execute an I/O operation at the address currently on the bus in 16-bit mode. This signal is generated from a decode of A[15:0] and AEN. Table 2-2 indicates the range of addresses that the CL-GD542X will generate IOCS16*:

Table 2-2. IOCS16* Addresses

Address	Function
3C4, 3C5	Sequencer
3CE, 3CF	Graphics controller
3B4/3D4, 3B5/3D5	CRT controller
3BA/3DA	Input Status register 1

Name	Type	Description
MCS16*	OC	**MEMORY CHIP SELECT 16*:** This open-collector output is driven low to indicate that the CL-GD542X can execute a memory operation at the address currently on the bus in 16-bit mode. Table 2-3 summarizes the conditions where MCS16* is made active.

Table 2-3. MSC16* Addresses

Resource	Address Bits	Address Range	Qualifier
Display memory	A[23:17]	A000:0-BFFF:F	SR8[6] = 1 (No other VGA card)
Display memory	A[23:17]	1 Mbyte	SR7[7:4] ≠ 0 Linear Addressing
BIOS	A[23:15]	C000:0-C7FF:F	CF[6] = 0 (16-bit BIOS)

NOTE: The SA bits are generated late enough to typically make them unusable for generating MCS16*. The CL-GD542X uses a fast path from SA[16:15] to MCS16*.

2.1 Host Interface — ISA Bus Mode *(cont.)*

Name	Type	Description
0WS*	OC	**ZERO WAIT STATE*:** This open-collector output is driven low to indicate that the current cycle can be completed without any additional wait states. The circumstances under which 0WS* will be made active are summarized in Table 2-4.

Table 2-4. Zero Wait State* Cycles

Cycle Type	Qualifier
Display memory write	Write buffer not full
BIOS Read	CF[1] = 0 (not on CL-GD5429)

Name	Type	Description
IRQ	TS	**INTERRUPT REQUEST:** This active-high output indicates the CL-GD542X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. This pin is typically unused in PC/AT add-in cards, but can be connected to IRQ2/IRQ9 via a jumper block. See register CR11 for a description of the controls for this pin.

2.2 Host Interface — MicroChannel® Bus Mode

Name	Type	Description
A[23:0]	I	**ADDRESS [23:0]:** These inputs are used to select the resource to be accessed during a memory or I/O operation. These address bits are latched with the falling edge of –CMD. A[23:17] have internal pull-ups, whereas A[16:0] do not.
D[15:0]	TS	**DATA [15:0]:** These bidirectional pins are used to transfer data during memory or I/O operation. These pins can be directly connected to the corresponding MicroChannel bus pins.
–SBHE	I	**–SYSTEM BYTE HIGH ENABLE:** This input is used in conjunction with A[0] to determine the width and alignment of a data transfer. This signal is latched with –CMD low. This pad has a pull-up resistor. –SBHE and A[0] are decoded as shown in Table 2-5.

Table 2-5. –SBHE/A0 Decoding

–SBHE	A0	Function
0	0	16-bit Transfer
0	1	Upper-byte Transfer
1	0	Lower-byte Transfer
1	1	Lower-byte Transfer *(on odd address)*

Name	Type	Description
MADE24	I	**MEMORY ADDRESS ENABLE 24:** This active-high input is latched the falling edge of –CMD. It indicates that the address is in the lower 16 Mbytes of address space. MADE24 must be high for the CL-GD542X to participate in a memory cycle.
–CD_SETUP	I	**–CARD SETUP:** When this active-low input is active, the CL-GD542X is placed in Setup mode. In Setup mode, the CL-GD542X will respond only to POS102 accesses. It will not respond to any other I/O accesses or to display memory accesses. It will respond to BIOS reads. This signal is latched with the falling edge of –CMD.

2.2 Host Interface — MicroChannel® Bus Mode *(cont.)*

Name	Type	Description
-S1	I	**-STATUS 1:** This signal, in conjunction with -S0 and M/-IO, is used to determine the cycle type that occurs. The encoding is shown in Table 2-6:

Table 2-6. MicroChannel® Cycle Type Encoding

M/-IO	-S0	-S1	Cycle
0	0	0	Reserved
0	0	1	I/O write
0	1	0	I/O read
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Memory write
1	1	0	Memory read
1	1	1	Reserved

Name	Type	Description
-CMD	I	**-COMMAND:** The falling edge of this input is used to latch the address bus, MADE24, -SBHE, -REFRESH, M/-IO, -CD_SETUP, -S0, and -S1. It is also used to time the actual data transfer. During I/O or memory-read cycles, the CL-GD542X drives valid data onto the bus prior to the trailing edge of this signal. During write cycles, the CL-GD542X expects valid data while this input is active and latches the data at the trailing edge.
M/-IO	I	**MEMORY/-IO:** This signal, in conjunction with -S0 and -S1, is decoded to determine the cycle type. See the description of -S1.
-S0	I	**-STATUS 0:** This signal, in conjunction with -S1 and M/-IO, is decoded to determine the cycle type. See the description of -S1.
RESET	I	**RESET:** This active-high signal is used to initialize the CL-GD542X to a known state. The trailing (falling) edge of this input loads the Configuration register CF[14:0] with the data on MD[30:16], determined by internal pull-up resistors and (optional) external pull-down resistors.
-REFRESH	I	**-REFRESH:** This active-low signal indicates that a DRAM refresh is occurring. This signal is latched with -CMD low. The CL-GD542X ignores memory-read operations occurring when -REFRESH is active since it controls the refresh of display memory.

2.2 Host Interface — MicroChannel® Bus Mode *(cont.)*

Name	Type	Description
CD_CHRDY	O	**CARD CHANNEL READY:** This output is driven low to request that additional wait states be inserted into the current display memory read or write cycle. This output is never driven low during I/O cycles or BIOS reads. During a display memory read cycle, this signal is always driven low as soon as -S1 goes low. When the data are ready to be placed on the System Data bus, this signal is driven high. During a display memory write cycle, this signal is driven high as soon as -S0 goes low if there is space in the Write Buffer. If there is no space in the Write Buffer, this signal is driven low as soon as -S0 goes low, and remains low until there is space. Once there is space in the Write Buffer, this signal is driven high.
-CD_SFDBK	OC	**-CARD SELECTED FEEDBACK:** This open-collector output is driven low to indicate that the CL-GD542X can respond to the addresses currently on the bus. This signal is generated from a decode of -REFRESH, MADE24, A[23:0], and M/-IO. This signal is made active for the Address Range C000:0–C7FF:F only if CF[6] = 0 (indicating a 16-bit BIOS). If CF[6] = 1, this signal will not be made active for Address Range C000:0–C7FF:F. Also, this signal will not be made active for Addresses 102 or 103 if M/-IO is low, indicating I/O.
-CD_DS16	OC	**-CARD SIZE 16:** This open-collector output is driven low to indicate that the CL-GD542X can execute a memory or I/O operation at the address currently on the bus in 16-bit mode. This output is generated from a decode of A[23:0], MADE24, -REFRESH, and M/-IO. Table 2-7 summarizes the conditions under which -CD_DS16 is made active.

Table 2-7. -CD_DS16 Addresses

Resource	Address Bits	Address Range
Display memory	A[23:15]	A000:0–BFFF:F
Display memory	A[23:15]	1 Mbyte
BIOS (CF[6] = 0 only)	A[23:11]	C000:0–C7FF:F
I/O	A[15:1]	3C4, 3C5 3CE, 3CF 3B/D4, 3B/D5 3B/DA

Name	Type	Description
-IRQ	OC	**-INTERRUPT REQUEST:** This open-collector output indicates the CL-GD542X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. This pin is typically connected to IRQ9 via a jumper block. See register CR11 for a description of the controls for this pin. This pin is never driven high.

2.3 Host Interface — Local Bus (CL-GD5424/'25/'26/'28/'29 only)

A number of bus interface pins are redefined according to the local bus type connecting to the CL-GD5424/'25/'26/'28/'29. The host interface pins are listed in Table 2-8 by CL-GD5424/'25/'26/'28/'29 pin number.

Table 2-8. Redefined Host Interface Pins

Pin	'386SX	'386DX	'486	VESA® VL-Bus™
13	(unused)	UADDR#	UADDR#	UADDR#
23	(unused)	BS16#	BS16#	LBS16#
24	BHE#	BE1#	BE1#	BE1#
27	BLE#	BE2#	BE2#	BE2#
28	A1	BE3#	BE3#	BE3#
46	CPU-RESET	CPU-RESET	GND	RDYRTN#
47	READY#	READY#	BRDY#	BRDY#
48	(unused)	BE0#	BE0#	BE0#
50	CLK2X	CLK2X	CLK1X	LCLK
51	GROUND	GROUND	GROUND	GROUND
73	(unused)	(unused)	OEH#	OEH#
74	(unused)	(unused)	OEL#	OEL#

2.3 Host Interface — Local Bus (CL-GD5424/'25/'26/'28/'29 only) *(cont.)*

Name	Type	Description
A[23:2]	I	**ADDRESS [23:2]:** These inputs are used to select the resource to be accessed during memory or I/O operations. A[23:17] have internal pull-up resistors; A[16:2] do not. A[3:2] are burst address bits for the '486.
D[15:0]	TS	**DATA [15:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. These pins are directly connected to D[15:0] of the '386SX or '386DX bus. These pins are connected via four bidirectional data transceivers to the 32 data pins of the '486 or VESA VL-Bus. The transceivers are controlled with OEH#, OEL#, and W/R#. These pads have pull-up resistors.
BE[3:0]#	I	**BYTE ENABLE [3:0]#:** These active-low inputs are directly connected to the '386DX/'486 or VESA VL-Bus byte enable outputs. In the case of the '386SX, BE0# is unused and can be left unconnected. BE1#, 2, and 3 are redefined as BHE#, BLE#, and A1, respectively. They must be directly connected to the corresponding '386 outputs.
ADS#	I	**ADDRESS STROBE:** This active-low input indicates that a new cycle has begun. It must be directly connected to the ADS# pin on the CPU. For VESA VL-Bus, this pin is connected to LADS#.
CPU-RESET	I	**CPU RESET:** When this active-high input is active, the CL-GD542X is forced into an initial condition. It is used to synchronize the CL-GD542X to CLK1X or CLK2X. This pin *must* be connected to the RESET pin of the CPU in a '386 system; it *must* be connected to ground in a '486 system; it *must* be connected to RDYRTN# in a VESA VL-Bus system.
W/R#	I	**WRITE/READ:** This input indicates whether a write or read operation is to occur. It must be directly connected to the W/R# pin on the CPU. If W/R# is high, a write will occur. If it is low, a read will occur.
CLK2X	I	**CLOCK 2X:** This is the timing reference for the CL-GD542X when connected to a '386SX or '386DX local bus. This is redefined as CLK1X for the '486 local bus. In either case, it must be directly connected to the corresponding CPU pin. For VESA VL-Bus, this pin is connected to LCLK.
M/IO#	I	**MEMORY/IO#:** This input indicates whether a memory or I/O operation is to occur. It must be directly connected to the M/IO# pin on the CPU. If M/IO# is high, a memory operation will occur. If it is low, an I/O operation will occur.
UADDR#	I	**UPPER ADDRESS:** This active-low input is a decode of the upper-CPU Address bits A[32:24]. This input is unused in the case of a '386SX local bus and can be left unconnected. Refer to appendixes in the *CL-GD542X Technical Reference Manual* for information on the generation of this signal.

2.3 Host Interface — Local Bus (CL-GD5424/'25/'26/'28/'29 only) *(cont.)*

Name	Type	Description
RESET	I	**RESET:** This active-high input initializes the CL-GD542X to a known state. The trailing (falling) edge of this input loads the Configuration register CF[14:0] with the data on MD[30:16], determined by internal pull-up resistors and (optional) external pull-down resistors.
RDY#	TS	**RDY #:** This active-low signal is used as an output to terminate a CL-GD542X bus cycle.
LBA#	TS	**LOCAL BUS ACKNOWLEDGE #:** This open-collector output is driven low to indicate that the CL-GD542X will respond to the current cycle. This signal is generated from a decode of A[23:2], UADDR#, and M/IO#. This output will be active before the middle of the first T2 after an active ADS#. For VESA VL-Bus, this pin is connected to LDEV#.
BS16#	OC	**BUS SIZE 16 #:** This active-low output is driven by the CL-GD542X to indicate that the current cycle addresses a 16-bit resource. The '386DX/'486 will convert the cycle to an appropriate number of 16-bit transfers. This pin is not used for a '386SX local bus and can be left unconnected. For VESA VL-Bus, this pin is connected to LBS16#.
INTR	TS	**INTERRUPT REQUEST:** This active-high output indicates the CL-GD542X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. See register CR11 for a description of the controls for this pin.
OEH#	O	**OUTPUT ENABLE HIGH#:** This active-low output controls the output enables for the data transceivers that connect the CL-GD542X SD[15:0] pins to the '486 or VESA VL-Bus D[31:16] pins.
OEL#	O	**OUTPUT ENABLE LOW#:** This active-low output controls the output enables for the data transceivers that connect the CL-GD542X SD[15:0] pins to the '486 or VESA VL-Bus D[15:0] pins.

2.4 Dual-Frequency Synthesizer Interface

Name	Type	Description
OSC	I	**OSCILLATOR INPUT:** This TTL input pin supplies the reference frequency for the dual-frequency synthesizer. It requires an input frequency of 14.31818 ± 0.01% MHz with a duty cycle of 50 ± 10%. This input can be supplied from the appropriate pin on the ISA or MicroChannel bus, from an oscillator, or with a series-resonant crystal connected between this pin and the XTAL pin. **NOTE:** When the CL-GD5425 (only) is configured for PAL/NTSC operation (pull-down installed on MD16), this pin should be driven with 17.734475 MHz. This is the reference frequency for PAL.
XTAL	I/O	**CRYSTAL:** This output pin allows the use of a crystal to supply the reference frequency for the synthesizer. A series-resonant crystal can be connected between this pin and the OSC pin. If this pin is not used for a crystal connection, it *must* be left unconnected (except for CL-GD5425). When the CL-GD5425 (only) is configured for PAL/NTSC operation (pull-down installed on MD16), this is an input pin and should be driven with 14.31818 MHz. This is the reference frequency for NTSC, the MCLK synthesizer, and VGA modes.
MFILTER	O	**MEMORY CLOCK FILTER:** This pin must be connected to a π RC filter returned to AVSS4. The values of the two capacitors and the resistor are shown in Appendix B17 in the *CL-GD542X Technical Reference Manual.* The filter components, especially the input capacitor and the resistor, must be placed as closely as possible to this pin.
VFILTER	O	**VIDEO CLOCK FILTER:** This pin *must* be connected to a π RC filter returned to AVSS1 or AVDD1, depending on processing. The values of the two capacitors and the resistor are shown in Appendix B17 in the *CL-GD542X Technical Reference Manual.* The filter components, especially the input capacitor and the resistor, *must* be placed as closely as possible to this pin.
MCLK	I/O	**MEMORY CLOCK:** This pin is normally an output and can be used to monitor the internal MCLK. Typically, it would not be connected. If CF[4] is a zero, MCLK will be an input and the internal MCLK oscillator will be disabled. This configuration is intended for testing only. **NOTE:** For the CL-GD5425 and CL-GD5429 only, this pin can be configured to output the internal VCLK VCO. If a pull-down is installed on MD31 (and no pull-down on MD20), the internal VCLK VCO (prior to the post-scalar) will be driven onto this pin.

2.5 Video Interface

Name	Type	Description
VSYNC	I/O	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin is put into high impedance when ESYNC* is low. This pin can be directly connected to the corresponding pin on the feature connector. **NOTE:** When the CL-GD5425 (only) is configured for VSYNC GENLOCK, by programming CR1C[7] to '1', VSYNC becomes an input.
HSYNC	I/O	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin is put into high impedance when ESYNC* is low. This pin can be directly connected to the corresponding pin on the feature connector. **NOTE:** When the CL-GD5425 (only) is configured for HSYNC GENLOCK, by programming CR1C[6] to '1', HSYNC becomes an input.
BLANK*	I/O	**BLANK*:** This is a bidirectional pin. If ESYNC* is high, BLANK* is an output. As an output, it supplies a blanking signal to the feature connector. If ESYNC* is low, BLANK* is an input. As an active-low input, it forces the RED, GREEN, and BLUE outputs to zero current. This pin can be directly connected to the corresponding pin on the feature connector. **NOTE:** When the CL-GD5425 (only) is configured for TV mode by programming CR30[3] to '1', this pin becomes the Color Carrier Reference (Nx fsc).
P[7:0]	I/O	**PIXEL BUS [7:0]:** These are bidirectional pins. If EVIDEO* is high, these pins are outputs and reflect the address into the palette DAC. If EVIDEO* is low, these pins are inputs and can be used to drive pixel values into the palette DAC. These pins can be directly connected to the corresponding pins on the feature connector.
DCLK	I/O	**VIDEO DOT CLOCK:** This is a bidirectional pin. If EDCLK* is high, this is an output and can be used to externally latch the data on the Pixel Bus. If EDCLK* is low, this is an input and can be used to clock data on the Pixel bus into the CL-GD542X. This pin can be directly connected to the corresponding pin on the feature connector.
ESYNC*	I/O	**ENABLE SYNC AND BLANK:** This input is used to control the buffers on HSYNC, VSYNC, and BLANK*. If ESYNC* is high, the controlled pins are outputs. If ESYNC* is low, BLANK* is an input. HSYNC and VSYNC are not driven by the CL-GD542X and must be driven externally to valid input levels. This pin can be directly connected to the corresponding pin on the feature connector. **NOTE:** For the CL-GD5425, the ESYNC* pin will be an output and will reflect SR8[2] whenever Overlay mode is selected by programming CR1A[3:2] to any value other than '0,0' or whenever TV mode is selected by programming CR30[3] to'1'.
EVIDEO*	I/O	**ENABLE VIDEO:** This input controls the buffers on P[7:0]. If EVIDEO* is high, P[7:0] are outputs; if EVIDEO* is low, P[7:0] are inputs. This pin can be directly connected to the corresponding pin on the feature connector. This pin is not limited to static operation; it can switch at the DCLK rate.

2.5 Video Interface *(cont.)*

Name	Type	Description
EDCLK*	I	**ENABLE DOT CLOCK:** This input is used to control the buffer on DCLK. If EDCLK* is high, DCLK is an output; if EDCLK* is low, DCLK is an input. This pin can be directly connected to the corresponding pin on the feature connector.
RED	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, either the 6-bit value from the LUT or a 5-, 6-, or 8-bit true-color value is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: $$If = (63/30) \times IREF$$ To maintain IBM VGA compatibility, each DAC output is typically terminated to monitor ground with a 75-Ω 2-percent resistor. This resistor, in parallel with the 75-Ω resistor in the monitor, will yield a 37.5-Ω impedance to ground. For a full-scale voltage of 700 mV, full-scale current output should be 18.7 mA.
GREEN	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
BLUE	O	**BLUE VIDEO:** This analog output supplies current corresponding to the blue value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
IREF	I	**DAC CURRENT REFERENCE:** The current drawn from AV_{DD} through this pin determines the full-scale output of each DAC. Connect this pin to a constant current source. A recommended circuit is provided in appendixes of the *CL-GD542X Technical Reference Manual.*

2.6 Display Memory Interface

Name	Type	Description
RAS*	O	**ROW ADDRESS STROBE *:** This active-low output is used to latch the row address from MA[9:0] into the DRAMs. This pin must be connected to the RAS* pins of all the DRAMs in the display memory array. These pads, and those for the other DRAM controls, are matched for one-to-four loads. If eight DRAMs are used, damping resistors may be required to control edge rates and undershoot on these, and other, control pins.
CAS*	O	**COLUMN ADDRESS STROBE *:** This active-low output is used to latch the Column Address from MA[9:0] into the DRAMs. This pin must be connected to the CAS* pins of all the DRAMs in the display memory array. **NOTE:** If CF[12] = 0 (dual-CAS* DRAMs), this pin becomes WE*.
OE*	O	**OUTPUT ENABLE *:** This active-low output is used to control the output enables of the DRAMs. For 256K × 4 DRAMs and 256K × 16 DRAMs with Dual-write Enables, this pin *must* be connected to the OE* pins of all the DRAMs in the display memory array. For 256K × 16 DRAMs with dual-CAS*, this pin is a no-connect. For the CL-GD5426/'28/'29 with 2 Mbytes of display memory, this pin becomes RAS1*. See the DRAM configuration tables in Section 4. **NOTE:** For the CL-GD5425 (only), this pin is ODD/EVEN when the chip is configured for TV-out and indicates which field is being displayed.
WE[3:0]*	O	**WRITE ENABLE [3:0]*:** These active-low outputs are used to control the write enable inputs of the DRAMs. These pins *must* be connected to the WE* pins of the DRAMs as indicated in the DRAM configuration tables in Section 4. **NOTE:** If CF[12] = 0 (dual-CAS* DRAMs) these pins become CAS[3:0]*. These pins can be connected to the CAS* pins of the DRAMs. WE[1:0]* are reserved on the CL-GD5420 (Revision 'A').
MA[9]	O	**MEMORY ADDRESS [9]:** This pin controls one address input of the DRAMs. See the DRAM configuration tables in Section 4. When the CL-GD5425 (only) is configured for TV mode, by programming CR30[3] to '1', this pin becomes CSYNC out. CSYNC includes all horizontal and vertical timing and serration pulses.
MA[8:0]	O	**MEMORY ADDRESS [8:0]:** These pins control the address inputs of the DRAMs. These pins must be connected to the address pins of the DRAMs. See the DRAM configuration tables in Section 4.
MD[31:0]	TS	**MEMORY DATA [31:0]:** These pins are used to transfer data between the CL-GD542X and the display memory. These pins must be connected to the data pins of the DRAMs. See the DRAM configuration tables in Section 4. These pins are forced into high impedance when RESET is active. This allows the configuration pull-down resistors to override the weak pull-ups and be loaded into the Configuration register CF. MD[15:0] are reserved on the CL-GD5420 (Revision 'A').

2.7 Miscellaneous Pins

Name	Type	Description
EECS	O	**EEPROM CHIP SELECT:** This pin is used to control the Chip Select of the optional configuration EEPROM, and should be directly connected to that pin (ISA and Micro-channel only). **NOTE:** This pin is redefined as OEL* for the '486 or VESA VL-Bus (CL-GD5424/'26/'28/'29 only).
EEDI	I	**EEPROM DATA IN:** This pin is used to read the data from the optional configuration EEPROM, and should be directly connected to the Data Out pin (ISA and Micro-channel only). **NOTE:** This pin is redefined as OEH* for the '486 or VESA VL-Bus (CL-GD5424/'26/'28/'29 only).
EROM*	O	**ENABLE ROM BUFFERS*:** This active-low output is used to control the Output Enable pins of up to two 8-bit bus drivers. These buffers are used to connect the data pins of the BIOS EPROMs to the System Data bus. This output is forced high when RESET is active. This output goes active only for memory read cycles to the address range C000:0–C7FF:F. It is gated with MEMR* in ISA mode, and with -CMD in MicroChannel mode. It is un-latched address decode in Local Bus modes.
OVRW	O	**OVERLAY WINDOW:** This output signal is active-high. It is intended to be used in applications involving video overlays. For additional connectivity information, see Appendix B14 in the CL-GD542X technical reference manual. OVRW is reserved on the CL-GD5420.
TWR*	I	**TEST LATCH LOAD ENABLE*:** This pin is intended for factory testing and must be pulled-up for normal operation. It can be used in board-level testing to disable most of the CL-GD542X output pins. For additional information, see Appendix B14 in the *True Color VGA Family — CL-GD542X Technical Reference Manual.*

2.8 Power Pins

Name	Type	Description
VDD[7:1]	Power	**PLUS FIVE (LOGIC):** These seven pins are used to supply +5 volts to the core logic of the CL-GD542X. Each pin *must* be connected to the VCC rail as described in Appendixes B1–B3 of the *True Color VGA Family — CL-GD542X Technical Reference Manual.* Each pin *must* be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, placed as closely to the pin as possible. If a multi-layer board is used, each VDD pin *must* be connected to the power plane as outlined in Appendixes B1–B3 in the *True Color VGA Family — CL-GD542X Technical Reference Manual.*
VSS[13:1]	Ground	**GROUND (LOGIC):** These 13 pins are used to supply ground reference to the core logic of the CL-GD542X. Each pin *must* be directly connected to the GND rail. If a multi-layer board is used, each VSS pin *must* be connected to the ground plane.
AVDD[1]	Power	**PLUS FIVE (VCLK):** This pin is used to supply +5 volts to the video clock synthesizer of the CL-GD542X. This pin must be connected to the VCC rail via a 33-Ω resistor, and bypassed to AVSS4 with a 10-µF capacitor.
AVSS[1]	Ground	**GROUND (VCLK):** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD542X. This pin *must* be connected to the GND rail.
AVDD[4]	Power	**PLUS FIVE (MCLK):** This pin is used to supply +5 volts to the memory clock synthesizer of the CL-GD542X. This pin must be connected to the VCC rail through a 33-Ω resistor and bypassed to AVSS4 with a 10-µF capacitor.
AVSS[4]	Ground	**GROUND (MCLK):** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD542X. This pin *must* be connected to the GND rail.
AVDD[3:2]	Power	**PLUS FIVE (DAC):** These two pins are used to supply +5 volts to the palette DAC of the CL-GD542X. Each pin must be directly connected to the VCC rail. Each pin must be bypassed, as closely to the pin as possible, with a 0.1-µF capacitor with proper high-frequency characteristics. If a multi-layer board is used, each VDD pin *must* be connected to the power plane.
AVSS[3:2]	Ground	**GROUND (DAC):** These two pins are used to supply the ground reference to the palette DAC of the CL-GD542X. Each pin must be connected to the GND rail. For various adapter board and motherboard solutions, see the appendixes in the *True Color VGA Family — CL-GD542X Technical Reference Manual.*

3. FUNCTIONAL DESCRIPTION

3.1 General

The CL-GD542X family of VGA controllers offers a complete VGA-standards-compatible solution. All of the hardware necessary for CPU updates to memory, screen refresh, and DRAM refresh is included in the CL-GD542X. A complete VGA motherboard solution can be implemented with one 256K × 16 DRAM with any CL-GD542X chip.

The chip block diagram in Figure 3-1 shows the CL-GD542X connection to the host, display memory, and monitor. Each member of the CL-GD542X family of VGA controllers is pin-to-pin compatible on the system bus.

3.2 Functional Blocks

The following functional blocks have been integrated into the CL-GD542X.

CPU Interface

The CL-GD542X connects directly to the ISA bus, E-ISA bus, MicroChannel bus, or '386 and '486 bus (CL-GD5424/'26/'28/'29 only). No glue logic is required. The CL-GD542X internally decodes a 16- or 24-bit address, and responds to the applicable control lines. It executes both I/O accesses and memory accesses as either an 8- or 16-bit device.

CPU Write Buffer

The CPU Write Buffer contains a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. Maintaining a queue allows the CL-GD542X to release the CPU as soon as it has recorded the address and data, and to execute the operation when display memory is available, increasing CPU performance.

Graphics Controller

The Graphics Controller is located between the CPU interface and the Memory Sequencer. It performs text manipulation, data rotation, color mapping, and other miscellaneous operations.

BitBLT

This is a unique GUI acceleration feature in the CL-GD5426/'28/'29. The BitBLT function moves data with ROPs (raster operations). This operation occurs in Packed-pixel modes with 8-, 16-, or 24-bit-per-pixel transfers. Color expansion can be used to translate monochrome images to 8- or 16-bit color. The source or destination of a BitBLT operation can be system memory.

Memory Arbitrator

The Memory Arbitrator allocates bandwidth to the four functions that compete for the limited bandwidth of display memory. These are CPU access, screen refresh, DRAM refresh, and BitBLT operations. DRAM refresh is handled invisibly by allocating a selectable number of CAS*-before-RAS* refresh cycles at the beginning of each scanline. Screen refresh and CPU/BitBLT accesses are allocated cycles according to the FIFO-control parameters, with priority given to screen refreshes.

Memory Sequencer

The Memory Sequencer generates timing for display memory. This includes RAS*, CAS* and multiplexed-address timing, as well as WE* and OE* timing. The Sequencer generates CAS*-before-RAS* refresh cycles, Random Read and Random Early Write cycles, and Fast-page mode Read and Early Write cycles. The Memory Sequencer generates multiple-CAS* or multiple-WE* signals according to the memory type used.

CRT Controller

The CRT controller generates the HSYNC and VSYNC Signals required for the monitor, as well as the BLANK* signals required by the palette DAC.

Video FIFO

The Video FIFO allows the Memory Sequencer to execute the display memory accesses needed for screen refresh at maximum memory speed rather than at the screen refresh rate. This makes it possible to collect the accesses for screen refresh near the beginning of the scanline, and to execute them in Fast-page mode rather than Random Read mode.

Attribute Controller

The Attribute Controller formats the display for the screen. Display color selection, text blinking and underlining are performed by the Attribute Controller. Alternate font selection also occurs in the Attribute Controller.

Palette DAC

The palette DAC block contains the color palette and three 8-bit digital-to-analog converters. The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue. The CL-GD5425 (only) supports YCrCb and AccuPak-to-RGB conversion.

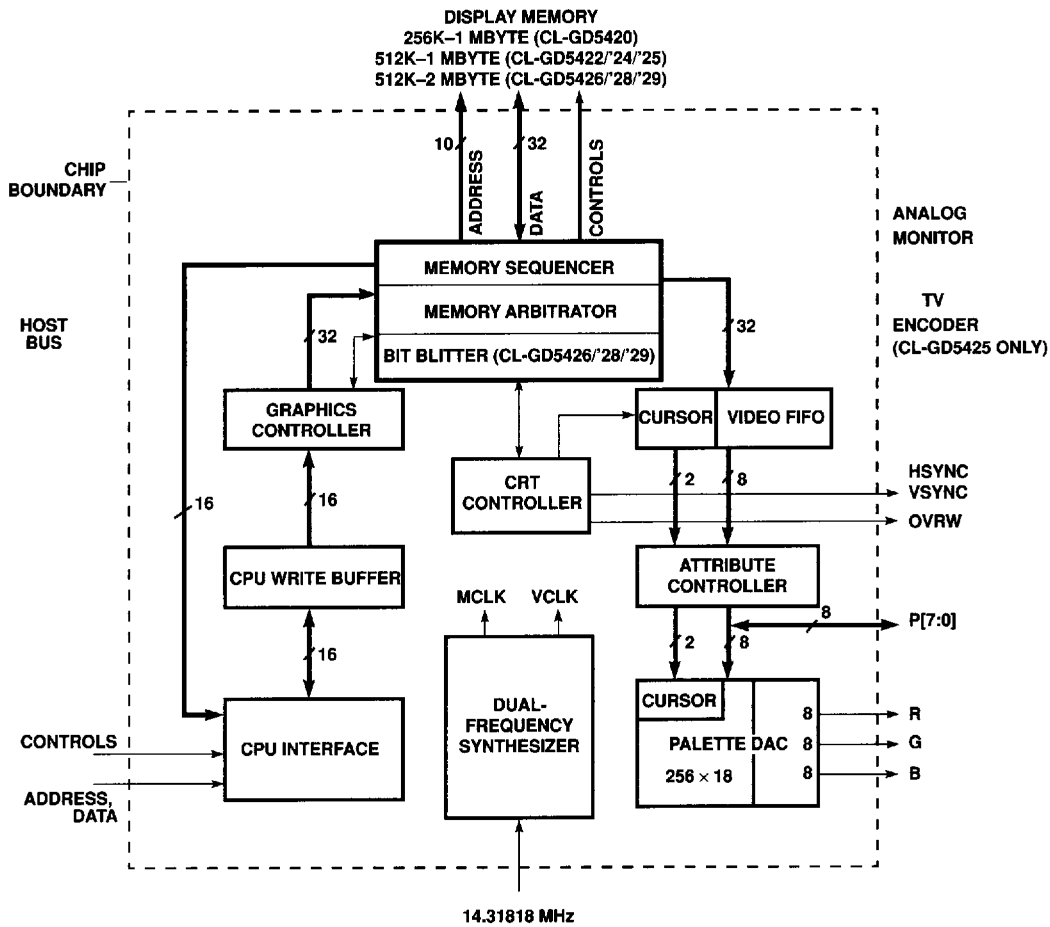


Figure 3-1. CL-GD542X Chip Block Diagram

Alternatively, the CL-GD542X (excluding the CL-GD5420) can be configured for 15-, 16-, or 24-bit pixels. This allows 32K, 65K, or 16 million simultaneous colors to be displayed on the screen. The bits are allocated as 8-8-8 for the 16 million colors, 5-6-5 for the 64K Color mode, or five to each (red, green, and blue) DAC for the 32K Color mode.

Dual-Frequency Synthesizer

The dual-frequency synthesizer generates the Memory Sequencer Clock and the Video Display Clock from a single reference frequency. The frequency of each clock is programmable. The reference frequency can be generated with an internal crystal-controlled oscillator. Alternatively, it can be supplied from an external TTL source.

VESA® Connector/VGA Pass-through Connector

The CL-GD542X is designed to connect directly to a VESA connector. It supports the three enable/disable inputs, and the Pixel bus can directly drive the connector. Through this connector, the overlay feature could be used in multimedia applications. This allows for internal DAC utilization in 16-bit-per-pixel mode. The CL-GD5425/'29 supports the VAFC (VESA Advanced Feature Connector) Baseline for Video Overlay.

TV Encoder (CL-GD5425 only)

The CL-GD5425 provides integrated scaling, flicker reduction, and a glueless encoder interface that delivers high-quality TV display at the lowest possible cost without the need for additional frame or line stores.

The programmable flicker-reduction function reduces interlaced artifacts inherent in computer-generated images displayed on interlaced TV monitors. The degree of filtering is selectable by the end-user.

3.3 Functional Operation

The four major operations handled by the CL-GD542X are discussed below.

CPU Access to Registers

The host can be any processor controlling an ISA, E-ISA, MicroChannel, or '386 and '486 local bus. It accesses CL-GD542X registers by setting up 16- or 24-bit addresses and making controls such as IORD* or IOWR* active. The CL-GD542X can respond either as an 8- or 16-bit peripheral, depending on how the chip has been designed into the system.

DRAM and screen refresh occur concurrently with, and independently of, register access (unless the host is changing display parameters or has suppressed refresh). Registers are described in detail in the *True Color VGA Family — CL-GD542X Technical Reference Manual.*

CPU Access to Display Memory

All host accesses to display memory are handled by the CL-GD542X. The host first sets up certain parameters, such as color and write masks, then generates a memory access in the range where the CL-GD542X is programmed to respond.

Display Memory Refresh

The CL-GD542X automatically generates a selectable number of CAS*-before-RAS* refresh cycles during each horizontal timing period.

Screen Refresh

The CRT monitor requires a near-constant rewriting since its only memory is the phosphor persistence. This persistence is typically only a few milliseconds. The CL-GD542X fetches information from the display memory for each scanline as quickly as possible, using Fast-page mode cycles to fill the Video FIFO. This allows the maximum possible time for the host to access the display memory.

3.4 Performance

The CL-GD542X is designed with the following performance-enhancing features:

- Accelerated Microsoft Windows with BitBLT (CL-GD5426/'28/'29 only)
- 16-bit CPU interface to I/O registers for faster host access
- 16-bit CPU interface to display memory for faster host access in all modes, including Planar mode
- 32-bit display memory data bus for faster access to display memory (CL-GD5422/'24/'25/'26/'28/'29)
- DRAM Fast-page mode operations for faster access to display memory
- Zero-wait-state performance and a CPU write buffer allows faster CPU access for writes to display memory
- Video FIFO to minimize memory contention
- 32 × 32 and 64 × 64 hardware cursor to improve Microsoft Windows performance
- Increased throughput with '386 and '486 local bus interface (CL-GD5424/'25/'26/'28/'29)

3.5 Compatibility

The CL-GD542X includes all registers and data paths required for VGA controllers.

The CL-GD542X supports extensions to VGA, including 1024 × 768 × 256 interlaced and non-interlaced, and 1280 × 1024 × 256 interlaced modes. Additionally, various 132-column text modes are supported.

3.6 Board Testability

The CL-GD542X chip is testable, even when installed on a PC board. By using pin scan testing, any IC signal pins not connected to the board or shorted to a neighboring pin or trace, will be detected. The Signature Generator allows the entire system, including the display memory, to be tested at speed. For further information on pin scan testing and the Signal Generator, refer to Appendixes B11 and B13 in the *True Color VGA Family — CL-GD542X Technical Reference Manual.*

4. CL-GD542X CONFIGURATION TABLES

4.1 Video Modes

Table 4-1. Standard VGA Modes

Mode No.	VESA® Mode No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Horiz. Freq. kHz	Vert. Freq. Hz
00/01	–	16/256	40 × 25	8 × 8	320 × 200	Text	31.5	70
00*/01*	–	16/256	40 × 25	8 × 14	320 × 350	Text	31.5	70
00+/01+	–	16/256	40 × 25	9 × 16	360 × 400	Text	31.5	70
02/03	–	16/256	80 × 25	8 × 8	640 × 200	Text	31.5	70
02*/03*	–	16/256	80 × 25	8 × 14	640 × 350	Text	31.5	70
02+/03+	–	16/256	80 × 25	9 × 16	720 × 400	Text	31.5	70
04/05	–	4/256	40 × 25	8 × 8	320 × 200	Graphics	31.5	70
6	–	2/256	80 × 25	8 × 8	640 × 200	Graphics	31.5	70
07*	–	Monochrome	80 × 25	9 × 14	720 × 350	Text	31.5	70
07+	–	Monochrome	80 × 25	9 × 16	720 × 400	Text	31.5	70
0D	–	16/256	40 × 25	8 × 8	320 × 200	Graphics	31.5	70
0E	–	16/256	80 × 25	8 × 8	640 × 200	Graphics	31.5	70
0F	–	Monochrome	80 × 25	8 × 14	640 × 350	Graphics	31.5	70
10	–	16/256	80 × 25	8 × 14	640 × 350	Graphics	31.5	70
11	–	2/256	80 × 30	8 × 16	640 × 480	Graphics	31.5	60
11+	–	2/256	80 × 30	8 × 16	640 × 480	Graphics	37.9	72
12	–	16/256	80 × 30	8 × 16	640 × 480	Graphics	31.5	60
12+	–	16/256	80 × 30	8 × 16	640 × 480	Graphics	37.9	72
13	–	256/256	40 × 25	8 × 8	320 × 200	Graphics	31.5	70

Table 4-2. Cirrus Logic Extended Video Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
14	–	16/256K	132 × 25	8 × 16	1056 × 400	Text	41.5	31.5	70
54	10A	16/256K	132 × 43	8 × 8	1056 × 350	Text	41.5	31.5	70
55	109	16/256K	132 × 25	8 × 14	1056 × 350	Text	41.5	31.5	70
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.8	60
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.9	60
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
5D†	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	87†
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	77	58	72
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
5E	100	256/256K	80 × 25	8 × 16	640 × 400	Graphics	25	31.5	70
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
60†	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	87†
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	77	58	72
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
64	111	64K	–	–	640 × 480	Graphics	25	31.5	60
64	111	64K	–	–	640 × 480	Graphics	31.5	37.9	72
65	114	64K	–	–	800 × 600	Graphics	36	35.2	56
65	114	64K	–	–	800 × 600	Graphics	40	37.8	60
65	114	64K	–	–	800 × 600	Graphics	50	48.1	72

Table 4-2. Cirrus Logic Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
66	110	32K‡	–	–	640 × 480	Graphics	25	31.5	60
66	110	32K‡	–	–	640 × 480	Graphics	31.5	37.9	72
67	113	32K‡	–	–	800 × 600	Graphics	36	35.2	56
67	113	32K‡	–	–	800 × 600	Graphics	40	37.8	60
67	113	32K‡	–	–	800 × 600	Graphics	50	48.1	72
68†	116	32K‡	–	–	1024 × 768	Graphics	44.9	35.5	87†
6C†	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	87†
6D†	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	87†
71	112	16M	–	–	640 × 480	Graphics	25	31.5	60
74†	117	64K	–	–	1024 × 768	Graphics	44.9	35.5	87†

NOTES:

1) Some modes are not supported by all CL-GD542X controllers. Refer to the CL-GD542X data book and software release kit for the list of video modes supported by the CL-GD542X BIOS.
2) Not all monitors support all modes. The fastest vertical refresh rate for the monitor type selected will be used automatically.
3) ‡ indicates 32K Direct-Color/256-color Mixed mode.
4) '†' indicates Interlaced mode.

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Table 4-3. NTSC TV Video Modes (CL-GD5425 only)

Mode No.	Colors	Screen Format	Char. × Row	Char. Cell	Display Mode	Note
00/01	16/256K	320 × 200	40 × 25	8 × 8	Text	–
02/03	16/256K	640 × 200	80 × 25	8 × 8	Text	–
04/05	4/256K	320 × 200	40 × 25	8 × 8	Graphics	Double scanned
06	2/256K	640 × 200	80 × 25	8 × 8	Graphics	Double scanned
0D	16/256K	320 × 200	40 × 25	8 × 8	Graphics	Double scanned
0E	16/256K	640 × 200	80 × 25	8 × 8	Graphics	Double scanned
10	16/256K	640 × 350	80 × 25	8 × 14	Graphics	7:8 expansion
11/12	16/256K	640 × 480	80 × 30	8 × 16	Graphics	6:5 scale
13	256/256K	320 × 200	40 × 25	8 × 8	Graphics	Double scanned
5E	256/256K	640 x 400	80 x 25	8 x 16	Graphics	–
5F	256/256K	640 × 480	80 × 30	8 × 16	Graphics	6:5 scale
64	64K	640 × 480	–	–	Graphics	6:5 scale
7A	64K	640 × 400	–	–	Graphics	–

Table 4-4. PAL TV Video Modes (CL-GD5425 only)

Mode No.	Colors	Screen Format	Char. × Row	Char. Cell	Display Mode	Note
00/01	16/256K	320 × 200	40 × 25	8 × 8	Text	5:6 expansion
02/03	16/256K	640 × 200	80 × 25	8 × 8	Text	5:6 expansion
04/05	4/256K	320 × 200	40 × 25	8 × 8	Graphics	Double Scanned 5:6 expansion
06	2/256K	640 × 200	80 × 25	8 × 8	Graphics	Double Scanned 5:6 expansion
0D	16/256K	320 × 200	40 × 25	8 × 8	Graphics	Double scanned 5:6 expansion
0E	16/256K	640 × 200	80 × 25	8 × 8	Graphics	Double scanned 5:6 expansion
10	16/256K	640 × 350	80 × 25	8 × 14	Graphics	5:7 expansion 490 scanlines
11/12	16/256K	640 × 480	80 × 30	8 × 16	Graphics	–
13	256/256K	320 × 200	40 × 25	8 × 8	Graphics	5:6 expansion
5E	256/256K	640 x 400	80 x 25	8 x 16	Graphics	5:6 Expansion
5F	256/256K	640 × 480	80 × 30	8 × 16	Graphics	–
64	64K	640 × 480	–	–	Graphics	–
7A	64K	640 × 400	–	–	Graphics	5:6 expansion

4.2 Configuration Register, CF1

When RESET (system power-on reset) goes active, the CL-GD542X samples the levels on several of the Display Memory Data MD[x] pins. These levels are latched into a write-only configuration register (CF1). The data bits in this register are not accessible to the host CPU. The levels on the Memory Data bus are, by default, a logic '1' during power-on reset due to internal 250-kΩ pull-up resistors. A logic '0' is achieved by installing an external 6.8-kΩ pull-down resistor on the memory data line corresponding to the appropriate bit in the Configuration register. The following table identifies the Configuration register bits and the particular VGA function enabled by the latched level on the Memory Data bus during power-on reset.

Table 4-5. Configuration Register Bits

CF Bits	Level	Description	Memory Data Bit	Pin Number
15	0 1	Source VCLK on MCLK pin (CL-GD5425/'29) Source MCLK on MCLK pin (CL-GD5425/'29)	MD31	97
14, 7, 5	000 001 010 011 100 101 110 111	Reserved '386DX local bus (CL-GD5424/'25/'26/'28/'29) '386SX local bus (CL-GD5424/'25/'26/'28/'29) '486SX/DX local bus (CL-GD5424/'25/'26/'28) VESA® VL-Bus™ > 33 MHz (CL-GD5425/'29) MicroChannel® bus VESA® VL-Bus™ (CL-GD5424/'25/'26/'28/'29) ISA bus	MD30, 23, 21	98, 108, 110
13	0 1	Asymmetric DRAM (Not CL-GD5425) Symmetric DRAM IREF Adjust (CL-GD5425)	MD29	99
12	0 1	CAS[3:0]*, single-WE* (Reserved in CL-GD5420/'25) WE[3:0]*, single-CAS*	MD28	100
11	0 1	7-MCLK RAS* cycle 6-MCLK RAS* cycle	MD27	102
10,9	00 01 10 11	50.11363-MHz MCLK (Reserved in CL-GD5425) 44.74431-MHz MCLK 41.16477-MHz MCLK 37.58523-MHz MCLK	MD26, 25	103, 104
8	0 1	64K ROM BIOS @ C0000–CFFFF 32K ROM BIOS @ C0000–C7FFF	MD24	105
6	0 1	16-bit BIOS ROM (ISA bus only) (MCS16* generated for 64K or 32K) 8-bit BIOS ROM (CL-GD5424 does not generate MCS16*)	MD22	109
4	0 1	External MCLK (pin 157 is an input) (Test) Internal MCLK (pin 157 is an output)	MD20	111
3	0 1	Port 3C3h is Video System Sleep register Port 46E8h is Video System Sleep register	MD19	112
2		Reserved	MD18	113
1	0 1 0 1	Zero wait enabled (except CL-GD5425/'29) Zero wait disabled (except CL-GD5425/'29) Disable NTSC Black-Level offset (CL-GD5425) Enable NTSC Black-Level offset (CL-GD5425)	MD17	114
0	0 1	XTAL, OSC configured for two ref (CL-GD5425) XTAL, OSC configured for one ref (CL-GD5425)	MD16	115

4.3 Host Interface Signals

With the pin connections listed below, the CL-GD542X will interface directly to an ISA, MicroChannel, or local bus.

Table 4-6. Bus Connections

CL-GD542X Pin	ISA Bus	MicroChannel® Bus	'386SX	'386DX	'486	VESA® VL-Bus™
[45..42], [39..29]	SA[16:2]	A[16:2]	A[16:2]	A[16:2]	A[16:2]	A[16:2]
28	SA1	A1	A1	BE3#	BE3#	BE3#
27	SA0	A0	BLE#	BE2#	BE2#	BE2#
[21..15]	LA[23:17]	A[23:17]	A[23:17]	A[23:17]	A[23:17]	A[23:17]
[11..8], [6..3]	SD[15:8]	D[15:8]	D[15:8]	D[15:8]	D[15:8]†	D[15:8]†
[63..62], [60..59], [57..54]	SD[7:0]	D[7:0]	D[7:0]	D[7:0]	D[7:0]†	D[7:0]†
24	SBHE*	–SBHE	BHE#	BE1#	BE1#	BE1#
25	BALE	MADE24	ADS#	ADS#	ADS#	ADS#
46	AEN	–CD_SETUP	CPU-Reset	CPU-Reset	Ground	RDYRTN#
49	IOR*	–S1	W/R#	W/R#	W/R#	W/R#
50	IOW*	–CMD	CLK2X	CLK2X	CLK1X	CLK1X
14	MEMR*	M/-IO	M/IO#	M/IO#	M/IO#	M/IO#
13	MEMW*	–S0	(unused)	UADDR#	UADDR#	UADDR#
41	RESET	CHRESET	RESET	RESET	RESET	RESET
48	REFRESH	–REFRESH	(unused)	BE0#	BE0#	BE0#
23	MCS16*	–CD_DS16	(unused)	BS16#	BS16#	BS16#
51	0WS*	(unused)	GROUND	GROUND	GROUN D	GROUND
52	IRQ	–IRQ	INTR	INTR	INTR	INTR
47	IOCHRDY	CD_CHRDY	READY#	READY#	RDY#	RDY#
22	IOCS16*	–CD_SFDBK	LBA#	LBA#	LBA#	LBA#
159	OSC	OSC	OSC	OSC	OSC	OSC
2	EROM*	EROM*	EROM*	EROM*	EROM*	EROM*

NOTES:

1) For ISA-bus applications, note that SA[19..17] are not found on the CL-GD542X; this means that an adapter board will only function in a 16-bit slot.
2) The OSC and EROM* pins are common in all configurations.
3) The OSC pin is an input for 14.31818 MHz.
4) † Data lines D[15:0] connect to external, data-steering transceiver.

5. VGA REGISTER PORT MAP

Table 5-1. VGA Register Port Map

Address	Port
94	POS 102 Access Control (3C3 sleep)
102	POS102 register
3B4	CRT Controller Index (R/W — monochrome)
3B5	CRT Controller Data (R/W — monochrome)
3BA	Feature Control (W), Input Status register 1 (R — monochrome)
3C0	Attribute Controller Index/Data (Write)
3C1	Attribute Controller Index/Data (Read)
3C2	Miscellaneous Output (W), Input Status register 0 (R)
3C3	MotherBoard Sleep
3C4	Sequencer Index (R/W)
3C5	Sequencer Data (R/W)
3C6	Video DAC Pixel Mask (R/W), Hidden DAC register (R/W)
3C7	Pixel Address Read mode (W), DAC State (R)
3C8	Pixel Mask Write mode (R/W)
3C9	Pixel Data (R/W)
3CA	Feature Control Readback (R)
3CC	Miscellaneous Output Readback (R)
3CE	Graphics Controller Index (R/W)
3CF	Graphics Controller Data (R/W)
3D4	CRT Controller Index (R/W — color)
3D5	CRT Controller Data (R/W — color)
3DA	Feature Control (W), Input Status register 1 (R — color)
46E8	Adapter Sleep

6. CL-GD542X REGISTERS

Table 6-1. External/General Registers

Abbreviation	Register Name	Index	Port
102 Access	POS 94: 102 Access Control	–	94
POS102	POS102	–	102
VSSM	Motherboard Sleep Address *(CL-GD5424/'25/'26/'28/'29 only)*	–	3C3
VSSM	Adapter Sleep	–	46E8
MISC	Miscellaneous Output	–	3C2 (Write)
MISC	Miscellaneous Output	–	3CC (Read)
FC	Feature Control	–	3?A (Write)[a]
FC	Feature Control	–	3CA (Read)
FEAT	Input Status Register 0	–	3C2
STAT	Input Status Register 1	–	3?A
3C6	Pixel Mask	–	3C6
3C7	Pixel Address Read Mode	–	3C7 (Write)
3C7	DAC State	–	3C7 (Read)
3C8	Pixel Address Write Mode	–	3C8
3C9	Pixel Data	–	3C9

[a] '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

Table 6-2. VGA Sequencer Registers

Abbreviation	Register Name	Index	Port
SRX	Sequencer Index	–	3C4
SR0	Reset	0	3C5
SR1	Clocking Mode	1	3C5
SR2	Plane Mask	2	3C5
SR3	Character Map Select	3	3C5
SR4	Memory Mode	4	3C5

Table 6-3. CRT Controller Registers

Abbreviation	Register Name	Index	Port
CRX	CRTC Index	–	3?4[a]
CR0	Horizontal Total	0	3?5
CR1	Horizontal Display End	1	3?5
CR2	Horizontal Blanking Start	2	3?5
CR3	Horizontal Blanking End	3	3?5
CR4	Horizontal Sync Start	4	3?5
CR5	Horizontal Sync End	5	3?5
CR6	Vertical Total	6	3?5
CR7	Overflow	7	3?5
CR8	Screen A Preset Row Scan	8	3?5
CR9	Character Cell Height	9	3?5
CRA	Text Cursor Start	A	3?5
CRB	Text Cursor End	B	3?5
CRC	Screen Start Address High	C	3?5
CRD	Screen Start Address Low	D	3?5
CRE	Text Cursor Location High	E	3?5
CRF	Text Cursor Location Low	F	3?5
CR10	Vertical Sync Start	10	3?5
CR11	Vertical Sync End	11	3?5
CR12	Vertical Display End	12	3?5
CR13	Offset	13	3?5
CR14	Underline Row Scanline	14	3?5
CR15	Vertical Blanking Start	15	3?5
CR16	Vertical Blanking End	16	3?5
CR17	Mode Control	17	3?5
CR18	Line Compare	18	3?5
CR22	Graphics Data Latches Readback	22	3?5
CR24	Attribute Controller Toggle Readback	24	3?5
CR26	Attribute Controller Index Readback	26	3?5

[a] '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

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Table 6-4. VGA Graphics Controller Registers

Abbreviation	Register Name	Index	Port
GRX	Graphics Controller Index	–	3CE
GR0	Set/Reset	0	3CF
GR1	Set/Reset Enable	1	3CF
GR2	Color Compare	2	3CF
GR3	Data Rotate	3	3CF
GR4	Read Map Select	4	3CF
GR5	Mode	5	3CF
GR6	Miscellaneous	6	3CF
GR7	Color Don't Care	7	3CF
GR8	Bit Mask	8	3CF

Table 6-5. VGA Attribute Controller Registers

Abbreviation	Register Name	Index	Port
ARX	Attribute Controller Index	–	3C0/3C1
AR0-ARF	Attribute Controller Palette	0:F	3C0/3C1
AR10	Attribute Controller Mode	10	3C0/3C1
AR11	Overscan (Border) Color	11	3C0/3C1
AR12	Color Plane Enable	12	3C0/3C1
AR13	Pixel Panning	13	3C0/3C1
AR14	Color Select	14	3C0/3C1

Table 6-6. Extension Registers

Abbreviation	Register Name	Index	Port
SR2	Enable Writing Pixel Extension	2	3C5
SR6	Unlock ALL Extensions	6	3C5
SR7	Extended Sequencer Mode	7	3C5
SR8	EEPROM Control	8	3C5
SR9	Scratch-Pad 0	9	3C5
SRA	Scratch-Pad 1	A	3C5
SRB	VCLK0 Numerator	B	3C5
SRC	VCLK1 Numerator	C	3C5
SRD	VCLK2 Numerator	D	3C5
SRE	VCLK3 Numerator	E	3C5
SRF	DRAM Control	F	3C5
SR10	Graphics Cursor Y Position	10	3C5
SR11	Graphics Cursor X Position	11	3C5
SR12	Graphics Cursor Attributes	12	3C5
SR13	Graphics Cursor Pattern Address Offset	13	3C5
SR14	Scratch-Pad 2 *(CL-GD5425/'26/'28/'29 only)*	14	3C5
SR15	Scratch-Pad 3 *(CL-GD5425/'26/'28/'29 only)*	15	3C5
SR16	Performance Tuning *(CL-GD5424/'25/'26/'28/'29 only)*	16	3C5
SR17	Configuration Readback and Extended Control *(except CL-GD5420)*	17	3C5
SR18	Signature Generator Control *(except CL-GD5420)*	18	3C5
SR19	Signature Generator Result Low Byte *(except CL-GD5420)*	19	3C5
SR1A	Signature Generator Result High Byte *(except CL-GD5420)*	1A	3C5
SR1B	VCLK0 Denominator and Post-Scalar Value	1B	3C5
SR1C	VCLK1 Denominator and Post-Scalar Value	1C	3C5
SR1D	VCLK2 Denominator and Post-Scalar Value	1D	3C5
SR1E	VCLK3 Denominator and Post-Scalar Value	1E	3C5
SR1F	BIOS ROM Write Enable and MCLK Select	1F	3C5
GR0	Write Mode 5 Background Extension	0	3CF
GR1	Write Mode 4, 5 Foreground Extension	1	3CF
GR9	Offset Register 0	9	3CF
GRA	Offset Register 1	A	3CF

Table 6-6. Extension Registers *(cont.)*

Abbreviation	Register Name	Index	Port
GRB	Graphics Controller Mode Extensions	B	3CF
GRC	Color Key *(CL-GD5424/'25/'26/'28/'29 only)*	C	3CF
GRD	Color Key Mask *(CL-GD5424/'25/'26/'28/'29 only)*	D	3CF
GRE	Miscellaneous Control *(CL-GD5425/'28/'29 only)*	E	3CF
GR10	16-bit Pixel BG Color High Byte *(except CL-GD5420)*	10	3CF
GR11	16-bit Pixel FG Color High Byte *(except CL-GD5420)*	11	3CF
GR18	Extended DRAM Controls *(CL-GD5429 only)*	18	3CF
CR19	Interlace End	19	3?5[a]
CR1A	Miscellaneous Control	1A	3?5
CR1B	Extended Display Controls	1B	3?5
CR1C	Sync Adjust and GENLOCK *(CL-GD5425 only)*	1C	3?5
CR1D	Overlay Mode Controls *(CL-GD5425/'29 only)*	1D	3?5
CR25	Part Status	25	3?5
CR27	ID	27	3?5
CR30	TV-Out Mode Control *(CL-GD5425 only)*	30	3?5
HDR	Hidden DAC *(except CL-GD5420)*	–	3C6

[a] '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

Table 6-7. CL-GD5426/'28/'29 BitBLT Registers

Abbreviation	Register Name	Index	Port
GR20	BLT Width Low	20	3CF
GR21	BLT Width High	21	3CF
GR22	BLT Height Low	22	3CF
GR23	BLT Height High	23	3CF
GR24	BLT Destination Pitch Low	24	3CF
GR25	BLT Destination Pitch High	25	3CF
GR26	BLT Source Pitch Low	26	3CF
GR27	BLT Source Pitch High	27	3CF
GR28	BLT Destination Start Low	28	3CF
GR29	BLT Destination Start Mid	29	3CF
GR2A	BLT Destination Start High	2A	3CF

Table 6-7. CL-GD5426/'28/'29 BitBLT Registers *(cont.)*

Abbreviation	Register Name	Index	Port
GR2C	BLT Source Start Low	2C	3CF
GR2D	BLT Source Start Mid	2D	3CF
GR2E	BLT Source Start High	2E	3CF
GR2F	BLT Write Mask Destination *(CL-GD5429 only)*	2F	3CF
GR30	BLT Mode	30	3CF
GR31	BLT Start/Status	31	3CF
GR32	BLT Raster Operation	32	3CF
GR34	Transparent Color Select Low *(except CL-GD5429)*	34	3CF
GR35	Transparent Color Select High *(except CL-GD5429)*	35	3CF
GR38	Transparent Color Mask Low *(except CL-GD5429)*	38	3CF
GR39	Transparent Color Mask High *(except CL-GD5429)*	39	3CF

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient temperature under bias	0° to 70° C
Storage temperature	–65° to 150° C
Voltage on any pin	V_{SS} –0.5 V to V_{CC} + 0.5 V
Operating power dissipation	1.5 Watts
Power supply voltage	7 Volts
Injection current (latch-up testing)	100 mA

NOTE: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

7.2 DC Specifications (Digital)

(V_{CC} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
V_{CC}	Power Supply Voltage	4.75	5.25	Volts	Normal Operation	
V_{IL}	Input Low Voltage	0	0.8	Volts		
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	Volts		
V_{OL}	Output Low Voltage		0.5	Volts	I_{OL} = 4 mA	1
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = 400 µA	2
I_{CC}	Supply Current				V_{CC} Nominal	3
I_{IH}	Input High Current		10	µA	V_{IL} = V_{DD}	
I_{IL}	Input Low Current	–10		µA	V_{DD} = 5.25, V_{IL} = 0	
I_{IHP}	Input High Current (pull-up)	–10	10	µA	V_{IL} = V_{DD}	
I_{ILP}	Input Low Current (pull-up)	–45	–12	µA	V_{DD} = 5.25, V_{IL} = 0	
I_{OZ}	Input Leakage	–10	10	µA	0 < V_{IN} < V_{CC}	
C_{IN}	Input Capacitance		10	pF		4
C_{OUT}	Output Capacitance		10	pF		4

NOTES:

1) I_{OL} is specified for a standard buffer. See the pin summary for further information.
2) I_{OH} is specified for a standard buffer. See the pin summary for further information.
3) I_{CC} is measured with VCLK and MCLK as indicated in the table below:

Part Number	VCLK	MCLK	I_{CC}
CL-GD5420	75 MHz	50 MHz	250 mA
CL-GD5422	80 MHz	50 MHz	260 mA
CL-GD5424/'25	80 MHz	50 MHz	260 mA
CL-GD5426/'28	80 MHz	50 MHz	260 mA
CL-GD5429	86 MHz	70 MHz	310 mA

4) This is not 100% tested, but is periodically sampled.

7.3 DC Specifications (Palette DAC)

(V_{CC} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
A_{VDD}	DAC Supply Voltage	4.75	5.25	Volts	Normal Operation	
I_{REF}	DAC Reference Current	–3	–10	mA		1

NOTE: See the Detailed Pin Description for information regarding nominal I_{REF}.

7.4 DC Specifications (Frequency Synthesizer)

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
A_{VDD}	Synthesizer Supply Voltage	4.75	5.25	Volts		

7.5 DAC Characteristics

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
R	Resolution	8	Max	Bits		
IO	Output Current	30	Max	mA	VO < 1V	
TR	Analog Output Rise/Fall Time	8	Max	ns		2, 3, 4
TS	Analog Output Settling Time	15	Max	ns		2, 3, 5
TSK	Analog Output Skew	tbd	Max	ns		2, 3, 6
DT	DAC-to-DAC Correlation	2.5	Max	%		6, 7
GI	Glitch Impulse		Typical	pV-sec.		2, 3, 6
IL	Integral Linearity	1.5	Max	LSB		
DL	Differential Lineaity	1.5	Max	LSB		

NOTES:

1) TD is measured from the 50% point of VCLK to the 50% point of full-scale transition.
2) Load is 50 Ω and 30 pF per analog output.
3) I_{REF} = –6.67 mA.
4) TR is measured from 10% to 90% full-scale.
5) TS is measured from 50% of full-scale transition to the output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the mid-point of the distribution of the three DACs measured at full-scale output.

7.6 List of Waveforms

Table/Figure **Title** **Page**

Table 7-1. I/O Write Timing (ISA Bus) [a]

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* setup to IOW* active	5	–	ns
t_2	IOW* pulse width	40	–	ns
t_3	Data setup to IOW* inactive	5	–	ns
t_4	Data hold from IOW* inactive	10	–	ns
t_5	Address, SBHE* hold from IOW* inactive	5	–	ns
t_6	IOW* inactive to any command active	80	–	ns

[a] AEN must be inactive.

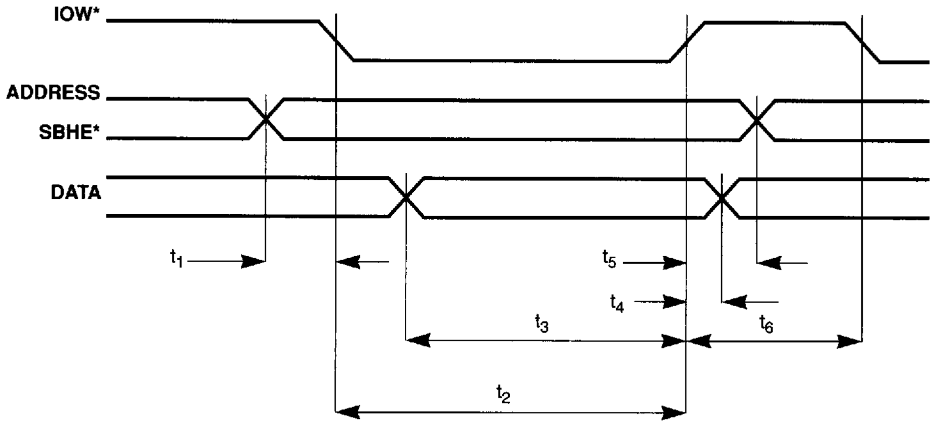


Figure 7-1. I/O Write Timing (ISA Bus)

Table 7-2. I/O Read Timing (ISA Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* setup to IOR* active	5	–	ns
t_2	IOR* active to low-impedance delay	0	–	ns
t_3	Data delay from IOR* active (IOR* access time)	–	60	ns
t_4	IOR* pulse width	70	–	ns
t_5	Data hold from IOR* inactive	0	20	ns
t_6	Address, SBHE* hold from IOR* inactive	0	–	ns
t_7	IOR* inactive to high-impedance delay	0	20	ns

[a] AEN must be inactive.

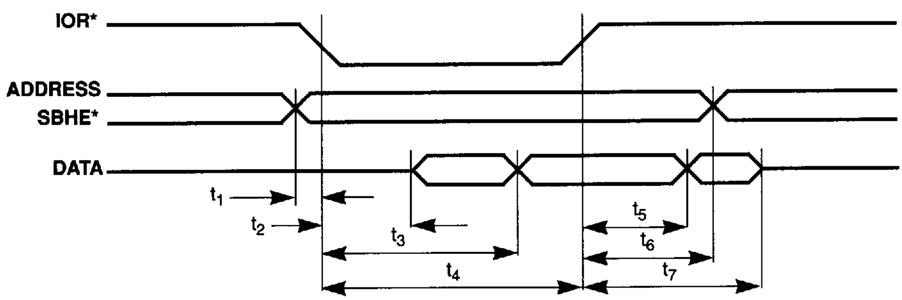


Figure 7-2. I/O Read Timing (ISA Bus)

Table 7-3. Memory Write Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* to SMEMW* active setup	5	–	ns
t_2	SMEMW* pulse width	3	–	m[a]
t_3	Data valid from SMEMW* active	–	3	m
t_4	Data hold from SMEMW* inactive	10	–	ns
t_5	Address, SBHE* hold from SMEMW* inactive	0	–	ns
t_6	SMEMW* inactive to next SMEMW*	3	–	m

[a] m = MCLK period.

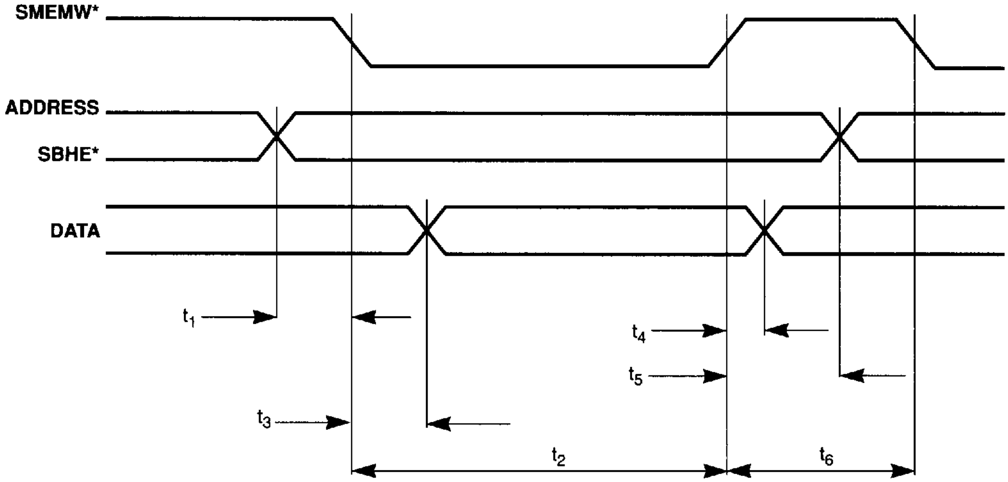


Figure 7-3. Memory Write Timing (ISA Bus)

Table 7-4. Memory Read Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* to SMEMR* active	5	–	ns
t_2	SMEMR* active to low-impedance delay	0	–	ns
t_3	Data delay from IOCHRDY active	–	15	ns
t_4	SMEMR* pulse width	–	[a]	ns
t_5	Data hold from SMEMR* inactive	0	20	ns
t_6	Address, SBHE* hold from SMEMR* inactive	0	–	ns
t_7	SMEMR* inactive to high-impedance delay	–	20	ns

[a] SMEMR* active-pulse width is determined by IOCHRDY.

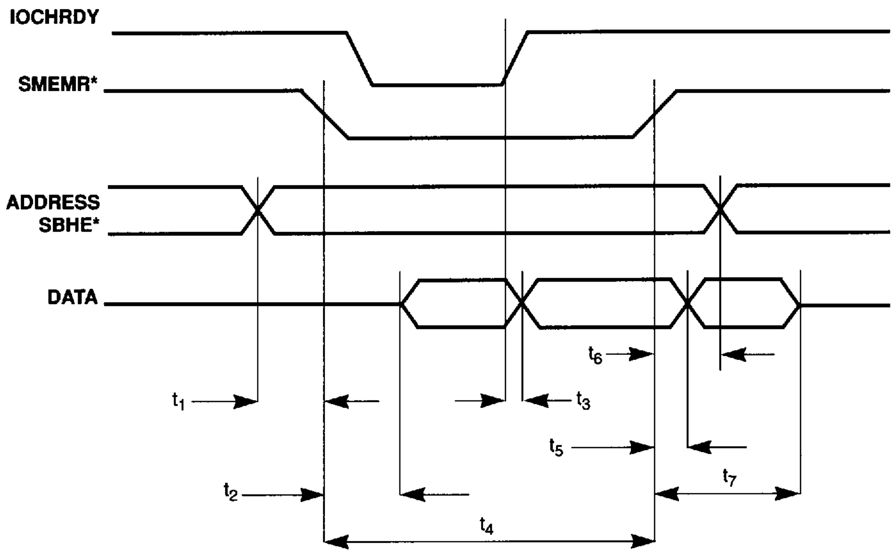


Figure 7-4. Memory Read Timing (ISA Bus)

Table 7-5. MCS16* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_{1a}	MCS16* active delay from LA[23:17] valid	–	20	ns
t_{1b}	MCS16* active delay from SA[16:15] valid	–	14	ns
t_2	MCS16* inactive delay from address invalid	–	25	ns

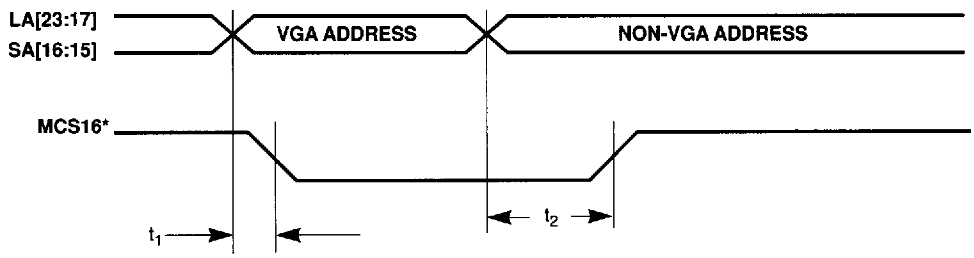


Figure 7-5. MCS16* Timing (ISA Bus)

Table 7-6. IOCS16* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	IOCS16* active delay from address	–	25	ns
t_2	IOCS16* inactive delay from address	–	30	ns

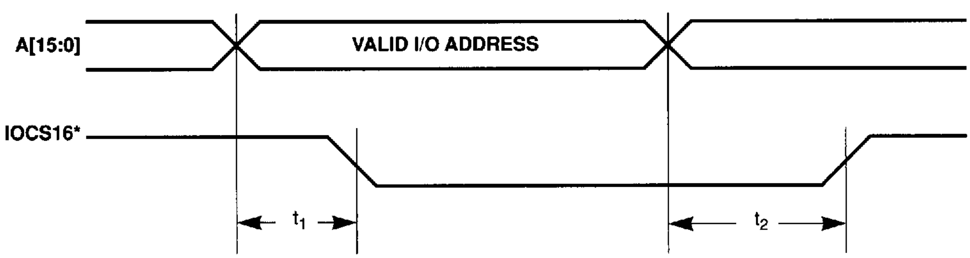


Figure 7-6. IOCS16* Timing (ISA Bus)

Table 7-7. BALE Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	LA[23:17] setup to BALE negative transition	20	–	ns
t_2	SBHE* setup to BALE negative transition	20	–	ns
t_3	LA[23:17] hold from BALE negative transition	20	–	ns
t_4	SBHE* hold from BALE negative transition	20	–	ns
t_5	BALE pulse width	20	–	ns

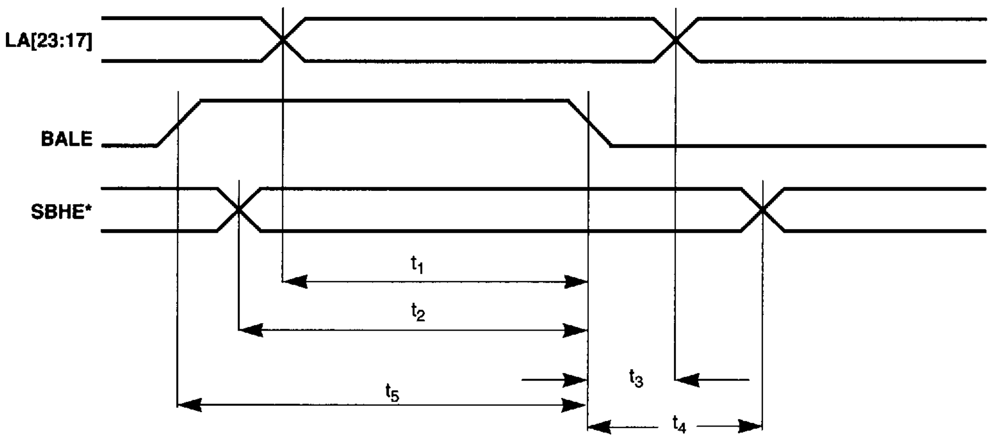


Figure 7-7. BALE Timing (ISA Bus)

Table 7-8. IOCHRDY for Memory Access Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	SMEMR* or SMEMW* active to IOCHRDY inactive low	–	28	ns
t_2	IOCHRDY inactive low pulse width	10	[a]	ns

[a] Video mode dependent.

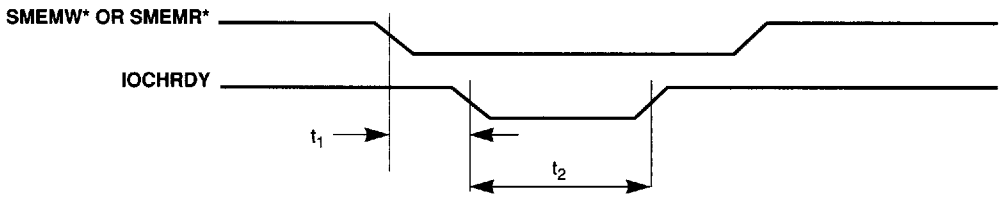


Figure 7-8. IOCHRDY for Memory Access Timing (ISA Bus)

Table 7-9. 0WS* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_{1a}	0WS* active delay from SMEMR* (BIOS ACCESS)	–	22	ns
t_{1b}	0WS* active delay from SMEMW* (display memory write)	–	18	ns
t_{2a}	0WS* high-impedance delay from SMEMR*	–	18	ns
t_{2b}	0WS* high-impedance delay from SMEMW*	–	19	ns

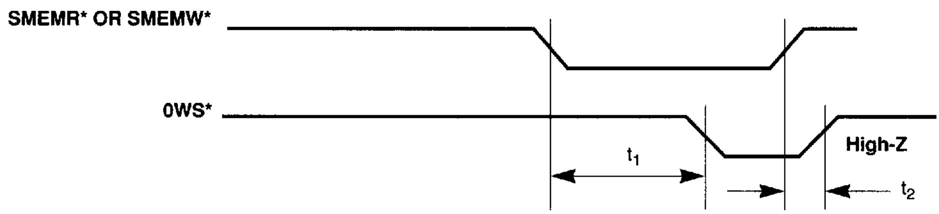


Figure 7-9. 0WS* Timing (ISA Bus)

Table 7-10. Refresh Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	REFRESH* active setup to SMEMR* active	20	–	ns
t_2	REFRESH* active hold from SMEMR* active	0	–	ns

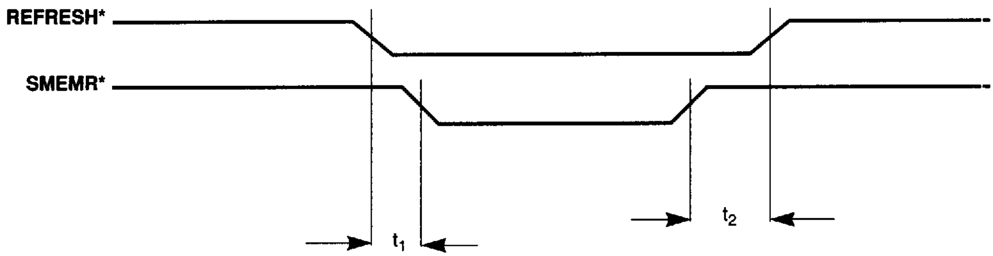


Figure 7-10. Refresh Timing (ISA Bus)

Table 7-11. EROM* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	EROM* active delay from SMEMR* active	–	30	ns
t_2	EROM* inactive delay from SMEMR* inactive	–	20	ns

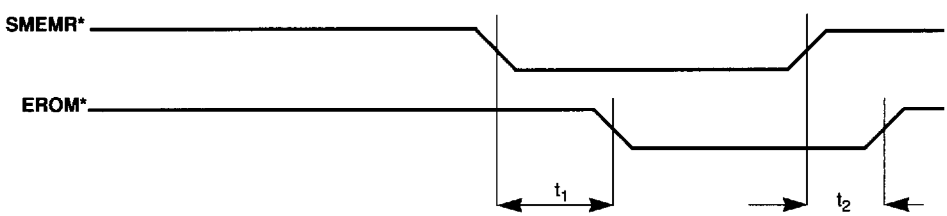


Figure 7-11. EROM* Timing (ISA Bus)

Table 7-12. AEN Timing (ISA Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	AEN setup to IOR* or IOW* active	5	–	ns
t_2	AEN hold from IOR* or IOW* inactive	5	–	ns

[a] AEN high, as shown below, will cause the CL-GD542X to **ignore** the I/O cycle.

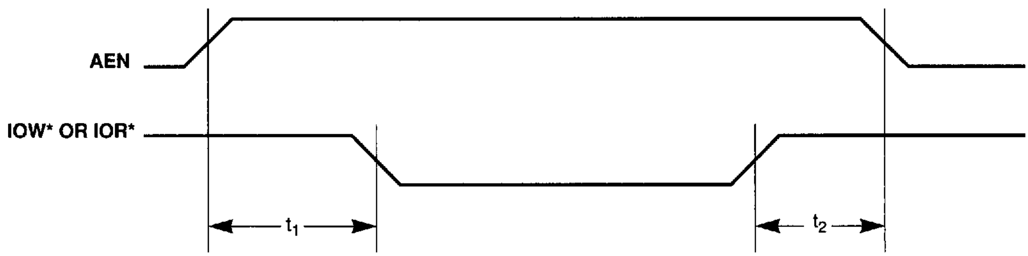


Figure 7-12. AEN Timing (ISA Bus)

Table 7-13. Write Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Data to –CMD active setup	–15	–	ns
t_{2a}	–CMD active pulse width (default cycle)	90	–	ns
t_{2b}	–CMD active pulse width (synchronous extended cycle)	190	–	ns
t_{2c}	–CMD active pulse width (asynchronous extended cycle)	[a]	[a]	ns
t_3	Data hold from –CMD inactive	0	–	ns
t_4	CD_CHRDY active to –CMD inactive delay	0	–	ns

[a] The maximum t_{2c} depends on display memory activity.

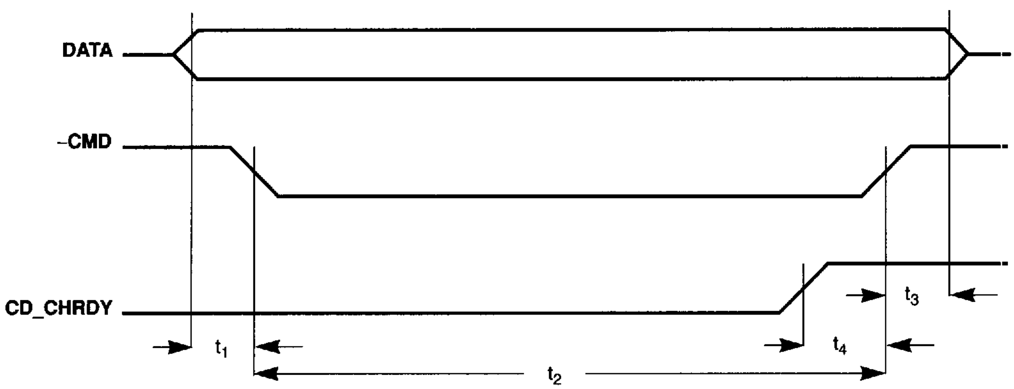


Figure 7-13. Write Timing (MicroChannel® Bus)

Table 7-14. Read Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	–CMD active to DATA valid delay (default cycle) (I/O read)	–	45	ns
t_2	CD_CHRDY active to DATA valid delay (memory read cycle)	–	45	ns
t_3	READ DATA hold from –CMD inactive	0	–	ns
t_4	READ DATA high-impedance from –CMD inactive	–	30	ns

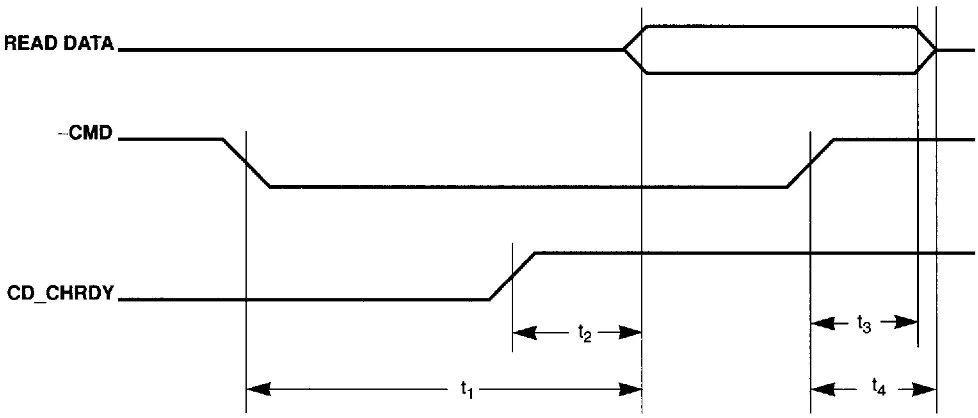


Figure 7-14. Read Timing (MicroChannel® Bus)

Table 7-15. –CD_DS16 Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	–CD_DS16 active from address, M/-IO, MADE24 valid	0	50	ns

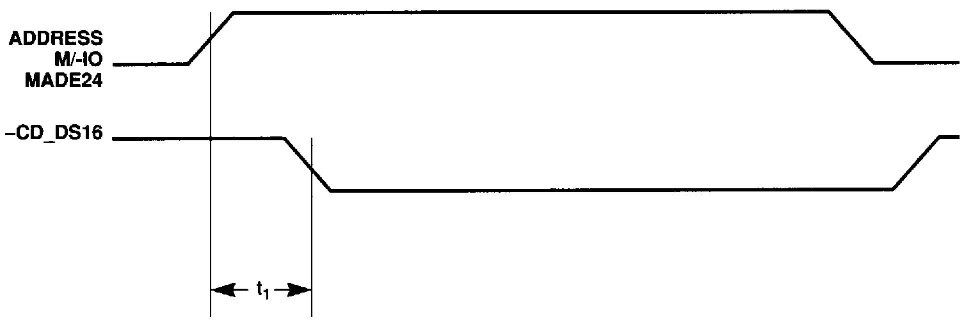


Figure 7-15. –CD_DS16 Timing (MicroChannel® Bus)

Table 7-16. –CMD Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Address valid setup to –CMD active	80	–	ns
t_2	Status active setup to –CMD active	50	–	ns
t_3	–SBHE valid setup to –CMD active	35	–	ns
t_4	–CMD pulse width	90	–	ns
t_5	Address, –SBHE hold from –CMD active	25	–	ns
t_6	Status hold from –CMD active	25	–	ns

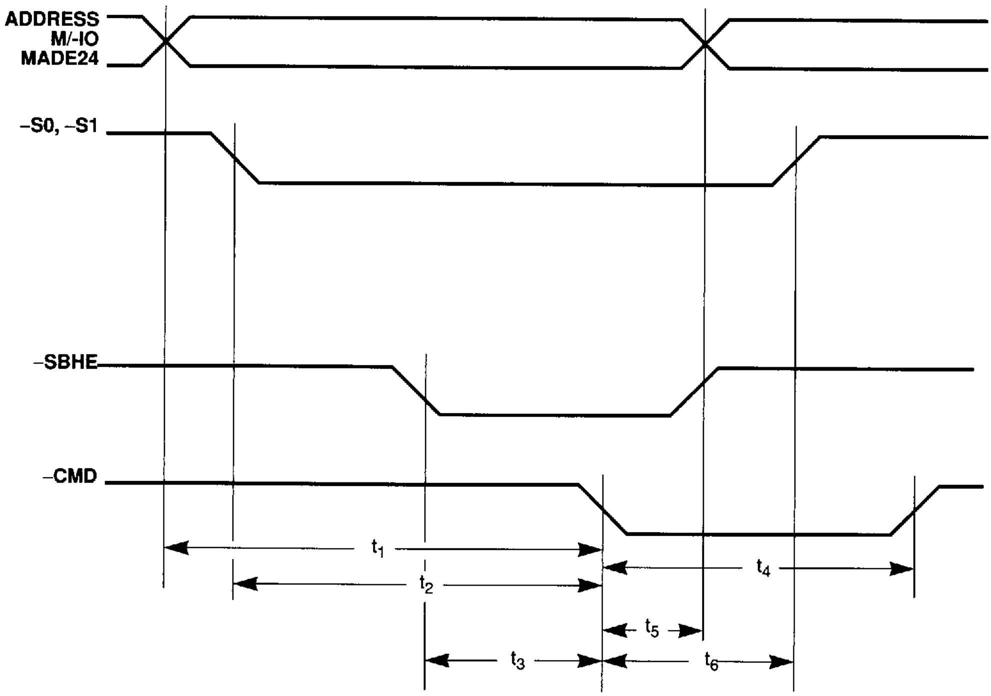


Figure 7-16. –CMD Timing (MicroChannel® Bus)

Table 7-17. CD_CHRDY Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	CD_CHRDY inactive (low) from Address valid	–	50	ns
t_2	CD_CHRDY inactive (low) from Status active	–	25	ns
t_3	CD_CHRDY inactive (low) pulse width	–	3.5	ms

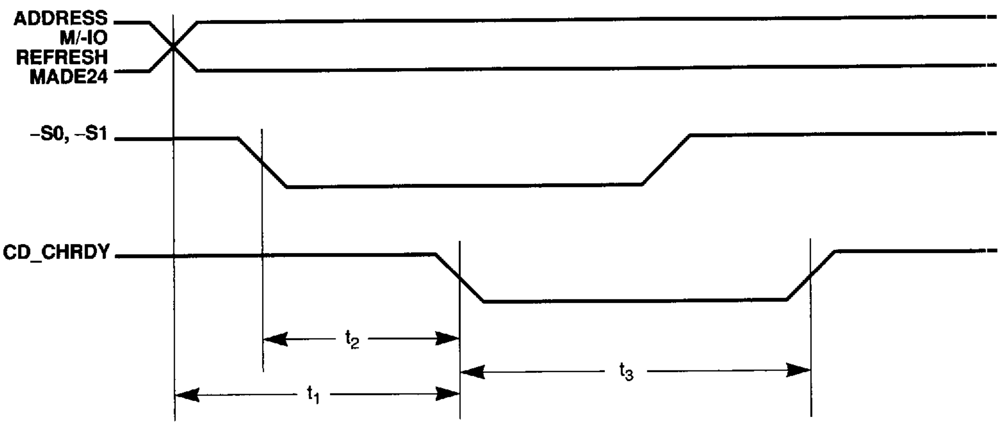


Figure 7-17. CD_CHRDY Timing (MicroChannel® Bus)

Table 7-18. –REFRESH Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	–REFRESH setup to –Status active	5	–	ns
t_2	–REFRESH setup to –CMD active	40	–	ns
t_3	–REFRESH hold from –CMD active	25	–	ns

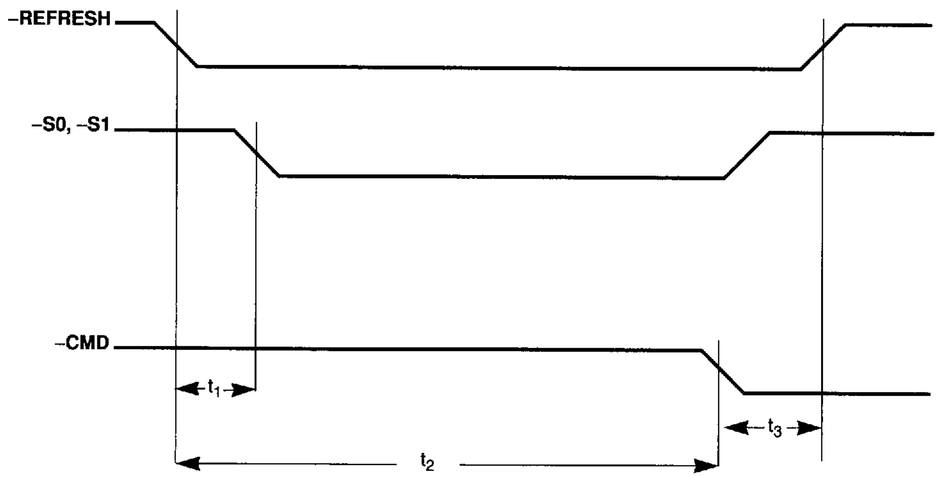


Figure 7-18. –Refresh Timing (MicroChannel® Bus)

Table 7-19. –EROM Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	–CMD active to –EROM active	–	30	ns
t_2	–CMD inactive to –EROM inactive	0	30	ns

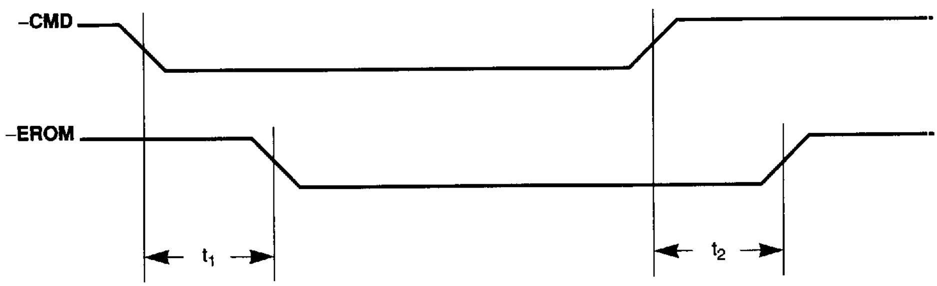


Figure 7-19. –EROM Timing (MicroChannel® Bus)

Table 7-20. –CD_SFDBK Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, M/-IO, MADE24 valid to –CD_SFDBK active delay	–	55	ns
t_2	Address, M/-IO, MADE24 invalid to –CD_SFDBK inactive delay	0	–	ns

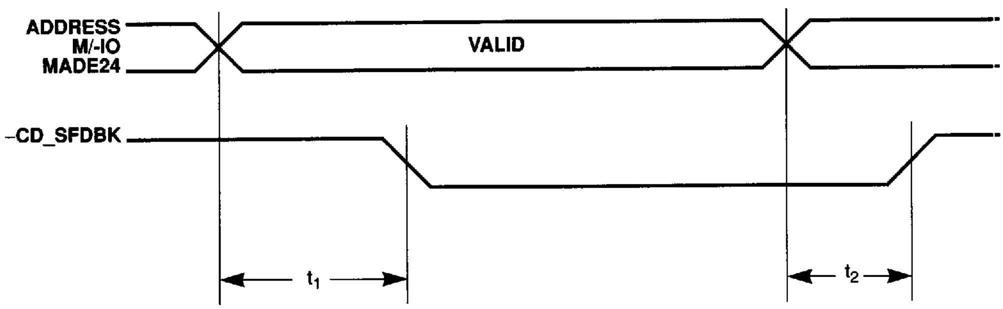


Figure 7-20. –CD_SFDBK Timing (MicroChannel® Bus)

Table 7-21. –CD_SETUP Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	–CD_SETUP active setup to –CMD active	10	–	ns
t_2	–CD_SETUP delay to CD_CHRDY inactive	–	95	ns
t_3	–CMD active to –CD_SETUP inactive hold	25	–	ns

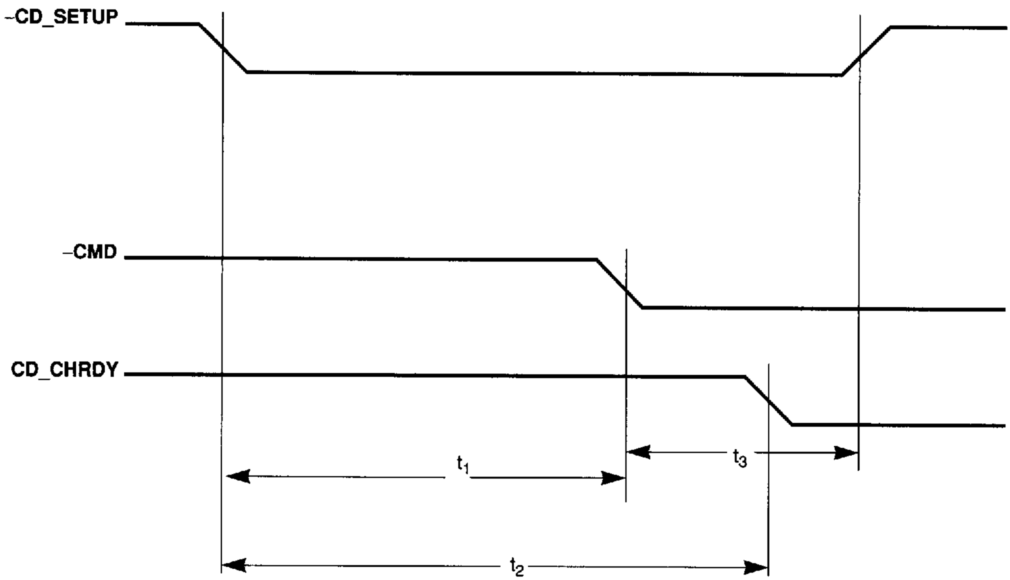


Figure 7-21. –CD_SETUP Timing (MicroChannel® Bus)

Table 7-22. CLK1X, CLK2X Timing (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Rise time (CLK1X) '486 (V_{IL} - V_{IH})	–	4	ns
t_2	Fall time (CLK1X) '486 (V_{IH} - V_{IL})	–	4	ns
t_3	High period (CLK1X) '486 (V_{IH} - V_{IH})	40	60	% t_5
t_4	Low period (CLK1X) '486 (V_{IL} - V_{IL})	40	60	% t_5
t_5	Period (CLK1X) '486	25	–	ns
t_5	Period (CLK1X) '486 (CL-GD5429)	20	–	ns
t_1	Rise time (CLK2X) '386 (V_{IL} - V_{IH})	–	4	ns
t_2	Fall time (CLK2X) '386 (V_{IH} - V_{IL})	–	4	ns
t_3	High period (CLK2X) '386 (V_{IH} - V_{IH})	40	60	% t_5
t_4	Low period (CLK2X) '386 (V_{IL} - V_{IL})	40	60	% t_5
t_5	Period (CLK2X) '386	12.5	–	ns

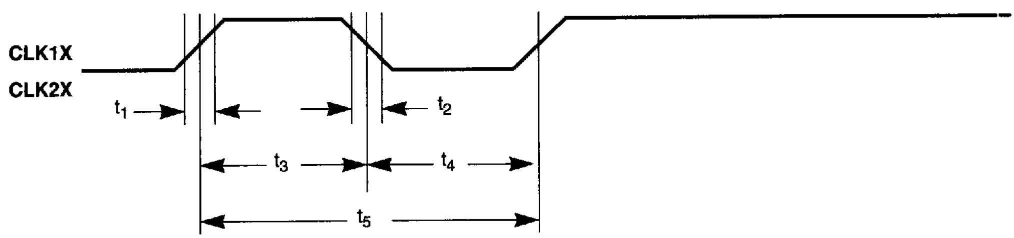


Figure 7-22. CLK1X, CLK2X Timing (Local Bus)

Table 7-23. RESET Timing (Local Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	CPU_RESET hold time from CLK2X	10	–	ns
t_2	CPU_RESET setup time to CLK2X	2	–	ns

[a] Applies to '386 only. For '486, pin 46 must be tied to ground. For VESA VL-Bus, pin 46 must be tied to RDYRTN#.

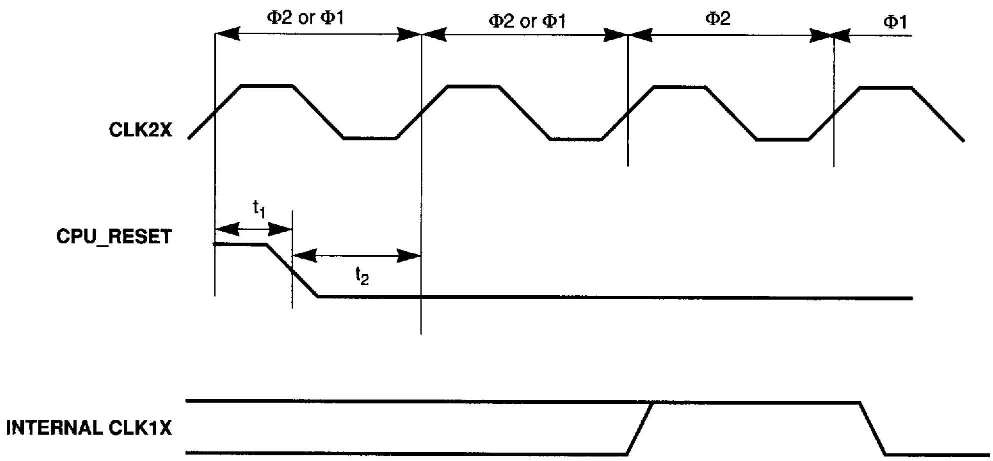


Figure 7-23. RESET Timing (Local Bus)

Table 7-24. ADS#, LBA#, BS16# Timing (Local Bus)

Symbol	Parameter	MIN '24/'26/'28	MAX '24/'26/'28	MIN '29	MAX '29	Units
t_1	Address, Status, ADS# setup to CLK1X	8	–	4	–	ns
t_2	LBA#/LDEV# active delay from Address, Status	–	15	–	15	ns
t_3	BS16# active delay CLK1X	–	15	–	3	ns
t_4	LBA# inactive delay from Address, Status	–	18	–	18	ns

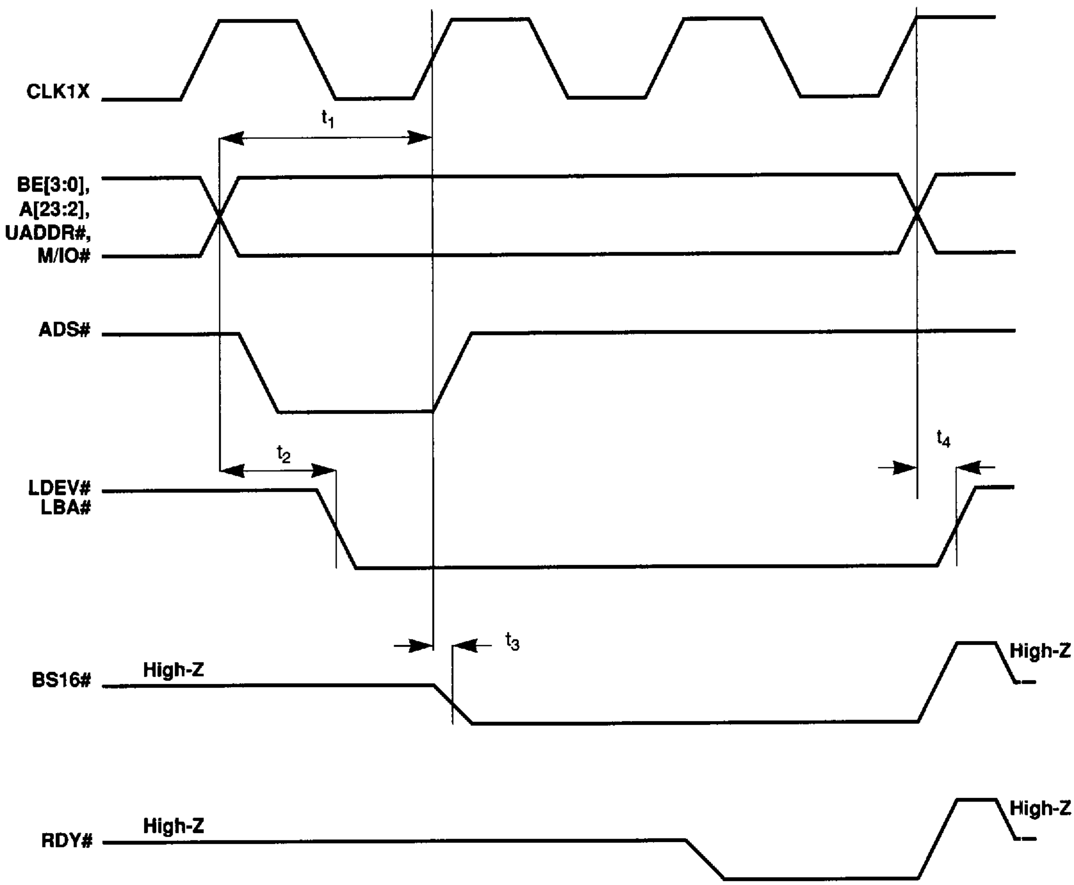


Figure 7-24. ADS#, LBA#, BS16# Timing (Local Bus)

Table 7-25. RDY# Delay (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	RDY# active delay from CLK1X	3	13	ns
t_2	RDY# inactive delay from CLK1X	–	23	ns
t_3	RDY# high before High-Z	–	1/2	CLK1X

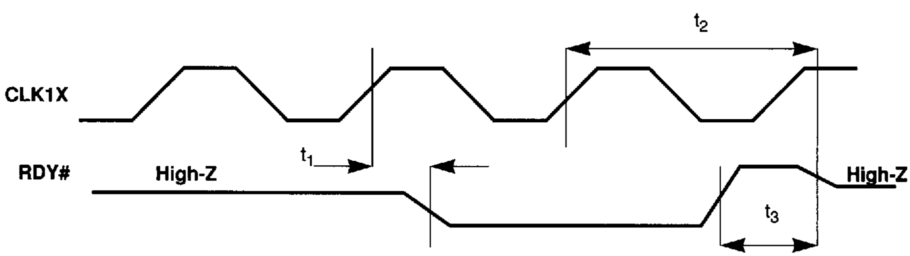


Figure 7-25. RDY# Delay (Local Bus)

Table 7-26. Read Data Timing (Local Bus)

Symbol	Parameter	MIN '24/'26/'28	MAX '24/'26/'28	MIN '5429	MAX '5429	Units
t_1	Read data setup to RDY# active	0	–	0	–	ns
t_2	Read data hold from RDY# inactive	12	–	12	–	ns
t_3	RDYRTN# setup to CLK1X	8	–	5	–	ns
t_4	RDYRTN# hold from CLK1X	5	–	2	–	ns

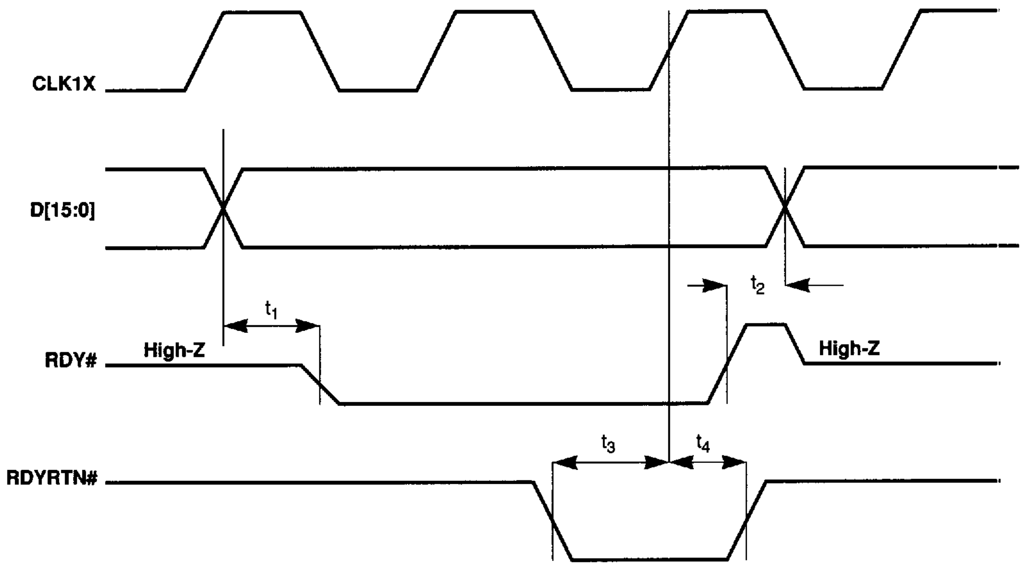
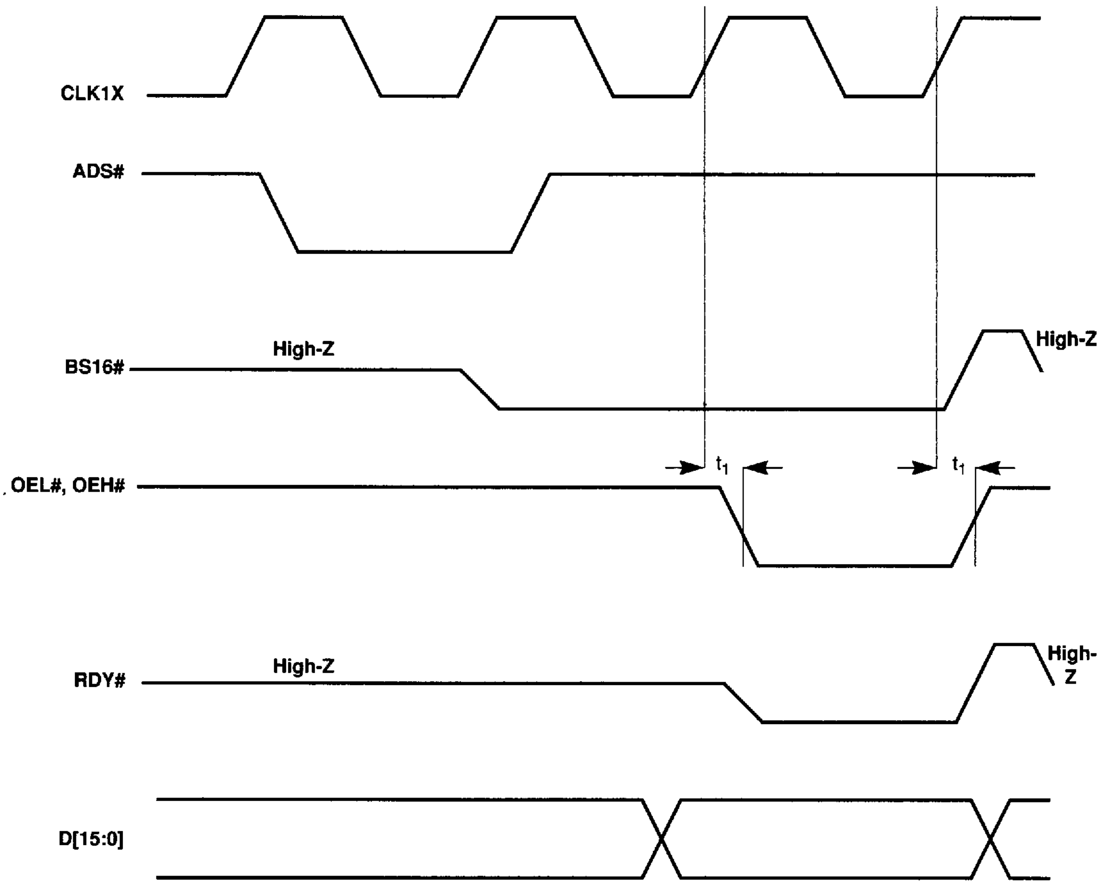


Figure 7-26. Read Data Timing (Local Bus)

Table 7-27. Buffer Control Timing – Read Cycle (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	OEL#, OEH# delay	0	14	ns

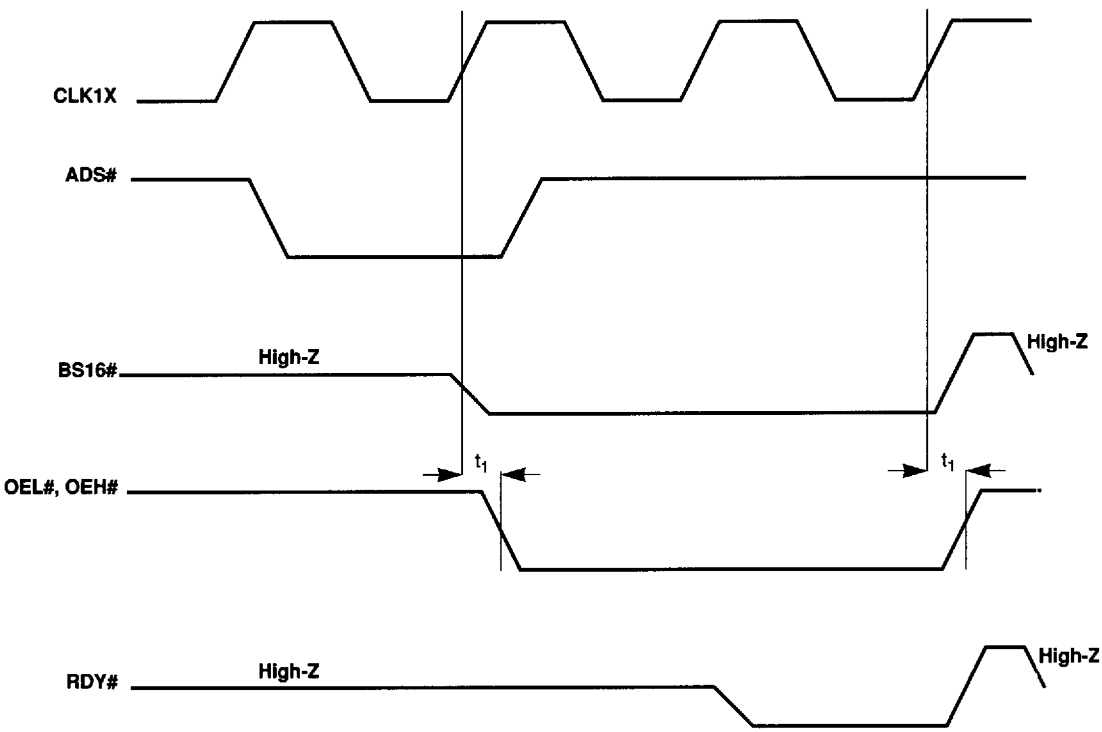


NOTE: Both OEL# and OEH# are active for read cycles.

Figure 7-27. Buffer Control Timing – Read Cycle (Local Bus)

Table 7-28. Buffer Control Timing – Write Cycle (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	OEL#, OEH# delay	0	14	ns



NOTE: Only one of OEL# and OEH# is active for write cycles.

Figure 7-28. Buffer Control Timing – Write Cycle (Local Bus)

Table 7-29. Display Memory Bus – Common Parameters

Symbol	Parameter	MIN	MAX
t_1	t_{ASR}: address setup to RAS* active	1.5m [a] – 2 ns	–
t_2	t_{RAH}: row address hold from RAS* active	1.5m	–
t_3	t_{ASC}: address setup to CAS* active	1m – 1 ns	–
t_4	t_{CAH}: column address hold from CAS* active	1m	–
t_5	t_{RCD}: RAS* active to CAS* active delay (standard RAS)	2.5m – 2 ns	–
t_5	t_{RCD}: RAS* active to CAS* active delay (extended RAS)	3m – 2 ns	–
t_6	t_{RAS}: RAS* pulse width low (standard RAS)	3.5m	–
t_6	t_{RAS}: RAS* pulse width low (extended RAS)	4m – 2 ns	–
t_7	t_{RP}: RAS* precharge (RAS* pulse width high — standard RAS)	2.5 m – 2 ns	–
t_7	t_{RP}: RAS* precharge (RAS* pulse width high — extended RAS)	3m	–
t_8	t_{CAS}: CAS* pulse width low	1m + 3 ns	1m + 6 ns
t_9	t_{CP}: CAS* precharge (CAS* pulse width high)	1m – 6 ns	1m – 3 ns
t_{10}	t_{RC}: Random cycle (standard RAS)	6m	–
t_{10}	t_{RC}: Random cycle (extended RAS)	7m	–
t_{11}	t_{PC}: Page mode cycle	2m	–

[a] m = MCLK

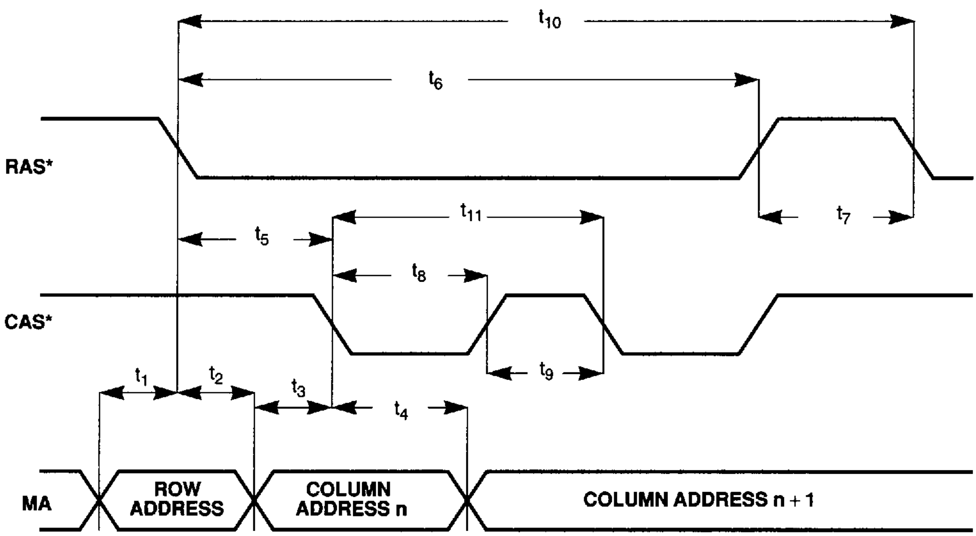


Figure 7-29. Display Memory Bus – Common Parameters

Table 7-30. Display Memory Bus – Read Cycles[a]

Symbol	Parameter	MIN	MAX
t_1	Read data setup to CAS* rising edge	0	–
t_2	Read data hold from CAS* high	10 ns	–
t_3 [b]	RAS* active to first CAS* rising edge delay (standard RAS)	–	4m – 1 ns
t_3	RAS* active to first CAS* rising edge delay (extended RAS)	–	4.5m – 1 ns
t_4 [c]	Column address valid to CAS* rising edge delay	–	2m
t_5 [d]	CAS* active pulse width	–	1m + 3 ns
t_6 [e]	CAS* period	–	2m

[a] Only parameters t_1 and t_2 are defined for the device. The remaining parameters in this table are calculated from parameters in the Table 7-29. They are provided so that system designers can determine DRAM requirements.

[b] Parameter t_3 corresponds to DRAM parameter t_{RAC} (access time from RAS*).

[c] Parameter t_4 corresponds to DRAM parameter t_{AA} (access time from column address).

[d] Parameter t_5 corresponds to DRAM parameter t_{CAC} (access time from CAS*).

[e] Parameter t_6 corresponds to DRAM parameter t_{CAP} (access time from CAS* precharge).

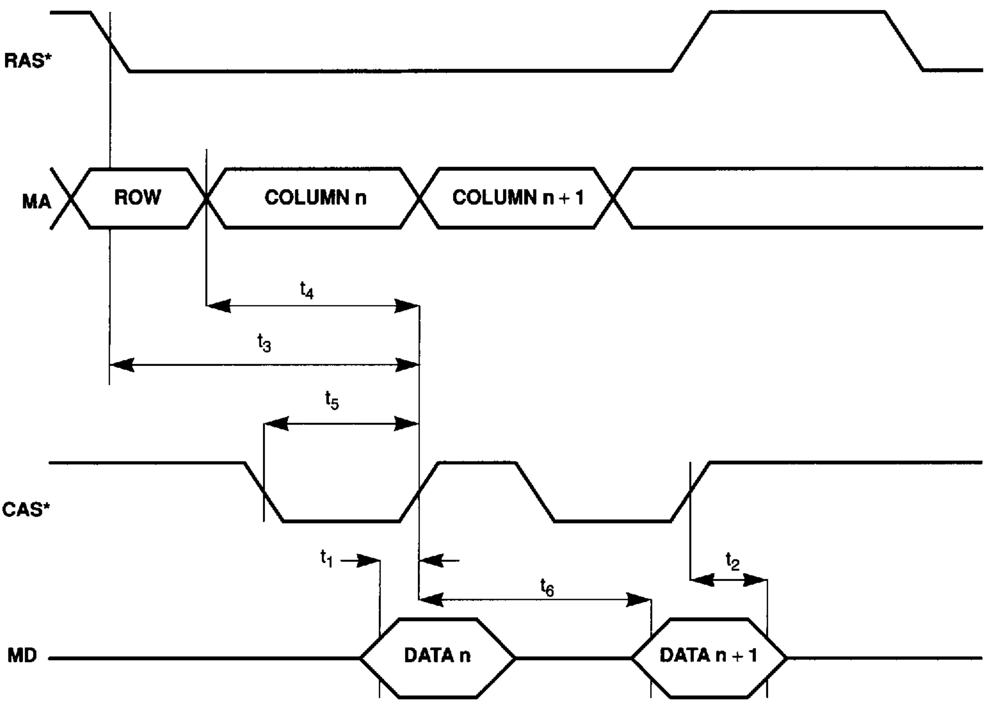


Figure 7-30. Display Memory Bus – Read Cycles

Table 7-31. Display Memory Bus – Write Cycles

Symbol	Parameter	MIN	MAX
t_1	t_{CWL}: WE* active setup to CAS* active	1m[a] + 2 ns	–
t_2	t_{DS}: Write data setup to CAS* active	1m – 2 ns	1m + 2 ns
t_3	t_{DH}: write data hold from CAS* active	1m + 1 ns	–
t4	t_{WCH}: WE active hold from CAS* active	1.5m	–

[a] m = MCLK

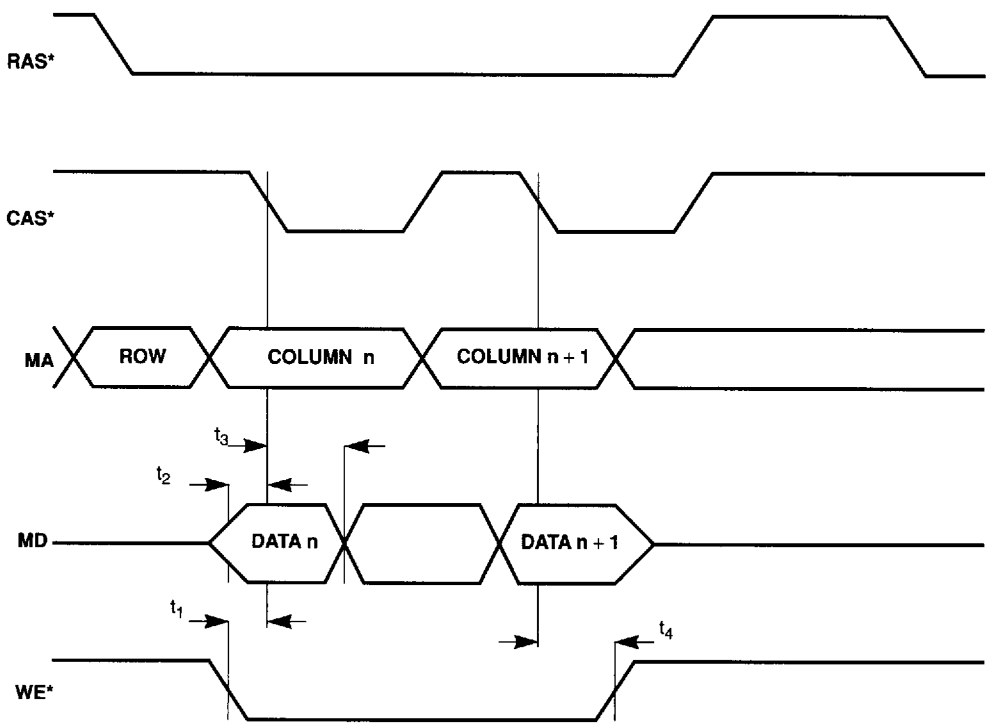


Figure 7-31. Display Memory Bus – Write Cycles

Table 7-32. CAS*-before-RAS* Refresh Timing (Display Memory Bus)[a]

Symbol	Parameter	MIN	MAX
t_1	t_{CSR}: CAS* active setup to RAS* active1	1m[b]	–
t_2	t_{RAS}: RAS* low pulse width	4m	–
t_3	t_{RP}: RAS* high pulse width	3m	–

[a] There will be either three or five RAS* pulses while CAS* remains low.
[b] m = MCLK

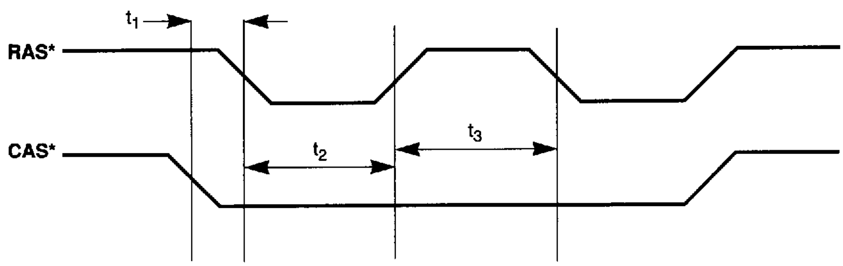


Figure 7-32. CAS*-before-RAS* Refresh Timing (Display Memory Bus)

Table 7-33. P-Bus as Inputs, 8-Bit Mode (DCLK input as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	P[7:0], BLANK* setup to DCLK	–1	–	ns
t_2	P[7:0], BLANK* hold from DCLK	7	–	ns

NOTE: CL-GD542X RAMDAC driven externally

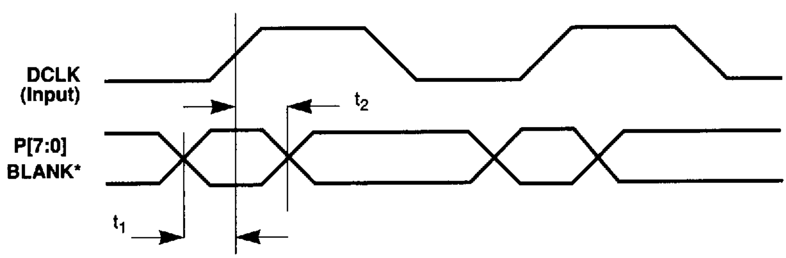


Figure 7-33. P-Bus as Inputs, 8-bit Mode (External DCLK)

Table 7-34. Feature Bus Timing, 8-Bit Mode, Outputs (DCLK output as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK to BLANK* delay	–1	1	ns
t_2	DCLK to HSYNC, VSYNC delay	1	3	ns
t_3	DCLK to P[7:0] delay	–2	0	ns
t_4	DCLK to OVRW delay	–1	1	ns

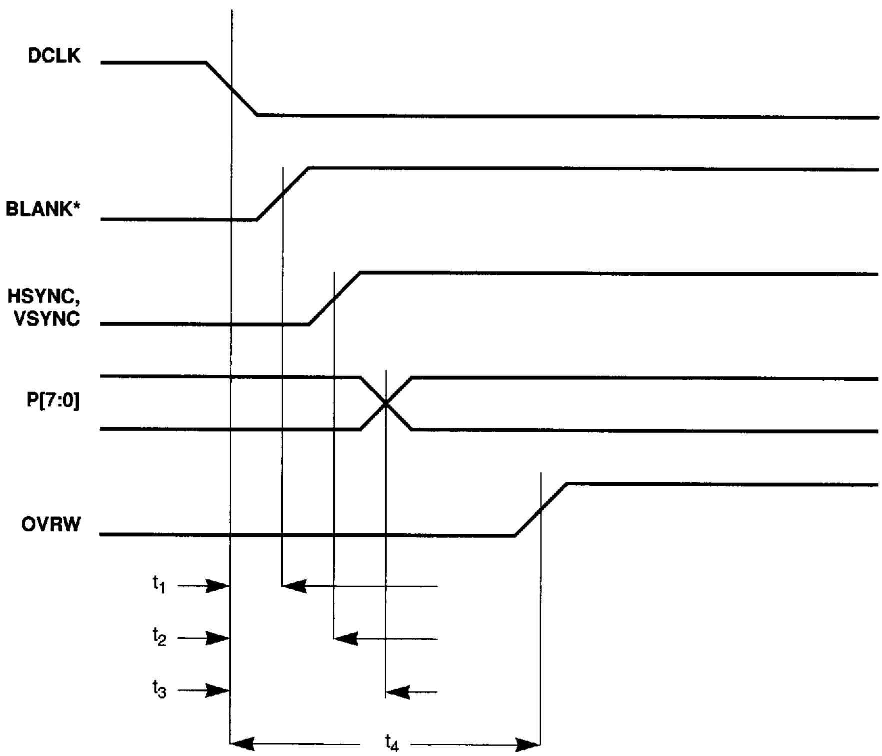


Figure 7-34. Feature Bus Timing, 8-Bit Mode, Outputs (Internal DCLK)

Table 7-35. P-Bus as Outputs, 16-bit Mode (DCLK output as reference) CL-GD5425/'28/'29 only[a]

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK (rising edge) to P[7:0] delay	–2	0	ns
t_2	DCLK (falling edge) to P[7:0] delay	–1	1	ns

[a] SR7[2:1] is programmed to '0,1' and GRE[0] is programmed to '1'.

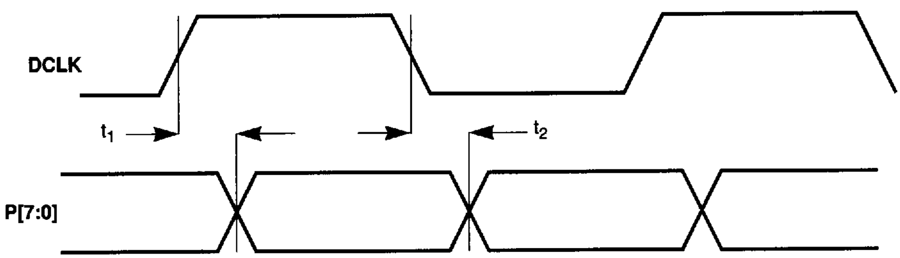


Figure 7-35. P-Bus as Outputs, 16-bit Mode (Internal DCLK) CL-GD5425/'28/'29 only

Table 7-36. P-Bus as Inputs, 16-Bit Mode, Clock Mode 1 (DCLK input as reference) [a]

Symbol	Parameter	MIN '24/'26	MIN '28	MIN '25/'29	Units
t_1	P[7:0] setup to DCLK (rising edge — external DCLK)	–1	–1	–3	ns
t_2	P[7:0] hold from DCLK (rising edge — external DCLK)	5	5	7	ns
t_3	P[7:0] setup to DCLK (falling edge — external DCLK)	–1	–1	–3	ns
t_4	P[7:0] hold from DCLK (rising edge — external DCLK)	5	5	7	ns

[a] Clock mode 1 selected in Hidden DAC register (D5 programmed to '0').

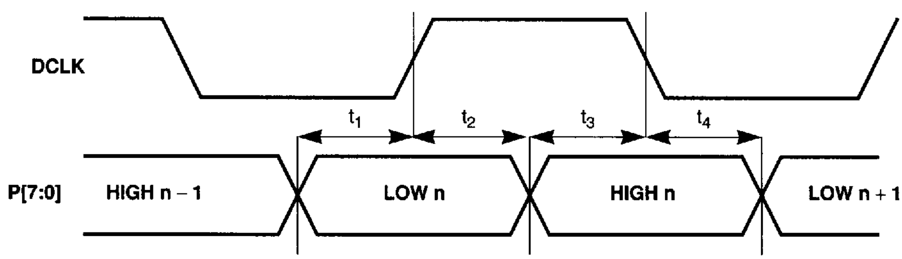


Figure 7-36. P-Bus as Inputs, 16-Bit Mode, Clock Mode 1 (External DCLK)

Table 7-37. P-Bus as Inputs, 16-Bit Mode, Clock Mode 2[a] (DCLK input as reference)

Symbol	Parameter	MIN '24/'26	MIN '28	MIN '25/'29	Units
t_1	P[7:0], BLANK*[b] setup to DCLK	–1	–2	–2	ns
t_2	P[7:0], BLANK* hold from DCLK	5	6	4	ns

[a] Clock mode 2 selected in HIdden DAC register (D5 = '1').

[b] The first low byte of 16-bit data input must be synchronized with BLANK* or the start of overlay window, whichever is later. The first high byte will be clocked on the next rising edge of DCLK.

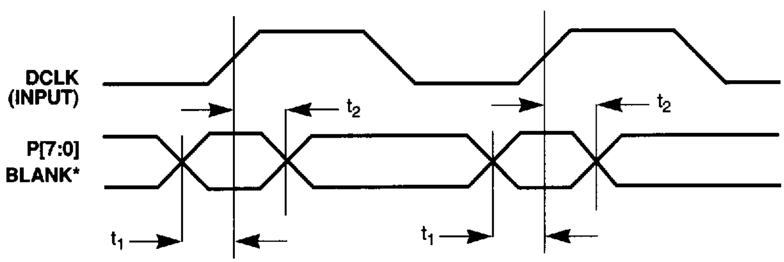


Figure 7-37. P-Bus as Inputs, 16-Bit Mode, Clock Mode 2 (External DCLK)

Table 7-38. P-Bus as Inputs, 16-Bit Mode (DCLK output as reference)[a]

Symbol	Parameter	MIN '24/'26	MIN '28	MIN '25/'29	Units
t_1	P[7:0] setup to DCLK (rising edge — internal DCLK)	3	2	3	ns
t_2	P[7:0] hold from DCLK (rising edge — internal DCLK)	1	1	1	ns
t_3	P[7:0] setup to DCLK (falling edge — internal DCLK)	3	2	3	ns
t_4	P[7:0] hold from DCLK (rising edge — internal DCLK)	1	1	1	ns

[a] Clock mode 1 selected in Hidden DAC register (D5 = '0').

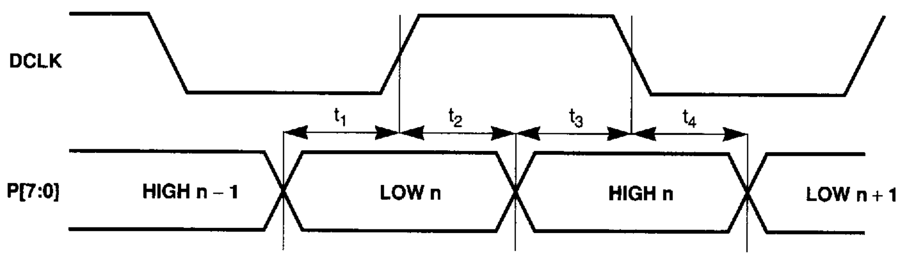


Figure 7-38. P-Bus as Inputs, 16-Bit Mode (External DCLK)

Table 7-39. DCLK as Input

Symbol	Parameter: CL-GD5420/'22/'24/'26/'28	MIN	MAX	Units
t_1	Rise time	–	3	ns
t_2	Fall time	–	3	ns
t_3	High period	40	60	% of t_5
t_4	Low period	40	60	% of t_5
t_5	Period	17	–	ns
	Parameter: CL-GD5425/'29			
t_1	Rise time	–	3	ns
t_2	Fall time	–	3	ns
t_3	High period: Clock mode 1	45	55	% of t_5
t_3	High period: Clock mode 2	30	70	% of t_5
t_4	Low period: Clock mode 1	45	55	% of t_5
t_4	Low period: Clock mode 2	30	70	% of t_5
t_5	Period (DCLK)	12.5	–	ns

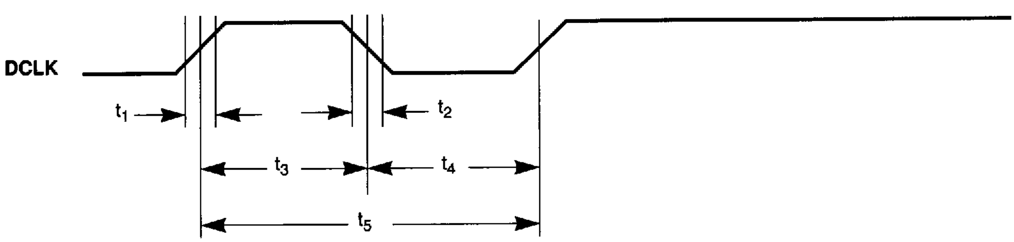


Figure 7-39. DCLK As Input

Table 7-40. RESET Timing

Symbol	Parameter	MIN	MAX	Units
t_1	RESET pulse width	12	–	MCLK
t_2	MD[31:16] setup to RESET falling edge	2	–	ns
t_3	MD[31:16] hold from RESET falling edge	25	–	ns
t_4	RESET low to first IOW*	12	–	MCLK

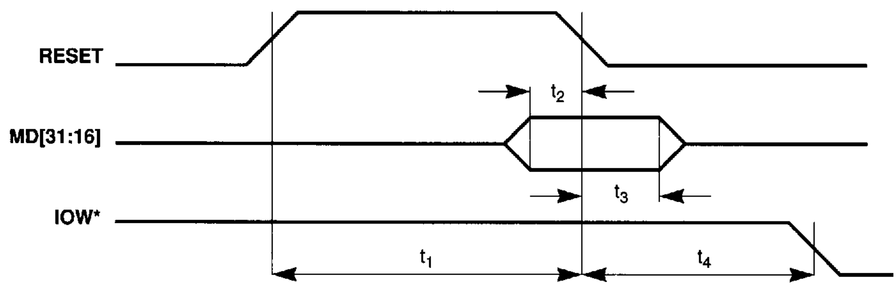


Figure 7-40. RESET Timing

Table 7-41. Horizontal Period (NTSC — CL-GD5425 only)

Symbol	Parameter	Nominal	Units
t_1	Horizontal period	63.56	µsec.
t_2	HSYNC pulse width (low)	4.65	µsec.

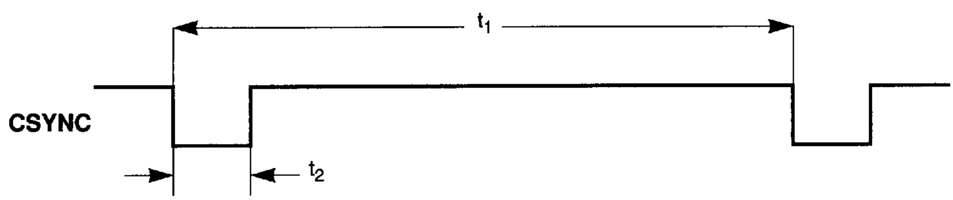


Figure 7-41. Horizontal Period (NTSC — CL-GD5425 only)

Table 7-42. NTSC Vertical Retrace (CL-GD5425 only)

Symbol	Parameter	Nominal	Units
t_1	Vertical blanking period	20	H-period

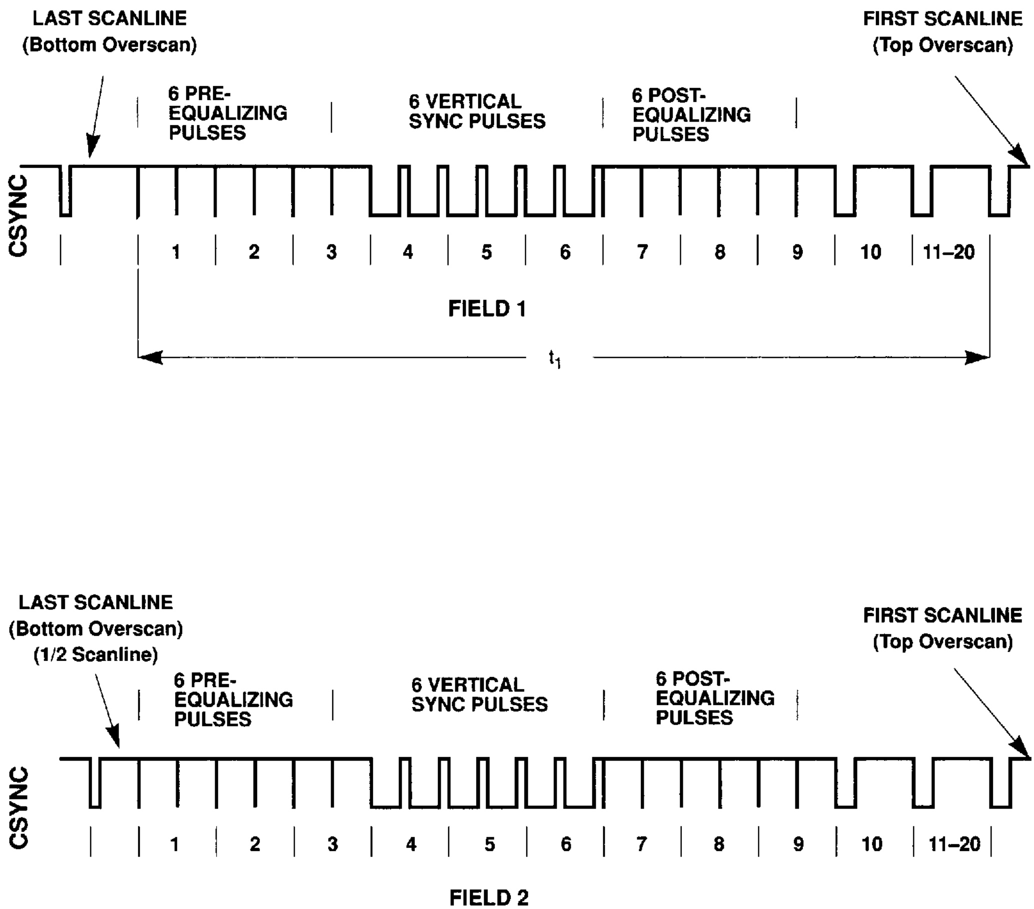


Figure 7-42. NTSC Vertical Retrace (CL-GD5425 only)

Table 7-43. NTSC Vertical Blanking Detail (CL-GD5425 only)

Symbol	Parameter	Nominal	Units
t_1	Equalizing pulse width (low)	2.32	µsec.
t_2	Serrations pulse width (high)	4.65	µsec.
t_3	Equalization to serration	1	H-period
t_4	First serration	1/2	H-period

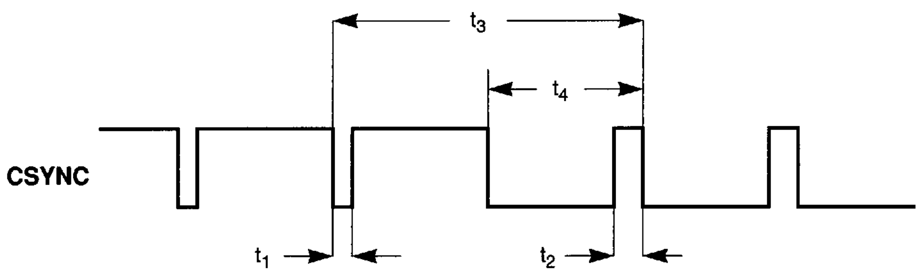


Figure 7-43. NTSC Vertical Blanking Detail (CL-GD5425 only)

Table 7-44. Horizontal Period (PAL — CL-GD5425 only)

Symbol	Parameter	Nominal	Units
t_1	Horizontal period	64.00	µsec.
t_2	HSYNC pulse width (low)	4.65	µsec.

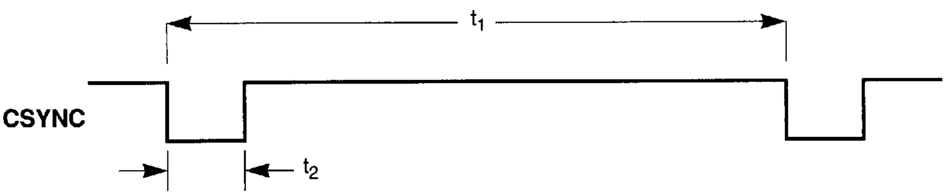


Figure 7-44. Horizontal Period (PAL — CL-GD5425 only)

Table 7-45. PAL Vertical Retrace (CL-GD5425 only)

Symbol	Parameter	Nominal	Units
t_1	Vertical blanking period	25	H-period

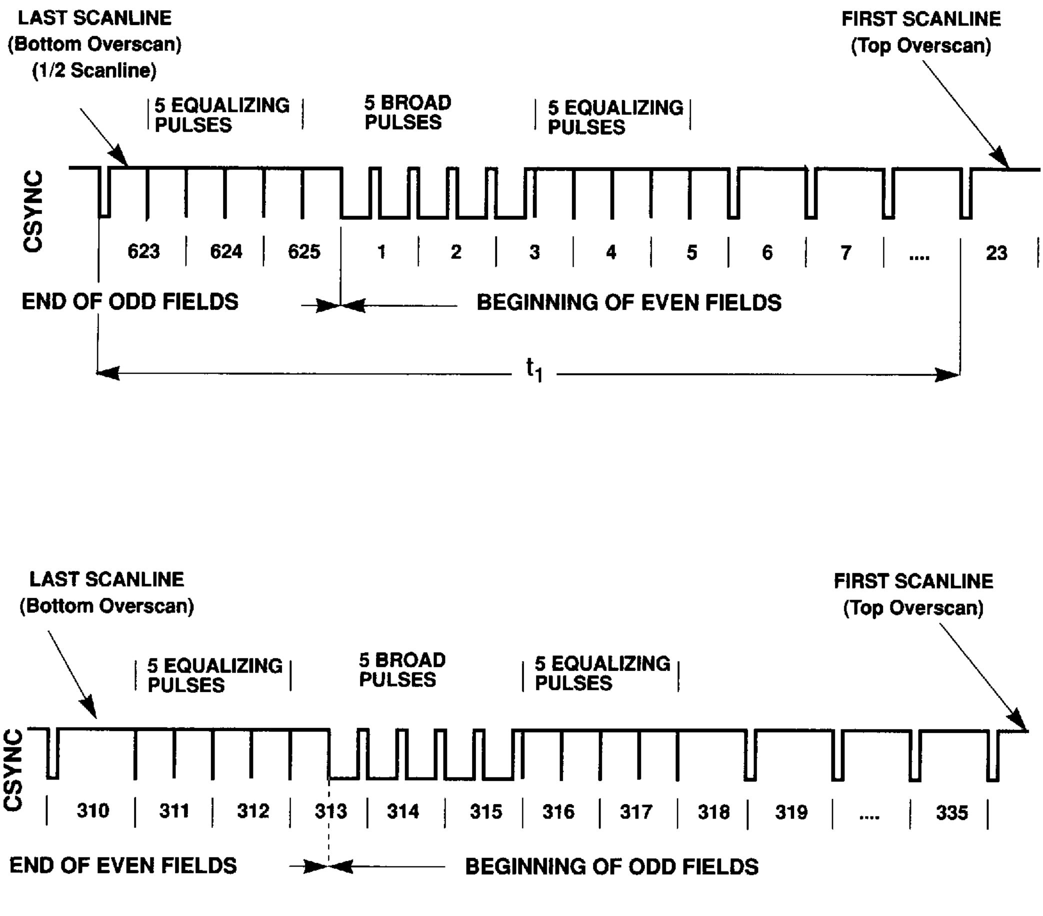
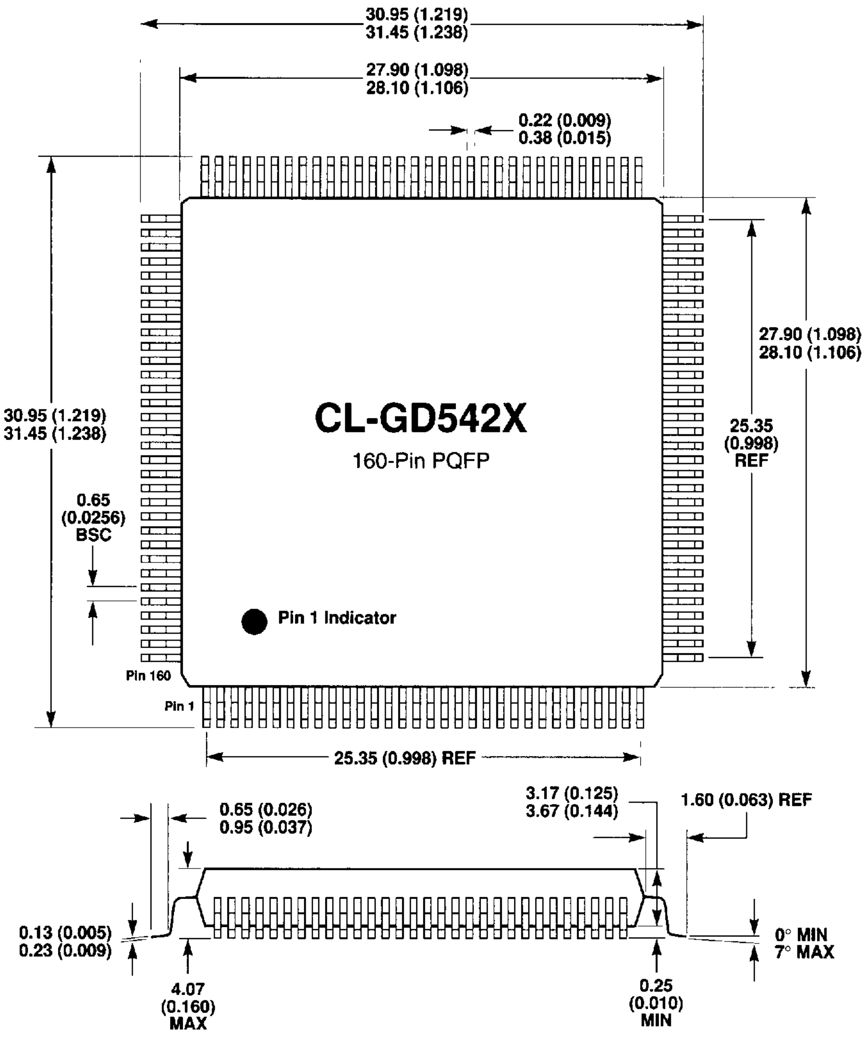


Figure 7-45. PAL Vertical Retrace (CL-GD5425 only)

8. PACKAGE DIMENSIONS



NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information..

CIRRUS LOGIC

9. ORDERING INFORMATION EXAMPLES

CL – GD542X* – 80 QC – A

- CL — Cirrus Logic Inc.
- G D — Graphics, Display
- 542X — Part Number
- 80 — Data Rate: 80 MHz Maximum Video Clock
- Q — Package Type: Q = Plastic Quad Flat Pack
- C — Temperature Range: C = Commercial
- A — Revision †

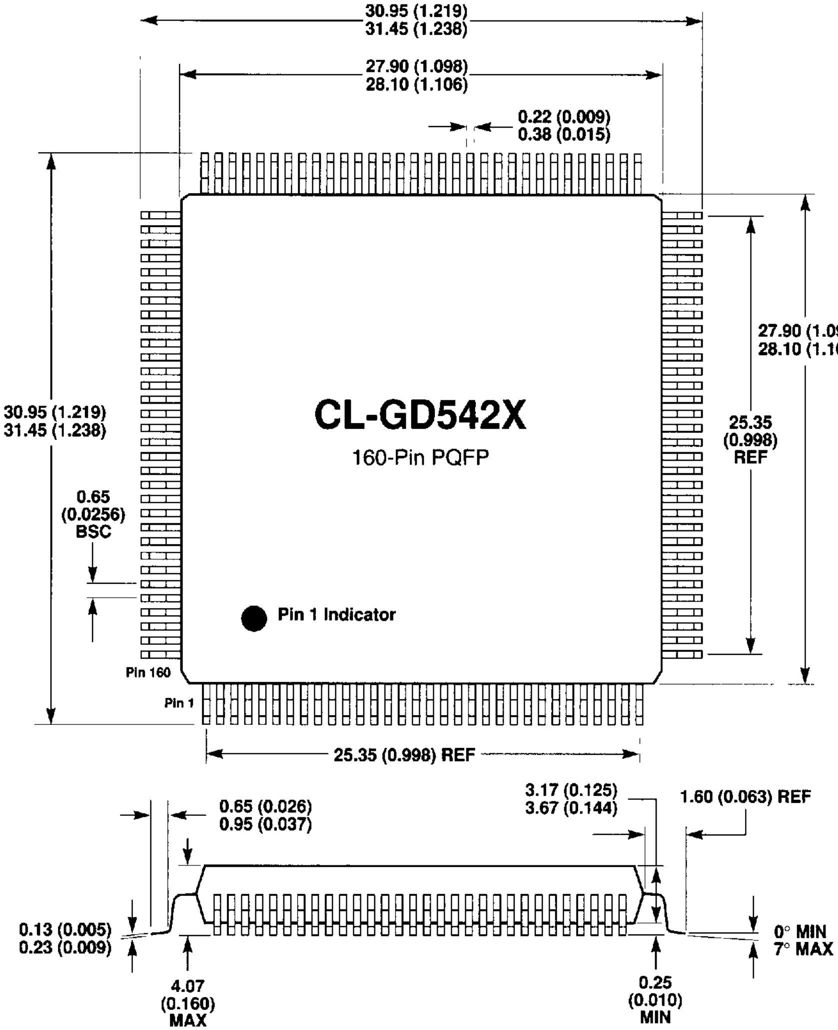
† Contact Cirrus Logic Inc. for up-to-date information on revisions.
* '2X' represents CL-GD5420/'22/'24/'26/'28/'29, respectively.

CL – GD5425 – TV QC – A

- CL — Cirrus Logic Inc.
- G D — Graphics, Display
- 5425 — Part Number
- TV — TV Output Device
- Q — Package Type: Q = Plastic Quad Flat Pack
- C — Temperature Range: C = Commercial
- A — Revision †

† Contact Cirrus Logic Inc. for up-to-date information on revisions.

8. PACKAGE DIMENSIONS



NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information..