CS9233

Integrated Wavetable Music Synthesizer

Features

- Highly integrated solution combines a specialized synthesis DSP and a microcontroller on a single chip

- Provides high quality wavetable synthesis with 32-note polyphony

- Capable of FM synthesis with AdLib register set emulation for DOS games compatibility

- Glueless interface to memories, DAC, and optional CS8905/CS8905A effects processor

- Flexible sample memory interface supports both ROM and/or DRAM based samples

- 18-bit audio output directly supports the 96 dB CS4331 Stereo DAC

General Description

The CS9233 is a highly integrated music synthesizer circuit designed for PC multimedia, Karaoke, arcade game and set-top applications. Interface logic is included on-chip for glueless connections to external memory, the CS4331 DAC, and the optional CS8905/CS8905A digital effects processor.

The CS9233, combined with microcontroller firmware and PCM sample data available from Crystal, provides a music synthesis solution which is compatible with a number of industry standards, including General MIDI (GM), Roland GS, the MPC Level 1 and Level 2 Guidelines for Synthesizer Implementation, and the MPU-401 (UART Mode) and AdLib register sets.

Crystal offers several reference design packages for the CS9233. These packages include schematics, Bill of Materials, and layout information for complete functional sound card or stand-alone synthesizer designs.

ORDERING INFORMATION
CS9233-CQ 144-pin TQFP (20x20x1.4mm)
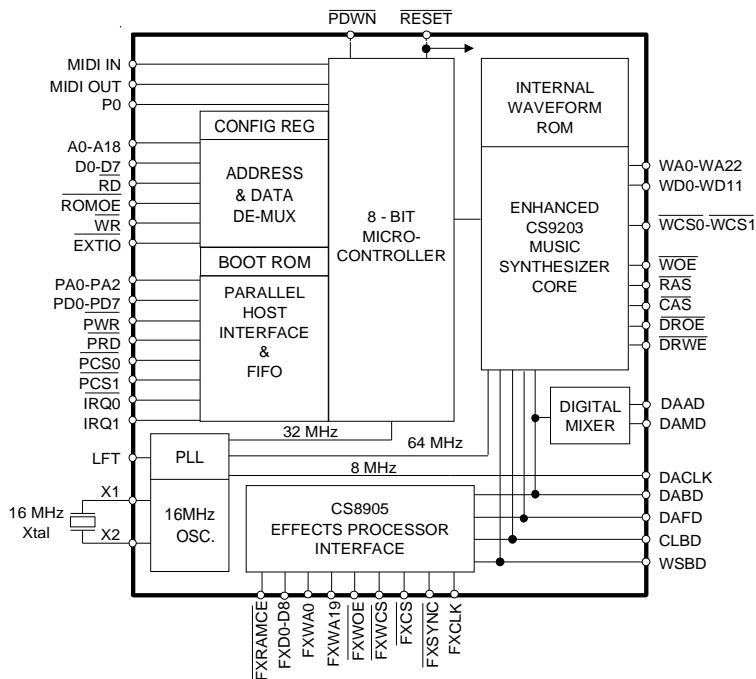
D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Typ	Max	Units
Low-Level Input Voltage	V_{IL}	-0.3	-	0.8	V
High-Level Input Voltage	V_{IH}	2.0	-	V_{CC}+0.3	V
Low-Level Output Voltage at I_{OL}=3.2 mA	V_{OL}	-	-	0.45	V
High-Level Output Voltage at I_{OH}=0.8 mA	V_{OH}	2.4	-	-	V
Power Supply Current (Note 1) crystal frequency=16.0 MHz	I_{CC}	-	-	150	mA

Notes: 1. Power Supply Current does not include output loading.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature (Power applied)	-	-40	-	+85	°C
Supply Voltage	Vcc	+4.75	-	+5.25	V
Supply Ground	GND	-0.25		+0.25	V
Oscillator Frequency	$1/t_{clcl}$	7	16	tbd	MHz

ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0V, GND=0V)

Parameter	Symbol	Min	Typ	Max	Units
Storage temperature	-	-65	-	+150	°C
Voltage on any pin	-	-0.5	-	V_{CC}+0.5	V
Supply Voltage to Ground Potential	V_{CC}	-0.5	-	6.5	V
Maximum I_{OL} per I/O pin	-	-	-	10	mA

ROM SAMPLE MEMORY ACCESS (T_A=25°C, V_{CC}=5V $\pm$5%, Digital Inputs at Logic "1" = Vcc;
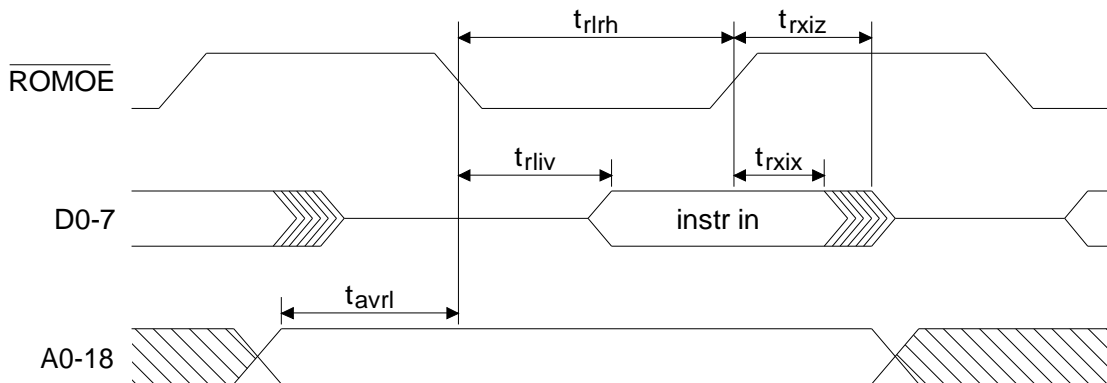Logic "0" = DGND, load capacitance=30pF for all outputs except X2. $T_{ck} = t_{clcl}$/2 in nanoseconds.)

Parameter	Symbol	Min	Typ	Max	Units
Address Valid	t_{acyc}	350	-	-	ns
Address valid to WCS0 or WCS1	t_{avwcs}	20	-	-	ns
Address valid to WOE low	t_{avwoe}	-3	-	10	ns
WCS0 or WCS1 pulse width	t_{cslcsh}	350	-	-	ns
WCS0 or WCS1 low to data valid	t_{wcsdv}	-	-	tbd	ns
Data hold after WCS0 or WCS1 high	t_{wcsdx}	0	-	tbd	ns
Address hold after WCS0 or WCS1 high	t_{wcsax}	0	-	-	ns
WOE pulse width	t_{oeloeh}	$7T_{ck}$	-	-	ns
WOE low to data valid	t_{woedv}		-	$7T_{ck}$ - 22	ns
Data hold after WOE	t_{woedx}	0	-	20	ns
Address hold after WOE	t_{woeax}	20	-	-	ns
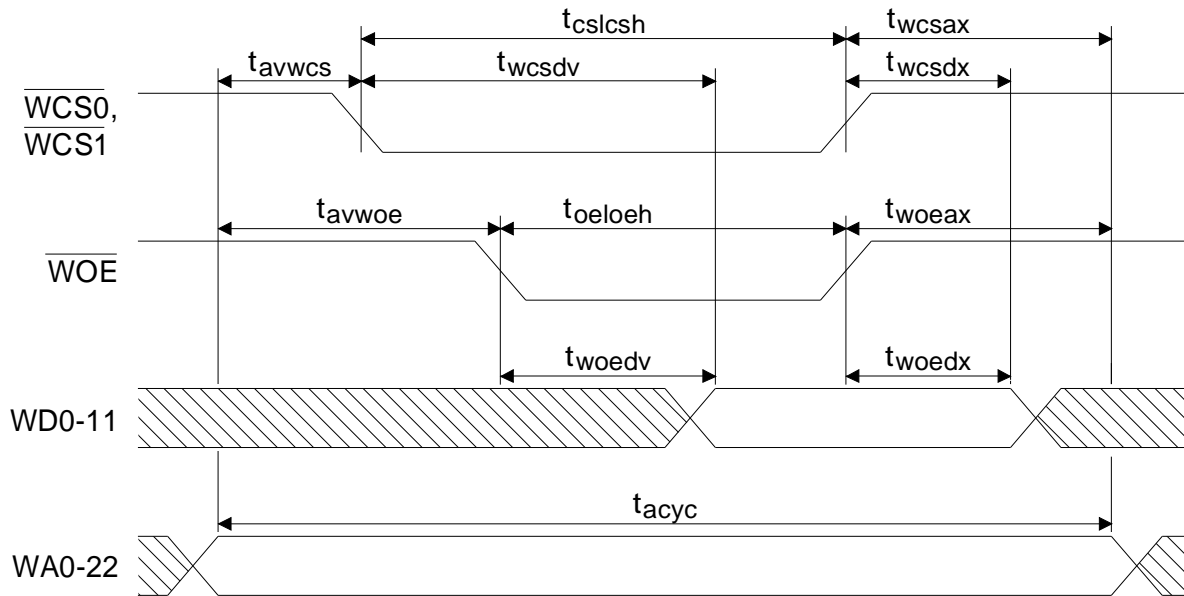
ROM Sample Memory Read Cycle

MICRO-CONTROLLER DATA BUS TIMING (T_A=25°C, V_{CC}=5V ±5%, Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, load capacitance=30pF for all outputs except X2. $T_{ck} = t_{clcl}/2$ in nanoseconds.)
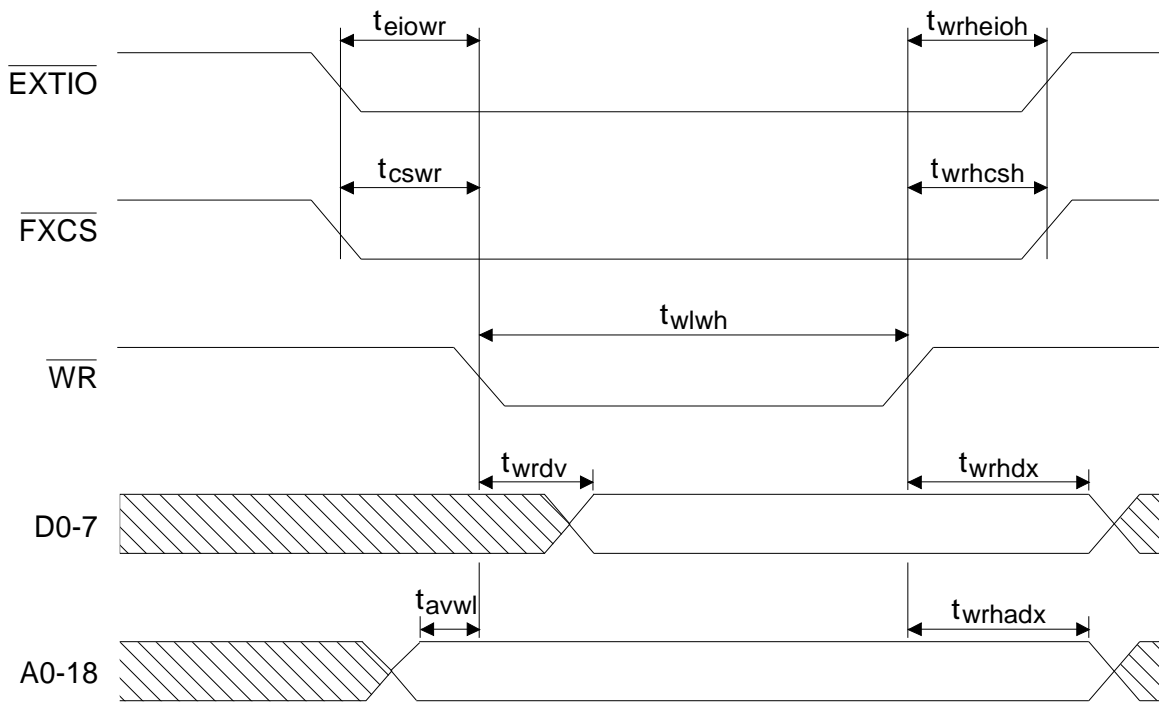
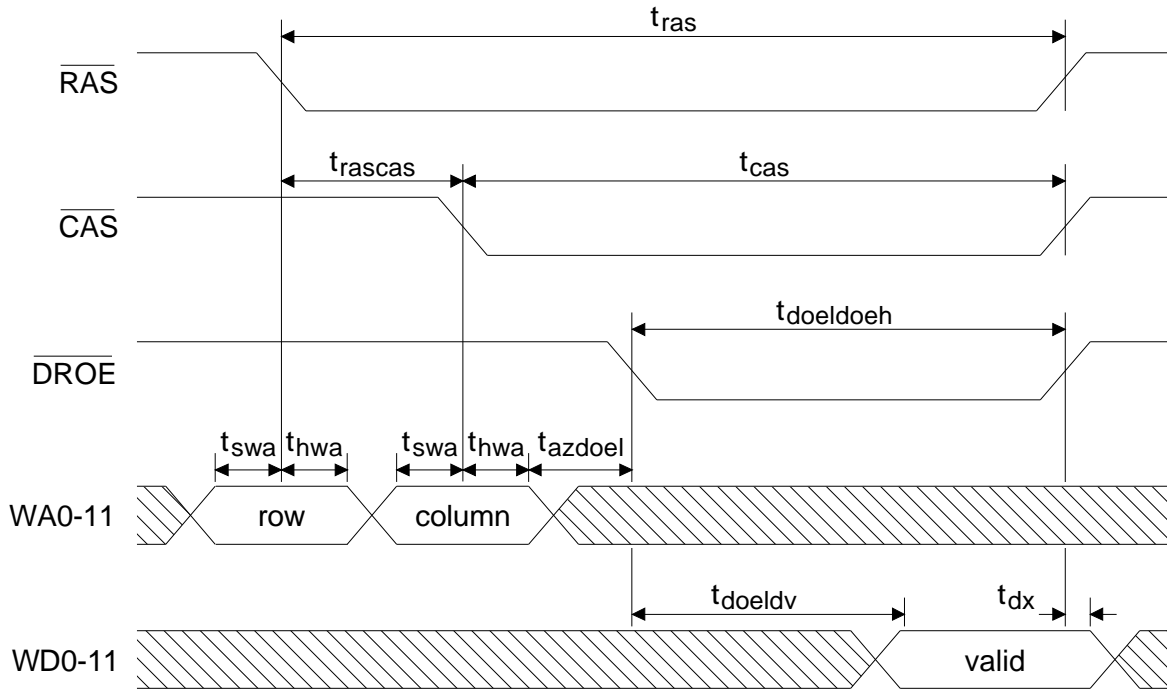| Parameter	Symbol	Min	Typ	Max	Units
ROMOE low to ROMOE high; ROMOE pulse width	t_{rlrh}	$3T_{ck}$ - 10	-	$3T_{ck}$ +10	ns
ROMOE low to valid instruction	t_{rliv}	-	-	$3T_{ck}$ -28	ns
Input instruction hold after ROMOE high	t_{rxix}	0	-	-	ns
Input instruction float after ROMOE high	t_{rxiz}	-	-	20	ns
Address valid to ROMOE low	t_{avrl}	$2T_{CK}$	-	$3T_{CK}$	ns
RD pulse width	t_{rdlrdh}	$5.5T_{ck}$ - 10	-	$5.5Tck$ +10	ns
RD low to data valid	t_{rddv}	-	-	$4.5T_{ck}$ - 27	ns
Data hold after RD high	t_{rdhdx}	0	-	20	ns
EXTIO low to RD low	t_{eiord}	$4T_{ck}$ - 10	-	-	ns
EXTIO high after RD high	$t_{rdheioh}$	0	-	-	ns
FXCS low to RD low	t_{csrd}	tbd	-	tbd	ns
FXCS high after RD high	t_{rdhcsh}	tbd	-	-	ns
Address hold after RD high	t_{rdhadx}	20	-	-	ns
Address valid after RD low	t_{avrdl}	-	-	10	ns
EXTIO low to WR low	t_{eiowr}	$4T_{ck}$ - 10	-	$4T_{ck}$ + 10	ns
EXTIO high after WR high	$t_{wrheioh}$	20	-	-	ns
FXCS low to WR low	t_{cswr}	tbd	-	-	ns
FXCS high after WR high	t_{wrhcsh}	tbd	-	-	ns
Address hold after WR high	t_{wrhadx}	20	-	-	ns
Address valid to WR low	t_{avwl}	$3T_{ck}$	-	-	ns
WR pulse width	t_{wlwh}	$5T_{ck}$ - 10	-	$5T_{ck}$ + 10	ns
Data valid to write transition	t_{wrdv}	tbd	-	10	ns
Data hold after WR high	t_{wrhdx}	0	-	20	ns

Micro-controller Program Memory Read Cycle
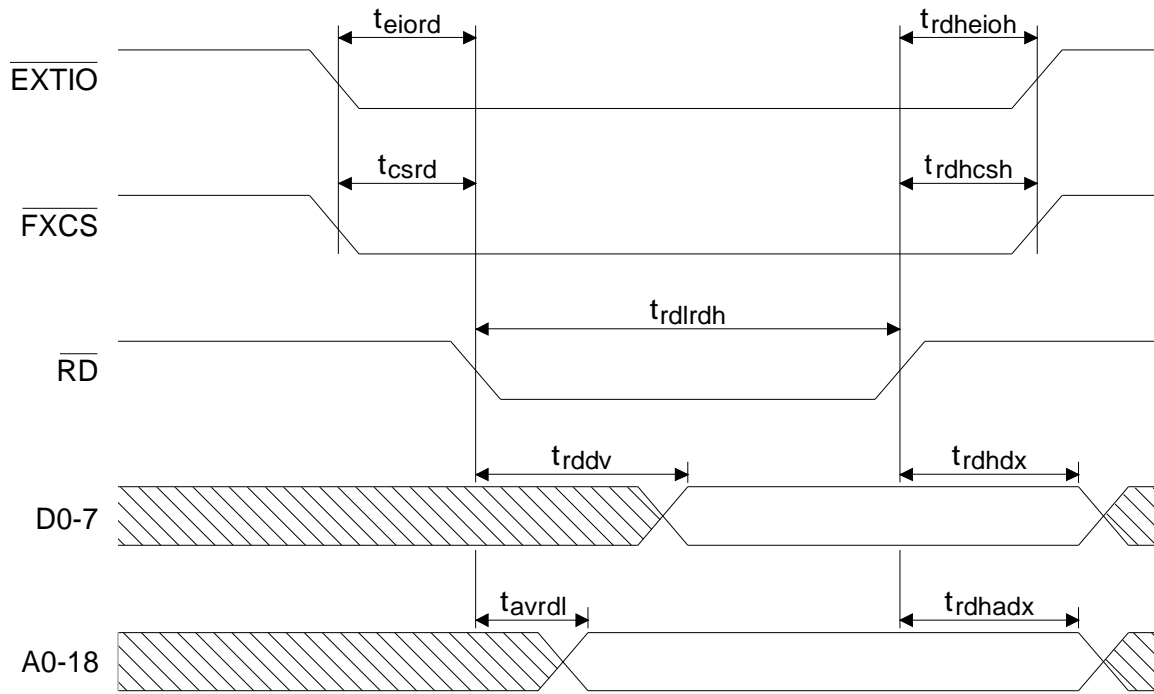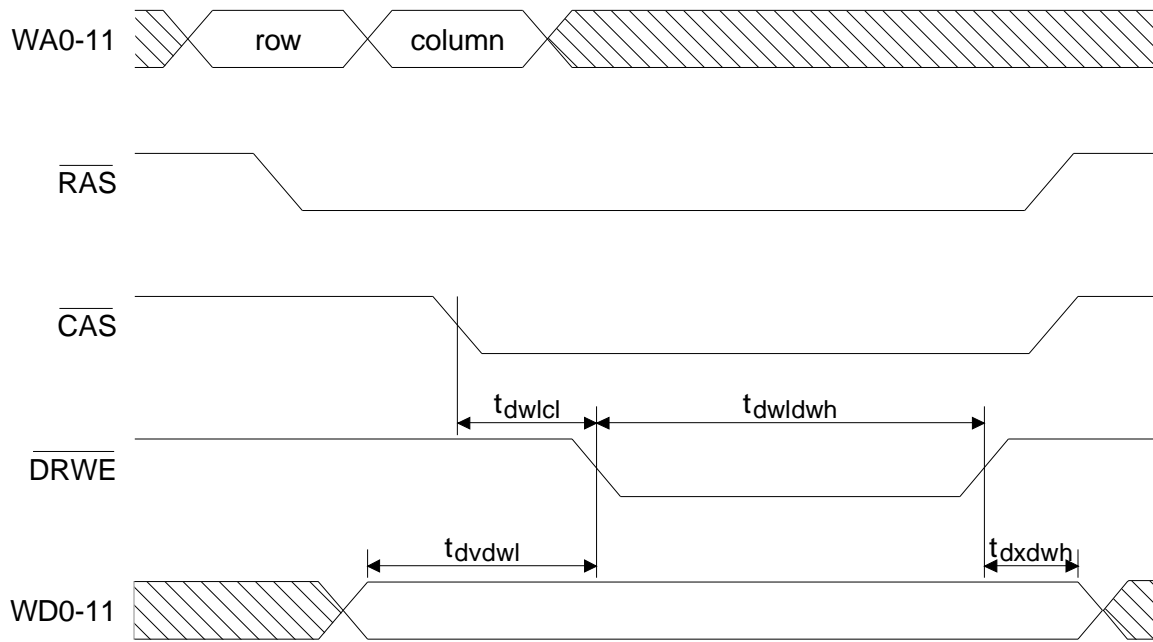
Micro-controller External Data Read

Micro-controller External Data Write

DRAM SAMPLE MEMORY ACCESS (T_A=25°C, V_{CC}=5V ±5%, Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, load capacitance=30pF for all outputs except X2. T_{ck} = t_{clcl}/2 in nanoseconds.)

Parameter	Symbol	Min	Typ	Max	Units
Address valid before RAS or CAS high to low	t_{swa}	T_{ck}/2 - 10	-	-	ns
Address valid after RAS or CAS high to low	t_{hwa}	T_{ck}/2 - 10	-	-	ns
RAS pulse width	t_{ras}	$9.5T_{ck}$ - 10	-	12.5Tck	ns
CAS pulse width	t_{cas}	$7.5T_{ck}$ - 10	-	$10T_{ck}$	ns
CAS delay after RAS	t_{rascas}	$2T_{ck}$ - 10	-	$2T_{ck}$ + 10	ns
Address floating to DROE low	t_{azdoel}	tbd	-	-	ns
DROE low to data valid	t_{doeldv}	-	-	$7T_{ck}$ -22	ns
DROE pulse width	$t_{doeldoeh}$	$7T_{ck}$ - 10	-	tbd	ns
Data hold after DROE high	t_{dx}	0	-	20	ns
DRWE low after CAS low	t_{dwlcl}	$2.5T_{ck}$ -10	-	$2.5T_{ck}$ +10	ns
Data valid before DRWE low	t_{dvdwl}	$4T_{ck}$ - 10	-	-	ns
Data hold after DRWE high	t_{dxdwh}	20	-	-	ns
DRWE pulse width	t_{dwldwh}	$2T_{ck}$ - 10	-	$2T_{ck}$ + 10	ns

CRYSTAL

t_{ras}

$\overline{RAS}$

t_{rascas} t_{cas}

$\overline{CAS}$

$t_{doeldoeh}$

$\overline{DROE}$

t_{swa} t_{hwa} t_{swa} t_{hwa} t_{azdoel}

WA0-11 row column

t_{doeldv} t_{dx}

WD0-11 valid

DRAM Sample Memory Read

WA0-11 row column

$\overline{RAS}$

$\overline{CAS}$

t_{dwlcl} t_{dwldwh}

$\overline{DRWE}$

t_{dvdwl} t_{dxdwh}

WD0-11

DRAM Sample Memory Write

EFFECTS PROCESSOR INTERFACE (T_A=25°C, V_CC=5V ±5%, Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, load capacitance=30pF for all outputs except X2)

Parameter	Symbol	Min	Typ	Max	Units
FXRAMCE low from FXWCS low AND FXWA19 low	t_{csce}	-	-	10	ns
FXRAMCE high from FXWCS high OR FXWA19 high	t_{cshceh}	-	-	10	ns
FXD8 active from FXWOE low	t_{oed8}	-	-	10	ns
FXD8 valid from FXD7 valid AND FXWA0 valid AND FXWOE low	t_{dvd8v}	-	-	10	ns
FXD8 high-impedance state from FXWOE high	t_{oed8x}	0	-	10	ns
FXD0-FXD7 valid from FXWCS low, FXWA19 high and FXWA0 valid	t_{csdv}	-	-	10	ns
FXD0-FXD7 data hold after FXWCS high	t_{csdx}	0	-	10	ns
FXWA0 valid until FXWCS low	t_{a0vcs}	tbd	-	-	ns
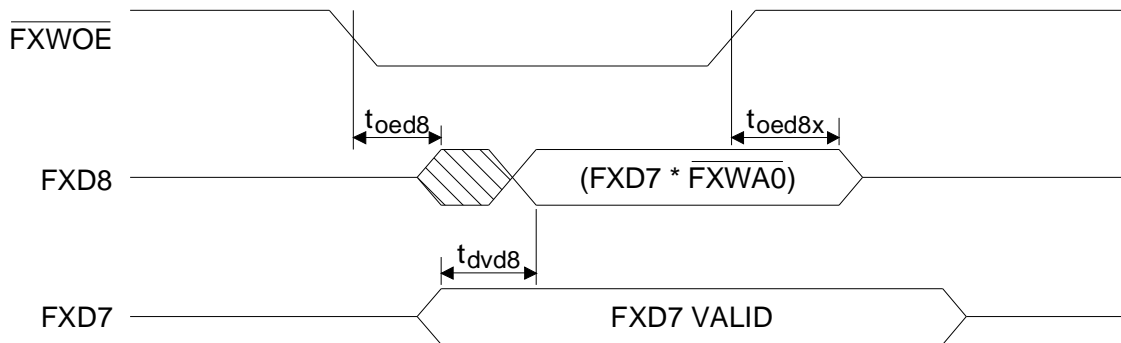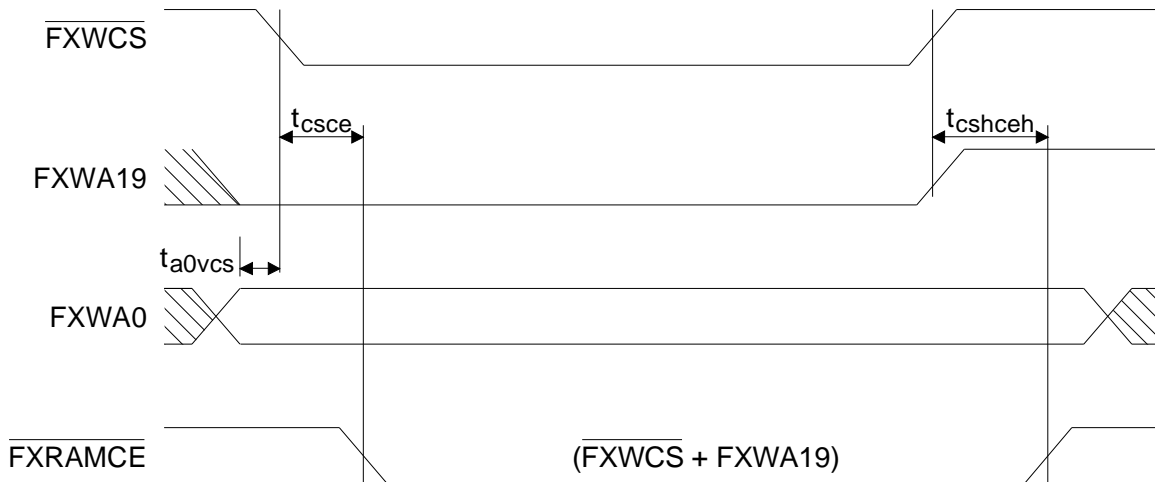
CS8905/CS8905A Read from RAM
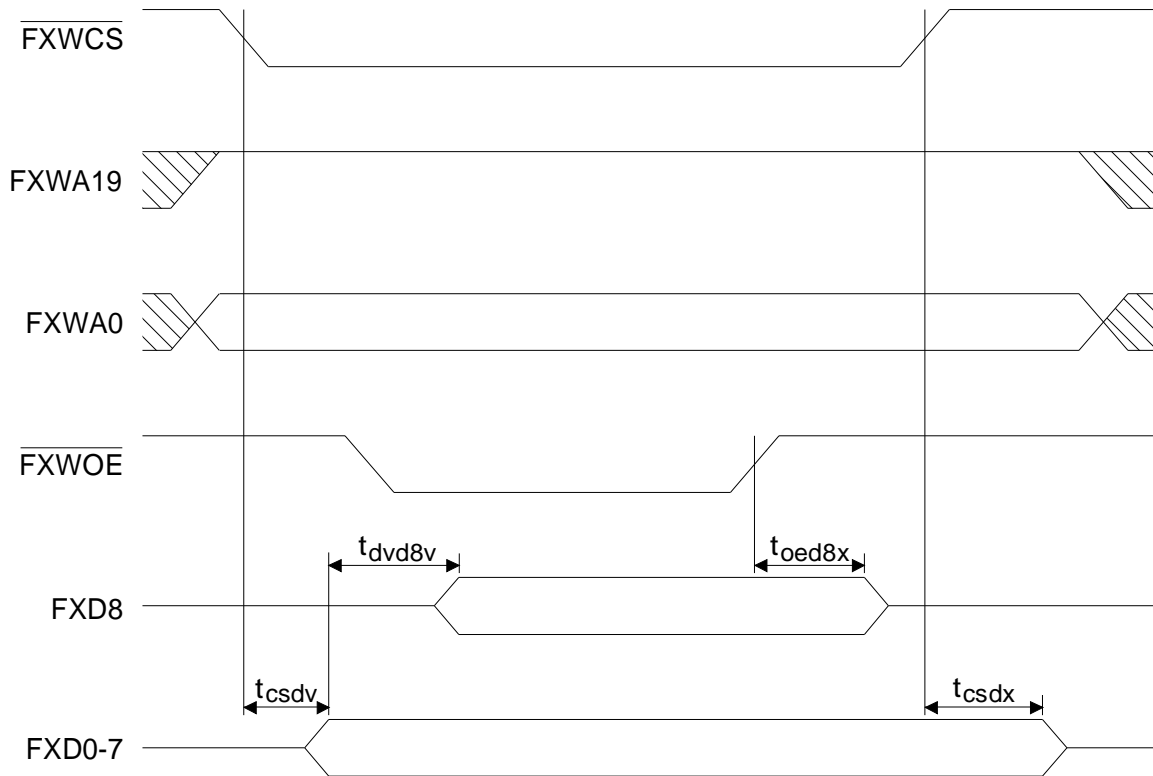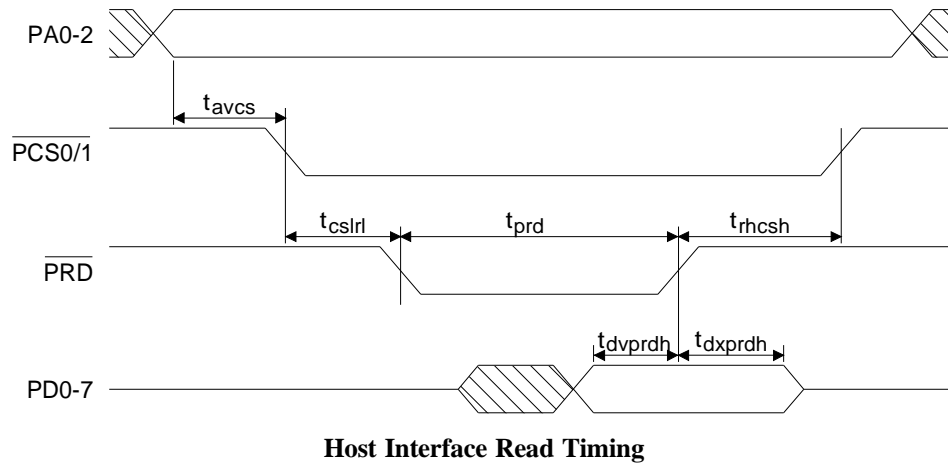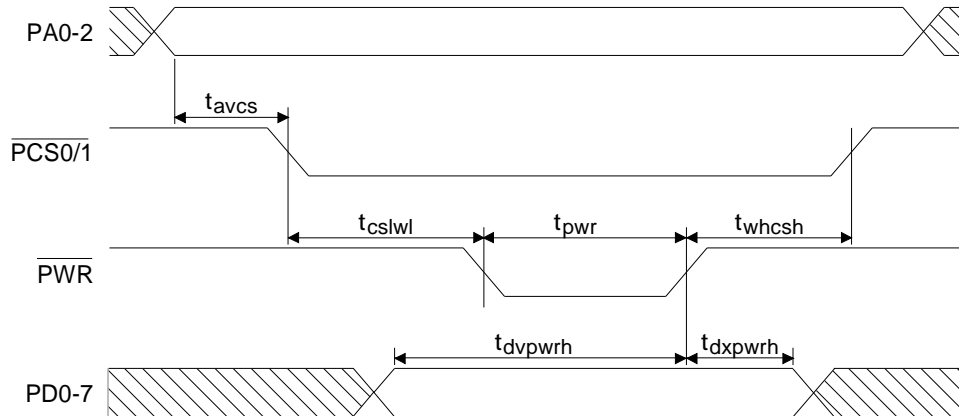
CS8905/CS8905A Read from CS9233 FXD0-FXD7

HOST INTERFACE (T_A=25°C, V_{CC}=5V $\pm$5%, Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, load capacitance=30pF for all outputs except X2.)

Parameter	Symbol	Min	Typ	Max	Units
Address valid to PCS0 or PCS1 low	t_{avcs}	0	-	-	ns
PRD low after PCS0 or PCS1 low	t_{cslrl}	0	-	-	ns
PCS0 or PCS1 high after PRD high	t_{rhcsh}	0	-	-	ns
PCS0 or PCS1 low to PWR low	t_{cslwl}	20	-	-	ns
PCS0 or PCS1 high after PWR high	t_{whcsh}	20	-	-	ns
Data hold after PRD high	t_{dxprdh}	0	-	-	ns
Data hold after PWR high	t_{dxpwrh}	0	-	20	ns
Data valid to PRD high	t_{dvprdh}	20	-	-	ns
PRD pulse width	t_{prd}	20	-	-	ns
Data valid to PWR high	t_{dvpwrh}	10	-	-	ns
PWR pulse width	t_{pwr}	20	-	-	ns

Host Interface Read Timing

Host Interface Write Timing

DIGITAL AUDIO INTERFACE (T_A=25°C, V_{CC}=5V ±5%, Digital Inputs at Logic "1" = Vcc; Logic "0" = DGND, load capacitance=30pF for all outputs except X2. T_{ck} = t_{clcl}/2 in nanoseconds.)

Parameter	Symbol	Min	Typ	Max	Units
CLBD pulse width low	t_{clbdl}	$8T_{ck}$ -10	-	-	ns
CLBD pulse width high	t_{clbdh}	$8T_{ck}$ -10	-	-	ns
CLBD rising to WSBD edge delay	t_{cwsd}	$7T_{ck}$ -10	-	-	ns
CLBD rising to WSBD edge setup time	t_{cwss}	$9T_{ck}$ -10	-	-	ns
DABD, DAMB, and DAFB valid to CLBD rising setup time	t_{sodlrs}	$8T_{ck}$ -10	-	-	ns
CLBD rising to DABD, DAMB, and DAFB hold time	t_{sodh}	$8T_{ck}$ -10	-	-	ns
DAAD valid to CLBD rising setup time	t_{sidlrs}	$8T_{ck}$ -10	-	-	ns
CLBD rising to DAAD hold time	t_{sidh}	$8T_{ck}$ -10	-	-	ns
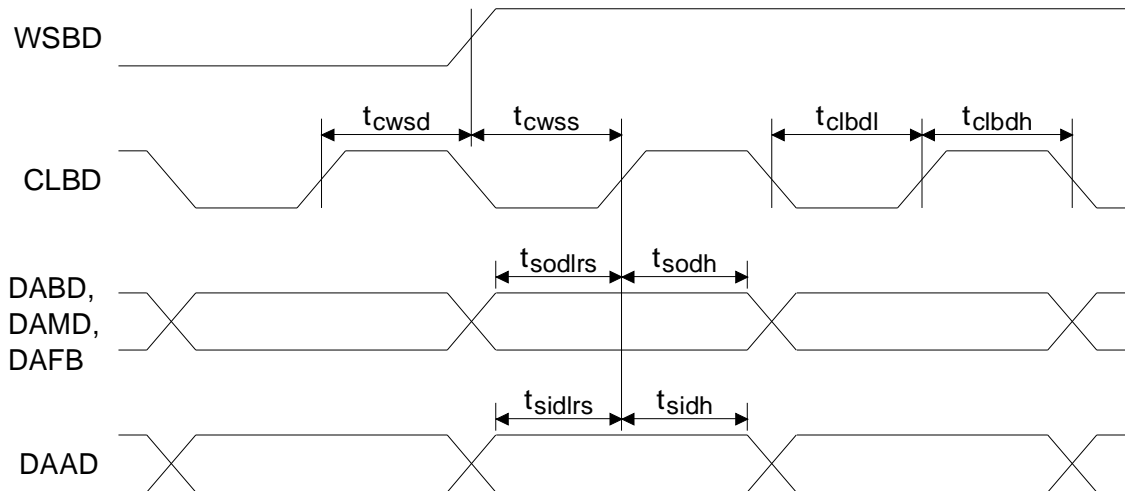
Digital Audio Serial Timing

Overview

The CS9233 is a high performance digital music synthesis device which combines a highly specialized signal processor engine with a general purpose microcontroller on a single integrated circuit. This device is available as the result of a technology partnership between Crystal Semiconductor Corporation and DREAM S.A. of France.

The CS9233, combined with microcontroller firmware and PCM sample data available from Crystal Semiconductor, provides a complete music synthesis solution with a minimal number of external components. A typical application would include only the CS9233 synthesizer, the CS4112 wavetable sample ROM, the CS4331 18-bit stereo DAC, one 128Kx8 EPROM and one 32Kx8 RAM. All of the "glue logic" typically required to interface with external components has been included on-chip with the CS9233. Digital reverb and chorus effects processing requires only two additional components; the CS8905/CS8905A effects processor and a second 32Kx8 RAM.

The microcontroller firmware and sample data available from Crystal provides compatibility with a number of industry standards, including General MIDI (MIDI Manufacturer's Association), Roland GS format (Roland Corp.), the MPC Level 1, Level 2, and Level 3 Guidelines for Synthesizer Implementation (Multimedia PC Marketing Council), the MPU-401 (UART Mode) register set (Roland Corp.), and the Ad-Lib FM synthesizer register set (AdLib Multimedia, Inc.).

The on-chip microcontroller is clocked at twice the frequency of the CS9233's external crystal (32 MHz when using a 16 MHz crystal). The CS9233 provides a glueless interface to the microcontroller's external ROM and RAM memories. A small Boot ROM is included in the CS9233 to allow ROMless designs (in this case

the microcontroller program code is downloaded from an external host processor through the CS9233 into external program RAM). The on-chip microcontroller includes a UART which is used to send and receive serial MIDI data from external devices.

The CS9233's synthesis processor is an enhancement of the original CS9203 synthesis processor. This extremely efficient architecture is capable of generating 32 simultaneous voices using high quality wavetable synthesis with linear interpolation and resonant filtering for each voice. The CS9233 synthesis processor is also capable of FM synthesis, allowing compatibility with older DOS games in multimedia computer applications. Synthesis algorithms are stored on-chip in microcode ROM. Synthesis parameter data is stored on-chip in RAM. The on-chip microcontroller controls the synthesis processor by writing parameter data into the synthesis parameter RAM. The synthesis processor is clocked at four times the frequency of the CS9233's external crystal (64 MHz when using a 16 MHz crystal).

The PCM instrument samples for wavetable synthesis may be stored in external ROM or in DRAM, or a combination of ROM and DRAM may be used (when DRAM sample memory is used, the DRAM-based instrument samples must be downloaded from an external host processor through the CS9233 into DRAM before they can be used for synthesis). The external data path for wavetable sample memory is 12-bits wide, and the internal system bus width is 19 bits. The synthesis processor addresses up to 8 Msamples of external wavetable sample memory.

The digital audio interface includes four 24-bit output accumulators which drive two stereo digital audio outputs, the main stereo output and the stereo effects send output. Separate level scaling is implemented at the input to each accumulator, allowing individual control of the main left and right levels, and the reverb and chorus send levels, for each voice being generated.

In addition to the microcontroller and synthesis processor, the CS9233 includes a parallel host interface, a parallel effects send interface, a digital effects return mixer, and a Phase Locked Loop clock generator circuit. The figure on the cover page of this document depicts these functional blocks.

The parallel host interface is used in multimedia PC applications to allow emulation of the industry-standard MPU-401 (UART mode) and/or AdLib register sets. The parallel host interface is also used for high-speed sample downloading in applications which include DRAM-based wavetable sample memory. The parallel effects send interface provides a glueless interface to the optional CS8905/CS8905A effects processor and the associated 32Kx8 RAM. The digital effects return mixer allows the CS9233 to accept a digital audio effects return output signal from an external effects processor such as the CS8905/CS8905A. The effects return signal is digitally mixed with the CS9233 main digital audio output, eliminating the need for separate DACs for the CS9233 and the effects processor. The Phase Locked Loop (PLL) clock generator circuit generates all clock frequencies required for the CS9233 itself, the CS4331 DAC, and the optional CS8905/CS8905A effects processor, from a single on-chip oscillator .
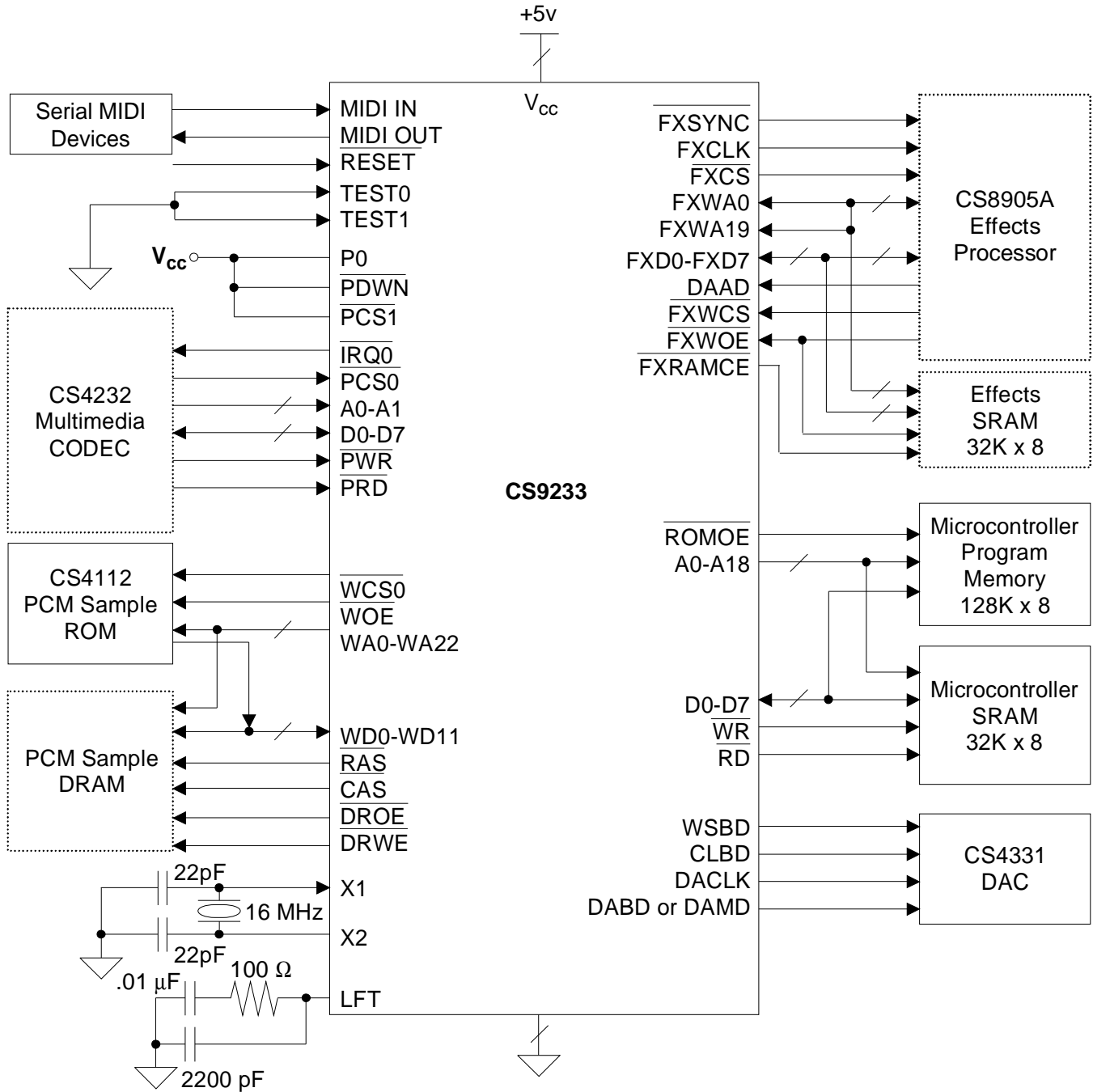
In a typical application, the CS9233's synthesis processor is responsible for the generation of musical tones as defined by the synthesis parameter values contained in the on-chip parameter RAM. The microcontroller is responsible for parsing commands and MIDI data from the serial MIDI UART and/or the parallel host interface, and then writing the appropriate parameter data to the synthesis processor's parameter RAM to control sound generation. The microcontroller is also responsible for low frequency synthesis functions such as generation of low frequency oscillators (LFO), and management of instrument amplitude and filter cutoff envelopes. The microcontroller implements these low frequency functions by periodically updating or modulating the parameter values written to the synthesis processor's parameter RAM.

Figure 1 shows the typical external connections for the CS9233, along with several of the optional external device connections. The external components required for a typical wavetable synthesis application include one 32Kx8 RAM, one 128Kx8 EPROM, the CS4112 1 Msample wavetable ROM, and the CS4331 18-bit stereo DAC. The RAM is the microcontroller's external data workspace. The EPROM contains both the microcontroller program code and the wavetable instrument parameter data. The instrument parameter data provides definitions of the envelopes, LFOs, and filter settings to be used for each instrument.

The CS4112 is a 1Mx8 wavetable sample ROM which contains the PCM sample data which is processed by the synthesis processor (Crystal also offers a 4Mx8 wavetable sample set consisting of the CS4110 and CS4111 sample ROMs). The CS4331 18-bit stereo DAC converts the stereo digital audio output data stream from the CS9233 into a stereo analog audio output.

The CS9233 can receive MIDI data in serial form through the MIDI IN pin, or in parallel form through the parallel host interface. For stand-alone wavetable synthesis applications such as wavetable daughtercards or Karaoke applications, only the serial MIDI interface is used. In multimedia PC applications, the CS9233's microcontroller may be programmed to emulate the MPU-401 (UART Mode) and/or AdLib register sets using the CS9233 parallel host interface. The MPU-401 register set provides the alternate parallel path for receiving/sending MIDI data from/to an external host processor. However, most multimedia PC designs utilize multimedia audio CODEC devices (such as the Crystal CS4232) which include the MPU-401 (UART Mode) function, so this capability of the CS9233 is typically not utilized.

Figure 1. Typical Connection Diagram

For multimedia PC applications which require FM synthesis and AdLib register compatibility, the CS9233 can generate sounds using FM synthesis in response to commands and data received from the ISA bus via the CS9233 host interface AdLib register set emulation.

Related Literature and Crystal Reference Designs

A number of related documents are available from Crystal Semiconductor. These include the CS9233 Microcontroller Firmware data sheet, the CRD9233-1 ISA Wavetable Sound Card Reference Design data sheet, the CRD9233-3 Wavetable Synthesizer Daughtercard Reference Design data sheet, the CS4110/CS4111 Wavetable Sample ROM data sheet, the CS4112 Wavetable Sample ROM data sheet, the CS4331 18-bit Stereo DAC data sheet, the CS4232 Multimedia CODEC data sheet, the CS8905/CS8905A Digital Musical Effects Processor data sheet, and an applications note titled "A Tutorial on MIDI and Wavetable Synthesis" by Jim Heckroth.

The CS9233 Microcontroller Firmware Data Sheet provides a description of the functions provided in the CS9233 firmware available from Crystal. This firmware is used in conjunction with the Crystal 1Mx8 sample ROM (CS4112), or the 4Mx8 sample ROM set (CS4110 plus CS4111). The firmware data sheet includes instrument lists for the 1Mx8 sample set and 4Mx8 sample set, complete MIDI implementation data, Self Test data, and sample downloading information.

The CRD9233-1 Reference Design is a complete ISA sound card design utilizing the CS4232, CS9233, CS4112 and CS4331. This high performance audio adapter card includes four different CD-ROM interfaces, and is Plug and Play configurable. The wavetable synthesizer implementation on the CRD9233-1 features the full General MIDI instrument set plus GS variations in sample ROM, and supports downloadable samples with a 512Kx8 sample memory DRAM.

The CRD9233-3 Reference Design is a complete wavetable daughter card design utilizing the CS9233, the CS4112, the CS4331, and the CS8905/CS8905A effects processor. This design utilizes the de-facto standard WaveBlaster 26-pin header pin-out. The high quality digital reverb and chorus effects provided by the CS8905A are adjustable on a per-MIDI channel basis through the CS9233 MIDI interface.

Crystal Reference Design packages include functional circuit boards, data sheets, schematics, Bill of Materials, layout information, and any applicable software.

Microcontroller

The CS9233 microcontroller core consists of a CPU, 256x8 on-chip RAM, bus interface logic, three 16-bit counter/timers, a full-duplex programmable UART, and parallel ports. The microcontroller address bus and data bus are fully de-multiplexed on-chip so that no external address latch is required. Address decoding logic and memory paging logic is also included on-chip, allowing a glueless interface to external microcontroller ROM and RAM memory devices.

The microcontroller's tasks typically include parsing and interpretation of incoming MIDI data and commands, tracking of envelopes for notes in progress, and generation of low-frequency oscillators (LFO). The microcontroller is clocked at twice the frequency of the CS9233's external crystal (32 MHz for the typical 16 MHz crystal frequency). The high speed of this microcontroller allows effective processing of dense MIDI traffic. This becomes particularly important when making use of the full 32-note polyphony of the CS9233.

The CS9233 microcontroller core directly addresses 64Kx8 external program memory (CODE space) and 64Kx8 external memory (XDATA space). On-chip XDATA paging logic has been included to allow expansion of the XDATA space to eight pages of 64Kx8 per page.

The CS9233 is operated in either of two memory map configurations. The CS9233 is configured for either the normal (ROM and RAM) microcontroller memory map or for the ROMless microcontroller memory map by connecting the CS9233 P0 input pin to +5V or ground, respectively.

In the normal memory map configuration (P0=1), the microcontroller program code and constant data are stored in external ROM. Up to 512Kx8 of external ROM and 32Kx8 of external RAM are directly supported in this configuration. The general memory map for the normal (ROM plus RAM) configuration is shown in Figure 2. The lowest 64Kx8 block of external ROM is automatically mapped into the microcontroller CODE space, and the remaining 448Kx8 of external ROM is mapped into the upper seven 64Kx8 pages of XDATA space. The 32Kx8 RAM and the microcontroller's internal memory-mapped peripheral devices are mapped into page 0 of the microcontroller XDATA space.

The $\overline{\text{EXTIO}}$ address block decode is provided to allow the addition of external I/O devices on the microcontroller bus with little or no additional glue logic. The $\overline{\text{EXTIO}}$ address decode is brought out to the CS9233 $\overline{\text{EXTIO}}$ output pin, and may be used in conjunction with the microcontroller data bus (D0-D7), read strobe ($\overline{\text{RD}}$), write strobe ($\overline{\text{WR}}$), and address bus (A0-A18) to interface with external peripherals. The $\overline{\text{EXTIO}}$ decode is useful in systems where external devices, such as switches, indicators, or other peripherals, must be controlled by the CS9233's on-chip microcontroller.

Figure 2 shows typical connections for a microcontroller memory complement of 32Kx8 SRAM and a 128Kx8 EPROM. If the CS9233 is using a 16 MHz crystal, these external memory devices must have a 120 nsec access time or better. The EPROM contains the microcontroller program code and tables of synthesis parameter data which define the instrument sounds for the application. The SRAM maps into the lower half of page 0 of the microcontroller's XDATA memory space. The lower half of the 128Kx8 EPROM maps into the microcontroller's 64Kx8 CODE space, and the upper half of the EPROM occupies page 1 of the XDATA space. In this example, pages 2 through 7 of XDATA memory space are not used.

The SRAM is addressed by the CS9233 address lines A0-A14, and A15 is used as a chip select. The EPROM is addressed using lines A0-A16. The ROMOE output from the CS9233 will be active any time the microcontroller accesses the CODE space or any of the upper seven pages of
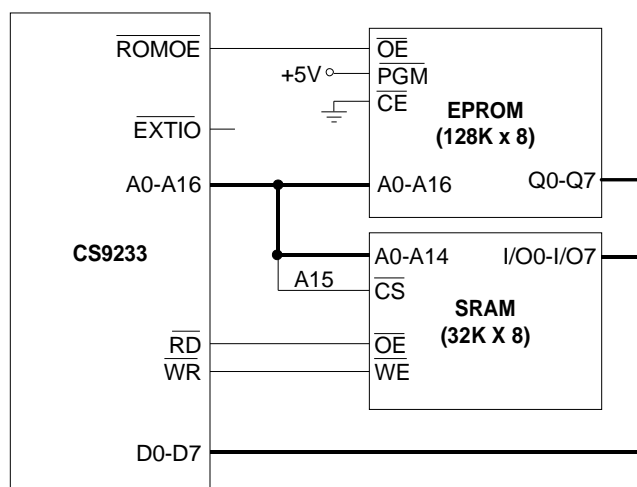
Figure 2. Typical Connection for Microcontroller Memory (128Kx8 EPROM + 32Kx8 SRAM).

data memory, allowing direct connection of ROM devices up to 512Kx8.

The hardware diagram and memory map for a typical ROMless configuration (P0=0) is shown in Figure 3. In this configuration the microcontroller program code and constant data are stored in external RAM memory. No ROM is used for the microcontroller. This configuration supports up to 512Kx8 of external RAM. At power up, or after a reset, the microcontroller automatically vectors to an on-chip bootstrap ROM. This ROM loads the RAM at power-up with a 256 byte program. This program then responds to a code load initiated by the host.
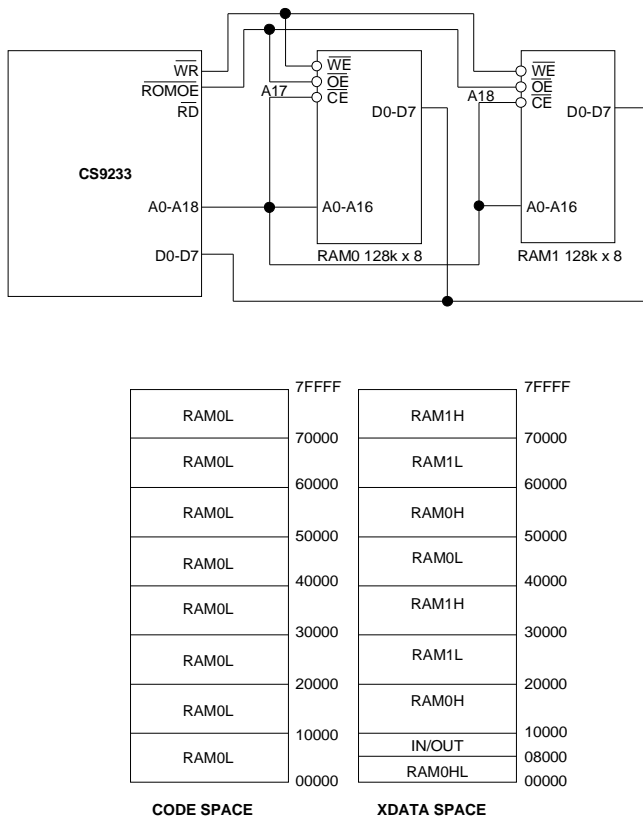

Figure 3. Typical Connections and Memory Map for ROMless Configuration.

Host Processor Interface

The CS9233 host processor interface logic provides a parallel interface to an ISA bus-based host processor. With appropriate firmware for the on-chip microcontroller, emulation of the industry standard AdLib and/or MPU-401 (UART Mode) register sets is possible. The host processor interface is also used for high-speed sample downloading when DRAM sample memory is used.

Externally, the host interface is comprised of two chip selects, $\overline{PCS0}$ and $\overline{PCS1}$; two interrupts, $\overline{IRQ0}$ and IRQ1; three address lines, PA0-PA2; and eight data lines, PD0-PD7. Normally, the $\overline{PCS0}$ chip select and $\overline{IRQ0}$ interrupt are used for AdLib register set emulation, and $\overline{PCS1}$ and IRQ1 are used for MPU-401 (UART mode) emulation. The external address and data lines are common to both register sets. Only one of the two chip selects may be active at a given time.

The external host writes to the CS9233 AdLib registers or MPU-401 registers using $\overline{PWR}$ strobe in conjunction with the appropriate chip select and the desired register address. When the host writes to the CS9233, the 3-bit register address, 8 bits of data, and a 1-bit register set ID (identifies chip select; 0 for $\overline{PCS0}$ or 1 for $\overline{PCS1}$) is captured in an internal 64 x 12-bit FIFO. An interrupt bit in the microcontroller is set to indicate that there is host data pending in the FIFO. The CS9233 microcontroller core can then read the data from the FIFO and interpret this data as appropriate for the register set being emulated.

The CS9233 microcontroller writes data to the host processor interface through the internal AdLib register set or the MPU-401 data registers. The external host may read from the AdLib register set ($\overline{PCS0}$ = 0) address 0, or from the MPU-401 register set ($\overline{PCS1}$ = 0) address 0 or 1. When the external host reads from the CS9233 AdLib register set address 0, it receives the data

which was written from the CS9233 microcontroller to the AdLib register set. An external host read from the CS9233 MPU-401 register set address 0 (the MPU-401 data register) returns the data which was written from the CS9233 microcontroller to the MPU-401 data register.

The CS9233 also has the ability to generate an interrupt, IRQ1, to the external host when data is available for the host to read from the MPU-401 data register. The CS9233 provides two hardware-generated status bits which may be read by the external host processor from the CS9233 MPU-401 register set address 1 (the MPU-401 status register). Bit 7 of the MPU-401 status register indicates when the CS9233's MPU-401 receive data register contains data which may be read by the host processor (bit 7 = 0 indicates data is waiting). Bit 6 of the MPU-401 status register indicates when the CS9233 host interface FIFO is full (bit 6 = 1 indicates FIFO is full). Bits 0-5 of the MPU-401 Status port are not used.

For PC multimedia applications where the CS9233 must be connected directly to the ISA bus, 24 mA buffering and ISA address decoding must be implemented externally. This external logic is depicted in Figure 4. However, in many cases, the CS9233 host interface signals can be connected directly to the external peripheral port of a multimedia CODEC such as the Crystal CS4232. The CS4232 provides the necessary buffering required to drive the ISA bus, and allows Plug and Play configuration for the CS9233 AdLib register set address. Figure 5 shows the typical connections between the CS9233 and the CS4232. In this application, the CS4232 provides a Plug and Play configurable MPU-401 (UART mode) register set emulation, so the CS9233 MPU-401 emulation is not used. MIDI
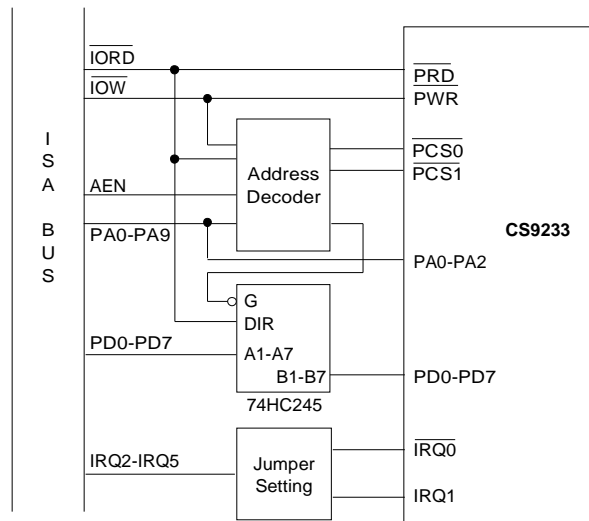
Figure 4. Typical Connection Diagram of CS9233 to ISA Bus
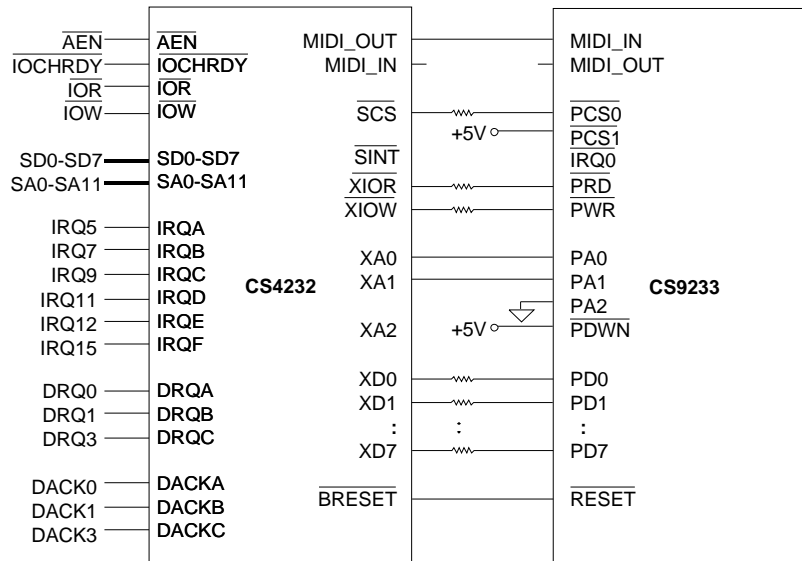
Figure 5. Typical Connections Between CS9233 and CS4232.

data is sent serially from the CS4232's MPU-401 compatible UART to the CS9233. Note that series termination resistors are recommended on the CS4232 $\overline{SCS}$, $\overline{XIOR}$, $\overline{XIOWR}$, and XD0-XD7 lines. The series terminators should be located near the CS4232 device. Typical values are 100 Ohms.

CS9233 Synthesis Processor

The CS9233 synthesis processor is a specialized signal processor designed for high-polyphony musical tone generation. The synthesis processor operates on a frame timing basis. The frame rate is equal to the CS9233 digital audio output word rate. The frame time is subdivided into 32 synthesis slots, and one synthesis algorithm is normally executed during each slot, allowing the generation of 32 simultaneous voices. The output data from each of the 32 synthesis slots is summed into four output accumulators which drive the main stereo output, DABD, and the stereo effects send, DAFD. The accumulator contents are shifted out the digital audio outputs once per synthesis frame. The synthesis processor is clocked at four times the CS9233 crystal frequency (64 MHz when using a 16 MHz crystal). A synthesis slot is 64 clock cycles long. The output word rate is equal to $1/(32$ slots x 64 clocks/slot x t_{clcl}), or 31.25 kHz when using a 16 MHz crystal.

Synthesis algorithms are stored in on-chip ROM. There are 11 synthesis algorithms plus three algorithms used to support DRAM sample memory. Synthesis parameters are stored in on-chip parameter RAM. The parameter RAM is divided into 32 blocks of 16 words per block. One block of parameter RAM is allocated to each of the 32 synthesis slot times which make up a synthesis frame. The parameter RAM word length is 19 bits.

The synthesis processor's internal data paths are 19-bits wide. The output sample data from each synthesis slot is accumulated into the four 24-bit output accumulators with separate level scaling for each accumulator. This allows separate control of the main left/right level and the reverb and chorus send level for each voice. Digital clipping circuitry is included to prevent the 24-bit output accumulators from overflowing.

Sample Memory Interface

The CS9233 can address up to a total of 8 Msamples of external PCM sample memory for wavetable synthesis. The external sample memory may be ROM, DRAM, or a combination of both. The sample memory address space is organized as 64 "pages" of memory, with each page containing 512 "waves" of 256 samples each. The end and loop addresses for each instrument sample fall on "wave boundaries" (multiples of 256 samples). A single instrument sample can occupy a maximum of one full page of memory (128 Ksamples). The data path to external sample memory is 12 bits wide. If 8-bit sample data is used, it is connected to the upper data lines WD4-WD11. The CS9233 has the ability to force the 4 lower data bits to zero internally when 8-bit sample memory is used, eliminating the need for external pull-down resistors on these lines.

The CS9233 provides on-chip sample memory address decoding to allow a glueless interface to external sample memory ROM devices. The $\overline{WCS0}$ and $\overline{WCS1}$ outputs are normally used to drive the active-low chip select inputs on external ROM devices. The CS9233 sample memory address decoding logic can be set to accommodate number of different external ROM configurations. The address decode logic to one of four possible configurations by the on-chip microcontroller. For one of these settings, $\overline{WCS0}$ and $\overline{WCS1}$ each decode a 512 Ksample address range (1 Msample total). The address ranges can be increased to 1 Msample per decode (2 Msample total), or 2 Msamples per decode (4 Msamples total). In the final configuration,

$\overline{\text{WCS0}}$ decodes a 4 Msample address range while $\overline{\text{WCS1}}$ decodes a 3 Msample address range (7 Msamples total). In any of these configurations, the upper 1 Msample address block of the CS9233's 8 Msample address range may be used for external DRAM sample memory. To utilize more than 1 Msample of DRAM, external address decoding logic is required. Figure 6 depicts the address range decode options for the $\overline{\text{WCS0}}$ and $\overline{\text{WCS1}}$ output signals.

The sample memory address is output over the CS9233 WA0-WA22 output pins. The sample memory address is output in a time-division multiplexed manner on lines WA0-WA11 to allow a glueless interface to DRAM sample

memory. The time division multiplexing of the CS9233 sample memory address bus is depicted in Figure 8 and in Table 1. DRAM devices demultiplex the address using the CS9233 $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ outputs. When external DRAM is used for PCM sample memory, one synthesis slot may be used for DRAM refresh, eliminating the need for off-board support logic. The CS9233 uses a $\overline{\text{CAS}}$ berfore $\overline{\text{RAS}}$ refresh cycle. Three refresh cycles occur during the synthesis refresh slot (once per synthesis frame). See Figure 7.

The entire 23-bit wide address bus is valid one clock cycle after the end of the $\overline{\text{CAS}}$ strobe (denoted time "$\overline{\text{CAS}}$+1" in accompanying figures), allowing direct connection of standard ROM devices.
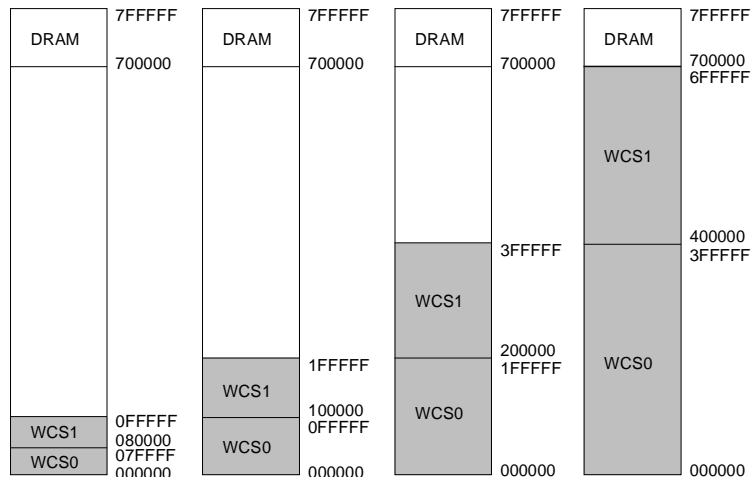

Figure 6. Four Configurations for WCS0/WCS1.

TIME	WA11	WA10	WA9	WA8	WA7	WA6	WA5	WA4	WA3	WA2	WA1	WA0
($\overline{\text{RAS}}$)	$\overline{\text{DRWE}}$	A20	A18	A17	A7	A6	A5	A4	A3	A2	A1	A0
($\overline{\text{CAS}}$)	A22	A21	A19	A16	A15	A14	A13	A12	A11	A10	A9	A8
($\overline{\text{CAS}}$+1)	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TIME	WA22	WA21	WA20	WA19	WA18	WA17	WA16	WA15	WA14	WA13	WA12
($\overline{\text{RAS}}$)	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
($\overline{\text{CAS}}$)	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
($\overline{\text{CAS}}$+1)	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12

Note: ($\overline{\text{CAS}}$ + 1) corresponds to one clock cycle after the falling edge of the $\overline{\text{CAS}}$ strobe.

Table 1. Sample Memory Address Multiplexing on WA0 - WA11 .
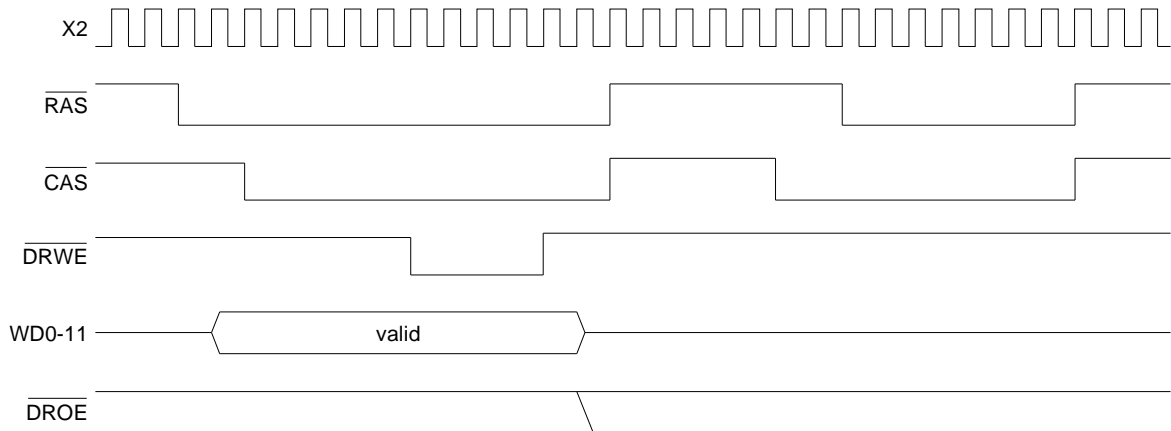
**Figure 7. External RAM Write, $\overline{CAS}$ Before $\overline{RAS}$ Refresh.**
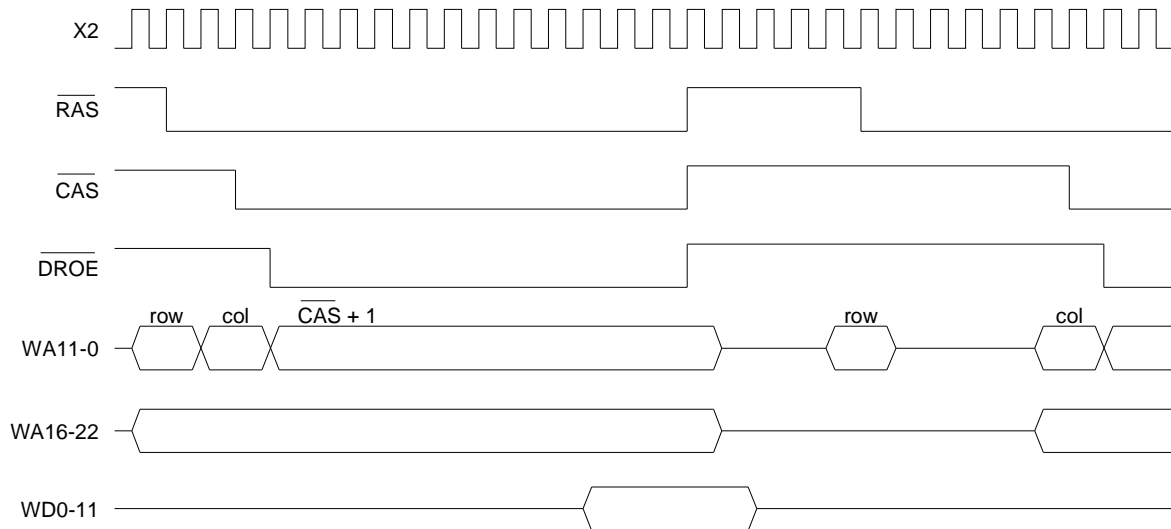
**Figure 8. Typical External Memory Read Sequences.**

Figure 9 shows a typical connection diagram of the CS9233 to the Crystal Semiconductor CS4112 1Mx8-bit PCM sample ROM and 512Kx8 DRAM. Figure 10 illustrates the connection to a 4Mx8 ROM sample memory with 1Mx12 DRAM.

Parallel Effects Send Interface for CS8905/CS8905A Effects Processor

The Crystal Semiconductor CS8905/CS8905A Programmable Effects Processor makes an excellent digital effects co-processor for the CS9233. The reverberation and chorusing effects pro-
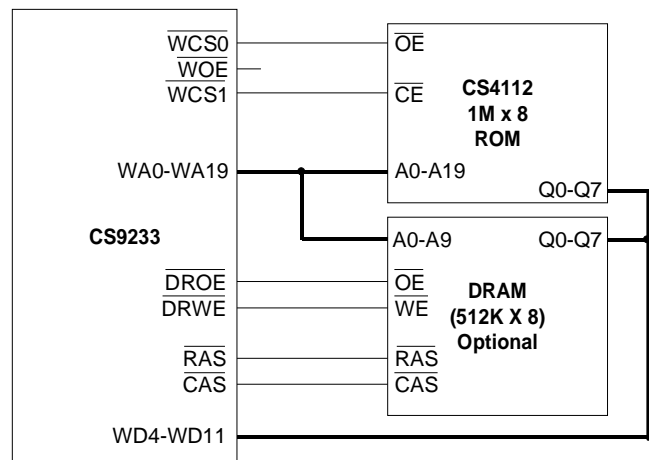
**Figure 9. Typical Connection for 1Mx8 Sample ROM with Optional DRAM Connection Shown.**
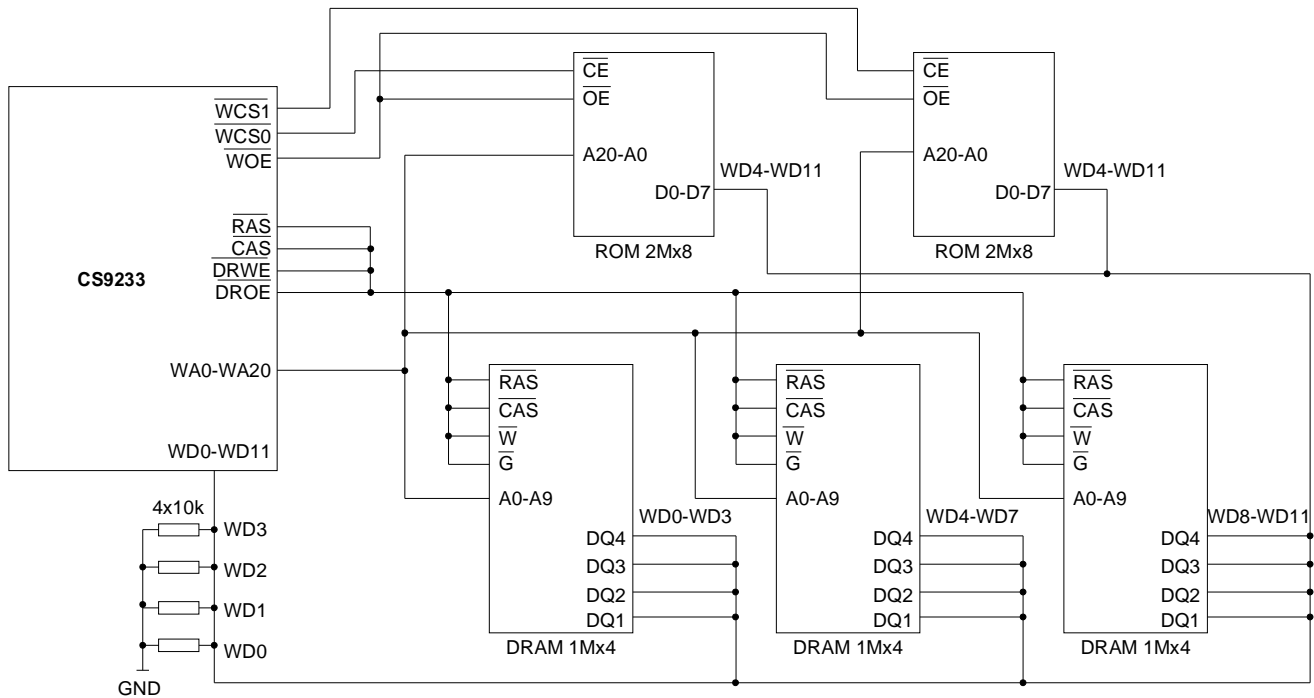
**Figure 10. Typical Connection for 4Mx8 Sample ROM + 1Mx12 DRAM.**

duced by the effects processor enhances the richness and depth of the CS9233 audio output. The CS9233 includes all of the necessary interface logic to allow a direct connection of the CS8905/CS8905A and the associated RAM device. No external interface or glue logic is required. The CS9233 provides a master clock to the effects processor at either 32 MHz (CS8905) or 64 MHz (CS8905A). A typical connection diagram for the CS9233 and the CS8905A Effects Processor is given in Figure 11.

Digital Audio Outputs

The CS9233 synthesis processor provides a main 18-bit stereo digital audio output, DABD, and a stereo effects send output, DAFD. The CS9233's digital effects return mixer circuit provides a stereo digital audio effects return input, DAAD, and a third digital audio output, DAMD, which is a combination of the main DABD output and the DAAD effects return. The CS9233 provides three digital audio clock output signals which are common to the DABD, DAFD, DAAD and DAMD digital audio data signals. These clock
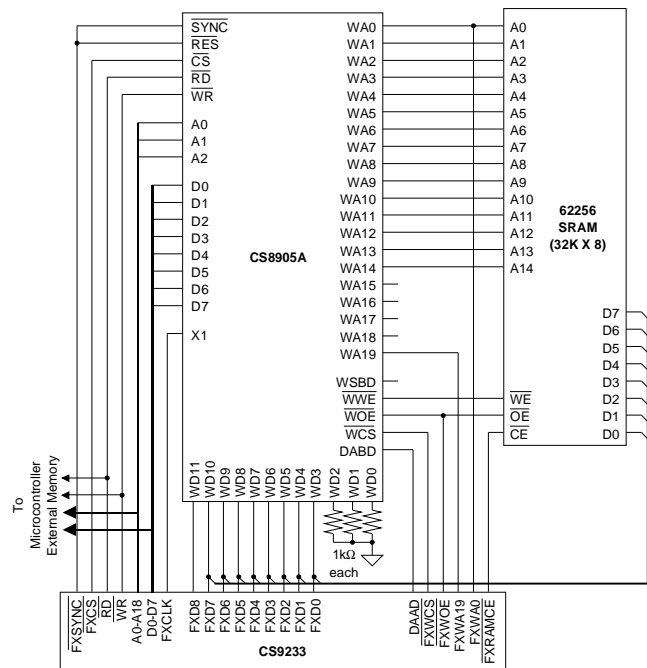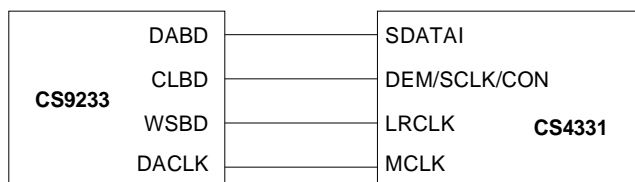

Figure 11. Typical Connection Diagram of CS9233 to CS8905/CS8905A Effects Processor
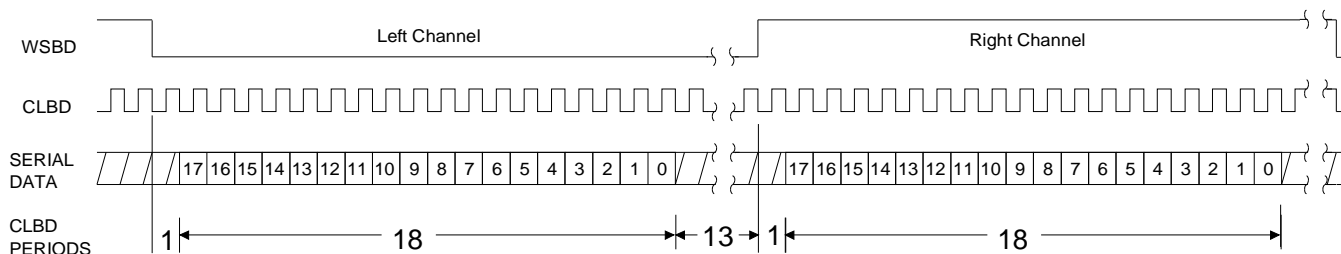
Figure 12. Typical Digital Audio Transfer Sequence.

signals are the left/right clock signal WSBD, the bit clock CLBD, and the 256Fs clock DACLK. All serial digital audio outputs are compatible with the Crystal Semiconductor CS4331 18-bit Stereo DAC. Figure 12 illustrates the CS9233 digital audio timing. Figure 13 shows the typical connections between the CS9233 and the CS4331 18-bit stereo DAC.

Effects Return Digital Mixer

When the CS8905/CS8905A external effects processor is used, the digital audio output from the effects processor is returned to the CS9233 at the CS9233 DAAD input. The effects return signal is internally mixed with the CS9233 main output, and the resulting mixed signal output, DAMD, is sent to the serial DAC. In this case, the DABD output is not connected. The formula used for adding the channels is:

DAMD = 0.5*DABD +DAAD.

Crystal Oscillator and PLL Circuitry

All CS9233 internal timing is generated from a single master clock. A Phase-Locked Loop (PLL) clock multiplier circuit is utilized to derive higher speed clocks from the master clock. The master clock may be generated using the on-chip crystal oscillator circuit, or a clock may be supplied from an external oscillator source. The on-chip oscillator circuit requires requires a fundamental-mode crystal (typically 16 MHz),

Figure 13. Typical Connection to CS4331 DAC.

compensated for a parallel resonant circuit with standard 20pF loading. The crystal is connected to the X1 and X2 signals at pins 99 and 98. External loading capacitors should be connected from each side of the crystal to ground as shown in Figure 1. Trace lengths should be kept to a minimum, and the board layout should include ground plane beneath the oscillator circuit components.

If an external oscillator source is utilized, the oscillator output is connected to the CS9233 X1 input at pin 99. Trace lengths should be kept to a minimum. The ground from the oscillator circuit should be a direct connection to the CS9233 GND at pin 100.

The PLL circuit generates a 2X clock (32 MHz) for the microcontroller and a 4X (64 MHz) clock for the synthesis processor. All digital audio

clocks are derived directly from the oscillator output (pre-PLL) to minimize jitter. The PLL clock multiplier requires an external passive low-pass filter circuit connected to the CS9233 LFT pin. The LFT filter circuit is illustrated in Figure 1.

Power-up Reset

The CS9233 $\overline{\text{RESET}}$ signal initializes all internal functions of the chip. At initial power-on, the the $\overline{\text{RESET}}$ input must be held low until the oscillator circuit has stabilized. The CS9233 internal oscillator is enabled during $\overline{\text{RESET}}$, other functions of the device are held in an idle mode while $\overline{\text{RESET}}$ is low.

Power-Down

The CS9233 provides a power-down mode which can be initiated externally using the $\overline{\text{PDWN}}$ pin. Power-down mode is terminated only by application of the $\overline{\text{RESET}}$ signal.

Power Supply, Ground, and Decoupling

All power and ground pins on the CS9233 device should be connected to the appropriate supply planes using the shortest trace lengths possible. Recommended decoupling consists of four 0.1uF ceramic decoupling capacitors between VCC and GND, one at each of the four sides of the IC. These capacitors should be placed as close to the IC as possible. In addition, place one high-quality 10uF Aluminum Electrolytic or 10uF Tantalum capacitor from VCC and pin 3 to GND at pin 5 with minimum trace and lead lengths.

PIN DESCRIPTIONS
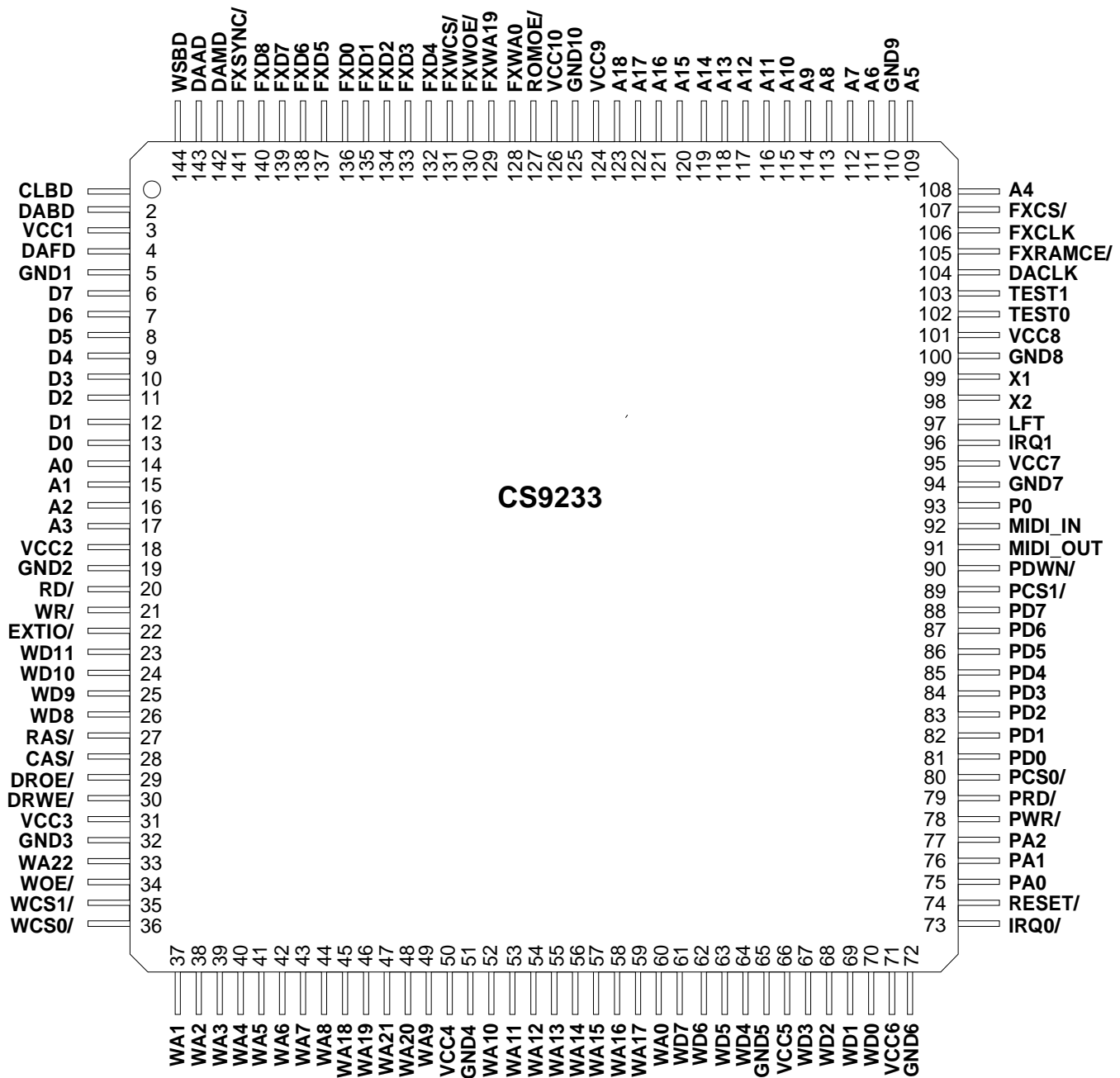
Power and Ground

GND - Power Ground. PINS 5, 19, 32, 51, 65, 72, 94, 100, 110, 125.
Ground pins. All ground pins should be connected to a low impedance ground plane.

VCC - Power +5V, ±5%. PINS 3, 18, 31, 50, 66, 71, 95, 101, 124, 126.
+5V power input pins. All V_{CC} pins should be connected to a low impedance +5V supply.

Serial MIDI Interface

MIDI_IN - Serial MIDI_IN, TTL Level. PIN 92.
> This input is used to receive serial MIDI data from an external MIDI device.

MIDI_OUT - Serial MIDI_OUT, TTL Level. PIN 91.
> This output is used to send serial MIDI data out to an external MIDI device.

External Host Processor Interface

PD0 - PD7 - Host Processor Data Bus. PINS 81 - 88.
> These bidirectional data lines are used to transfer parallel data between the CS9233 and an external host processor. The CS9233 host interface is normally used to emulate MPU-401 (UART Mode) and/or the AdLib register sets in the ISA environment.

PA0 - PA2 - Host Processor Address Bus. PINS 75 - 77.
> These input address lines are used in conjunction with the PD0-PD7, $\overline{PCS0}$, $\overline{PCS1}$, $\overline{IRQ0}$, and IRQ1 signals to transfer data between the CS9233 and an external host processor. The CS9233 host interface is normally used to emulate MPU-401 (UART Mode) and/or the AdLib register sets in the ISA environment, and the PA0-PA2 address lines are used to identify a logical register location within the emulated register set(s).

$\overline{PCS0}$, $\overline{PCS1}$ - Host Processor Chip Selects. Active Low. PINS 80, 89.
> These chip select inputs are used in conjunction with the PD0-PD7, PA0-PA2, $\overline{IRQ0}$, and IRQ1 signals to transfer data between the CS9233 and an external host processor. The CS9233 host interface is normally used to emulate MPU-401 (UART Mode) and/or the AdLib register sets in the ISA environment. The $\overline{PCS0}$ chip select is used for AdLib register emulation, and $\overline{PCS1}$ is used for MPU-401 (UART Mode) emulation. These signals should be tied to +5V when not used.

$\overline{IRQ0}$ - Interrupt Request 0. Active Low. PIN 73.
> The $\overline{IRQ0}$ and $\overline{IRQ1}$ interrupt outputs are used in conjunction with the PD0-PD7, PA0-PA2, $\overline{PCS0}$, and $\overline{PCS1}$ signals to transfer data between the CS9233 and an external host processor. The CS9233 host interface is normally used to emulate MPU-401 (UART Mode) and/or the AdLib register sets in the ISA environment. The active low $\overline{IRQ0}$ output signal is asserted by the CS9233 to interrupt the external host processor as required for the AdLib register set emulation.

IRQ1 - Interrupt Request 1. Active High. PIN 96.
> The $\overline{IRQ0}$ and $\overline{IRQ1}$ interrupt outputs are used in conjunction with the PD0-PD7, PA0-PA2, $\overline{PCS0}$, and $\overline{PCS1}$ signals to transfer data between the CS9233 and an external host processor. The CS9233 host interface is normally used to emulate MPU-401 (UART Mode) and/or the AdLib register sets in the ISA environment. The active high IRQ1 output signal is asserted by the CS9233 to interrupt the external host processor as required for the MPU-401 (UART Mode) register set emulation.

PWR - Host Processor Write Strobe. Active Low. PIN 78.
This active low input strobe causes the data on lines PD0-PD7 to be written to the CS9233 register emulation logic (see PD0-PD7, PA0-PA2, PCS0, PCS1, IRQ0, IRQ1).

PRD - Host Processor Read Strobe. Active Low. PIN 79.
This active low input strobe causes the CS9233 to output data from the CS9233 register emulation logic on lines PD0-PD7 (see PD0-PD7, PA0-PA2, PCS0, PCS1, IRQ0, IRQ1).

On-chip Microcontroller RAM, ROM, Effects Processor, & I/O interface

A0-A18 - On-Chip Microcontroller Address Bus. PINS 14 - 17, 108-109, 111-123.
These address output lines from the CS9233's internal microcontroller are used to address the microcontroller's external RAM and program ROM, the optional CS8905/CS8905A effects processor control registers, and expansion I/O.

D0-D7 - On-Chip Microcontroller Data Bus. PINS 13-6.
These bidirectional data lines are used to transfer data between the CS9233's internal microcontroller and the microcontroller's external RAM and program ROM, the optional CS8905/CS8905A effects processor control registers, and expansion I/O.

ROMOE - Read Strobe for External ROM. Active Low. PIN 127.
This active low output strobe is asserted by the CS9233's internal microcontroller to read data from the external program ROM. This output is high while the CS9233's microcontroller reads from external RAM, the effects processor control registers, or expansion I/O.

RD - Read Strobe for External RAM, Effects Processor, I/O. Active Low. PIN 20.
This active low output strobe is asserted by the CS9233's internal microcontroller to read data from external RAM, the effects processor control registers, or expansion I/O.

WR - Write Strobe for External RAM, Effects Processor, I/O. Active Low. PIN 21.
This active low output strobe is asserted by the CS9233's internal microcontroller to write to external RAM, the effects processor control registers, or expansion I/O.

EXTIO - Additional External I/O Decode. Active Low. PIN 22.
This active low address decode signal is asserted by the CS9233's internal microcontroller to indicate accesses to the expansion I/O space.

External Effects Processor Parallel Interface

FXSYNC - Effects Processor Sync Output. Active Low. PIN 141.
This active low signal is used for synchronization between the CS9233 and the CS8905 effects processor.

FXCLK - Effects Processor Master Clock Output (64 MHz). PIN 106.

This clock signal output is used as the master clock for the CS8905/CS8905A effects processor. The CS9233 is capable of switching the FXCLK frequency to 32 MHz for use with the original CS8905 device

$\overline{\text{FXCS}}$ - Effects Processor Chip Select Output. Active Low. PIN 107.

This active low chip select output signal is asserted by the CS9233's internal microcontroller to indicate an access to the CS8905/CS8905A effects processor control registers.

$\overline{\text{FXWCS}}$ - Effects Processor CS Input. Active Low. PIN 131.

This active low input to the CS9233 is used to indicate an effects data request from the CS8905/CS8905A effects processor. This pin should be tied to Vcc if not being used.

$\overline{\text{FXWOE}}$ - Effects Processor OE Input. Active Low. PIN 130.

This active low input to the CS9233 is used to indicate an effects data request from the CS8905/CS8905A effects processor. This pin may be tied to the $\overline{\text{WOE}}$ output of the CS8905 effects processor. This pin should be tied to Vcc if not being used.

FXWA19 - Effects Processor WA19 Input (Data Type Select). PIN 129.

This input to the CS9233 is used in conjunction with the $\overline{\text{FXWCS}}$ and $\overline{\text{FXWOE}}$ signals to enable the CS8905/CS8905A to read effects data from the external delay buffer RAM or from the CS9233. This pin should be tied to either Vcc or ground if not being used.

FXWA0 - Effects Processor WA0 Input (Byte Select). PIN 128.

This input to the CS9233 is used to select whether a high or low byte of effects data is being transferred across the FXD0-FXD8 data lines. This pin should be tied to either Vcc or ground if not being used.

FXD0 - FXD8 - Effects Processor Send Data Bus. PINS 136-132, 137-140.

This tri-state data bus output from the CS9233 is used to transfer effects data from the CS9233 to the CS8905 effects processor. FXD7 (Pin 139) should be tied to ground if the interface is not being used.

$\overline{\text{FXRAMCE}}$ - Effects Processor RAM Chip Enable Decode Output. Active Low. PIN 105.

This active low output from the CS9233 is a chip enable for the delay buffer RAM used by the CS8905/CS8905A for effects processing. The $\overline{\text{FXRAMCE}}$ signal will be active when both $\overline{\text{FXWCS}}$ is active and FXWA19 is at a logic low level.

PCM Sample ROM/DRAM Interface

WA0-WA22 - PCM Sample ROM/DRAM Address. PINS 60, 37-44, 49, 52-59, 45-46, 48, 47, 33

These address output lines are used to address external PCM sample memory.

WD0-WD11 - PCM Sample Data, PINS 70-67, 64-61.

These bidirectional data lines are used to pass PCM sample data between the CS9233's synthesis core and external PCM sample memory.

$\overline{\text{WCS0}}$, $\overline{\text{WCS1}}$ - Programmable PCM ROM Chip Selects. Active Low. PINS 36, 35.

    These active low chip select output signals are PCM ROM chip selects from the CS9233 synthesis engine. The decode logic within the CS9233 which generates these chip selects is configured by the CS9233's internal microcontroller.

$\overline{\text{WOE}}$ - PCM ROM Output Enable. Active Low. PIN 34.

    This active low output signal is an output enable for the external PCM ROM memory.

$\overline{\text{RAS}}$ - PCM DRAM Row Address Strobe. Active Low. PIN 27.

    This memory address strobe output is used in conjunction with the address output lines WA0-WA22 to address DRAM sample memory.

$\overline{\text{CAS}}$ - PCM DRAM Column Address Strobe. Active Low. PIN 28.

    This memory address strobe output is used in conjunction with the address output lines WA0-WA22 to address DRAM sample memory.

$\overline{\text{DROE}}$ - PCM DRAM Output Enable. Active Low. PIN 29.

    This active low output signal is an output enable for external DRAM sample memory.

$\overline{\text{DRWE}}$ - PCM DRAM Write Enable. Active Low. PIN 30.

    This active low output signal is a write strobe for external DRAM sample memory.

Digital Audio I/O

DACLK - Master clock for oversampling DAC 256X fs (8 MHz). PIN 104.

    The output from the CS9233 provides a clock signal at 256 times the CS9233 output word rate.

DABD - Stereo Synthesis Digital Audio Output. PIN 2.

    This output is the primary stereo serial digital audio output from the CS9233.

DAFD - Stereo Effects Send Digital Audio Output. PIN 4.

    This output is the effects send stereo serial digital audio output from the CS9233.

DAAD - Stereo Effects Return Digital Audio Input. PIN 143.

    This input is the serial digital audio effects return input from an external effects processor such as the CS8905. This pin should be tied to ground if not being used.

DAMD - Stereo Mix Digital Audio Output (Synth + Effects). PIN 142.

    This stereo serial digital audio output represents a mix of the DABD output signal and the DAAD effects return signal.

CLBD - Digital Audio Bit Clock. PIN 1.

    This output signal is the bit clock for the CS9233 digital audio signals DABD, DAFD, DAAD and DAMD.

WSBD - Digital Audio Word Select (Left/Right Clock). PIN 144.

This output signal is the left/right word clock for the CS9233 digital audio signals DABD, DAFD, DAAD and DAMD.

Control and Miscellaneous I/O

P0 - Normal Microcontroller Memory Map Select. PIN 93.

This active high input pin is used to select the normal (ROM + RAM) memory map for the CS9233's internal microcontroller. When the P0 input signal is tied low, the ROMless memory map option is selected.

$\overline{\text{RESET}}$**- Reset Input, Schmidt trigger input. Active Low. PIN 74.**

This active low input to the CS9233 is used to reset and initialize the CS9233.

$\overline{\text{PDWN}}$ **- Power Down Input. Active Low. PIN 90.**

This active low input may be used to force the CS9233 into a low power consumption state. This signal must be pulled high for normal operation.

X1 - 16 MHz Oscillator Input (crystal or clock source). PIN 99.

A 16 MHz crystal, with 22 pF loading capacitance, may be connected between this pin and X2. If the on-chip crystal oscillator is not used, then an external oscillator clock source may be connected to this pin, with X2 left floating.

X2 - 16 MHz Oscillator Output. PIN 98.

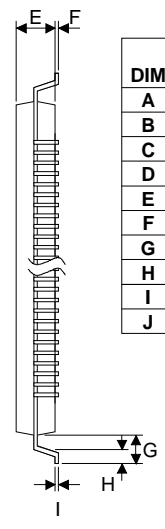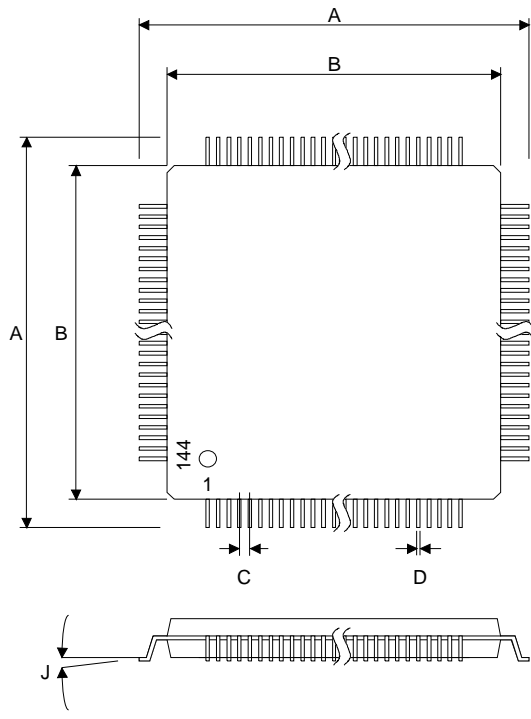This signal is the internal oscillator output.

TEST0, TEST1 - Test Mode Inputs. PINS 102-103.

These inputs should be connected to ground during normal operation.

LFT - PLL External R-C network connection. PIN 97.

This pin must be connected to ground through a series 100Ω resistor and 0.01μF capacitor.

MECHANICAL DESCRIPTION

144-pin TQFP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.00 BSC.		0.8661 BSC.	
B	20.00 BSC.		0.7874 BSC.	
C	0.50 BSC.		0.0197 BSC.	
D	0.17	0.27	0.0067	0.0106
E	1.35	1.45	0.0531	0.0571
F	0.05	0.15	0.0020	0.0059
G	1.00 REF		0.0394 REF	
H	0.45	0.75	0.0177	0.0295
I	-	0.08	-	0.0031
J	0°	7°	0°	7°

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