GC201

EGA / MULTI-MODE GRAPHICS CONTROLLER

FEATURES

- 160 pin single chip design
- 100% EGA, CGA, MDA and Hercules hardware & software compatible
- Built in auto mode switch logic
- All video modes software switchable and supported on EGA type monitors
- 4 plane bit mapped graphics capability
- Soft scrolls, pans, and windows, through a 1 Meg. pixel memory
- Supports 256K bytes of memory using 64K x 4 DRAMS
- Light pen interface
- Double scan capability for better CGA appearance. 320 x 200, 640 x 200 displayed as 320 x 400 and 640 x 400
- Hercules supported on CGA type monitors

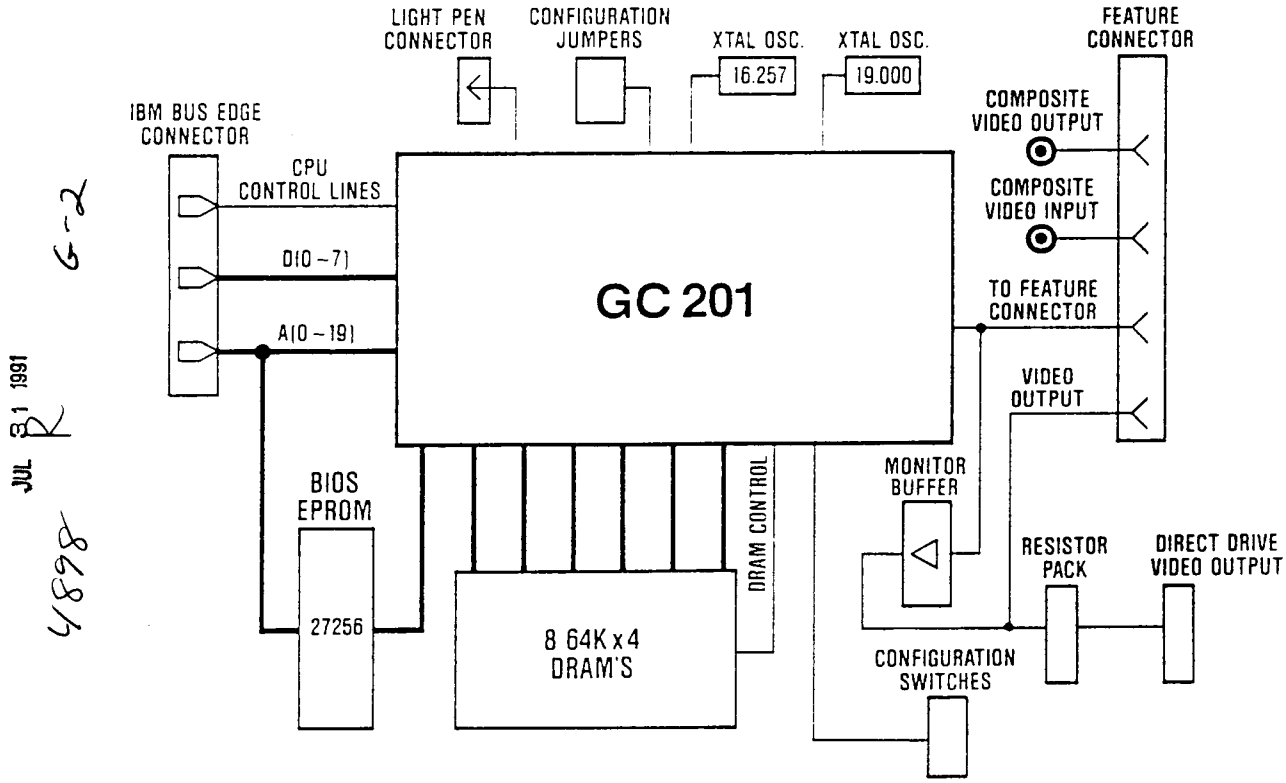
DESCRIPTION

The GC201 Multi Mode Video Controller presents an optimum approach to achieving an IBM compatible display adapter. The chip provides a low cost solution, and maximizes the options available to the user. Only 1 additional chip plus-memory is required to implement an EGA, CGA, MDA, and Hercules adapter.

The GC201 consists of a combined Graphics Controller, Sequencer, and Attributes Controller, (GSA Controller). The GSA Controller is optimized for CGA, MDA, and Hercules by pre)loading EGA registers. All display modes can be achieved on an EGA compatible monitor. Subsets can be achieved on monochrome or color monitors.

Compatibility with the IBM CGA, MDA, and the Hercules graphics card is achieved with a CRT controller. On chip this controller can be operated as anEGA CRTC, or as a 6845S CRTC.

The IBM Color Graphics Adapter is supported with EGA emulation modes, or through complete hardware compatibility. The MDA, and Hercules modes can be displayed on a TTL monochrome monitor, or, alternatively, on an EGA color monitor. Monochrome modes can be displayed on EGA type monitor with multiple combinations of colors such as green/black and amber/black. In addition, color simulation support for 16 shades of gray on monochrome display is provided.



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Preliminary

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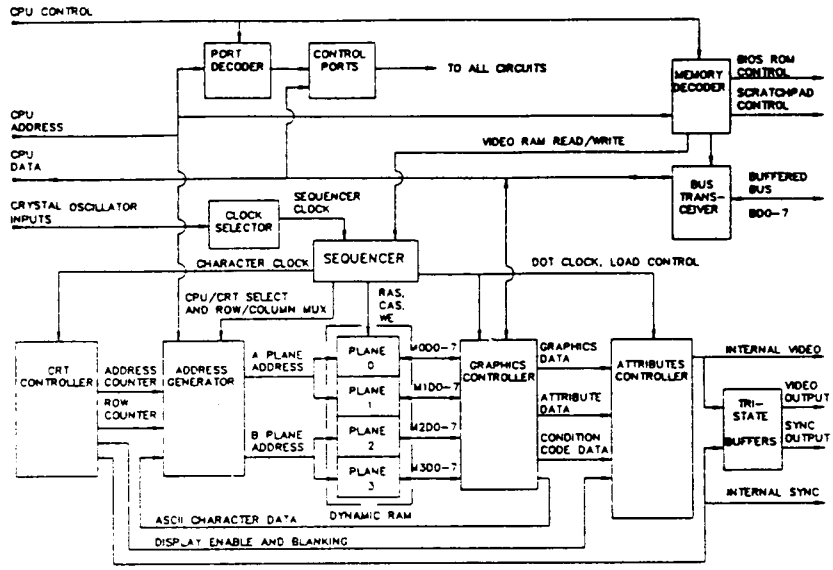
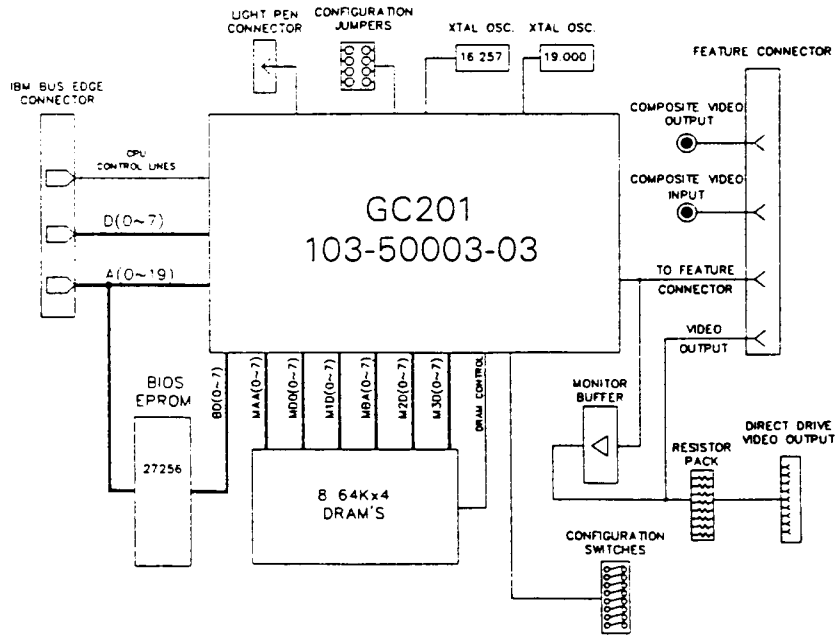
Functional Diagram



TEST BOARD:



MULTI MODE GRAPHICS

NUMBER OF COLORS	PIXELS	DOT CLOCK MHz
16	640 x 200 320 x 200	14.318
16	640 x 350	16.257
16	640 x 480	24.0
16	752 x 410	24.0
16	800 x 600	34.0
MONOCHROME	720 x 350	16.257

BIOS:

G-2 will provide an IBM compatible EGA BIOS to its customers free of charge. This BIOS will allow the end user full access to all the features of the GC201.

DRIVERS:

G-2 is committed to writing custom software drivers to support the high resolution features of the GC201.

TEST SOFTWARE:

G-2 will provide the customer with test software to enable quick testing of the GC201.

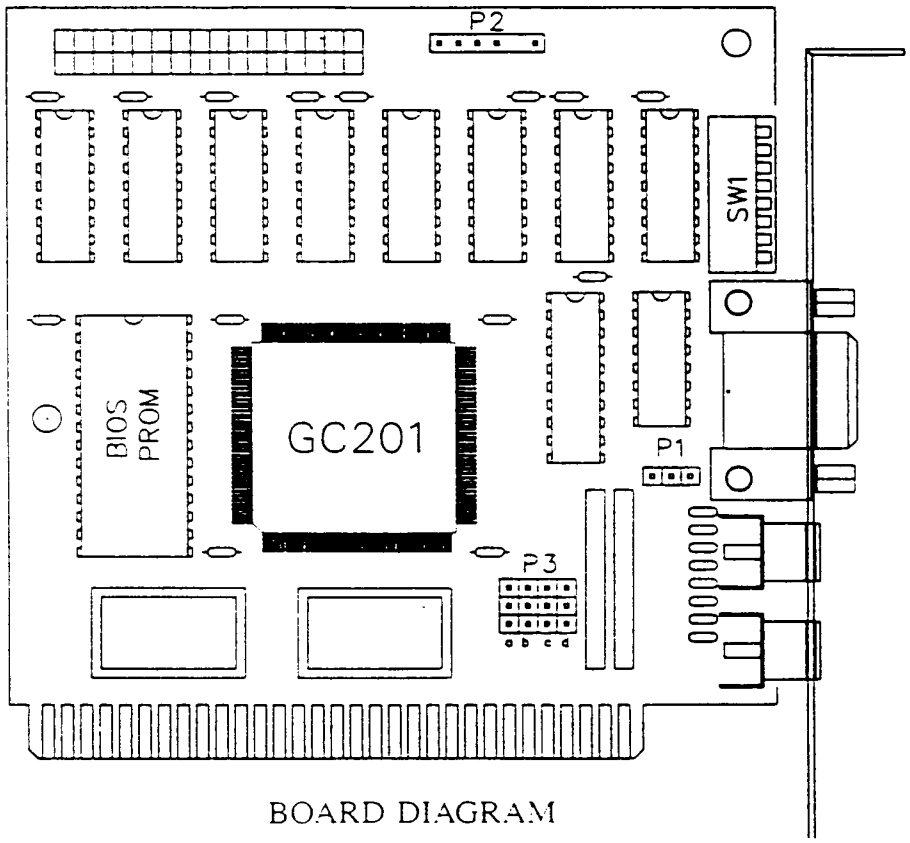
MANUFACTURING DOCUMENTATION:

G2 will provide full manufacturing documentation, including PWB artwork, material lists and mechanical specification.

TEST BOARD

GC201 OEM Test Board Description

The GC201 OEM test board represents a typical GC201 Multi Function Video Controller implementation. This typical implementation consists of the GC201 (single chip) video controller, 256k bytes of RAM (using 8 64k×4-bit dynamic RAMS), EGA BIOS, and one LS244TTL driver to provide drive signal compatibility with IBM Enhanced Color Displays.



BOARD DIAGRAM

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Absolute Maximum Ratings

V_{SS} = 0 V
T_A = 25 C

PARAMETER	SYMBOL	LIMITS	UNITS
Power Supply Voltage	V_{DD}	$V_{SS}-0.3$ to 7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Input Current	I_{IN}	±10	mA
Output Current	I_{OUT}	±10	mA
Power Consumption	PD	100	mW
Power Supply Current*	I_{DD}/I_{SS}	±40	mA
Storage Temp.	T_{STG}	−65 to 150	C

NOTE: * Power Supply Current: Is the allowable current flow in or out of the power terminals (V_{DD} or V_{SS})

Recommended Operating Conditions (TTL Input)

V_{SS} = 0V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temp.	T_{OPR}	0		70	C

Electrical Characteristics

V_{SS} = 0V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current	I_{DDS}	V_{DD} = MAX			100	uA
Input Leak	I_L		−10		10	uA
Input Voltage "H"	V_{IH}	V_{DD} = 5.25V	2.0			V
Input Voltage "L"	V_{IL}				0.8	V
Output Voltage "H"	V_{OH}	I_{OH} = 2.4.8 mA	V_{DD} −0.4			V
Output Voltage "L"	V_{OL}	I_{OL} = 4.6.14 mA V_{DD} = 4.75V			V_{SS} +0.4	V

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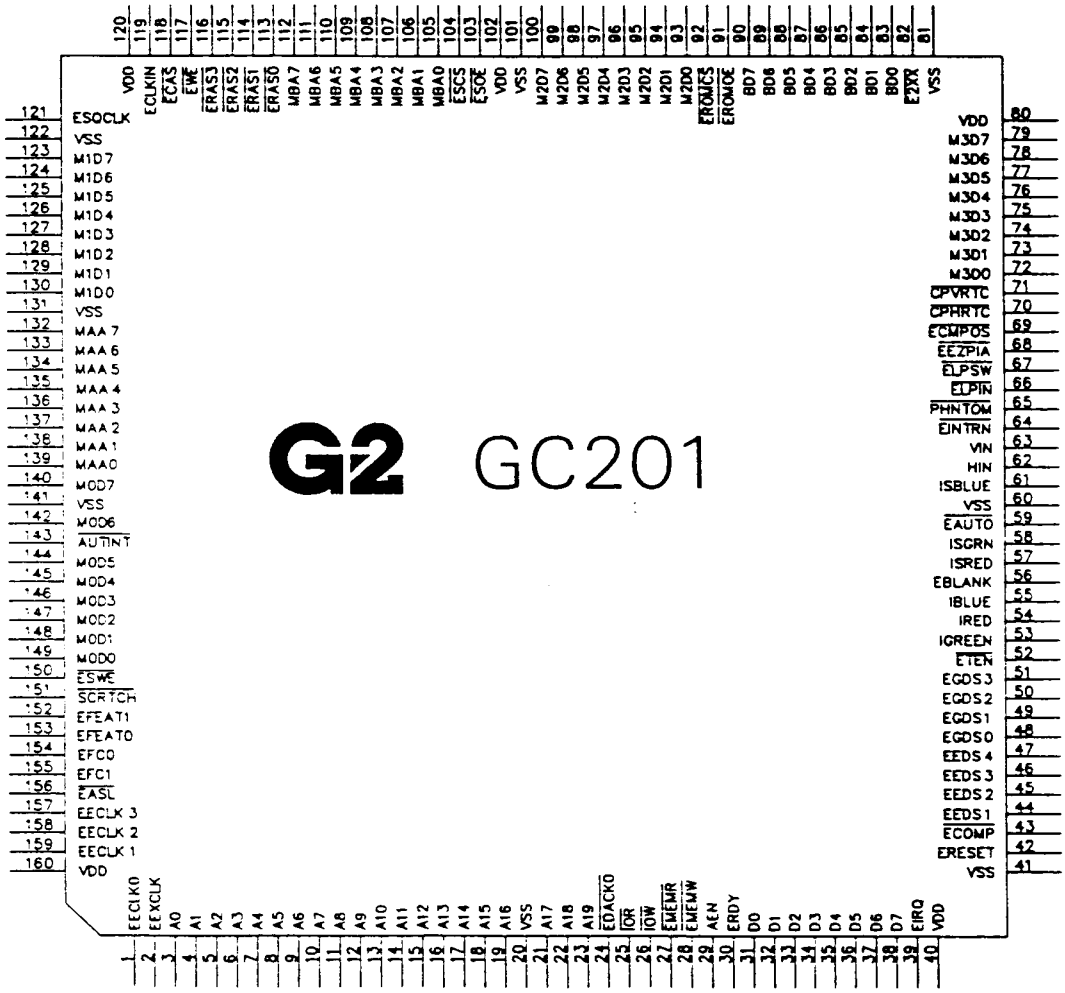
PIN ASSIGNMENT



Pin Description (/ = an active low signal)

VSS	20 41 60 81 101 122 131 141	Power	Chip ground
VDD	40 80 102 120 160	Power	Chip 5VDC supply
AEN	29	Input	AEN is an active high signal, from the CPU bus, that disables access to the ports.
EECLK0	1	Input	EECLK0 is the standard EGA colour card clock, which is connected to the system bus. It is 14.318 MHz.
EECLK1	159	Input	EECLK1 is the standard EGA clock, that is connected to the 16.257 MHz. oscillator package.
EECLK2	158	Input	This is a standard external clock input, from the feature connector.
EECLK3	157	Input	EECLK3 is an external clock, from a crystal oscillator module, that can be internally selected. It is meant to be 19.000 MHz., and is used for Hercules emulation on an EGA type monitor.
EEDS1 EEDS2 EEDS3 EEDS4	44 45 46 47	Input	EEDSW1-4 are the standard EGA dip switch inputs
EEXCLK	2	Input	EEXCLK is an optional clock input that can be internally selected.
EFEAT1 EFEAT0	152 153	Input	EFEAT0-1 are inputs from the feature connector, to the EGA status port 0
EGDS0 EGDS1 EGDS2 EGDS3	48 49 50 51	Input	EGDSW0-3 are inputs from a dip switch that sets configuration modes.
ESQCLK	121	Input	ESQCLK is the sequencer clock input. It is normally driven by signal ECLKIN
/CPHRTC	70	Input	CPHRTC is connected to a board jumper. When it is grounded, the polarity of signals HIN, and HOUT is reversed.
CPVRTC	71	Input	CPVRTC is connected a to board jumper. When it is grounded, the polarity of signals VIN, and VOUT is reversed.
E2XX	82	Input	E2XX is a jumper used to select the I/O address range: 1 = Port addresses are 3XXh 0 = Port addresses are 2XXh
EAUTO	59	Input	EAUTO is an active low jumper input used to enable the auto mode switch interrupt of the MASTER CONTROL PORT 1 is properly programmed.
/ECMPOS	69	Input	ECMPOS is connected to a board jumper. When it is grounded, VIN and VOUT become composite sync outputs.
EDACK0	24	Input	EDACK0 is an active low signal from the CPU bus, that indicates a DMA access. When this signal is low, accesses to the EGA memory devices are inhibited.
EEZPIA	68	Input	EEZPIA This pin is connected to +5 VDC, for proper operation.
ELPIN	66	Input	ELPIN is an active low signal, that is driven by the light pen. When this signal transitions from high to low, the light pen latch is set, and the light pen register is loaded.
ELPSW	67	Input	This is an active low input, from a light pen switch.
EMEMR	27	Input	EMEMR is an active low signal, from the CPU bus, that initiates a read cycle to the video RAM when it is low.
EMEMW	28	Input	EMEMW is an active low signal, from the CPU bus, that initiates a write cycle to video RAM when it is low.
/ETEN	52	Input	ETEN Is an active low input used for internal testing and MUST be connected to + 5 VDC, for proper operation.
/SCRTCH	153	Input	SCRTCH This pin MUST be connected to +5 VDC, for proper operation.
IOR	25	Input	I/O Read is an active low signal from the CPU bus, that enables reads from ports.
IOW	26	Input	I/O Write is an active low signal from the CPU bus, that enables writes to the ports.
EBLANK	56	Output	EBLANK is an active high output that forces the display to black when it is asserted.
ECLKIN	119	Output	ECLKIN is the sequencer clock that is internally selected from the clock inputs. It is normally connected to ESQCLK.
EFC0 EFC1	154 155	Output	EFC0-1 are control outputs that are connected to the feature connector.
EIRQ	39	Output	EIRQ is an active high signal that is connected to the IRQ2 line on the CPU bus. When an EGA vertical interrupt occurs, this line goes high.
ERDY	30	Output	ERDY is an open collector signal that synchronizes the CPU board wait states with the sequencer operations. It is forced low while waiting for a VRAM access.
HIN	62	Output	HIN is the horizontal retrace output. It is always active.
IBLUE	55	Output	This is an active high output, for the primary blue video signal. It is always driven.
IGREEN	53	Output	This is an active high output, for the primary green video signal. It is always driven.
IRED	54	Output	This is an active high output, for the primary red video signal. It is always driven.
ISBLUE	61	Output	This is an active high output, for the secondary blue video signal. It is always driven.
ISGRN	58	Output	This is an active high output, for the secondary green video signal. It is always driven.
ISRED	57	Output	This is an active high output, for the secondary red video signal. It is always driven.
VIN	63	Output	VIN is the vertical retrace output, it is always active.
/AUTINT	143	Output	AUTINT is an active low open collector output used to signal an auto mode switch interrupt.
/EASL	156	Output	This is an active low output, that is connected to the feature connector. It indicates that the attributes controller shift registers are being loaded.
/ECAS	118	Output	ECAS is an active low output, that causes the column addresses of the video RAMs to be loaded.
/ECOMP	43	Output	ECOMP is an open collector composite sync output, that is used to force the composite driver to a sync level.
/EINTRN	64	Output	EINTRN is an active low output to the feature connector. It indicates that the EGA video drivers are enabled.
/ERAS0	113	Output	ERAS0 is an active low output that loads the row addresses for video RAM plane 0.
/ERAS1	114	Output	ERAS1 is an active low output that loads the row addresses for video RAM plane 1.
/ERAS2	115	Output	ERAS2 is an active low output that loads the row addresses for video RAM plane 2
/ERAS3	116	Output	ERAS3 is an active low output that loads the row addresses for video RAM plane 3
/EROMCS	92	Output	EROMCS is an active low output that is connected to the chip select of the BIOS ROM.
/EROMOE	91	Output	EROMOE is an active low output that enables the output of the BIOS ROM.
/ESCS	104	Output	ESCS This is not currently used and MUST NOT BE connected.
/ESOE	103	Output	ESOE This is not currently used and MUST NOT BE connected.
/ESWE	150	Output	ESWE This is not currently used and MUST NOT BE connected.
/EWE	117	Output	EWE is an active low output that is connected to the write line of all the video RAMs.
/PHNTOM	65	Output	PHNTOM is an active low line used to generate the CARD SLCTD input on slot 8 of the IBM PC.

Pin Description

A0	3	Input	A0-A19 are the CPU address bits. They are connected directly to the CPU bus.
A1	4		
A2	5		
A3	6		
A4	7		
A5	8		
A6	9		
A7	10		
A8	11		
A9	12		
A10	13		
A11	14		
A12	15		
A13	16		
A14	17		
A15	18		
A16	19		
A17	21		
A18	22		
A19	23		
D0	31	In/Out	D0 – D7 are the 8 bidirectional data lines, from CPU data bus.
D1	32		
D2	33		
D3	34		
D4	35		
D5	36		
D6	37		
D7	38		
BD0	83	In Out	BD0-BD7 are the on-board data bus bits, for the BIOS ROM
BD1	84		
BD2	85		
BD3	86		
BD4	87		
BD5	88		
BD6	89		
BD7	90		
M0D0	149	In Out	M0D0-7 are the bidirectional data lines from the video RAM plane 0.
M0D1	148		
M0D2	147		
M0D3	146		
M0D4	145		
M0D5	144		
M0D6	142		
M0D7	140		
M1D0	130	In Out	M1D0-7 are the bidirectional data lines from the video RAM plane 1.
M1D1	129		
M1D2	128		
M1D3	127		
M1D4	126		
M1D5	125		
M1D6	124		
M1D7	123		
M2D0	93	In/Out	M2D0-7 are the bidirectional data lines from the video RAM plane 2.
M2D1	94		
M2D2	95		
M2D3	96		
M2D4	97		
M2D5	98		
M2D6	99		
M2D7	100		
M3D0	72	In/Out	M3D0-7 are the bidirectional data lines from the video RAM plane 3.
M3D1	73		
M3D2	74		
M3D3	75		
M3D4	76		
M3D5	77		
M3D6	78		
M3D7	79		
MAA0	139	Output	MAA0-MAA7 are the address bits that are connected to the A plane video RAM chips (planes 0 and 1).
MAA1	138		
MAA2	137		
MAA3	136		
MAA4	135		
MAA5	134		
MAA6	133		
MAA7	132		
MBA0	105	Output	MBA0-MBA7 are the address bits that are connected to the B plane video RAM chips (planes 2 and 3).
MBA1	106		
MBA2	107		
MBA3	108		
MBA4	109		
MBA5	110		
MBA6	111		
MBA7	112		
ERESET	42	Input	ERESET is an active high signal that puts Multi Function Video Controller in a standard EGA mode. After ERESET has been asserted, the CGA, and Hercules can't be accessed until the master port is modified. The Multi Function Video Controller is in the following state after ERESET: a. The vertical and horizontal polarity controls are initialized to 0. b. Mode register bits 4 and 7 are cleared. c. All counters in the CRT Controller are reset. d. The master control register is cleared. Multi Function Video Controller changes to an EGA mode of operation. e. The feature control bits, PGSEL, and other bits in the miscellaneous register are cleared. f. All internal state latches are set to a known state that facilitates the required CRT Controller start-up sequence. g. All other user programmable control registers remain unchanged.

MECHANICAL SPECIFICATIONS