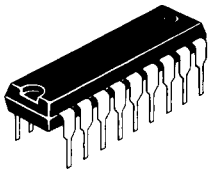
M5M4416P-12, -15

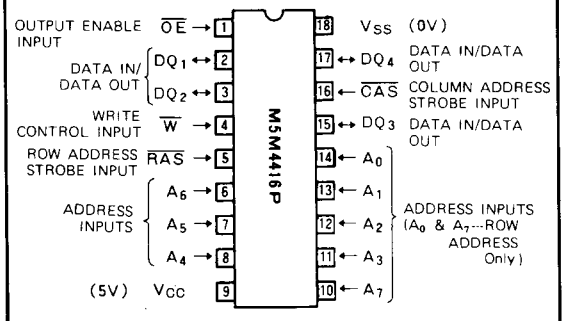
65 536-BIT (16 384-WORD BY 4-BIT) DYNAMIC RAM



DESCRIPTION

This is family of 16348-word by 4-bit dynamic RAMs, fabricated with the high performance N-channel silicon-gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 18-pin package configuration and an increase in system densities. The M5M4416P operates on a 5V power supply using the on-chip substrate bias generator.

PIN CONFIGURATION (TOP VIEW)



Outline 18 P4

FEATURES

- Performance ranges

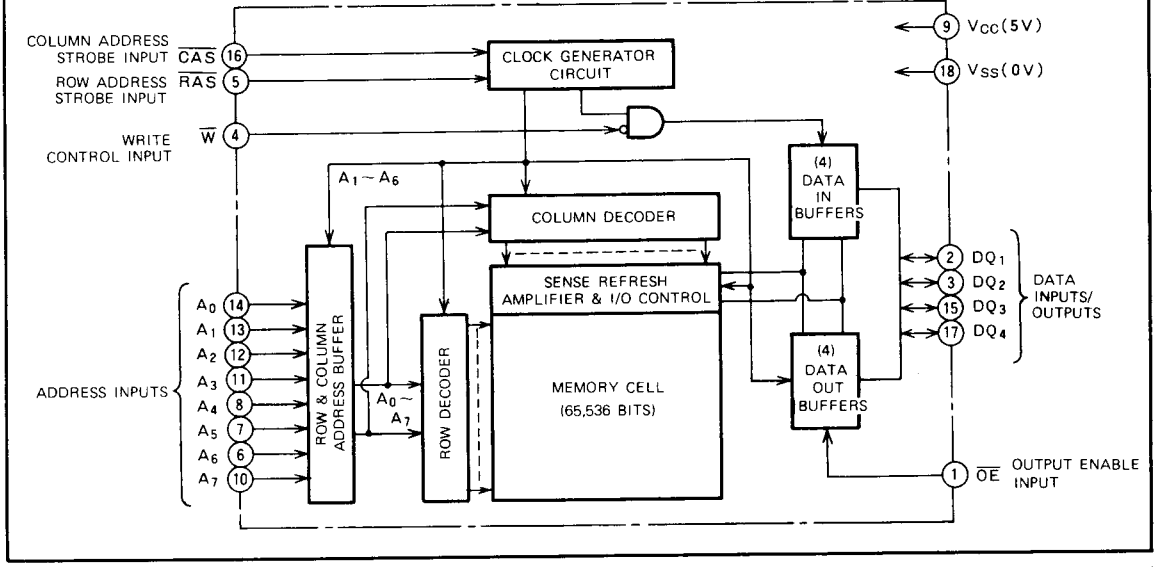
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4416P-12	120	220	175
M5M4416P-15	150	260	150

- 16,384 x 4 Organization
- Industry standard 18-pin dual in line package
- Single 5V ±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  M5M4416P-12 275mW (max)
  M5M4416P-15 250mW (max)
- All Inputs, outputs TTL compatible and low capacitance
- 3-State unlatched outputs
- 128 refresh cycles/2ms. Pin 10 is not needed for refresh
- Early write or $\overline{OE}$ to control output buffer impedance
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh and Page mode capabilities
- Wide $\overline{RAS}$ pulse width for Page mode ..... 30μs max

APPLICATION

- Refresh memory for CRT

BLOCK DIAGRAM



FUNCTION

The M5M4416P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, hidden refresh, and delayed-write. The input conditions and output states for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column adress	Input DQ	Output DQ		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Page mode identical
Write (Early Write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only retfesh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT active, NAC nonacitive, DNC don't care, VLD valid, APD applied, OPN open.

SUMMARY OF OPERATIONS

address (AO through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins AO through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state allowing a write cycle with $\overline{OE}$ grounded.

data-in (DQ1 through DQ4)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data-out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_a(C)$ that begins with the negative transition of $\overline{CAS}$ as long as $t_a(R)$ and $t_a(OE)$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OEHD}.

output enable ($\overline{OE}$)

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

Page-Mode Operation

This operation allows for multiple-column operating at the same row address, and eliminates the power dissipation associated with the cycling of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 128 rows (A_0~A_6) of the M5M4416P must be refreshed every 2 ms to maintain data. The methods of refreshing for the M5M4416P are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the outputs in the high-impedance state with a typical power reduction of 20% over a read or write cycle.

3. Hidden Refresh

A features of the M5M4416P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is refered to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data ports indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4416P is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4416P as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4416P operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	parameter	Condtions	Limits	Unit
V_{CC}	Supply volrage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta＝25°C	700	mW
Topr	Operating free-air temperature range		0～70	°C
Tstg	Storage temperature range		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}＝−2mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}＝4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V, All other pins ＝0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{cc}, operating (Note 3,4)	M5M4416P-12	$\overline{RAS}$, $\overline{CAS}$ cycling			55	mA
		M5M4416P-15	tc(rd)＝tc(w) ＝ min output open			50	mA
I_{CC2}	Supply current from V_{cc}, standby		$\overline{RAS}$＝V_{IH} output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{cc}, retreshing (Note 3)	M5M4416P-12	$\overline{RAS}$ cycling $\overline{CAS}$＝V_{IH}			45	mA
		M5M4416P-15	tc(Prd) ＝ min, output open			40	mA
$I_{CC4(AV)}$	Average supply current from V_{cc}, page mode (Note 3,4)	M5M4416P-12	$\overline{RAS}$＝V_{IL}, $\overline{CAS}$ cycling			45	mA
		M5M4416P-15	tc(Prd) ＝ min, output open			40	mA

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta＝0～70°C, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I＝V_{SS} f＝1MHz V_i＝25mVrms			5	pF
$C_{I(OE)}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(W)}$	Input capacitance, write control input				7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input				10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input				10	pF
$C_{I/O}$	Input/Output capacitance, data ports				10	pF

SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Alternative Symbol	M5M4416P-12 Limits Min	M5M4416P-12 Limits Max	M5M4416P-15 Limits Min	M5M4416P-15 Limits Max	Unit
$t_{a(C)}$	Access time from $\overline{CAS}$	(Note 6,7)	t_{CAC}		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	(Note 6,8)	t_{RAC}		120		150	ns
$t_{a(OE)}$	Access time from $\overline{OE}$	(Note 6)	—		30		40	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	(Note 9)	t_{OFF}	0	25	0	30	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 9)	—	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCCL} \geqq t_{RLCL}$ max.
8: Assume that $t_{RLCL} < t_{RLCL}$ max. If t_{RLCL} is greater than t_{RLCL} max then $t_{a(R)}$ will increase by the amount that t_{RLCL} exceeds t_{RLCL} max.
9: $t_{dis(CH)}$ max and $t_{dis(OE)}$ max define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to V_{OH} min or V_{OL} max.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

(T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, See notes 10,11)

Symbol	Parameter		Alternative Symbol	M5M4416P-12 Limits Min	M5M4416P-12 Limits Max	M5M4416P-15 Limits Min	M5M4416P-15 Limits Max	Unit
$t_{C(RF)}$	Refresh cycle time		t_{REF}		2		2	ms
$t_{W(RH)}$	$\overline{RAS}$ high pulse width		t_{RP}	90		100		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 12)	t_{RCD}	25	60	30	75	ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 13)	t_{CRP}	−20		−20		ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low		t_{ASR}	0		0		ns
$t_{su(CA)}$	Column address setup time before $\overline{CAS}$ low		t_{ASC}	0		0		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low		t_{RAH}	15		20		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low		t_{CAH}	20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low		t_{AR}	80		100		ns
t_T	Transition time (rise and fall)	(Note 14)	t_T	3	50	3	50	ns

Note 10: The timing requirements are assumed t_T=5ns.
11: V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals.
12: t_{RLCL} max is specified as a reference point only; if t_{RLCL} is less than t_{RLCL} max, access time is $t_{a(R)}$. if t_{RLCL} is greater than t_{RLCL} max, access time is $t_{RLCL} + t_{a(C)}$. t_{RLCL} min is specified as t_{RLCL} min. = $t_{h(RA)} + 2t_T + t_{su(CA)}$.
13: t_{CHRL} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
14: t_T is measured between V_{IH} min and V_{IL} max.

Read and Refresh Cycles

Symbol	Parameter		Alternative Symbol	M5M4416P-12 Limits Min	M5M4416P-12 Limits Max	M5M4416P-15 Limits Min	M5M4416P-15 Limits Max	Unit
$t_{C(rd)}$	Read cycle time		t_{RC}	220		260		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	120	10000	150	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	60		75		ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width		t_{CPN}	30		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low		t_{CSH}	120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low		t_{RSH}	60		75		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low		t_{RCS}	0		0		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high	(Note 15)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high	(Note 15)	t_{RRH}	10		10		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low		—	30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low		—	30		40		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low		—	60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		—	120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		—	0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		—	25		30		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		—	0		0		ns

Note 15: Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for a read cycle.

Write Cycles (Early Write and Delayed Write)

Symbol	Parameter		Alternative Symbol	M5M4416P-12 Limits		M5M4416P-15 Limits		Unit
				Min	Max	Min	Max	
$t_{c(w)}$	Write cycle time		t_{RC}	220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	60		75		ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width		t_{CPN}	30		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low		t_{CSH}	120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low		t_{RSH}	60		75		ns
$t_{su(WCL)}$	Write setup time before $\overline{CAS}$ low	(Note 17)	t_{WCS}	−5		−5		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low		t_{WCH}	40		45		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low		t_{WCR}	100		120		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low		t_{CWL}	40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low		t_{RWL}	40		45		ns
$t_{w(W)}$	Write pulse width		t_{WP}	40		45		ns
$t_{su(D)}$	Data setup time		t_{DS}	0		0		ns
$t_{h(WLD)}$	Data hold time after Write low		t_{DH}	40		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low		t_{DH}	40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low		t_{DHR}	100		120		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		—	25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after Write low		—	25		30		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Alternative Symbol	M5M4416P-12 Limits		M5M4416P-15 Limits		Unit
				Min	Max	Min	Max	
$t_{c(rdW)}$	Read write/read modify write cycle time	(Note 16)	t_{RWC}	295		345		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	195	10000	255	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	135		180		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low		t_{CSH}	195		255		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low		t_{RSH}	135		180		ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width		t_{CPN}	30		30		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low		t_{RCS}	0		0		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to Write low	(Note 17)	t_{CWD}	90		110		ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to Write low	(Note 17)	t_{RWD}	150		185		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after Write low		t_{CWL}	40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after Write low		t_{RWL}	40		45		ns
$t_{w(W)}$	Write pulse width		t_{WP}	40		45		ns
$t_{su(D)}$	Data setup time		t_{DS}	0		0		ns
$t_{h(WLD)}$	Data hold time after Write low		t_{DH}	40		45		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low		—	60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		—	120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		—	0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		—	25		30		ns

Note 16: $t_{c(rdW)}$ is specified as $t_{c(rdW)}$ min = $t_{a(R)}$ max + t_{OEHD} min + $t_{h(WRH)}$ min + $t_{w(RH)}$ min + 4 t_T.

17: $t_{su(WCL)}$, t_{CLWL} and t_{RLWL} are specified as reference points only. If $t_{su(WCL)} \geqq t_{su(WCL)}$ min, the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CLWL} \geqq t_{CLWL}$ min and $t_{RLWL} \geqq t_{RLWL}$ min, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition is satisfied, the condition of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

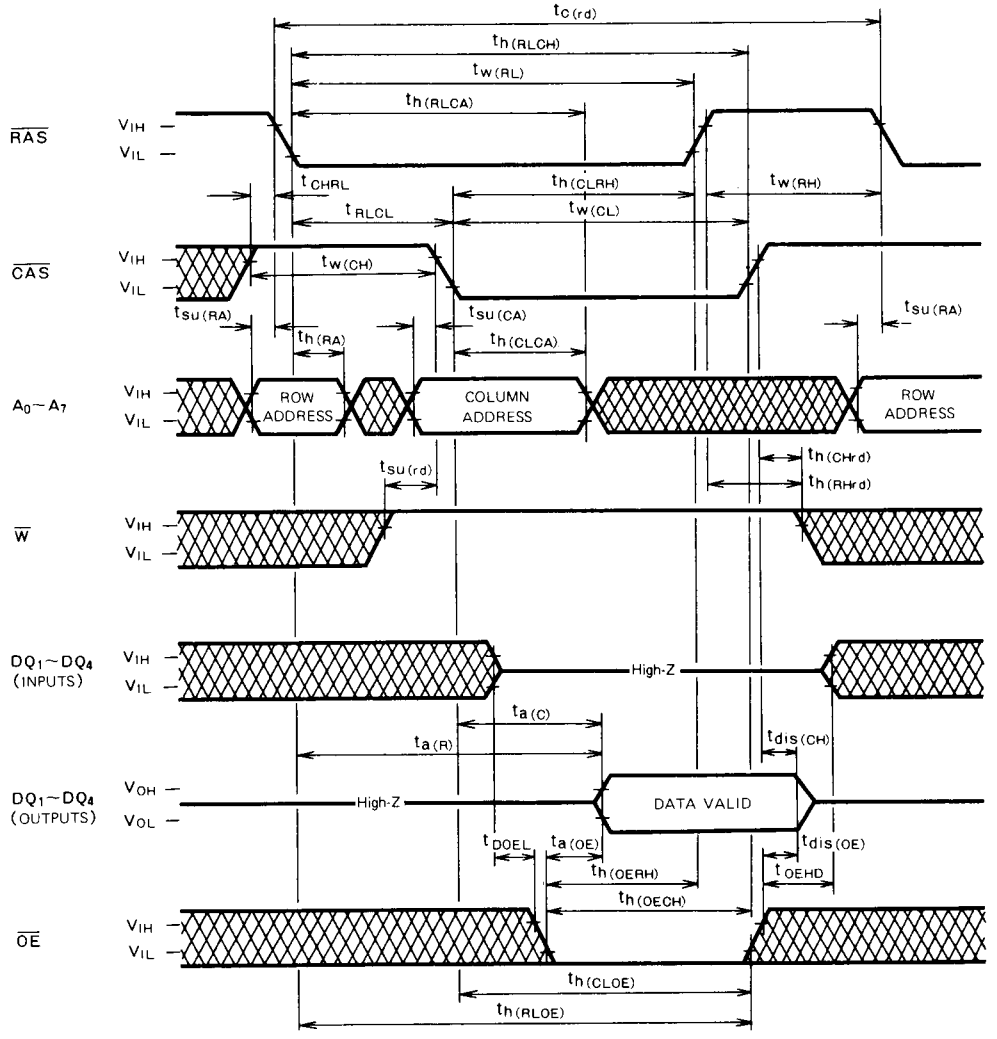
Page-Mode Cycle (Note 18)

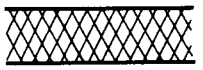
Symbol	Parameter	Alternative Symbol	M5M4416P-12		M5M4416P-15		Unit
			Limits		Limits		
			Min	Max	Min	Max	
$t_{C(Prd)}$	Read cycle time	t_{PC}	120		145		ns
$t_{C(PW)}$	Write cycle time	t_{PC}	120		145		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 19)	t_{RAS}	240	30000	295	30000	ns
$t_{C(PrdW)}$	Read write/read modify write cycle time	—	195		250		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width (Note 20)	t_{RAS}	390	30000	505	30000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CP}	50		60		ns

Note 18: All previously specified timing requirements and switching characteristics are applicable to their respective page mode timing.
19: Specified for read or write cycle.
20: Specified for read-write or read-modify-write cycle.

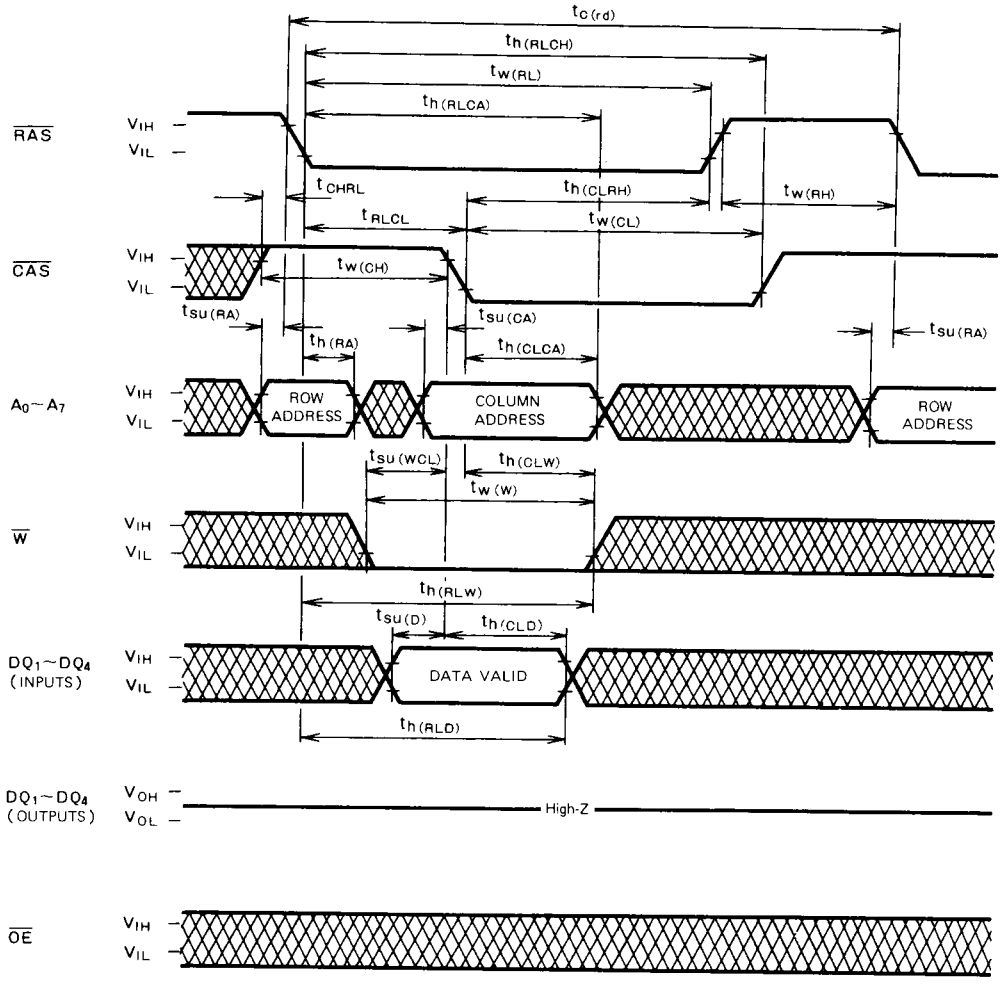
TIMING DIAGRAMS (Note 21)

Read Cycle

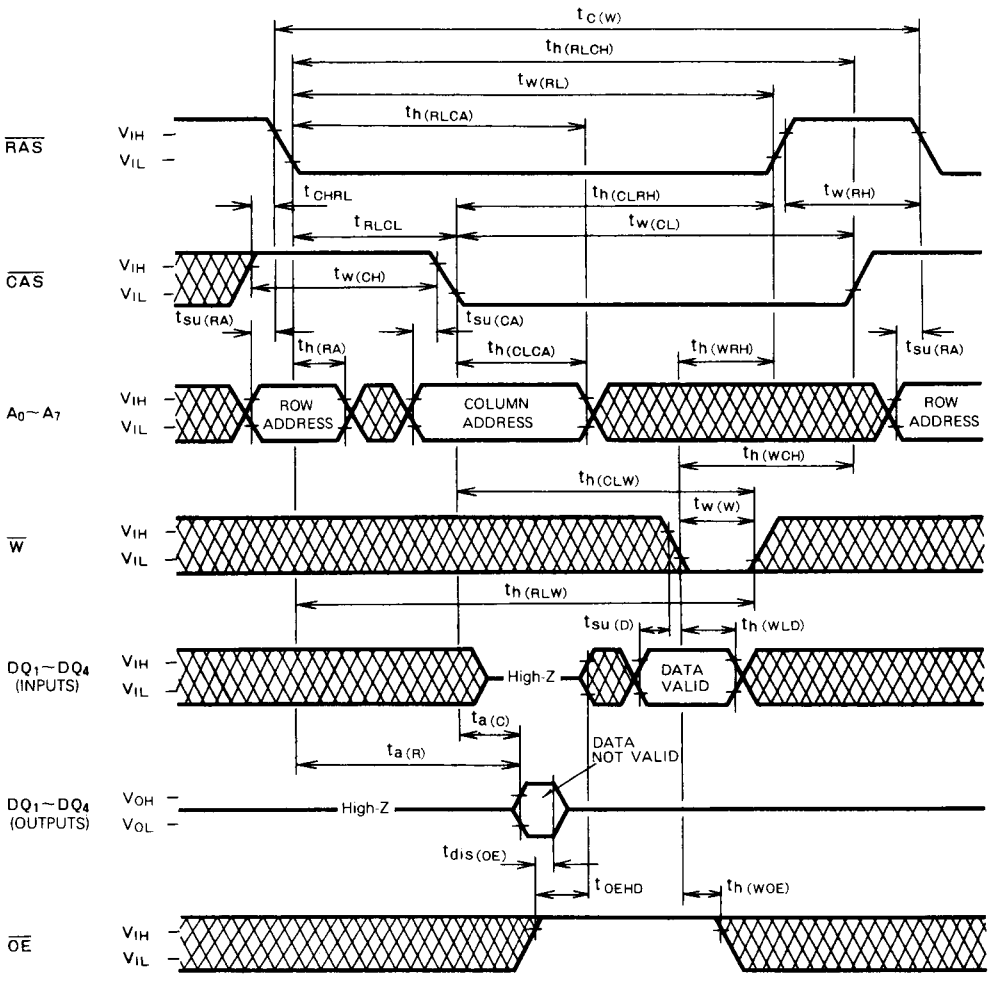


Note 21.  Indicates the don't care input.

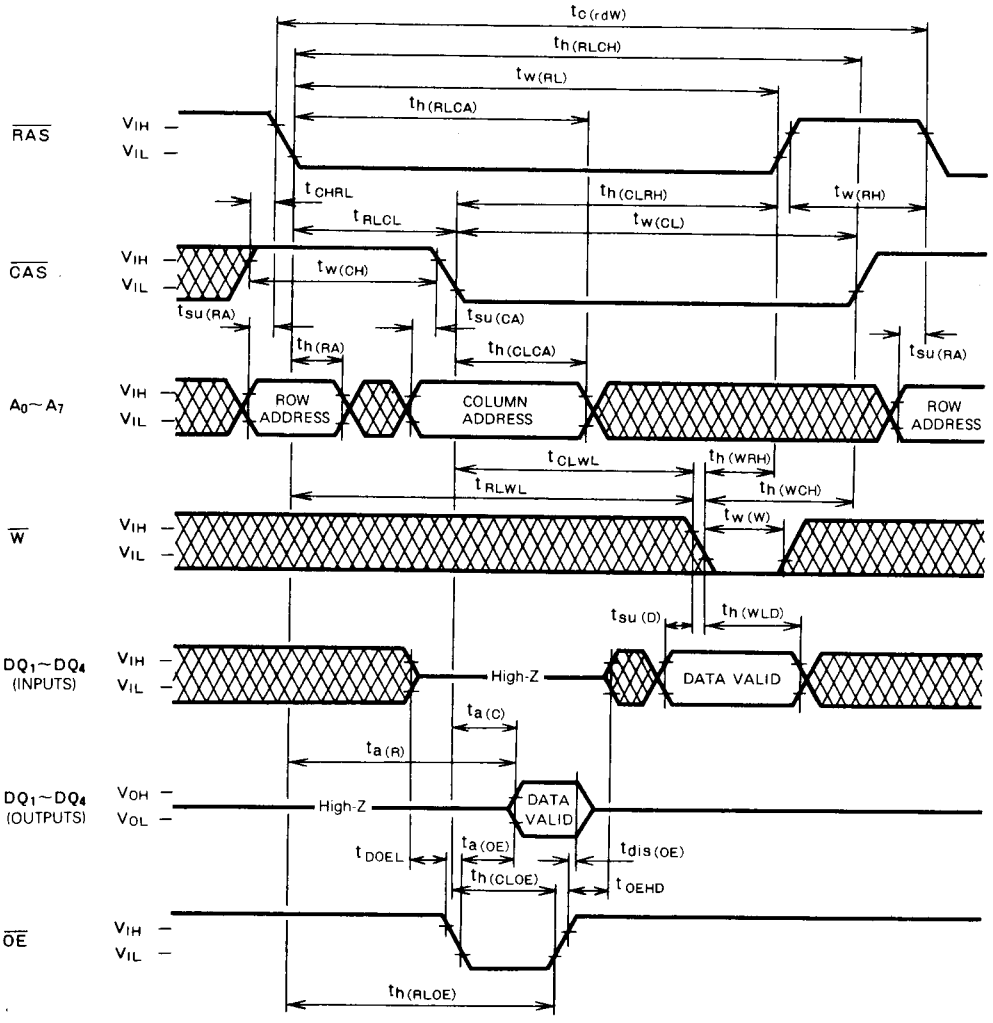
Write Cycle (Early Write)



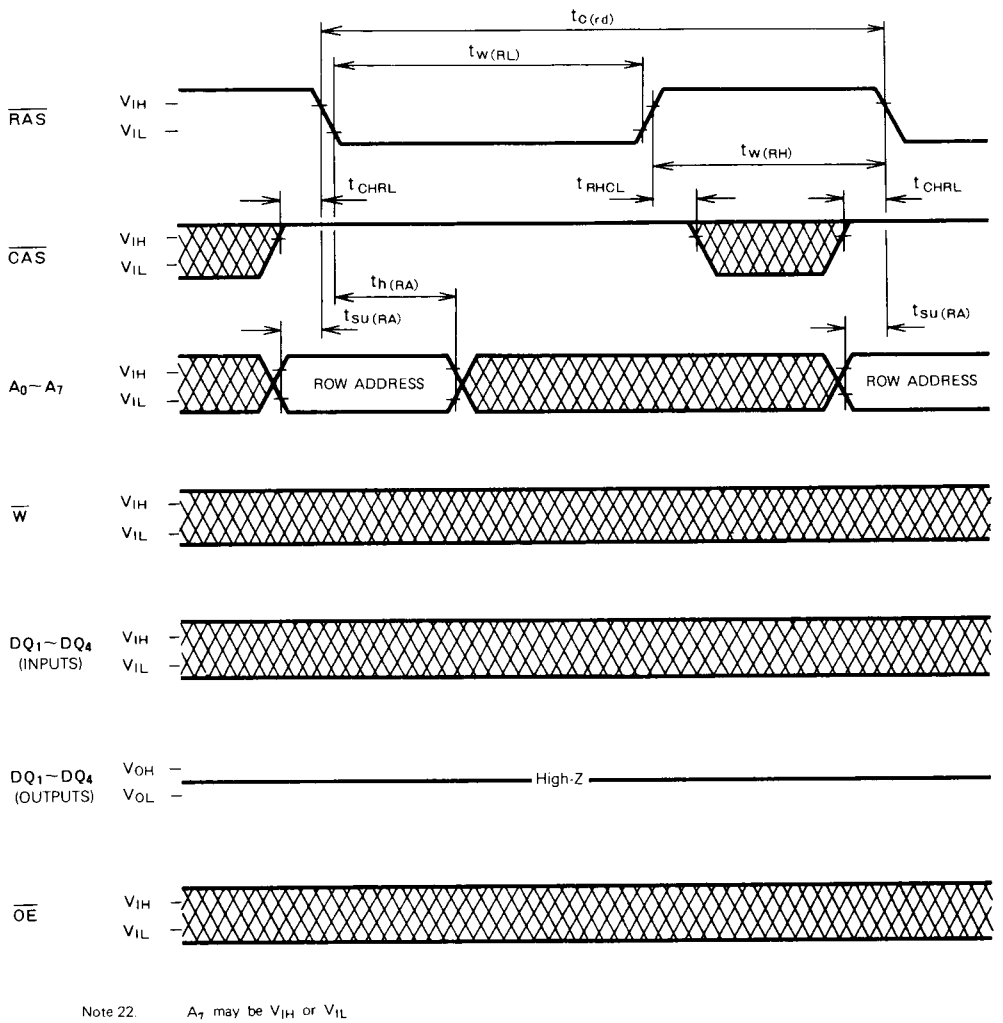
Write Cycle (Delayed Write)



Read-Write and Read-Modify-Write Cycles

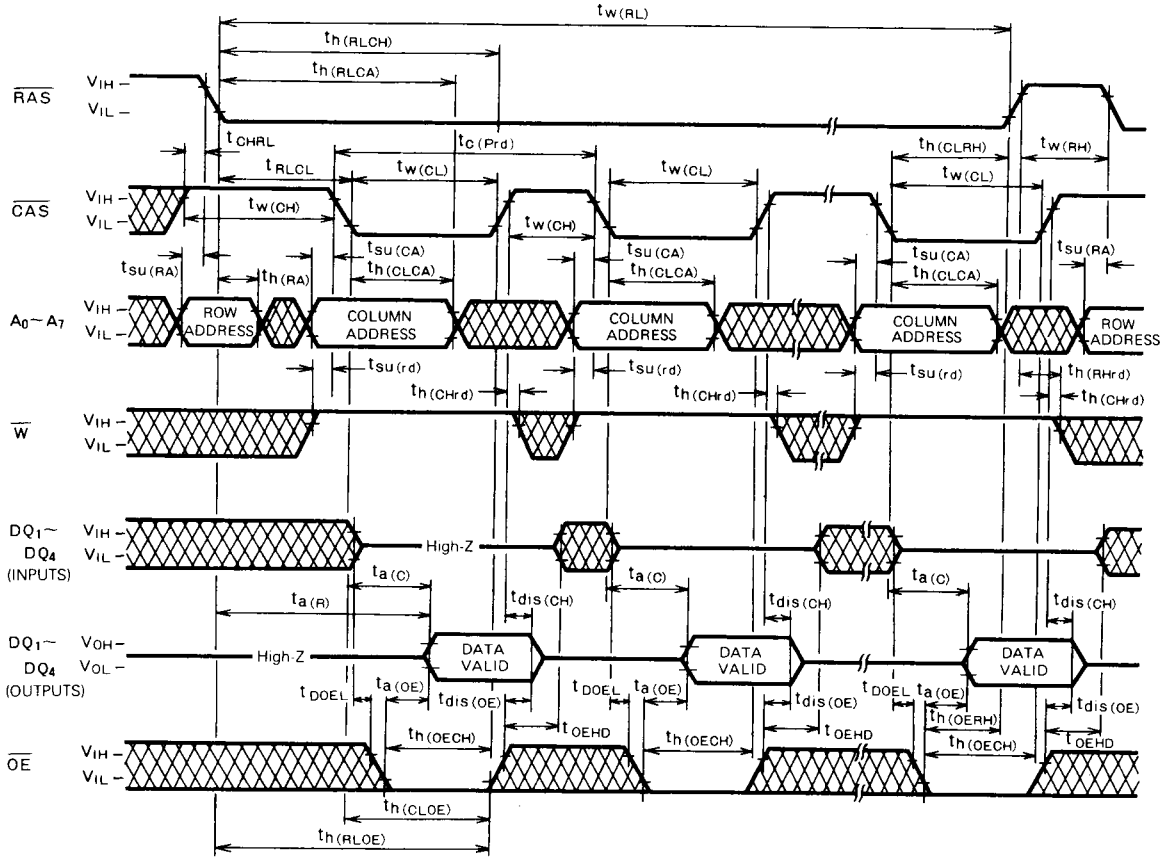


$\overline{RAS}$-Only Refresh Cycle (Note 22)

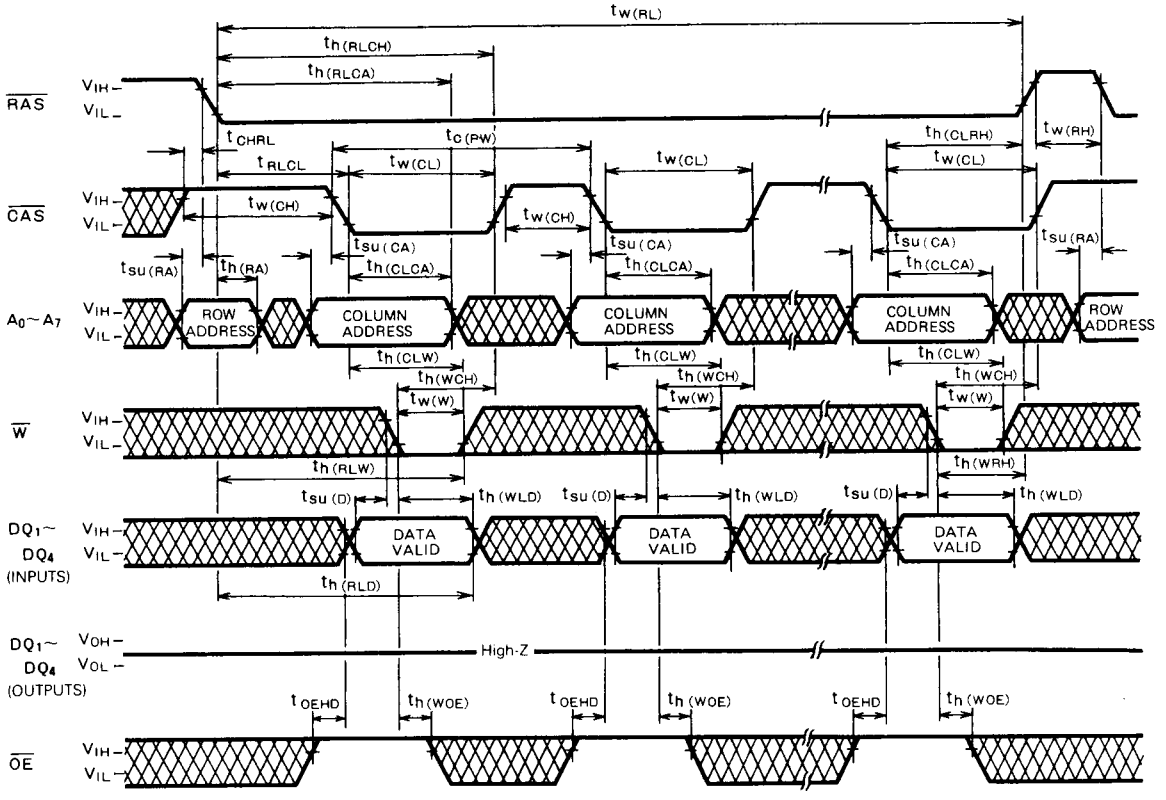


Note 22. A_7 may be V_{IH} or V_{IL}

Page-Mode Read Cycle



Page-Mode Write Cycle



Hidden Refresh Cycle