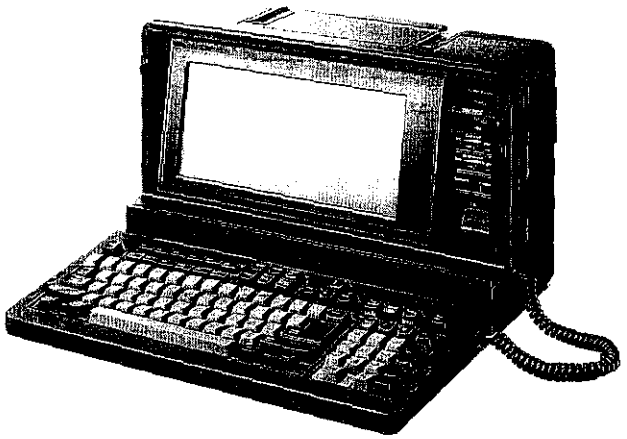
SHARP SERVICE MANUAL

CODE: 00ZPC7200SM-E



PERSONAL COMPUTER

MODEL PC-7200

CONTENTS

SHARP CORPORATION

PREFACE

SCOPE

This manual contains the theory of operation for the PC-7200 microcomputer system, and is primarily intended for service technicians working in the field or in repair centers. In addition, the manual can also be used as a reference document for technical personnel requiring knowledge of this computer. The contents of this manual are as simple and clear as possible, however, users of this manual should be acquainted with computer hardware.

About The Manual

This manual is divided into seven chapters:

CHAPTER 1 PRODUCT DESCRIPTION
Provides general information on the computer such as specifications and external and internal configurations.

CHAPTER 2 THEORY OF OPERATION
Describes the logical and electrical functions of each circuit block.

CHAPTER 3 FLOPPY DISK DRIVE

CHAPTER 4 HARD DISK INTERFACE

CHAPTER 5 HARD DISK DRIVE

CHAPTER 6 ADJUSTMENT

CHAPTER 7 APPENDIX

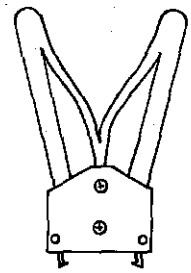
NOTES: The 7200 Manual is generally concerned with the PC-7221 product configuration which includes the high density (2HD) floppy disk drive and 20MB hard disks drive.
PC-7201/7202/7221 are common except the difference showed by the next list.
The difference from PC-7201, PC-7202 and PC-7221

	PC-7201	PC-7202	PC-7221
FDD	1×FDD(2HD)	2×FDD(2HD)	1×FDD
HDD	none	none	1×HDD
FDD, HDD Indicator	FDD	FDD	FDD
	FDD/HDD	FDD	HDD

SPECIAL SERVICE TOOLS

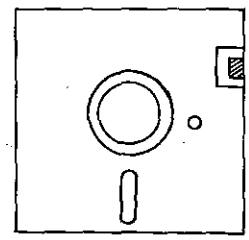
	PARTS CODE	PRICE BANK	TOOL NAME
1	UKOGM2018CSZZ	CK	LSI (CPU 80286) extraction tool
2	DFLP-1083ACZZ	BF	Diagnostic media
3	DFLP-1084ACZZ	BF	Aging test media

1. UKDGM2018CSZZ



2. DFLP-1083ACZZ

3. DFLP-1084ACZZ



CHAPTER 1. SYSTEM SPECIFICATION

1-1. FEATURES

The PC-7200, provided with numerous special features and functions, can be used as a single-user or multi-user computer. It is a powerful office tool that can satisfy the diverse demands for high-speed data processing and large-scale memory management for the high-end personal computer and low-end multi-user configuration.

80286 Microprocessor

The computer's central processing unit (CPU) has an 10MHz 16-bit 80286 microprocessor, permitting upward compatibility with 8088/8086 processor operation. It performs versatile data processing at a faster speed than the 8088/8086 processors.

Memory

The computer has 640K bytes of Random Access Memory (RAM) and 64K bytes of system Read Only Memory (ROM). ROM contains IPL, BIOS, and diagnostic programs as well as graphics character fonts.

LCD Display

A large-capacity LCD with 640×200 pixel configuration.
Features a backlight and adjustable tilt feature for better visibility.

Built-in Interfaces

For the input/output of data to and from the computer, various peripherals have been provided, including a 5-1/4", high-density floppy disk drive, a built-in 20M byte hard disk and hard disk controller (PC-7221 only), and a RS-232C interfaces, and a Centronics-compatible printer interface.

Functional Expandability

Besides the standard features above, the functions of the computer can be expanded by mounting optional devices such as the 80287 Numeric Processor Extension, or by installing any of various option boards in the internal options slots.

Modem Card

Designed exclusively for the PC-7200, and directly attaches to the main board.

Operating System

A DOS (Disk Operating System) allows the user to communicate with the computer and its peripheral devices, performing data transfer and managing the memory resources of the various equipment.
In the single-user system configuration of DOS, MS-DOS version 3.2 is used. This version permits use of a wide range of commercially available application programs. The computer can also be run under XENIX 286 Version (multi-user configuration) and GW-BASIC, version 3.2.

IBM Compatibility

Most of the application software, peripherals and options designed for the IBM PC, XT, and AT can also be used with the PC-7200.

1-2. SYSTEM CONFIGURATION

Figure 1-1 illustrates system architecture. As demonstrate, the system's main components include the system unit and the keyboard unit.
The system unit includes the main PCB, floppy disk drive, hard disk drive (PC7221 only), and optional adapter.

The System Unit

The main PCB is composed of the following components:

- 80286 16-bit microprocessor
- Control Circuits
- 64K-byte (two 32 byte chips) ROM which contains the power-on diagnostic program, BIOS, initial program loader (IPL), and graphic character fonts.
- Standard 640K-byte D-RAM.
- Real time clock (RTC) which stores information related to the system configuration and updates the date and time even if the computer power is turned off.
- Keyboard interface
- Centronics-compatible parallel printer interface
- Floppy disk interface which can control up to two double-density (2D) or high-capacity (2HD) floppy disk rives.
- Asynchronous serial interface which conforms to the EIA RS-232C standard.
- One options slots – This slot can use both IBM PC/XT compatible, 8-bit type, and IBM AT compatible, 16-bit type.
- A large-capacity LCD with 640×200 pixel configuration, as a standard feature.
- Modem card designed exclusively for the PC-7200 directly attaches to the main unit as an optional device.

A high density (2HD) floppy disk drive is installed as a standard feature.
Mounted at the center of the chassis is a 3.5 inch hard disk drive with storage capacity of 20M-bytes.
The power supply unit has six levels of power output: +5V, −5V, +12V, −12V, −15V and AC120V. Because these voltages are stabilized with the switching regulator, the power supply takes less space and is light in weight.
Inside the system unit, there is a Ni-Cd battery. This battery backs up the real time clock, permitting it to maintain information related to the system configuration, and to update the date and time, even when the power is down.

SYSTEM CONFIGURATION

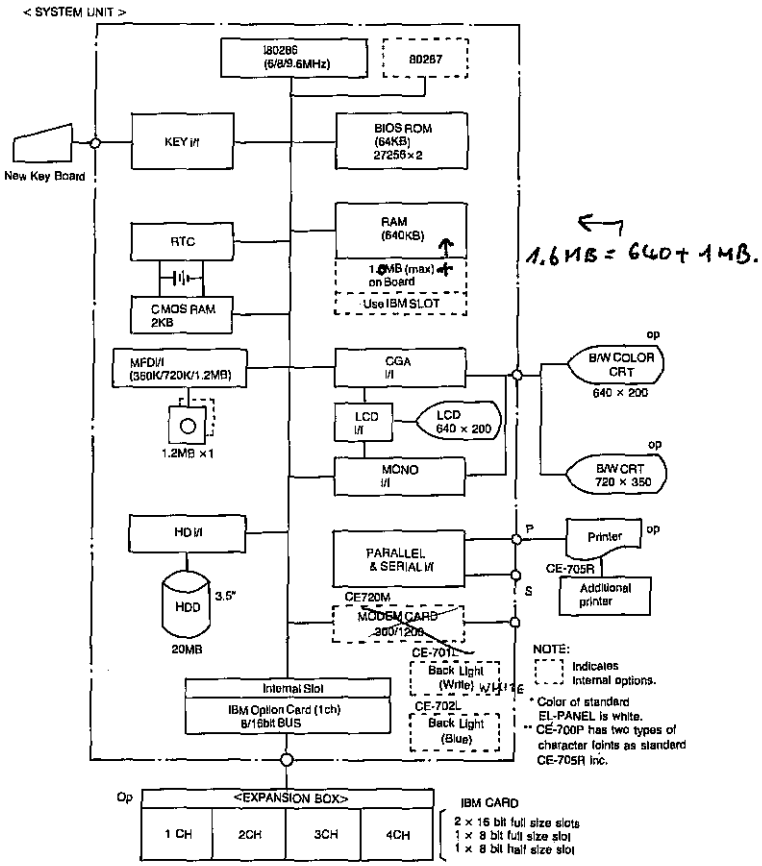


Figure 1-1

The Keyboard Unit

The keyboard is connected to the system unit using a 6-Pin Modular jack connector with a coiled cable. A one chip microprocessor is used as an interface with the keyboard unit and the system unit. When the power of the system unit is turned on, the processor automatically checks its own RAM and ROM by executing the self-diagnostic program.

1-3. MAIN COMPONENT FUNCTIONAL DESCRIPTION

This section describes the functions of the two main components – system unit and keyboard.

1-3-1. System Unit

Figure 1-2 shows the external and internal views of the system unit, respectively.

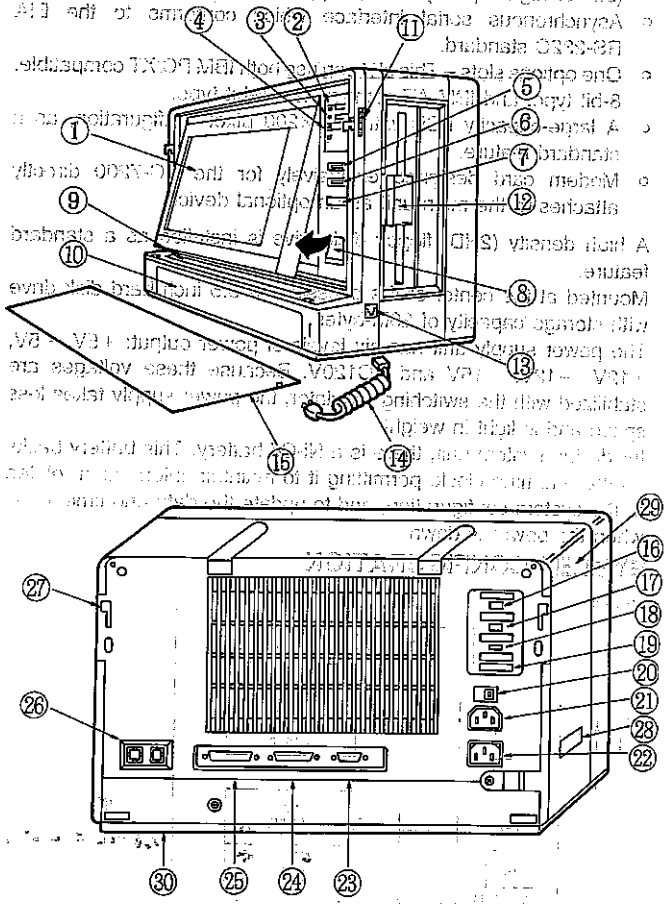


Figure 1-2

(1) LCD

(2) Display standby indicator
This indicator is used to indicate that the EL backlight is out during time out or CRT mode.

(3) POWER status indicator

(4) FDD and HDD status indicators
When the computer accesses the floppy disk or hard disk, the relevant indicator lights up.

(5) LCD contrast adjust knob
This knob is provided to adjust the LCD contrast to an optimum.

(6) EL backlight brightness control knob
This knob is provided to adjust the brightness of the EL backlight. Normally, set to the middle position.

(7) Display background select switch
This switch is provided to select the LCD background mode; NORMAL or REVERSE.

(8) LCD tilt stand
This tilt stand is provided to adjust the angle of the display screen to an optimum angle to eye position.

(9) Keyboard cable compartment
The keyboard cable is housed in this compartment when the keyboard cable is not in use.

(10) Option card slot
The IBM PC/AT option card is mounted in this slot.

(11) Keyboard latch
Used to latch the keyboard to the main unit.

(12) Floppy disk drive
a 1/3-height, 1.2M byte floppy disk drive is mounted.

(13) KEYBOARD connection jack
Connect a coiled cable with plug from the keyboard unit into this jack.

(14) Keyboard cable
This cable is used to interface the keyboard with the PC-7200.

(15) Keyboard

(16) CPU clock select switch
This switch is provided to select the CPU clock speed; 6MHz/8MHz/10MHz.

(17) Display mode select switch
This switch is provided to select the display mode; CGA, MDA, or other. In the case of other, use of the display option card is required.

(18) LCD/CRT select switch
This switch is provided to select the display device; LCD or CRT.

(19) Sound control knob
This knob is provided to control internal speaker volume.

(20) Supply voltage select switch
This switch is provided to select the power supply voltage; 100 or 200V.

(21) AC power outlet
Plug a power cord of a peripherals unit etc. into this outlet. This outlet is controlled by the power switch. When the power switch is turned on, this outlet is powered, and when the power switch is off, this outlet is not powered. This outlet handles AC current in a maximum of 0.4A. Be careful not to exceed this value when using this outlet.

(22) AC power inlet
Insert AC power cord with jack into this outlet.

(23) Color/Monochrome CRT connector
Connect a 9-pin plug with cord suitable for this connector to make a connection between the computer and a color/monochrome CRT monitor.

(24) Printer connector
To print out data, information, or programs, connect a printer's cable to this connector.

(25) RS-232C connectors
Plug a special cable into these connectors when communication with a host computer, another personal computer, or a serial printer.

(26) MODEM/TELEPHONE jack
This jack is connected to the telephone jack, when the modem card option is used.

(27) Printer latch
Used to latch the printer to the main unit.

(28) Power switch

The POWER switch turns the computer on and off. When turning on the system, turn the power of the peripherals on first then turn on the computer power.

(29) Cooling fan

Prevents the computer against excessive heat generated during operation. Do not block this ventilation opening by positioning the computer too close to a wall etc.

(30) Expansion connector

Used for connection of the expansion box.

1-3-2. Keyboard

Figure 1-3 shows the keyboard layout for the PC-7200. The keyboard has the standard QWERTY layout with 10-programmable function keys, numeric keypad/cursor movement keys and special keys. The three status indicators show the ON/OFF status of the Caps (Capitals) Lock, Num (Numeric) Lock, and Scroll Lock keys.

Keyboard Layout

EXP: USA-English

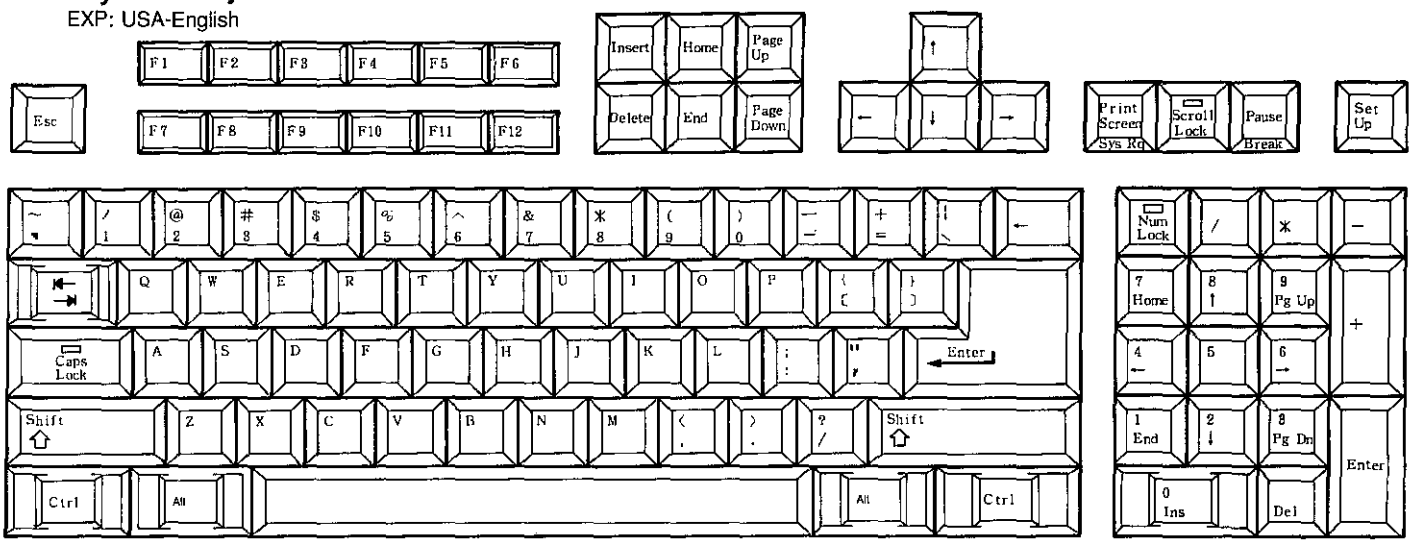


Figure 1-3

1-4. SPECIFICATIONS

The specifications below apply to the system unit and keyboard unit.

1-4-1. System Unit Specifications

Main Logic

CPU
- Processor 80286
- Clock frequency ... 6MHz/8MHz/9.6MHz

MPX (Option)
- Processor ... 80287

ROM
- Element ... 27256 EP-ROM×2
- Capacity ... 64K bytes
- include IPL, BIOS, diagnostic program and graphics character fonts

RAM
- Element ... MOS LSI 256K ×1 bit D-RAM×16, 64K ×4 bit D-RAM ×4
- Capacity ... 640K bytes

OPTION
- Element ... MOS LSI 256K ×4 bit D-RAM ×8
- Capacity ... 1M bytes

Clock/Calendar ... HD146818 (MC146818 compatible) battery back-up

DMA ... 7 channels (8237A-5×2)

Interrupt Level ... 15 (8259×2)

1-2. Specifications

1-2-1. Physical specifications

The physical specifications for the PC-7200 are shown below.

• Main unit (includes keyboard)

(1) Dimensions
- Width: 410mm (16.1″)
- Depth: 160mm (6.3″)
- Height: 243mm (9.6″)

(2) Weight
- Net: 7201 8.5kg (18.8 lb)
- 7202 9.3kg (20.5 lb)
- 7021 9.5kg (21.0 lb)
- (with the keyboard)

(3) Power requirements
- 100V type
  - 90–132V AC 50/60Hz
  - 1.0A (includes output for CE-700P)
  - 0.8W
- 200V type
  - 180–264V AC 50/60Hz
- Cable length: 2.0m (78.7″)

(4) Environment
- Temperature:
- 10 to 35 degrees C operating (50 to 95 degrees F)
- −28 to 60 degrees C storage (0 to 140 degrees F)
- Humidity:
- 20 to 80% operating with no condensation; up to 90% storage

1-2-2. Component specifications and characteristics

The PC-7200 consists of the following components, whose specifications and characteristics are shown below.

• KEYBOARD

(1) Unit dimensions
- Width: 410mm (16.1″)
- Depth: 182.5mm (7.2″)
- Height: 37.5mm (max.) (1.5″)

(2) Unit weight
- 1.05kg (2.4 lb)

(3) Coiled cable
- Diameter: 15mm (0.6″)
- Length: 270±10mm coiled state (10.6±0.4″)
- 1,500mm stretched state (4′11″)
- Weight: 55g (1.94 oz)

(4) Style
- Low profile
- Cylindrical key top
- Step sculpture

(5) Keys
102 keys (including three keys with LED)

(6) Layout
See Figure 1-3.

(7) LEDs
Color: Green
Key name:

U.Y.H	F	I	B
S.W.X	↓	↓	↓
"Caps Lock"	Maj	Bloc Mai	Shift Lock
"Num Lock"	Verr Num	Bloc Num	Num Lock
"Scroll Lock"	Arret defil	Bloc Scorr	Scroll Lock

(8) Rollover
N-key rollover

(9) Key switch operating force
80±30 g
60±25 g
65±25 g

(10) Key top Pull force
1 kg

(11) Lifetime
3,000,000 operations (keys with LED)
10,000,000 operations (keys without LED)

(12) Tilt adjustment
3-6-9 degrees

(13) Electrical characteristics
Power requirements: 180mA + 5V DC
Signal level: TTL

• LCD

(1) Unit dimensions
Width: 282.5mm (11.1")
Depth: 142mm (5.6")
Height: 9.3mm (366 mils)

(2) Unit weight
325 g (0.717 lb)

(3) Backlight panel
Dimensions
Width: 276.5mm (10.9")
Depth: 131mm (5.2")
Thickness: 1.3mm (max.) (51 mils)
Weight: 55 g (1.94 oz)

(4) Effective display size
Width: 239.96mm (9.4")
Height: 104.96mm (4.1")

(5) Graphic format
Horizontal: 640 dots
Vertical: 200 dots

(6) Text format
Row: 25 lines
Column: 80 characters/line
Character: 8×8 dots

(7) LCD connector
20 pin 2.54mm pitch connector

(9) Backlight connector
4-pin, 2.5-mm pitch nylon connector

(10) Electrical characteristics
Power requirements: 0.1mA (max.)
130V AC (max.)

• FLOPPY DRIVE

Refer to CHAPTER 3 (page 3-1).

• HARD DISK

Refer to CHAPTER 5 (page 5-1).

• RS-232C

(1) Interface
EIA RS-232C (voltage interface)

(2) Transmission method
- Asynchronous only
- Full or half duplex

(3) Baud rate
110, 150, 300, 600, 1200, 2400, 4800 or 9600

(4) Data length
7 or 8 bits

(5) Parity
None, even, odd

(6) Stop bit
1 or 2 bits

(7) Connector
25-pin "D"-type shell male connector

(8) Electrical characteristics
Signal level:
VOL = −5V to −15V
VOH = +5V to +15V
VIL = −3V to −15V
VIH = +3V to +15V

State:

Level	Data	Condition	Control
VOL, VIL	1	Mark	OFF
VOH, VIH	0	Space	ON

• PARALLEL INTERFACE

(1) Interface
Centronics-type interface

(2) Connector
25-pin "D" type shell female connector

(3) Electrical characteristics
Signal level: TTL
VIL = less than 0.8V
VIH = more than 2.0V
VOL = less than 0.4V
VOH = more than 2.4V

• SPEAKER

(1) Size
Diameter: 29mm (2.24")
Thickness: 6.8mm (0.74")

(2) Impedance
8Ω

(3) Variable frequency
670~3,000Hz

(4) Input power
Rating: 0.1W
Maximum: 0.15W

• CALENDAR

(1) Function
- Counts and presents year, month, date, hour, minute, second, and day of the week
- Automatic correction for days-per-month
- Automatic leap-year correction
- Battery backup

(2) Accuracy
Mean monthly error: ±45 s

(3) Battery
Type: 3-51FT
Enclosed type Ni-Cd rechargeable battery
Capacity: 50mAH
Cell: three cells (3.6V)
Charging method: Continuous trickle charge

(4) Charge/backup characteristics
Charge time: 50 hours (0 to 100%)
Backup time: 500 hours (approx. 20 days)

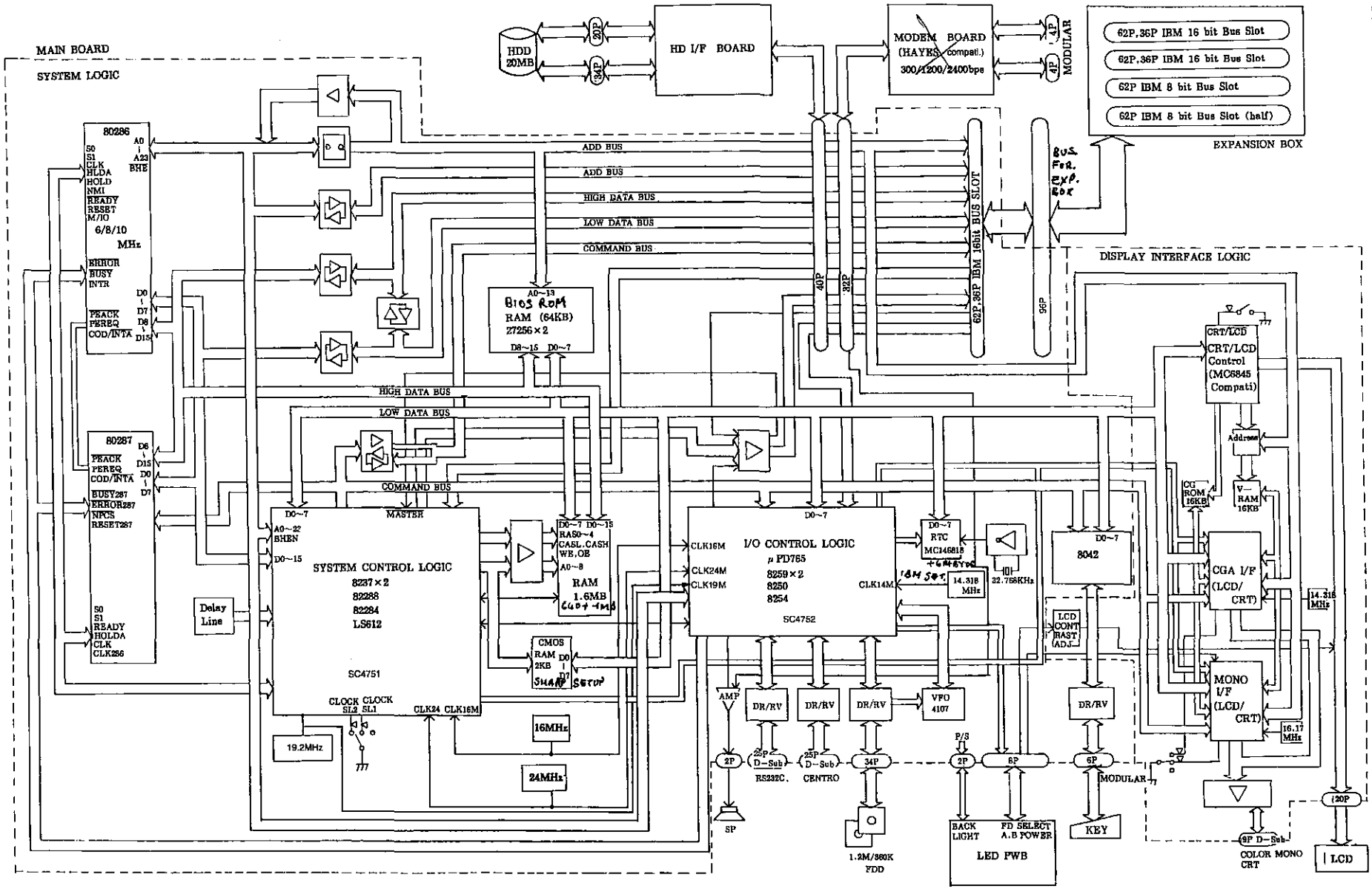


Figure 2-1. System block diagram

2-1-2. MEMORY MAP

The 80286 CPU has two memory managing modes – real mode and protect mode. In the real mode, the CPU can access up to 1M bytes of memory area using its A0 through A19 address signals. In the protect mode, the 80286 can physically access up to 16M bytes of memory area using its A0 through A23 address signals. In addition to the features mentioned above, the 80286 can logically use up to 1G-byte vertual address space per task. The memory space of the computer is made up of BIOS-ROM, RAM, V-RAM and optional ROM irrespective of the CPU operation mode.

Address allocation for the basic 640K-byte RAM is 000000H through 09FFFFH and additional 1M-byte RAM can be mounted on the main board.

The RAM area 080000H through 09FFFFH can be disabled by the jumper strap.

Expansion ROM area 0E0000H through 0EFFFFH can not be mounted on the main board, it can be mounted on the I/O slot.

Table 2-1. Memory map

Address	Name	Function	
000000 – 09FFFF	640KB System Memory	standard RAM on main board	REAL MODE
0A0000 – 0AFFFF	64KB V-RAM	Reserved for EGA	
0B0000 – 0B0FFF	4KB V-RAM	For Monochrome Display Adapter (standard)	<*>
0B1000 – 0B7FFF	48KB V-RAM		
0B8000 – 0BBFFF	16KB V-RAM	For CGA Adapter (standard)	<*>
0C0000 – 0DFFFF	128KB ROM	Reserved for ROM on I/O slot	PROTECT MODE
0E0000 – 0EFFFF	64KB ROM	Reserved for ROM on I/O slot	
0F0000 – 0FFFFF	64KB BIOS ROM	64KB Bios ROM on main board Duplicated code assignment at address FF0000	
100000 – 1F0000	1MB RAM	Expansion RAM on main board (option)	
200000 – FDFFFF	14MB RAM	Optional RAM area on I/O slot	
FE0000 – FEFFFF	64KB ROM RAM	Reservd for RAM on I/O slot	
FF0000 – FFFFFF	64KB BIOS ROM	64KB BIOS ROM on main board. Duplicated code assignment at address 0F0000	

<*> Only one V-RAM can be enabled by H/W switch selection, except option-boards.

2-1-3. I/O Map

The CPU controls the I/O address space through which the CPU accesses I/O ports of external devices. There are 64K discrete 8-bit ports in this I/O address area, and any adjacent two ports can be used as a 16-bit port. Table 2-2 shows the I/O map.

Table 2-2. I/O map

I/O Address	Write	Read	
0000	CH0 base, current address	CH0 current address	DMAC #1
0001	CH0 base, current word count	CH0 current word count	
0002	CH1 base, current address	CH1 current address	
0003	CH1 base, current word count	CH1 current word count	
0004	CH2 base, current address	CH2 current address	
0005	CH2 base, current word count	CH2 current word count	
0006	CH3 base, current address	CH3 current address	
0007	CH3 base, current word count	CH3 current word count	
0008	Command register	Status	
0009	Request register	X	
000A	Single mask register	X	
000B	Mode register	X	
000C	Clear byte pointer flip-flop	X	
000D	Master clear	Temporary register	
000E	Clear mask register	X	
000F	All mask register bit	X	
0020	ICW1, OCW2, OCW3	IRR, ISR/Interrupt level	PIC #1
0021	ICW2, ICW3, ICW4, OCW1	IMR	

I/O Address	Write	Read	
0040	Counter #0 load	Counter #0 read	PIT
0041	Counter #1 load	Counter #1 read	
0042	Counter #2 load	Counter #2 read	
0043	Control word	X	
0060	Data write	Data read	Keyboard
0064	Command write	Status read	I/F
			(8742)
0061	Port B write	Port B read	Port B
0070	(NMI mark register)	Address generator	RTC(NMI
0071	Data register write	Data register read	mask)
0087	DMA channel 0	DMA channel 0	DMA page
0083	DMA channel 1	DMA channel 1	register
0081	DMA channel 2	DMA channel 2	
0082	DMA channel 3	DMA channel 3	
008B	DMA channel 5	DMA channel 5	
0089	DMA channel 6	DMA channel 6	
008A	DMA channel 7	DMA channel 7	
008F	Refresh	Refresh	
00A0	ICW1, OCW2, OCW3	IRR, ISR/Interrupt level	PIC #2
00A1	ICW2, ICW3, ICW4, OCW1	IMR	
00C0	CH base, current address	CH0 current address	DMAC #2
00C2	CH base, current word count	CH0 current word count	
00C4	CH base, current address	CH1 current address	
00C6	CH base, current word count	CH1 current word count	
00C8	CH base, current address	CH2 current address	
00CA	CH base, current word count	CH2 current word count	
00CC	CH base, current address	CH3 current address	
00CE	CH base, current word count	CH3 current word count	
00D0	Common register	Status	
00D2	Request mask ragister	X	
00D4	Single mask register	X	
00D6	Mobe register	X	
00D8	Clear byte pointer flip-flop	X	
00DA	Master clear	Temporary register	
00DC	Clear mark register	X	
00DE	All mask register bit	X	
00F0	Clear math copeocessor busy	X	NPX
00F1	Reset math coprocessor	X	(Option)
00F8	Math coprocessor	Math coprocessor	
|			
00FF			
01F0	Data ragister	Data ragister	HDC
01F1	Write precomp.	Error register	(option)
01F2	Sector count	Sector count	
01F3	Sector number	Sector number	
01F4	Cylinder low	Cylinder Yow	
01F5	Cylinder high	Cylinder high	
01F6	Drive/head	Drive/head	
01F7	Command register	Status register	
0020			Game I/O
|			(Option)
0207			
0278	Parallel data write	Parallel deta raad	Parallel
0279	X	Status register	printer
027A	Parallel control	Parallel control	port 2
			(Option)

I/O Address	Write	Read	
02F8	TX buffer	RX buffer(0)*	Serial
02F8	Divisor latch LSB(0)*	Divisor latch LSB(0)*	port 2
02F9	Divisor latch LSB(1)*	Divisor latch LSB(1)*	(factory
02F9	Interrupt enable register(0)*	Interruupt enable register(1)*	option)
02FA	Interrupt ID register	Interrupt ID register	
02FB	Line control register	Line control register	
02FC	Mobem control register	Modem control register	
02FD	Line status ragister	Line stetus register	
02FE	Modem status register	Modem status register	
02FF	Reserved	Reserved	
	*A number enclosed in( )shows the divisor latch access bit.		
0300 | 031F			Proto-type board (Option)
0360 | 036F			Reserved
0378	Parallel data write	Parallel deta read	Parallel
0379	X	Status register	printer
037A	Parallel control	Parallel control	port 2
0380 | 038F			SDLC bisync. 2 (Option)
03A0 | 03AF			Bisync. 1 (Option)
03B4	68B45 inbex register	X	CRTC
03B5	68B45 deta registre	68B45 deta register	(mono-
03B8	CRT control port	X	chrome)
03BA	X	CRT status port	
03D4	68B45 index register	X	CRTC
03D5	68B45 deta register	68B45 deta register	(color)
03D8	Mode contrl register	X	
03DA	Color select register	X	
03DB	Reset light pen latch	X	
03DC	Set light pen latch	X	
03F2	Digital output register(DOR)	X	FDC and
03F4	Command register	Status register	FDD I/F
03F5	Data register	Data register	
03F7	Drive control register(DCR)	Digital input register(DIR)	
03F8	TX buffer	RX buffer(0)*	serial
03F8	Divisor latch LSB(0)*	Divisor latch LSB(0)*	Port1
03F9	Divisor latch LSB(1)*	Divisor latch LSB(1)*	
03F9	Interrupt enable register(0)*	Interrupt enable register(1)*	
03FA	Interrupt ID register	Interupt ID register	
03FB	Line control register	Line control register	
03FC	Modem control register	Modem control register	
03FD	Line status register	Line statas register	
03FE	Modem status register	Modem status registter	
03FF	Reserved	Reserved	

*A numbr enclosed in( )shows the divisor latch access bit.

2-2. MAIN PWB OPERATION

The main PWB whose dimension is approximately 11.8 inches ×15 inches is mounted on the chassis of the system unit. Figure 2-1 shows a functional block diagram of the main PCB.

2-2-1. LSI Circuits (Figure 2-1)

The LSI circuits used in the main PCB are described below. (Abbreviations are used in the remaining section of this manual when describing these LSI circuits.)

- Central Processing Unit (CPU): 80286
  A 16-bit microprocessor that can directly access 1M-bytes of memory address in the real mode, 16M bytes in the protect mode, and 64K bytes of I/O address.
- Numeric Processor Extension (NPX): 80287
  This optional LSI circuit is a coprocessor for performing arithmetic operations. The 80287 can be installed into the internal 40-pin IC socket on a user's request.

* SC4751

The SC4751 has the following functional devices:

- **8237A-5 Direct Memory Access Controller (DMAC)**
  Controls data transfer between I/O devices connected to the DMA channels and memory without a CPU intervention.
  The computer uses two DMACs and they are connected in cascade.

- **82288 Bus Control Unit (BCU)**
  This chip generates signals necessary for controlling I/O devices and memory by receiving the $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$ status signals from the CPU.

- **82284 Clock Generator (CG)**
  Generates clock and reset signals necessary for the CPU. The 82284 also controls the SRDY (Synchronous ReaDY) signal and ARDY (Asynchronous ReaDY) signal to be sent to the CPU.

- **LS612 Memory Mapper**
  High order address register file for DMA which is used to expand the DMA address space from 64KB to 16MB.

- **System Control Logic (4K gate array)**
  Controls the system memory (ROM, RAM), memory refresh, hold conversion, and 8-bit/16-bit bus conversion.

* SC4752

The SC4752 has the following functional devices:

- **8259A Programmable Interrupt Controllers (PIC)**
  Accepts interrupt signals from the I/O devices, and gives priority to one of them. The interrupt signal selected by the 8259A is sent to the CPU. The system employs two PICs, and they are connected in cascade.

- **8250 Universal Asynchronous Receiver/Transmitters (UART)**
  Controls the RS-232C interface. Parameters for communication such as baud rate, word length, stop bit, and parity can be controlled by the CPU via these LSI circuits. A second UART is available as a factory option.

- **765 Floppy Disk Controller (FDC)**
  Controls the built-in floppy disk drive.

- **8254-2 Programmable Interval Timer (PIT)**
  Generates an interrupt signal when the predetermined timer becomes active, and determines the frequency of the signal to be sent to the speaker. The 8254-2 also generates trigger signals for DRAM refreshment.

- **Other I/O control logic (3K gate array)**
  Controls the printer, 80287, and display time out.

- **8742 Keyboard Controller**
  Controls data transfer between the CPU and the keyboard.

- **1288 LCD/CRT Controller**
  Controls the video memory data to display on the LCD or CRT.

- **1294 CGA Controller**
  Controls color display mode in conjunction with the 1288.

- **1292 MDA Controller**
  Controls monochrome display mode in conjunction with the 1288.

- **27256 Read Only Memory (ROM)**
  The computer uses two PROMs whose storage capacity is 32768 words×8 bits. They contain the power-on diagnostic program, BIOS, 128 character dot patterns in graphics mode and the floppy disk bootstrap loader.

- **27128 Read Only Memory (ROM)**
  Contains the character fonts for CGA and MDA.

- **41256 (41464) Random Access Memory (RAM)**
  A 640KB RAM area is provided on the main board, which consists of 16 chips of 256K×1-bit dynamic RAM (DRAM) and 4 chips of 64K×4-bit DRAM.

- **41464-10 Random Access Memory (RAM)**
  A 64KB RAM area is provided on the main board for the video memory. A 48KB RAM area is not used.

2-2-2. CPU (Figure 2-2)

The computer uses the 80286 microprocessor. Figure 2-3 shows pin assignments for the 80286, and Table 2-3 lists pin descriptions:

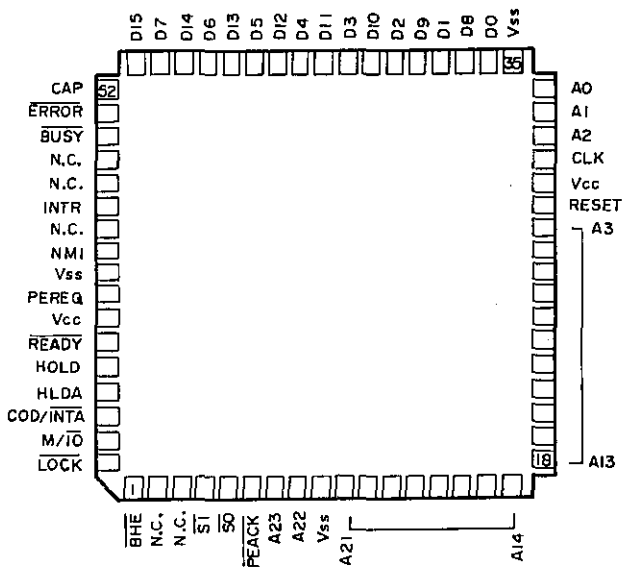


Figure 2-2. 80286 pin assignment

Table 2-3. 80286 pin descriptions

Signal	Pin No.	I/O	Name and Function
Vcc	30, 62	I	System power: +5V power supply.
Vss	9, 35, 60	I	System ground: 0V
RESET	29	I	System Reset clears the internal logic of the 80286 and is active HIGH. The CPU may be reinitialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET remains active, the output pins of the CPU enter the state shown below: 80286 Pin State During Reset Pin Value — Pin Names 1 (HIGH) — S0, S1, PEACK, A23–A0, BHE, LOCK 0 (LOW) — M/IO, COD/INTA, HLDA 3-state OFF — D15–D0 Operation of the 80286 begins after a HIGH to LOW transition of RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the CPU for interanl initializations before the first bus cycle to fetch a code from the power-on execution address is performed. A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.
CLK	31	I	System Clock provides the fundamental timing for 80286 systems. It is divided by two inside the CPU to generate the processor clock. The internal divide-by two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.
D15–D0	51–36	I/O	Data Bus inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
A23–A0	7, 8, 10–28, 32–34	O	Address bus outputs physical memory and I/O port addresses. A0 is LOW when data is to be transferred pins D7–D0. A23–A16 are LOW during I/O transfers. The address bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
$\overline{BHE}$	1	O	Bus High Enable indicates transfer of data on the upper bytes of the data bus, D15–D8. Eight-bit oriented devices assigned to the upper bytes of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active LOW and floats to 3-state OFF during bus hold acknowledge. $\overline{BHE}$ and A0 Encodings $\overline{BHE}$ Value — A0 Value — Fuaction L — L — Word transfer L — H — Byte transfer on upper half of data bus (D15–D8) H — L — Byte transfer on lower half of data bus (D7–D0) H — H — Reserved
$\overline{ST}$, $\overline{S0}$	4, 5	O	Bus Cycle status indicates initiation of a bus cycle and, along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is a Ts state whenever one or both are LOW. $\overline{ST}$ and $\overline{S0}$ are active LOW and float to 3-state OFF during bus hold acknowledge. 80286 Bus Cycle Status Definition COD/$\overline{INTA}$ — M/$\overline{IO}$ — $\overline{ST}$ — $\overline{S0}$ — Bus Cycle Initiated L — L — L — L — Interrupt acknowledge L — L — L — H — Reserved L — L — H — L — Reserved L — L — H — H — None; not a status cycle L — H — L — L — If A1=1 then halt; else shutdown L — H — L — H — Memory data read L — H — H — L — Memory data write L — H — H — H — None; not a status cycle H — L — L — L — Reserved H — L — L — H — I/O read H — L — H — L — I/O write H — L — H — H — None; not a status cycle H — H — L — L — Reserved H — H — L — H — Memory instruction read H — H — H — L — Reserved H — H — H — H — None; not a status cycle

(Continued)

Signal	Pin No.	I/O	Name and Function
M/$\overline{IO}$	67	O	Memory−I/O Select distinguishes memory access from I/O access. If HIGH during Ts, a memory cycle or a halt/shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. M/$\overline{IO}$ floats to 3−state OFF during bus hold acknowledge.
COD/$\overline{INTA}$	66	O	Code/Interrupt Acknowledge distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{INTA}$ floats to 3−state OFF during bus hold acknowledge. Its timing is the same as M/$\overline{IO}$.
$\overline{LOCK}$	68	O	Bus Lock indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{LOCK}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by 80286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{LOCK}$ is active LOW and floats to 3−state OFF during bus hold acknowledge.
$\overline{READY}$	63	O	Bus Ready terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{READY}$ LOW. $\overline{READY}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{READY}$ is ignored during bus hold acknowledge.
HOLD HLDA	64 65	I O	Bus Hold Request and Hold Acknowledge control ownership of the 80286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the 80286 will float its bus drivers to 3−state OFF and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the 80286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH.
INTR	57	I	Interrupt Request requests the 80286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8−bit interrupt vector that identifies the source of the interrpt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.
NMI	59	I	Non−Maskable Interrupt Request interrupts the 80286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80286 flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.
PEREQ $\overline{PEACK}$	61 6	I O	Processor Extension Operand Request and Acknowledge extend the memory management and protection capabilities of the 80286 to processor extensions. The PEREQ input requests the 80286 to perform a data operand transfer for a processor extension. The $\overline{PEACK}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH and floats to 3−state OFF during bus hold acknowledge. $\overline{PEACK}$ may be asynchronous to the system clock. $\overline{PEACK}$ is active LOW.
$\overline{BUSY}$ $\overline{ERROR}$	54 53	I I	Processor Extension Busy and Error indicate the operating condition of a processor extension to the 80286. An active $\overline{BUSY}$ input stops 80286 program execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (HIGH). The 80286 may be interrupted while waiting for $\overline{BUSY}$ to become inactive. An active $\overline{ERROR}$ input causes the 80286 to perform a processor extension interrupt when execution WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.
CAP	52	I	Substrate Filter Capacitor: a 0.047 μF ± 20% 12V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum DC leakage current of 1 uA is allowed through the capacitor. For correct operation of the 80286, the substrate bias generator must charge this capacitor to its operating voltage. The capacitor chargeup time is 5 milliseconds (maximum) after Vcc and CLK reach their specified AC and DC parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the 80286 processor clock can be phase synchronized to another clock by pulsing RESET LOW synchronous to the system clock.

2-2-3. Clock generator (Fig.2-3, 2-4)

Fig.2-3 shows the circuit of the PC-7200 clock generator which is contained in the SC4751.

Clock input to the SC4751 internal 82284 logic is selected to 19.2MHz, 16MHz, or12MHz by the signal received from the CPU clock select switch (S1). A 24MHz clock is internally divided into one half. The clock input is inverted inside the 82284 to supplied as CPU clock, PROCLK.

PROCLK is divided into 1/2, 1/4, and 1/16 by the internal frequency divider, to be supplied as SYSCLK, DMACLK, and SDCLK. Synchronization is attained with PROCLK by the signal $\overline{S1}$ from the CPU at the first cycle immediately after reset. Fig. 2-4 shows its timing.

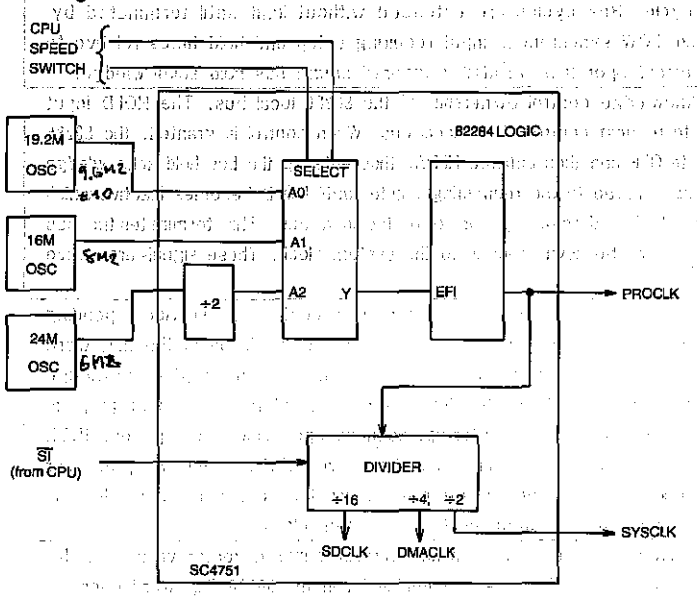


Figure 2-3. Clock generator circuit

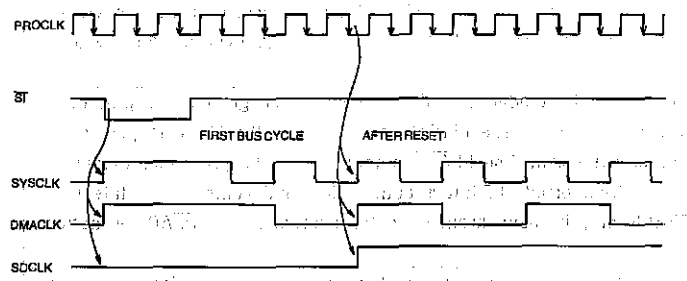


Figure 2-4. Timing chart of clock circuit

2-2-4. Reset Circuit (Figures 2-5, 2-6 and 2-7)

Figure 2-5 is a block diagram of the reset circuit, and Figure 2-6 shows a timing chart for this circuit. There are two methods in resetting the computer:

- System Reset
  This reset is performed by the RESET and $\overline{\text{RESET}}$ signals. The RESET signal is obtained by synchronizing this pulse signal with the system clock at the 82284 LOGIC.
  On the other hand, since the SC4751 emits the CPU RESET signal at the reception of the RESET signal, the entire system including the CPU is reset.
- CPU Reset
  This reset state is controlled by the CPU RESET signal. This reset signal is emitted when a CPU shutdown occurs, or when the RC signal from the keyboard interface controller (8042) is output. The shutdown state occurs when the CPU detects an internal error that prevents the execution of an instruction. If this happens, the CPU denotes this state to the reset circuit making the $\overline{S0}$ and $\overline{S1}$ signals LOW, M/$\overline{IO}$ signal HIGH, and A1 signal LOW. The RC signal is generated by the keyboard interface controller on the CPU's order. This RC signal is used in the case when the CPU changes its operation mode from the protect mode to the real mode.

When the CPU is reset, it first begins to execute instructions in the real mode. Before the CPU executes the power-on diagnostic program, it reads the shutdown status byte located at the address 0FH in the internal RAM of the RTC. Then the CPU checks the reason for the shutdown, and begins processing according to the information written in the shutdown status byte. The CPU RESET signal is output for the period of at least 16 bus cycles. Figure 2-8 shows the timing chart for the CPU reset.

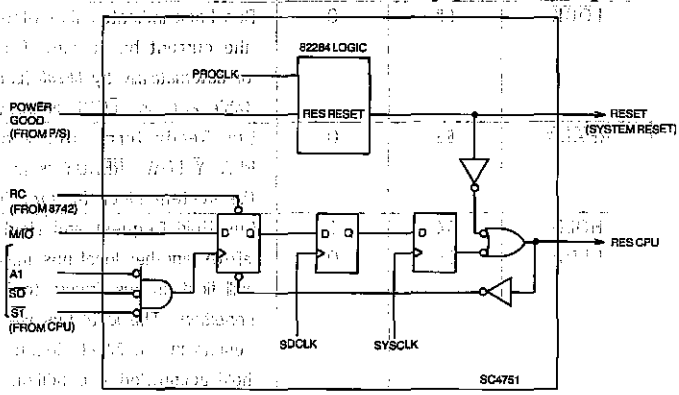


Figure 2-5. Reset circuit

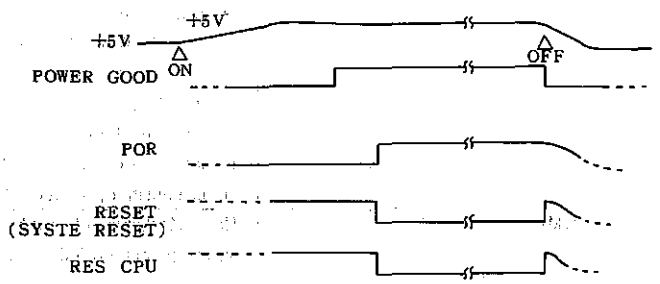


Figure 2-6. Timing chart of reset circuit

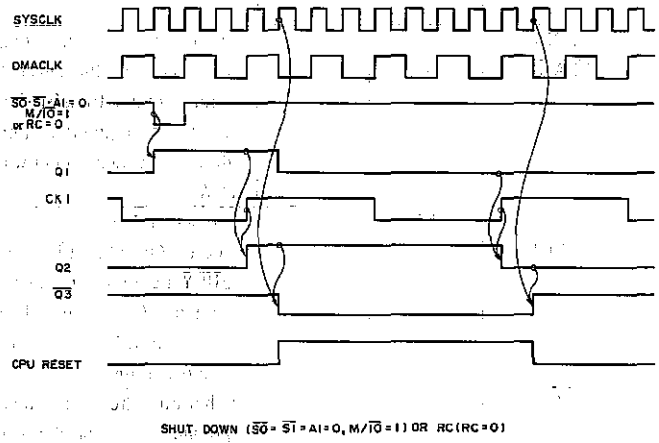


Figure 2-7. Timing chart of CPU reset

2-2-5. NMI and INTR Control Circuit (Figure 2-8)

The 80286 has two interrupt terminals; one is the Non-Maskable Interrupt (NMI) and the other is the Interrupt. However, in this system, the NMI signal is masked by the NMICS, ENAIOCK (Enable I/O Check) signals. (Refer to Figure 2-8.)

The NMI terminal is used to detect a malfunction of I/O devices connected to the optional slots.

CLRNMI signal is output from the 4-bit latch addressed at 061H, and the CS70H signal addressed at 070H is output from the I/O address decoding circuit in the SC4752.

The INTR signal is controlled by two PICs (PIC MASTER and PIC SLAVE) connected in cascade. The INT terminal of the PIC SLAVE

is connected to the IR2 terminal of the PIC MASTER; therefore, the PIC MASTER acts as a master PIC and the PIC SLAVE acts as a slave PIC. When the CPU is interrupted at the INTR terminal, it returns the interrupt acknowledge status to the BCU in the SC4751 by setting M/$\overline{IO}$, S0 and S1 terminals to LOW. When the BCU receives this status, it recognizes that the CPU could enter the interrupt acknowledge cycle, and the BCU asserts the INTA signal to the master PIC. The PIC sends the preassigned vector address corresponding to the I/O device to the CPU via the data bus. Table 2-4 lists the assignments of the IO0 to IR15 signals.

Table 2-4. Interrupt priority

Level		Function
PIC #1	PIC #2	
IRQ0		Timer output 0
IRQ1		Keyboard interface (output buffer full)
IRQ2		Interrupt from PIC #2
	IRQ8	Realtime clock interrupt (RTC)
	IRQ9	Software redirected to INT OAH (IRQ2)
	IRQ10	Reserved (option slot)
	IRQ11	Reserved (option slot)
	IRQ12	Reserved (option slot)
	IRQ13	NPX
	IRQ14	HDC (option slot)
	IRQ15	Reserved
IRQ3		Serial port 2 (UART)
IRQ4		Serial port 1 (UART)
IRQ5		Parallel port 2 (printer I/F)
IRQ6		FDC
IRQ7		Parallel port 1 (printer I/F)

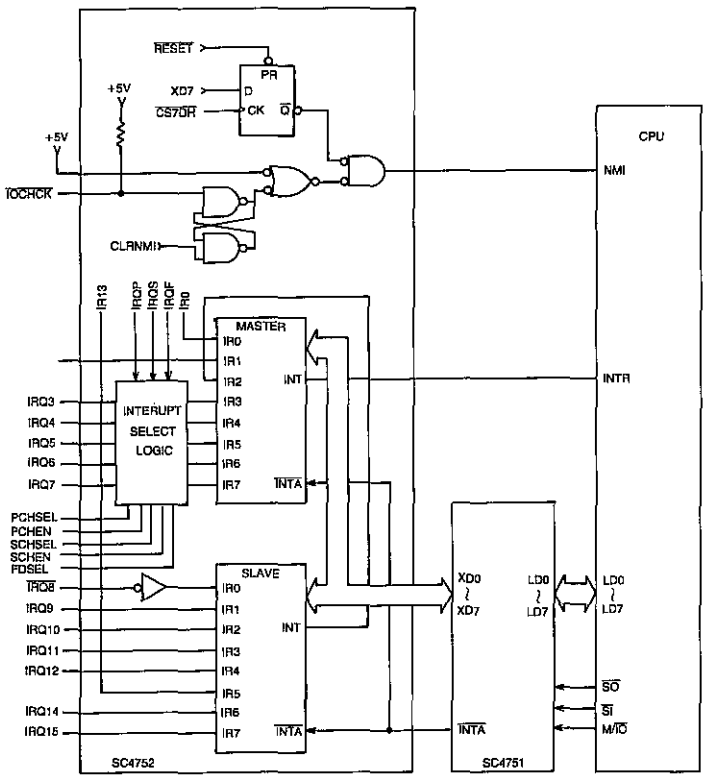


Figure 2-8. NMI and INTR control circuit

2-2-6. Bus Construction (Figure 2-1)

There are two buses on the main PWB; one is the address bus and the other is the data bus. These buses can further be divided in their functions. They are the address bus, data bus, and the data conversion circuit that controls these two buses.

2-2-6-1. Address Bus (Figure 2-2)

This bus is classified into 3 categories of functions:

1. **LA0 through LA23**
   These bus signals are directly output from the A1 through A23 terminals of the CPU to the memory address decoding circuit. The A0 signal is used by the SC4751 to simulatively assert the lowest bit (AA0) when the CPU performs a word access to an 8-bit device.
2. **SA0 through SA19**
   The SA1 through SA19 are obtained by latching the A1 through A19 signals with the ALE signal sent from the SC4751 at the latches. When the D-RAM chips are being refreshed, the SC4751 outputs the refresh address from its internal counter. The SA0 signal is obtained by buffering the AA0 signal. The SA0 through SA19 signals are used to address the V-RAMs on the main PCB and memory and an I/O device located on an option board. If there is an external microprocessor on the option board, the processor can handle resources on the main PWB, provided that the processor outputs addresses to this bus.
3. **ELA17 through ELA23**
   These signals are obtained by driving the LA17 through LA23 signals at the buffer, and they enable the 16M bytes memory access by the CPU in the protect mode. These signals are sent not to the devices on the main PWB but to the option slots. If an external microprocessor on the option board utilizes the resources on the main PWB, the processor outputs address signals to the LA17 through LA23 and SA0 through SA16 address buses.

2-2-6-2. Data Bus (Figure 2-9)

Like the address bus, the data bus can be classified into the following five categories: (Refer to Figure 2-9.)

1. **LD0 through LD7, XD8 through XD15**
   These data bus signals are sent directly to the CPU and NPX. And XD8 through XD15 signals are provided for odd address of the D-RAMs and ROM.
2. **SD0 through SD7, SD8 through SD15**
   The SD0 through SD15 signals are usually obtained by driving the D0 through D7 signals at the bi-directional buffer.
   When the CPU reads data from an 8-bit device or memory, data bus signals SD0 through SD7 are latched at SC4751. This is for maintaining the first data from even address until the CPU read the next odd address. In this case, the swap-buffer transfers an odd address data output to the SD0 through SD7 bus lines to the SD8 through SD15 bus lines. The operations mentioned above are controlled by the data conversion circuit described in Section 2-2-6-3.
3. **XD0 through XD7**
   These bus signals are used by I/O devices on the main PCB except for the FDC.

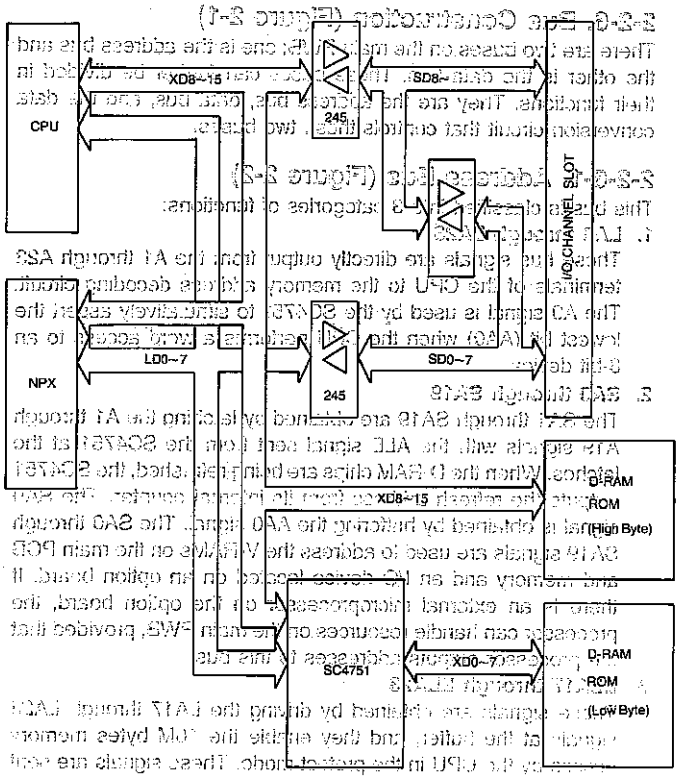


Figure 2-9. Data bus operation

2-2-6-3. Data Conversion Circuit

Fig.2-10 shows the concept of the data conversion circuit consisting of the SC4751, and Fig.2-11 shows a timing chart related to the circuit operation for an 8-bit memory or I/O device.

The data conversion circuit starts to operate when the CPU accesses an odd number word data of an 8-bit device.

When the SC4751 recognizes an access to an 8-bit device, the cycle is separated into two cycles of an even number byte and odd number byte. Because the CPU is in not ready state until the end of the second cycle, it operates as if these two cycles are in one cycle.

1.Even word read from an 8-bit device through XD0~7

(1) At the even number byte read cycle (first cycle), data received from bus XD0~7 are latched in the SC4751.

(2) At the odd number byte read cycle (second cycle), data received from bus XD0~7 are sent onto bus XD8~15 and, at the same time, the even byte data latched in the SC4751 are sent through bus XD0~7.

(3) After receiving the word data through LD0~7 and LD8~15, the CPU terminates accessing.

2.Odd word write to an 8-bit device through bus XD0~7

(1) At the even number byte write cycle (first cycle), data on bus LD0~7 are sent through XD0~7 to write.

(2) At the odd number byte write cycle (second cycle), data on bus XD8~15 are sent through XD0~7 to write.

3.Even word read from an 8-bit device through bus SD0~7

(1) At the even number byte read cycle (first cycle), data received from bus SD0~7 are sent onto LD0~7 and internally latched.

(2) At the odd number byte read cycle (second cycle), data received from bus SD0~7 are sent onto bus XD8~15 via the swap gate and, at the same time, the even byte data latched in the SC4751 are sent through bus LD0~7.

(3) After receiving the word data, the CPU terminates accessing.

4.Odd word write to an 8-bit device through bus SD0~7

(1) At the even number byte write cycle (first cycle), data on bus LD0~7 are sent through SD0~7 to write.

(2) At the odd number byte write cycle (second cycle), data on bus XD8~15 are sent to SD0~7 via the high gate and swap gate to write.

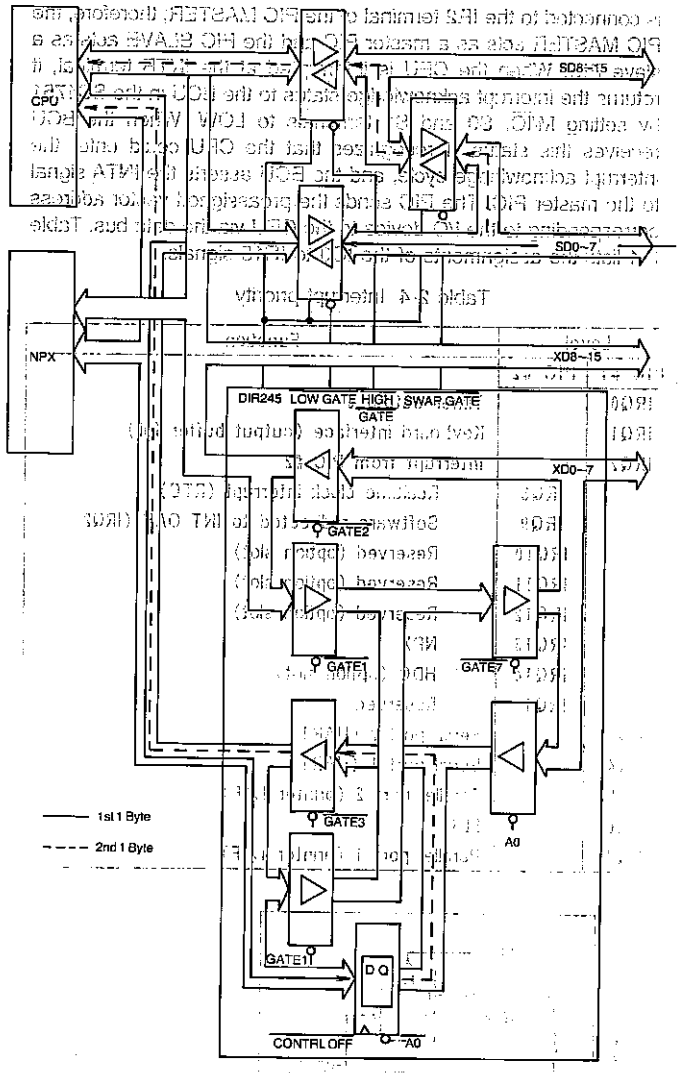


Figure 2-10. Word read operation for external 8 bit devices

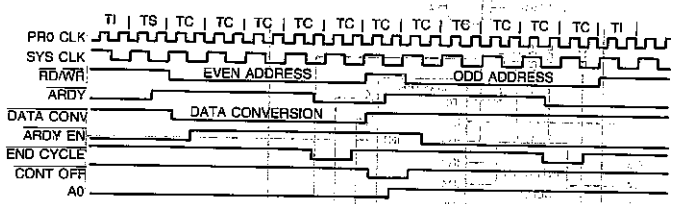


Figure 2-11. Timing chart

Table 2-5. Bus buffer control

Type	Byte Bus Cycle	LOWGATE	HIGHGATE	SWAPGATE	DIR245	Remarks
CPU	Even Memory Read	H	H	H	L	Memory on the main PWB
	Odd Memory Read	H	H	H	L	
	Even Memory Write	L	H	H	H	
	Odd Memory Write	H	L	H	H	
	Even I/O Read	H	H	H	L	8-bit I/O on the main PWB
	Odd I/O Read	H	H	H	L	
	Even I/O Write	L	H	H	H	
	Odd I/O Write	H	L	H	H	
	Even Memory Read	L	H	H	L	8-bit memory on the option slot
	Odd Memory Read	H	L	L	L	
	Even Memory Write	L	H	H	H	
	Odd Memory Write	H	L	L	H	
DMA	Even Memory Read (IOW)	H	H	H	L	I/O to/from memory on the main PWB
	Odd Memory Read (IOW)	H	H	H	L	
	Even Memory Write (IOR)	H	H	H	H	
	Odd Memory Write (IOR)	H	H	H	H	
	Even Memory Read (IOW)	L	H	H	L	I/O to/from 8-bit memory on the option slot
	Odd Memory Read (IOW)	H	L	L	L	
	Even Memory Write (IOR)	L	H	H	H	
	Odd Memory Write (IOR)	H	L	L	H	
MASTER	Even Memory Read	L	H	H	H	Memory on the main PWB
	Odd Memory Read	H	L	H	H	
	Even Memory Write	L	H	H	L	
	Odd Memory Write	H	L	H	L	
	Even I/O Read	L	H	H	H	8-bit I/O on the main PWB
	Odd I/O Read	H	L	H	H	
	Even I/O Write	L	H	H	L	
	Even I/O Write	H	L	H	L	

2-2-7. Memory

As a standard configuration, 16 chips of 256K-bit×1 DRAMs and 4 chips of 64K×4 DRAMs are implemented to constitute the memory size of 640KB. As there is a space of installing extra 8 chips of 256K-bit×4 DRAMs as an option, it is possible to expand to 1,664KB. Two chips of 32KB ROMs are on the board.

2-2-7-1. Memory address decoder

The SC4751 is employed to decode memory address. Address is created from address A16 to A23, A0, BHE, jumper S5, and $\overline{\text{REFRESH}}$ internally generated in the SC4751. Refer to Table 2-6 for the SC4751 output signals.

ROMCS

ROMCS is an output for address 0F0000H to 0FFFFFH and FF0000H to FFFFFFH, regardless of the switch S5 position.

CASL

1. Jumper S5 at "1-2"
CASL is an output when data of an even address side is accessed for address 000000H to 09FFFFH and 100000H to 1FFFFFH.

2. Jumper S5 at "2-3"
CASL is an output when data of an even address side is accessed for address 000000H to 07FFFFH and 100000H to 1FFFFFH.

CASH

1. Jumper S5 at "1-2"
CASH is an output when data of an odd address side is accessed for address 000000H to 09FFFFH and 100000H to 1FFFFFH.

2. Jumper S5 at "2-3"
CASH is an output when data of an odd address side is accessed for address 000000H to 07FFFFH and 100000H to 1FFFFFH.

RAS0

Regardless of the jumper S5 position, RAS0 is an output for address 000000H to 7FFFFFH.

RAS1

1. Jumper S5 at "1-2"
RAS1 is an output for address 080000H to 09FFFFH.

2. Jumper S5 at "2-3"
RAS1 is not an output.

RAS2

Regardless of jumper S5 position, RAS3 is an output for address 100000H to 17FFFFH.

RAS3

Regardless of jumper S5, RAS2 is an output for address 180000H to 1FFFFFH.

NOTE: When $\overline{\text{REFRESH}}$ is at a low, RAS1, RAS2, RAS3, and RAS4 are issued.

Table 2-6. SC4751 address assignment

Input												Output								
BHE	A0	A23	A22	A21	A20	A19	A18	A17	A16	S5	REFRESH	CASL	CASH	RAS0	RAS1	RAS2	RAS3	ROMCS	
×	×	×	×	×	×	×	×	×	×	×	0	0	0	1	1	1	1	0	REFRESH
0	0	0	0	0	0	0	×	×	×	×	1	1	1	1	0	0	0	0	000000H~07FFFFH word
0	0	0	0	0	0	1	0	0	×	0	1	1	1	0	1	0	0	0	080000H~09FFFFH word
×	×	0	0	0	0	1	0	0	×	1	1	0	0	0	0	0	0	0	080000H~09FFFFH any
×	×	0	0	0	0	1	1	1	1	×	1	0	0	0	0	0	0	1	0F0000H~0FFFFFH any
0	0	0	0	0	1	0	×	×	×	×	1	1	1	0	0	0	1	0	100000H~17FFFFH word
0	0	0	0	0	1	1	×	×	×	×	1	1	1	0	0	1	0	0	180000H~1FFFFFH word
×	×	1	1	1	1	1	1	1	1	×	1	0	0	0	0	0	0	1	FF0000H~FFFFFFH any
0	1	0	0	0	0	0	×	×	×	×	1	0	1	1	0	0	0	0	000000H~07FFFFH odd
0	1	0	0	0	0	1	0	0	×	0	1	0	1	0	1	0	0	0	080000H~09FFFFH odd
0	1	0	0	0	1	0	×	×	×	×	1	0	1	0	0	0	1	0	100000H~17FFFFH odd
0	1	0	0	0	1	1	×	×	×	×	1	0	1	0	0	1	0	0	180000H~1FFFFFH odd
1	0	0	0	0	0	0	×	×	×	×	1	1	0	1	0	0	0	0	000000H~07FFFFH even
1	0	0	0	0	0	1	0	0	×	0	1	1	0	0	1	0	0	0	080000H~09FFFFH even
1	0	0	0	0	1	0	×	×	×	×	1	1	0	0	0	0	1	0	100000H~17FFFFH even
1	0	0	0	0	1	1	×	×	×	×	1	1	0	0	0	1	0	0	180000H~1FFFFFH even

NOTE-1: The above table applies to memory read and write.

NOTE-2: The jumper S5 is "1" for "1-2" and 0 for "2-3".

2-2-7-2. RAM addressing (Figures 2-12 and 2-13)

Two chips of 256K-bit (32×8-bit) ROMs are mounted on the main board as a BIOS ROM.

Fig.2-12 below shows the block diagram and Fig.2-13 the timing chart.

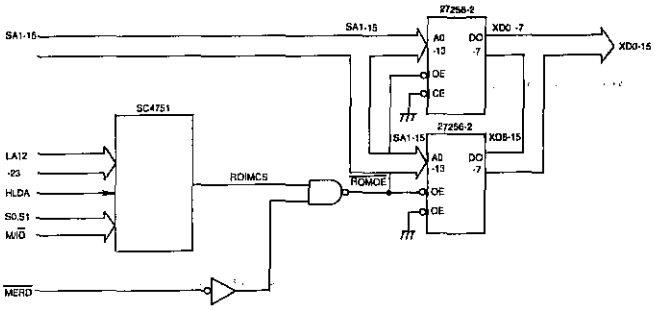


Figure 2-12

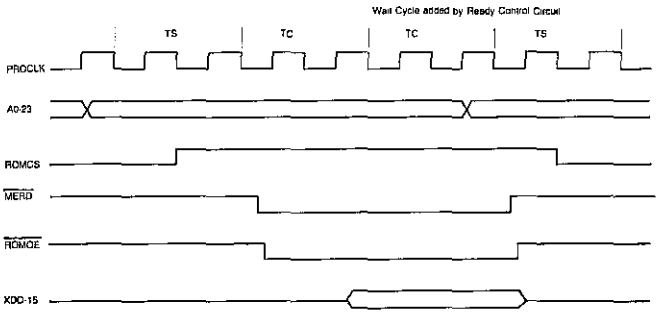


Figure 2-13. Timing chart of ROM addressing

2-2-7-3. RAM addressing

As a standard configuration, 20 chips of DRAMs (16 chips of 256K-bit×1 DRAMs and 4 chips of 64K-bit×4 DRAMs) are mounted on the main board, and, it is possible as an option to implement 8 chips of 1M-bit DRAMs (256K-bit×4 DRAMs).

Fig.2-14 below shows the block diagram and Fig.2-15 the timing chart.

The RAM areas are divided into eight groups.

① 000000H through 07FFFEH having even addresses
② 000001H through 07FFFFH having odd addresses
③ 080000H through 09FFFEH having even addresses
④ 080001H through 09FFFFH having odd addresses
⑤ 100000H through 17FFFEH having even addresses
⑥ 100001H through 17FFFFH having odd addressses
⑦ 180000H through 1FFFFEH having even addresses
⑧ 180001H through 1FFFFFH having odd addresses

① to ④ are the standard configuration RAM area and ⑤ to ⑧ are option RAM area. Each group is selected by CASL, CASH, RAS0, RAS1, RAS2, and RAS3 sent from the SC4751.

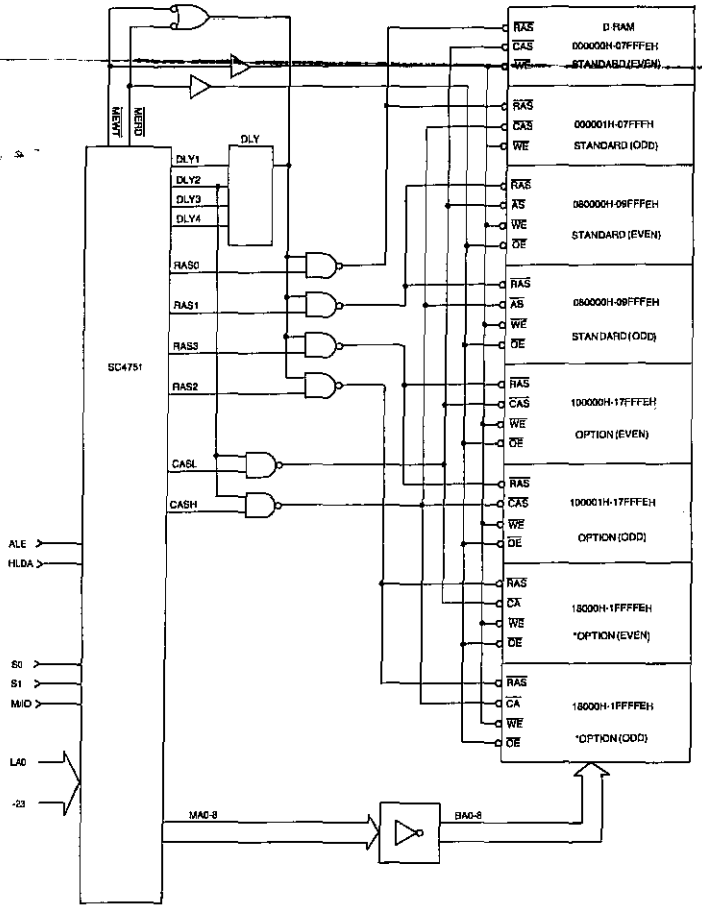


Figure 2-14. RAM addressing

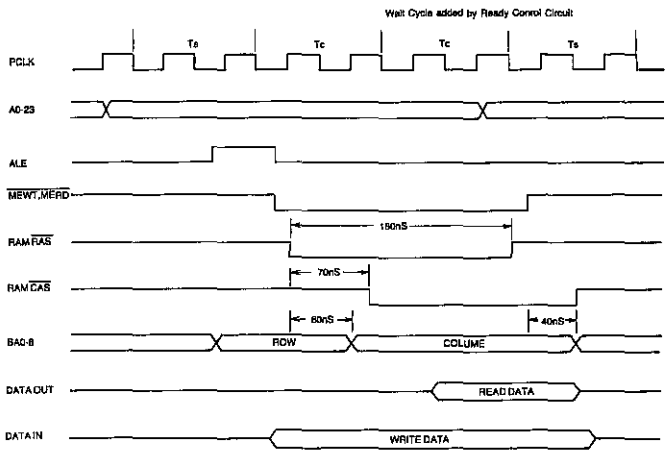


Figure 2-15. Timing chart of RAM addressing

2-2-7-4. D-RAM Refreshment (Figures 2-16 and 2-17)

Refreshment for D-RAM chips is performed by the refresh address counter and the hold control logic inside the GA1. D-RAM refreshment starts on a clock signal sent every 15 microseconds from the OUT1 terminal of the PIT. After the OUT1 terminal becomes HIGH, the GA1 sends the CPUHRQ signal to the CPU at the second falling edge of the DMACLK signal.

When the CPU receives the CPUHRQ (D-RAM refresh request) signal, it returns the CPUHLDA signal to the GA1 at the next CPU cycle, and then repeats the hold cycle. At this time, the $\overline{\text{REFRESH}}$ signal become LOW, and the GA1 makes the simulative memory read signal $\overline{\text{MEMR}}$ LOW for refreshment. Then the GA1 outputs a refresh address to the SA0 through SA7 address bus, after it counts up the refresh address counter inside it. Therefore, it requires 256 × 0.015 = 3.84 milliseconds to count up 256 row addresses

(256K-bit D-RAMs); 1.92 milliseconds to count up 128 row addresses (64K-bit D-RAMs). Figure 2-16 shows D-RAM refreshment, and Figure 2-17 shows the D-RAM refreshment timing chart.

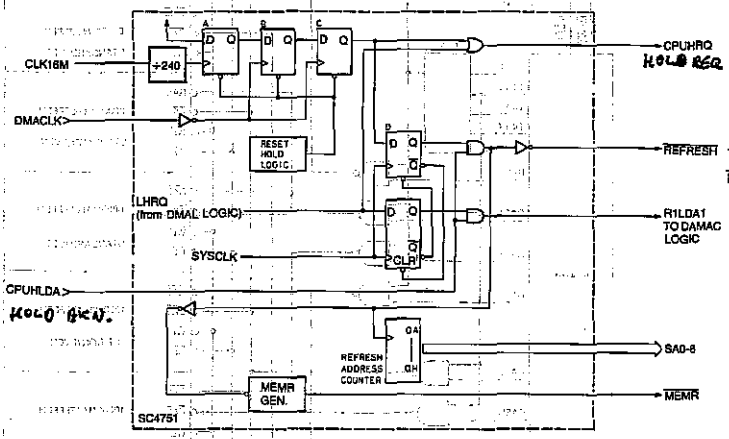


Figure 2-16. D-RAM refreshment

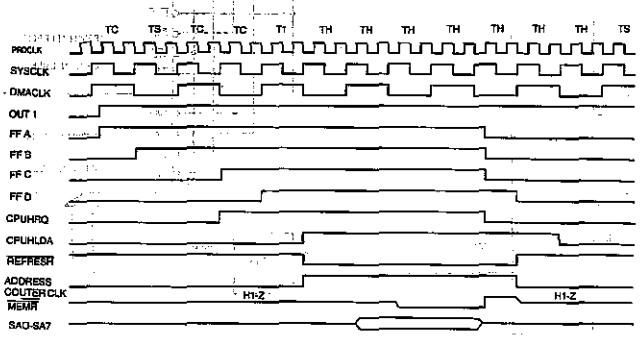


Figure 2-17. Timing chart of D-RAM refreshment

2-2-8. I/O Address Decoding Circuit (Figure 2-18)

This circuit is included in the SC4752 as shown in Figure 2-18. The role of this circuit is to output the chip select signals to each related circuit according to the address signals XA0 through XA9. However, an enable/disable status and channel select status of the following interface circuit is selected by DIP switches S4-1 through S4-5 as shown table 2-7.

* Floppy disk drive interface circuit
* Printer interface circuit
* Serial interface

The AEN signal, obtained by ANDing the HLDA and $\overline{\text{MASTER}}$ signals, indicates that the CPU is executing hold cycles. This signal is emitted on these conditions: DMA operation, refreshment for D-RAMs, and accessing of the resources on the main PWB by an external microprocessor. When the AEN signal becomes HIGH, the I/O decoding circuit is deactivated. Table 2-8 shows the relationship between the I/O address and the chip select signal.

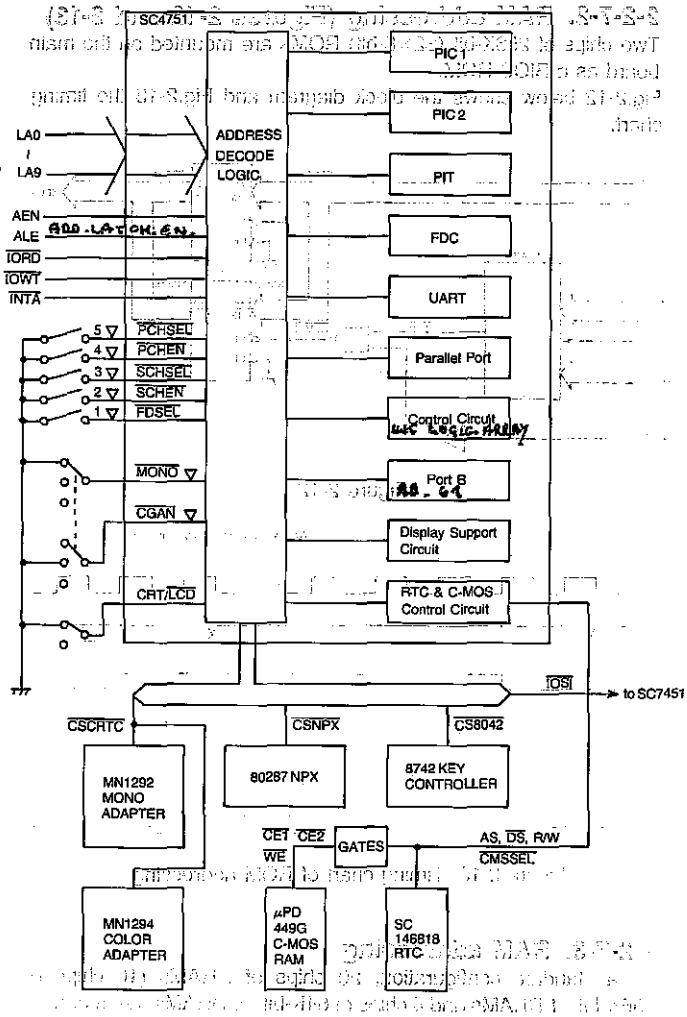


Figure 2-18. Address decoder block

Table 2-7. Dip switch S4

No.		ON	OFF
1	Internal FDC Address Select	L:3F0~3F7	H:370~377
2	Internal UART Enable/Disable	L:Enable	H:Disable
3	Internal UART Address Select	L:3F8~3FF	H:2F8~2FF
4	Internal Parallel Port Enable/Disable	L:Enable	H:Disable
5	Internal Parallel Port Address Select	L:378~37A	H:278~27A

Table 2-8. I/O address and chip select signal

Signal Name	Address	R/W	Device
$\overline{\text{CS8042}}$	60, 64	R/W	Keyboard Interface
AS	70	W	RTC Address Strobe
$\overline{\text{CMSSEL}}$	70	W	C-MOS RAM SELECT
$\overline{\text{DS}}$	71	R	RTC/C-MOS RAM Read
R/$\overline{\text{W}}$	71	W	RTC/MRS RAM Write
$\overline{\text{CSNPX}}$	F8-FF	R/M	80287 NPX
$\overline{\text{CSCRTC}}$	3B0-3BF	R/W	Monochrome Adaptor ($\overline{\text{MONO}}$=LOW)
	3D0-3DF	R/W	Color Graphic Adaptor ($\overline{\text{CGA}}$=LOW)
$\overline{\text{IOSI}}$		R/W	This signal LOW indicates CPU or MASTER Device accesses the device in the SC4752.

2-2-9. Ready Control Circuit (Figure 2-19, 2-20 and 2-21)

This circuit is included in SC4751, and controls the timing of the READY signal to be sent to the CPU. The READY signal is used to have the CPU continue the bus cycles until an actually accessing I/O device or memory becomes ready to be written/read data.

When the READY signal is HIGH, the CPU senses that the I/O device or memory is not ready to be accessed, and it repeats the TC cycles. When the READY signal becomes LOW, the CPU terminates its bus cycle. The READY signal is synthesized from the SRDY, SRDYEN, ARDY and ARDYEN signals at the internal circuit of the CG. The SRDY (Synchronous READY) signal is sampled by the CG at a falling edge of the phase 1 clock of the TC cycle, provided that the SRDYEN signal is LOW. The ARDY (Asynchronous READY) signal is sampled at the beginning of each TC cycle, provided that the ARDYEN signal is LOW.

In this computer, the SRDY signal is connected to the 0WS (Zero Wait Cycle) signal sent from the I/O device on the option slot, if the I/O device does not require a wait cycle. Therefore, if the 0WS signal is LOW, the CPU does not insert wait cycles.

The ARDY signal is controlled directly by the IOCHRDY signal sent from the memory or I/O device on the option slot. In conjunction with the ENDCYCLE signal, the ARDY signal controls the TC cycle (wait cycle) when the CPU performs the following operation:

operation \ clock	6MHz/8MHz	9.6MHz
8bit I/O	4wait	* 5wait Data conver.
16bit I/O	1wait	1wait
8bit Memory	4wait	* 5wait
16bit Memory (0-1FFFFF)	1wait	1wait
16bit Memory (200000-FFFFFF)	1wait	2wait
BIOS-ROM	1wait	1wait
16bit Memory (80000-9FFFF) (100000-1FFFFF)	1wait	2wait

The ARDYEN signal is used to concatenate even and odd addresses when the CPU performs a word access to an 8-bit memory or I/O device. (Refer to Section 2-2-6-3). Therefore, when the data conversion operation is performed, additional waits are inserted to the wait cycles listed above.

Figure 2-19 shows the ready control circuit. The IOCS16 signal shown in the figure is sent from the option slot to the SC4751, and becomes LOW when the I/O device is a 16-bit device. In other words, when this signal is LOW, the ENDCYCLE signal becomes LOW after one wait cycle passes, resets the flip-flop A in the GA1, and makes the ARDY signal LOW.

The FSYS16 is an ORed signal of the MEMCS16 signal sent from the option slot and the chip select signal sent from the ROM and RAM decode logic in SC4751. When the FSYS16 signal is HIGH, it indicates that addressed memory is 16-bit. The RAS signal is obtained by NORing the MEMR and MEMW signals. The RES/0WS signal is available by NORing the 0WS signal from the option slot and RESET signal from the CG.

The ready control circuit also inserts a wait cycle to the DMAC when in the DMA operation, using the DMARDY signal at the flip-flop C and D in the SC4751 Figure 2-19 shows the timing chart of a word access to the 16-bit memory or I/O device, and Figure 2-21 shows the timing chart of the DMARDY signal in DMA operation.

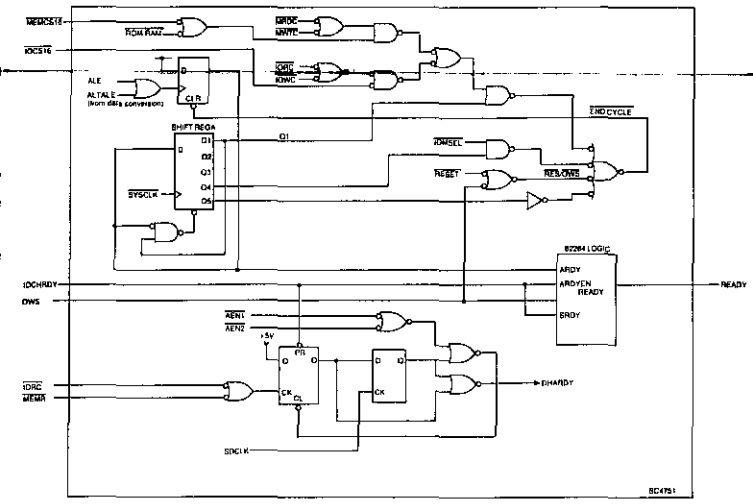


Figure 2-19. Ready control circuit

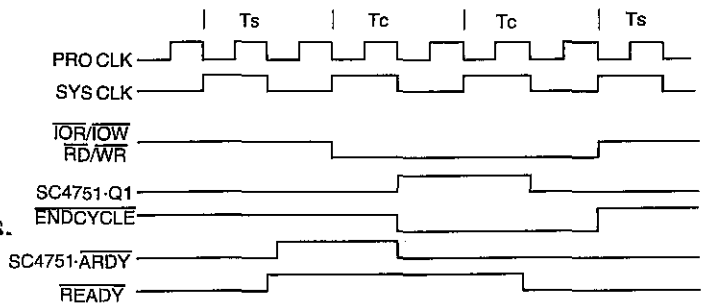


Figure 2-20. Timing chart of word access

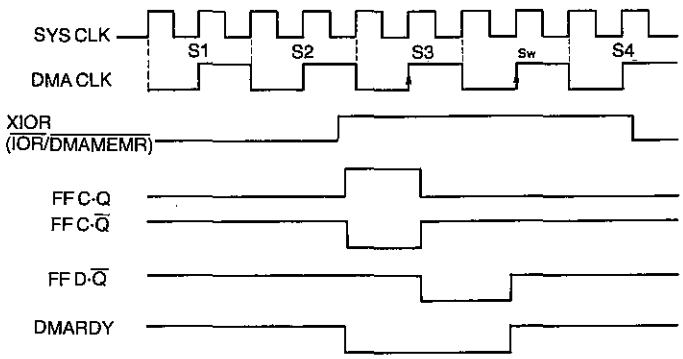


Figure 2-21. Timing chart of DMARDY signal

2-2-10. DMA (Figure 2-22 and 2-23)

Two DMACs are utilized to provide fast, efficient transfer of data from the I/O devices to memory, or vice versa, without intervention by the CPU. (The CPU is held in the hold cycle while the DMA operation is performed.) The DMACs are linked in a master/slave relationship, with the master and the slave, by connecting the hold request (HRQ) terminal of the slave DMAC with the service request input (DREQ4) terminal of the master DMAC, and the hold acknowledge input (HLDA) terminal of the slave with the DMA acknowledge (DACK4) terminal of the master DMAC. (See Figure 2-22). The master DMAC controls DMA channels 4 through 7, and the slave DMAC controls DMA channels 0 through 3. Channel 4 is used to connect the slave DMAC in cascade. The master DMAC is used to perform a word-by-word data transfer, and the slave DMAC is related to a byte-by-byte data transfer.

Table 2-9 lists the DMA channel assignments.

Table 2-9. DMAC channel assignments

Channel		Connection
Slave	0	Option slot
	1	Option slot
	2	FDC or option slot
	3	Option slot
Master	4	Cascade for slave
	5	Option slot
	6	Option slot
	7	Option slot

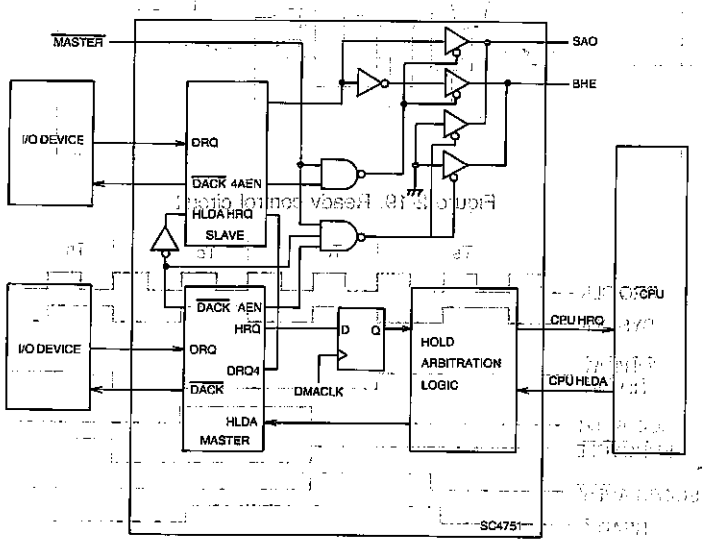


Figure 2-22. DMA operation

DMA operation is performed by the DMAC after making the CPU hold, using the CPUHRQ signal. The sequence for the DMAC operation is described below. (Refer to Figure 2-23.)

1. A DMAC service request is supplied by I/O devices by rising the corresponding DRQ input to HIGH.
2. The DMAC determines the validity of the request and outputs an active HIGH HRQ1 signal which is latched at HOLD ARBITATION LOGIC by the DMACLK signal.
3. The latched signal LHRQ is sent to the SC4751 and judges whether the D-RAM refresh circuit in the SC4751 is active or not. The refresh circuit makes the CPU hold with the CPUHRQ signal.
4. When the CPU receives the CPUHRQ signal, it enters in the hold state after a current bus cycle is completed. Then the CPU makes the impedance of the control lines and bus lines high, and returns the CPUHLDA signal to the SC4751.
5. The SC4751 judges whether the CPUHLDA signal sent from the CPU is a hold acknowledge signal for the internal D-RAM refreshment or for the DMA itself. If it is for the DMAC, the HOLD ARBITATION LOGIC outputs the HLDA1 signal to the DMAC in SC4751.
6. When the HLDA1 input is HIGH, the DMAC gains control of the bus and outputs HIGH level AEN signal to put the memory address on the bus. Since the DMAC can output only 16-bit address signals, the 8-bit page register that outputs an upper 8-bit address is provided in the system. This enables addressing up to 16M-byte memory areas.
   When the DMA transfer is a byte-by-byte basis, BHE is LOW, provided that the SA0 is HIGH (odd address). In the word-by-word transfer, this circuit forces both the SA0 and BHE signals LOW. (Refer to Figure 2-25 on this point.)
7. The DMAC outputs the DACK signal to select the requesting I/O device.
8. The DMAC activates the MRDC line to read data from memory and load it into the I/O device, or activates the MWTC line to read data from the I/O device and load it into the memory address.
9. The end-of-process (EOP) signal is output at the completion of the DMA cycle.

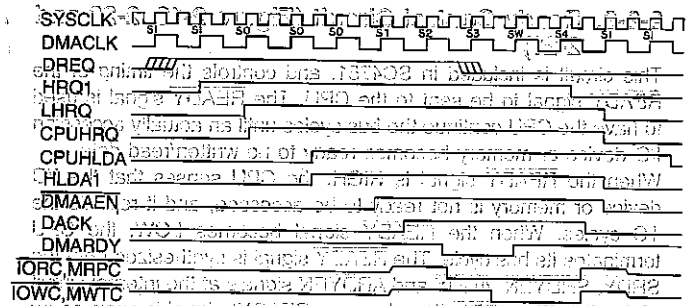


Figure 2-23. DMAC operation sequence

2-2-11. Printer Interface and System Status Port Circuit (Figure 2-24 and 2-25)

Figure 2-24 shows a functional block diagram of the printer interface circuit. this circuit consists of the print data register, printer status port and printer control register. The print data register, which is assigned at the I/O address 378H or 278H (selected by DIPSW S4-2) stores data to be sent to the printer. The contents of this register can be read by the CPU at the I/O address 378H via the buffer. The printer status port reads status information sent from the printr. This port is assigned at the I/O address 379H or 279H (selected by DIPSW S4-2)

The printer control register stores control codes to be sent to the printer. This register is assigned at the I/O address 37AH or 27AH (selected by DIPSW S4-2). Bit 4 of this register determines whether the ACK signal from the printer makes enable or disable as the CPU interrupt signal. When this bit is HIGH, interruption is disabled. The contents of this register can be read by the CPU at the I/O address; Figure 2-28 shows the timing chart for printing.

System status port

The system status port is a register provided to allow sensing the present system status by means of software and is mapped in the address same as the printer port. See Table 2-10 for bit assignment. Two signal lines are allocated to each bit, and alternately changes (toggle) each time the address 379H/279H is read. It is possible to know by interrogating the bit 7 which status is being checked. To know the correct status, 379H/279H must be read first, then 37AH/207A should be accessed to check the bit 7 to know which status is being checked.

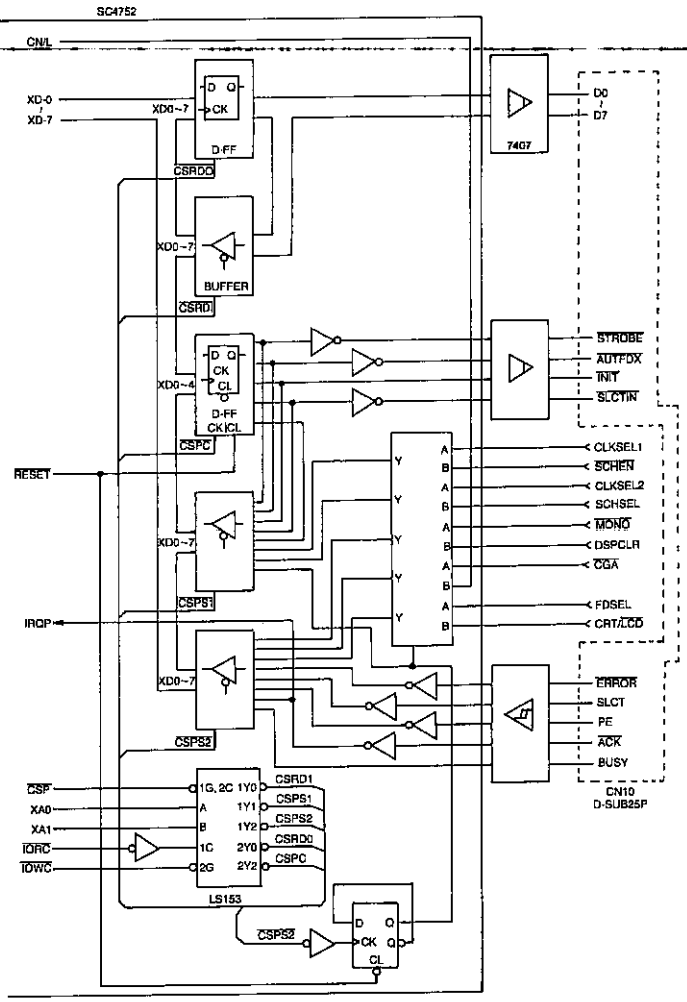


Figure 2-24. Printer interface circuit and system port

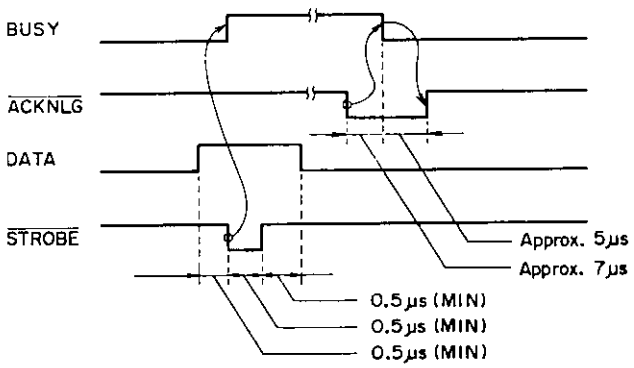


Figure 2-25. Timing chart for printing

Table 2-11. I/O address definition

I/O Address	Bit	Write	Read
378/278	0	Print deta 0(LSB)	Print deta 0 (LSB)
	1		
	2		
	3		
	4		
	5		
	6		
	7	Print deta 7 (MBS)	rint deta 7 (MSB)
I/O Address	Bit	Write	Read
379/279	0	—	CLKSEL1 $\overline{\text{SCHEN}}$
	1	—	CLKSEL2 SCHSEL
	2	—	$\overline{\text{MONO}}$ DSPCLR
	3	—	ERRORP
	4	—	SLCTP
	5	—	PE
	6	—	ACK
	7	—	BUSY
I/O Address	Bit	Write	Read
37A/27A	0	STB	STB
	1	AUTOFEED	AUTOFEED
	2	$\overline{\text{INITIALIZE}}$	$\overline{\text{INITIALIZE}}$
	3	SELECT	SELECT
	4	ENABLE IRQ	ENABLE IRQ
	5	—	$\overline{\text{CGA}}$ E/L
	6	—	FDSEL CRT/$\overline{\text{LCD}}$
	7	—	0 1

2-2-12. Serial Interface Circuit (Figure 2-26)

The computer is equipped with a serial interface as a standard feature. I/O addresses assigned for these interfaces are as follows:

* Standard interface: 3F8H through 3FFH or 2F8H through 2FFH

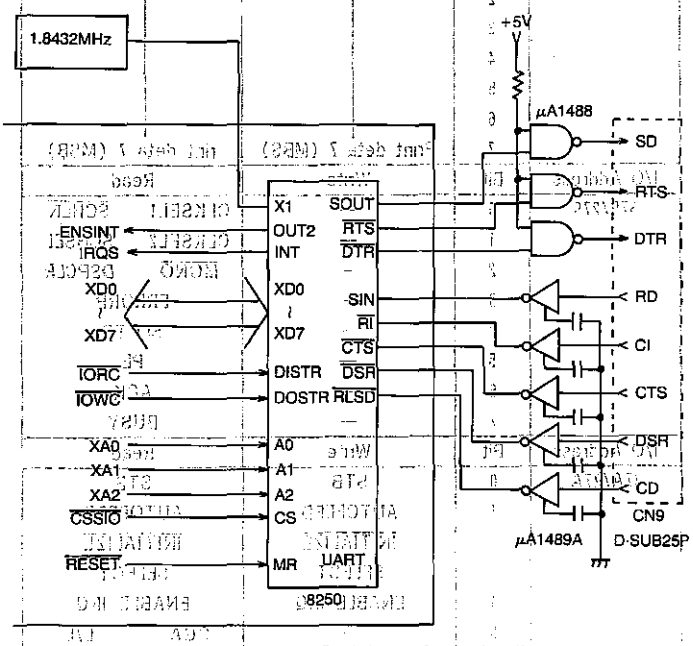


Figure 2-26. Serial interface circuit

The serial interface circuit consists of transmitter μA1488, receivers μA1489A and the UART (8250). The μA1488 convert TTL compatible signals sent from the UART to −12V to +12V signals conforming to the EIA standard, and output them via the RS-232 connector. The convert the EIA level reception signal to the TTL level and send it to the UART. The functional configuration of the UART is programmed by software via the data bus.

The UART performs a serial-to-parallel conversion of data characters received from a peripheral device or a mode, and performs a paralle-to-serial conversion of data characters received from the CPU. The CPU can read the complete status of the UART any time during the functional operation. Status information includes the type and condition of the transfer operations performed by the UART, and provides error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator. Also the UART has a complete modem control capability and a processor-interrupt system that minimizes the computing time for handling the communications link.

When the CPU assigns one of the addresses 3F8H through 3FFH as an I/O address, the LOW level $\overline{\text{CSSIOAA}}$ signal sent from the I/O address decoding circuit is emitted to the UART. The UART then selects the internal register to be ZORC connected to the data bus according to the state of the DLAB (Divisor Latch Access Bit). The DLAB is bit 7 of the line control register. Table 2-11 lists the states of registers indicated at each I/O address, and Table 2-12 lists the bit assignment of each register.

Table 2-12. Register status

I/O Address	A2	A1	A0	$\overline{\text{XIOR}}$	$\overline{\text{XIOW}}$	DLAB	
3F8	L	L	L	L	H	X	Receive buffer register
3F8	L	L	L	H	L	X	Transmit holding register
3F8	L	L	L	*	*	1	Divisor latch LSB
3F9	L	L	H	*	*	1	Divisor latch LSB
3F9	L	L	H	*	*	0	Interrupt enable register
3FA	L	H	L	*	*	X	Interrupt identification register
3FB	L	H	H	*	*	X	Line control register
3FC	H	L	L	*	*	X	Modem control register
3FD	H	L	H	*	*	X	Line status register
3FE	H	H	L	*	*	X	Modem status register

$\overline{\text{XIOR}}$ becomes LOW at read operation
$\overline{\text{XIOR}}$ becomes LOW at write operation
X: Not applicable.

Table 2-13. Register bit assignments

I/O Address	Bit	Description
3F9 Interrupt enable register	0	H:Enable data
	1	H:Enable TX holding register empty interrupt
	2	H:Enable receive line status interrupt
	3	H:Enable modem status interrupt
	4−7	Always LOW
3FA Interrupt identification register	0	H:No interrupt pending
	1	Interrupt identification bit 0
	2	Interrupt identification bit 1
	3−7	Always LOW
3FB Line control register	0	Word length select bit 0
	1	Word length select bit 1
	2	Numeer of stop bit
	3	Parity enable
	4	Even parity select
	5	Stuck parity
	6	Set break
	7	Divisor latch access bit (DLAB)
3FC Modem control register	0	Data terminal ready (DTR)
	1	Request to send (RTS)
	2	Out 1
	3	Out 2
	4	Loopback
	5−7	Always LOW
3FD Line status register	0	Data ready (DR)
	1	Overrun error (OR)
	2	Parity error (PE)
	3	Framing error (FE)
	4	Break interrupt (BI)
	5	Transmit holding register empty (THRE)
	6	TX Shift empty (TSRE)
	7	Always LOW
3FE Modem status register	0	Delta clear to send (DCTS)
	1	Delta data set ready (DDSR)
	2	Trailing edge ring indicator (TERI)
	3	Delta data carrier detect (DDCD)
	4	Clear to send (CTS)
	5	Data set ready (DSR)
	6	Ring indicator (RI)
	7	Delta carrier detect (DCD)

2-2-13. Timer and Speaker Driver Circuit (Figure 2-27)

Figure 2-27 shows the timer and buzzer driver circuit. This circuit has the following functional features:

* Generates an interruption signal when the predetermined timer becomes active.
* Determines the frequency of a signal to be sent to the buzzer. (Counter 2)

These operations are based on 1.19 MHz of clock signal which is obtained by dividing 14.31818 MHz signal into 12 at SC4752. The PIT has three 16-bit counters. The OUT0 signal sends an interruption request toi the CPU via PIC when the predetermined timer counting has been completed. The OUT1 terminal is not used by the system. The OUT2 signal and audio frequency signal to the speaker according toi the requirements of the software. This signal is NANDed with the signal sent from the PORTB, and then drives transistor Q2 to sound the buzzer.

Command signals related to the speaker are output by writing data to the latch assigned at the I/O address 61H, called PORTB. Similarly, these states can be read from the buffer assigned at the I/O address 61H. Table 2-14 lists data loading and reading for each counter.

Table 2-14. Counter assignments

I/O Address	A1	A0	RD−	WR−0	
0040	L	L	L	H	Read counter No.0
0040	L	L	H	L	Load counter No.0
0041	L	H	L	H	Read counter No.1
0041	L	H	H	L	Load counter No.1
0042	H	L	L	H	Read counter No.2
0042	H	L	H	L	Load counter No.2
0043	H	H	L	H	No−operation (3−state)
0043	H	H	H	L	Write control word

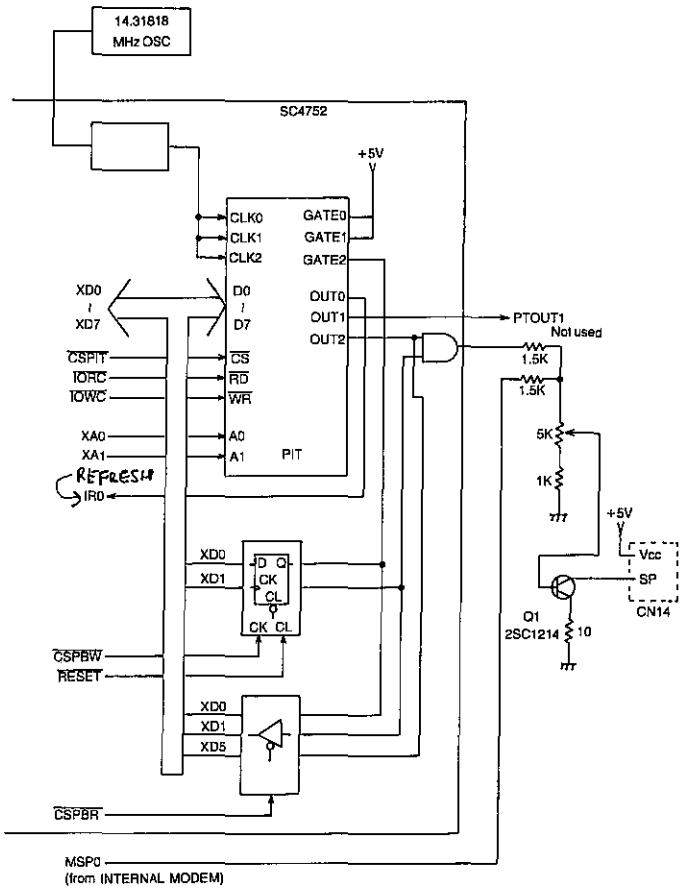


Figure 2-27. Timer & speaker driver circuit

2-2-14. Real Time Clock and C-MOS RAM Circuit (Figure 2-28)

Not only does the RTC (146818) act as a real-time clock, but it has a 64-byte RAM backed up by the battery. The CPU can access the RTC only when the POWER GOOD signal sent from the power supply unit is HIGH. Normally, a HIGH level POWER GOOD signal means that the system unit is turned on.

When the CPU writes/reads data to/from the RTC, it first assigns an internal address of the RTC to be written/read data at the I/O address 70H, then transfers data via the I/O address 71H. When the CPU sends a write command to the I/O address 70H, a short HIGH level pulse is sent to the AS (Address Strobe) terminals of the RTC. The AS terminal is used to latch contents of AD0-AD7 into the address latch of the RTC.

Then the CPU sends a read/write command to the I/O address 71H, the HIGH/LOW level R/W signal according to the read/write command and LOW/HIGH level DS signal are output from the address decoding circuit, in the SC4752. At this time, the RTC puts the data of its RAM addressed by the I/O address 70H to/from the data bus.

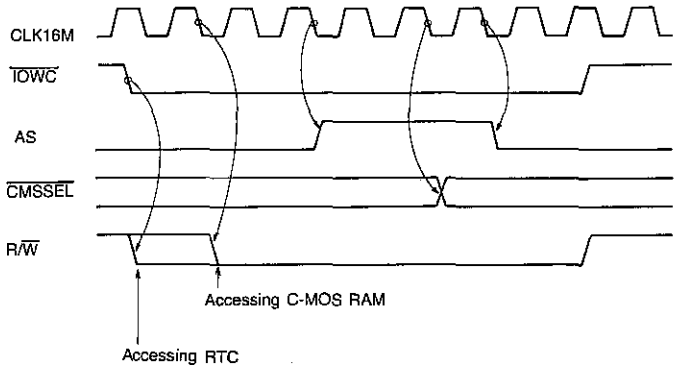


Figure 2-28. Timing chart of RTC & C-MOS RAM access

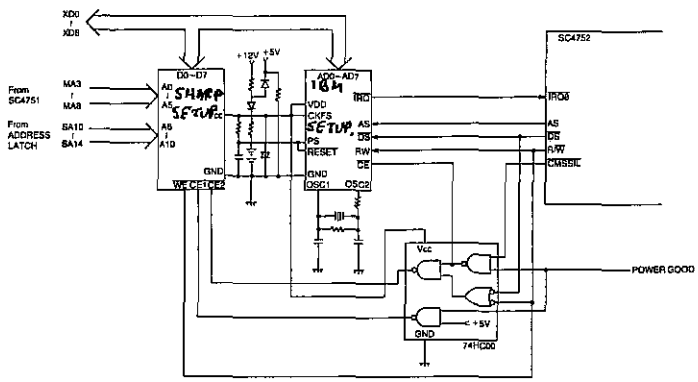


Figure 2-29. RTC & C-MOS RAM circuit

Fourteen bytes of the 64-byte RAM in the RTC are used for real-time clock function. Figure 2-9 shows the RTC circuit, and Table 2-15 shows the memory map of the RTC.

Table 2-15. RTC memory map

Address	Function
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	*Diagnostic status byte
0F	*Shutdown status byte
10	Disk drive type byte—drives A and B
11	Reserved
12	Hard disk type byte—drives C and D
13	Reserved
14	Equipment byte
15	Low-base memory byte
16	High base-memory byte
17	Low expansion memory byte
18	High expansion memory byte
19—2D	Reserved
2E—2F	2—byte C—MOS checksum
30	*Low expansion memory byte
31	*High expansion memory byte
32	*Date century byte
33	*Information flags(set during power on)
34—3F	Reserve

① Similar as the RTC, the CMOS RAM is battery backed up and can be accessed only when POWERGOOD is at a high. CMOS RAM is accessed in the same manner as RTC RAM. The addresses assigned to CMOS-RAM are 40h to 7Fh.

② Six bits A0 through A5 of the CMOS RAM address lines are connected to MA3~8 of the SC4751. In MA3~8 are latched XD0~5 when the I/O address 70H was written, and sent out. In A6~A10 are connected with signals SA10~14 in which latched the address from the CPU.
The signal $\overline{\text{CMSSEL}}$ turns high with a "0" state of XD6 when the address 70H is written and turns low when XD6 is "1". The CMOS RAM is enabled to read and write when $\overline{\text{CMSSEL}}$ is at a low, and the RTC can be accessed when it is at a high.

Table 2-16. C-MOS RAM memory mapping

Backed Up C-MOS RAM information

Address	Description
40	Reserved
41	Cursor type
42	Backlight timeout
43-44	Setting serial port
45	Logical device
46	Internal SI0*
47	Printer interface
48	Printer style
49	Printer mode
4A	Internal modem parameter
4B	Internal modem setup
4C-4F	Reserved
50-63	Printer setup code
64-7E	Reserved
7F	CMOS check sum

2-2-15. FDD Interface Circuit (Figure 2-30)

The FDD interface circuit supports up to two floppy disk drives. Figure 2-32 is a block diagram of this circuit. An FDC μPD765AC (manufactured by NEC) is the heart of this circuit, and it interfaces between the floppy disk drive units and the CPU.

The computer was designed so that it can read data from the FDD at three different transfer rates, three of them-250 Kbps, 300Kbps and 600 Kbps VFOs—are included in the one-chip LSI MB4107. The DIR (Digital Input Register) was originally an 8-bit read-only register; however, since bits 0 through 6 of it are used to control hard disk drives, only bit 7 is used for FDDs. The DOR (Digital Output Register) is a write-only register. It selects drives and control the FDC.

There is a DCR (Drive Control Register), pre-compensation circuit, and clock generation circuits as other interface circuits. The DCR, a 2-bit write-only register, selects the clock frequency of the FCLK (FDC Clock) and WCLK (Write Clock), and selects the VFO circuit.

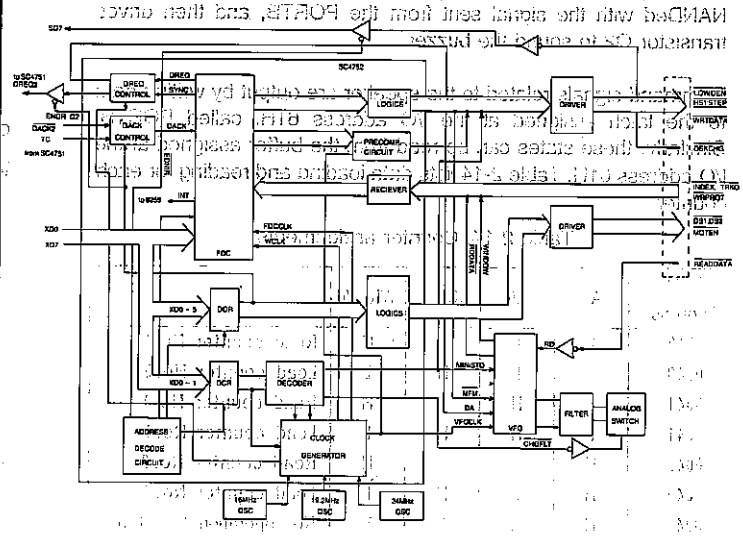


Figure 2-30. Block diagram of FDD interface

2-2-15-1. FDC

The FDC employs the μPD765AC device in the SC4752LSI. Using a data bus, the FDC transfers status and data corresponding to the command sent from the CPU. To detect the selection by the CPU, the chip select signal and A0 signals are used.

The FDC has two important registers: a status register and a data register. The status register stores the status information of the FDC and floppy disk drives. The status register is assigned by the I/O address 3F4H or 374H and the data register is 3F5H or 375H. Table 2-17 lists the FD interface signals.

FD Interface

CLK24M	24MHz input.
CLK16M	16MHz input.
$\overline{\text{ENDIR}}$	Port decode signal to read drive status, active low.
DS1	Drive-1 select, active high.
DS2	Drive-2 select, active high.
MOTEN	Drive unit motor enable, active high.
HS1	Head select, side-1 when high.
STEP	Head stepping signal, active high.
DIR	Seek direction signal.
WRTDATA	Data write to disk.

WRTEN Write enable, active high.

$\overline{\text{INDEX}}$ Index pulse input from drive, active low.

$\overline{\text{WRTPROT}}$ Write protect indication, active low.

$\overline{\text{TRK0}}$ Head track 0 signal, active low.

$\overline{\text{RDDATA}}$ Read signal from VFO.

WINDOW Read data window signal from VFO.

$\overline{\text{MFM}}$ MFM/FM discriminating signal (MFM: low).

MINID/$\overline{\text{STD}}$ Mini floppy disk/standard floppy disk select output (standard floppy disk: low).

DA Output to indicate the MB4107 external VFO data field.

VFOCLK Clock output to external VFO MB4107.

FDSEL Internal FDC address select input.
03F2H~03F7H: low
0372H~0377H: high

CLK19M 19MHz input.

$\overline{\text{CHGFLT}}$ VFO external resistor select signal. Low in the 2DD/2HD mode.

TABLE 2-17. FD INTERFACE SIGNALS

2-2-15-2. DOR

This register selects drive A or B, controls the drive motors, reset FDC and defines whether to permit an interruption of the FDC or DMA request or not.
The DOR consists of 16-bit flip-flop circuits. Description for each bit are listed in Table 2-18.

Table 2-18. DOR bit descriptions

I/O Address	Bit	Description
3F2	0	This bit selects the disk drive. LOW: drive A (drive1) HIGH: drive B (drive2)
	1	Low level of this bit enables the drive select signal.
	2	FDC is reset when this bit is LOW.
	3	HIGH level of this bit allows FDC interrupt and DMA request.
	4	HIGH level of this bit enables the drive motor and the drive A can be selected.
	5	HIGH level of this bit enables the drive motor and the drive B can be selected.

Data transfer between FDD and memory is executed by the DMAC and FDC. The FDC sends the DREQ signal to DMAC when data transfer to/from the FDD becomes enable. This signal delays four 2MHz clocks (2 ms) for adjustment of DREQ timing. After the delay the signal is sent to the DMAC DREQ2 line.
After passing through the tristate gate, control is done by the bit 3 of the FDD control register.

When the DMAC receives a DMA request from the FDC, it places the CPU in hold state, and then sends the DACK2 signal to the FDC after it is ANDed with bit 3 of the FDD control register to begin data transfers.
When the byte-by-byte base data transfer is completed, the FDC sends an interruption signal via the IRQ6 terminal of the PIC. In this case, if bit 3 of this register is LOW, the DMA request and interruption are disabled.

2-2-15-3. DIR

The DIR was used as an 8-bit read-only register assigned at the I/O address 3F7H or 377H; however, 7 of 8 bits are reserved for hard disk drives in actual use. The CHANGE signal selects this CNG signal. This bit is active unless a disk is present and a step pulse is received when the drive is selected.

2-2-15-4. DCR

This write-only register is assigned at the I/O address 3F7H, and it selects the VFO, and sets the condition of the FCLK and WCLK signals. Table 2-19 lists the bit assignment of this register.

Table 2-19. DCR bit assignment

Bit 1	Bit 0	Transfer Rate	FDC Clock	Write Clock	Applicable Drive	Applicable Medium
L	L	500 Kbps	8MHz	1MHz	2HD	2HD
L	H	300 Kbps	4.8MHz	0.6MHz	2HD	2D
H	L	250 Kbps	4MHz	0.5MHz	2D	2D
H	H	250 Kbps	4MHz	0.5MHz	2D	2D

Because the data concerning the disk drive type is stored in the RAM of the RTC, the CPU reads the data before it accesses FDDs. Then the CPU writes the data to the DCR to select the VFO and to set the $\overline{\text{LOWDEN}}$, WCLK, VFOCLK and FCLK signals. A 2HD FDD can also read a 2D medium.

2-2-15-5. Clock Generator Circuit

This circuit is included in the SC4752, and generates the signals listed below.

FCLK

A clock signal for the FDC. It is switched to one of 8 MHz, 4.8 MHz and 4 MHz by the DCR.

WCLK

The FDC synchronizes write data with clock signal WCLK. The frequency of the WCLK signal can also be switched to one of 1 MHz, 0.6 MHz and 0.5 MHz by the DCR.

2-2-15-6. Data Separation Circuit

Using the VFO, this circuit generates the window signal to separate data bits and clock bits from the raw data read from the FDD. VFO used in 500Kbps, 300bps and 250Kbps transfer rates are included in the one-chip LSI (MB4107) respectively. Table 2-20 listes the assignment of the VFO.

Table 2-20. VFO assignment

FDD	Medium	Transfer Rate	CLK	WCLK	Bit1 of DCR	Bit0 of DCR
2HD	2HD	500 Kbps	8MHz	1MHz	L	L
2HD	2D	300 Kbps	4.8MHz	0.6MHz	L	H
2D	2D	250 Kbps	4MHz	0.5MHz	H	x

2-2-15-7. Pre-compensation Circuit

This circuit is included in the SC4752, and advances or delays write data sent from the FDC to the FDD according to the write data pattern. The FDC changes the status of the PS0 and PS1 signals in response to the pattern of the write data sent from the CPU. Figure 2-31 shows the timing chart of this circuit.

Table 2-21. Write data pattern

PS1	PS0	Write Pattern	
L	L	Normal	
L	H	Late	0001 or 110
H	L	Early	1000 or 011

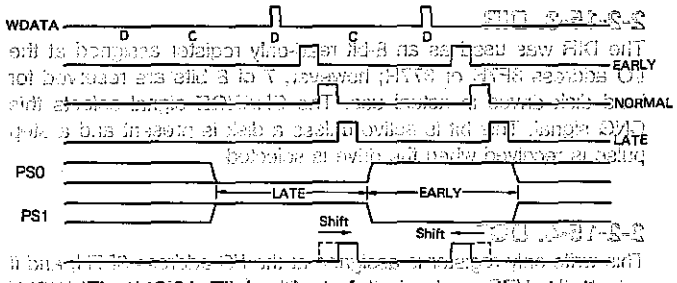


Figure 2-31. Timing chart of pre-compensation circuit

2-2-16. Keyboard Interface (Figure 2-32 and 2-33)

This interface circuit employs the one-chip microprocessor 8742, and is assigned at I/O address 60H or 64H. This processor has a 2KB ROM and 128-byte RAM, and interfaces between the keyboard and the CPU. The 8042 receives serial key scan codes consisting of an 8-bit key code and a 1-bit parity sent from the keyboard. It converts the codes to a parallel format system scan code to be sent to the CPU. The 8042 also receives commands from the CPU, and sends commands to the keyboard after interpreting them.

In addition to the functions described above, the keyboard interface can modify the keyboard interface protocol and the key scan codes during power-on initializing.

With the four output terminals and two input terminals, the 8042 performs the following operations.

*** P16 (input)**
Detects the type of a display adapter reading the status of switch S-2.

*** P17 (input) ... INH**
Reads the status of the keylock from SC4752 LSI. If the key is locked, this terminal is LOW. If it is LOW, the keyboard interface cancels data from the keyboard.

*** P24 (output) ... OPT BUF FULL**
A one-byte data sent from the kyboard makes this terminal active, indicating that the output buffer in the keyboard interface is full. This signal is sent to the IRQ1 terminal of the PIC, requesting that the CPU reads these data.

*** P21 (output) ... A20GATE**
When this signal becomes LOW, the A20 signal on the address bus is forced to LOW.

*** P20 (output) ... RC**
When the CPU requires a change in its operation mode from protect mode to real mode, it sends certain commands to make the terminal HIGH. The RC signal is sent to the SC4751 and the CPU RESET signal is generated. Finally, the CPU is reset and thus returns to the real mode.

*** P23 (output) ... KEYINP**
When a key depression is sensed, a short pulse of low state is sent to the SC4752.

The keyboard and the keyboard interface are related by the KCLK and KDATA lines. Before the 8042 sends data, it always makes the KCLK line HIGH and KDATA line LOW. The keyboard CPU always monitors the status of these two lines. If the two lines are in the condition above, the keyboard enters the data reception mode. Then the 8042 sends a start bit, an 8-bit data, a one-bit odd parity, and a stop bit to the keyboard synchronized with the KCLK signal sent from the keyboard.

Figure 2-39 shows a block diagram of this circuit, and Figure 2-40 shows the timing chart in data transmission.

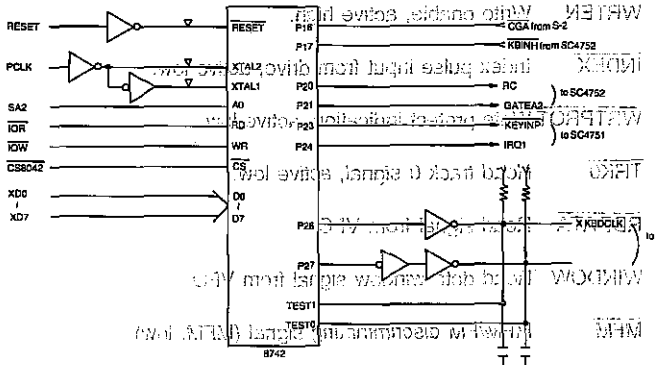


Figure 2-32. Block diagram of keyboard interface

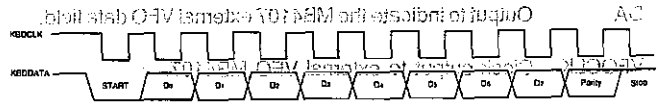


Figure 2-33. Timing chart of data transmission

2-2-17. Display circuit

General

The display circuit consists of three LSI, CG-ROM, V-RAM, and some TTLs.

It has three interfaces – CRT (720×350) and LCD (640×200) – and supports five display modes as below.

MTM: Monochrome Text Mode
CGM: Color Graphic Text Mode

	Display Mode	Display capacity & dots
1	MTM(text)	80×25 characters
2	CGM(text)	80×25 characters
3	CGM(text)	40×25 characters
4	CGM(graphic)	640×200 dets
5	CGM(graphic)	350×200 dets

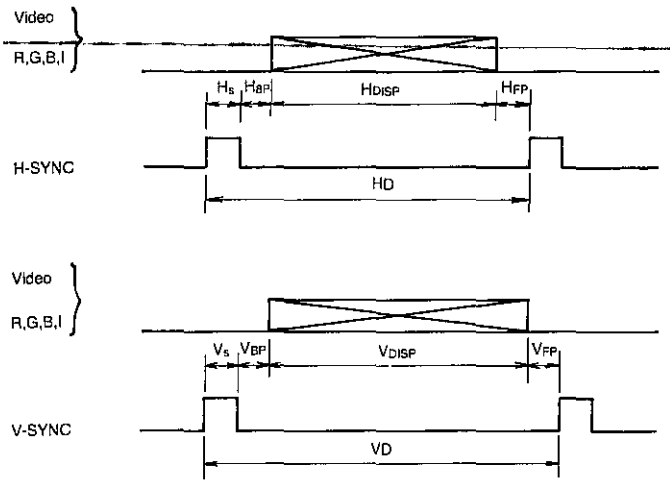
Specifications

1. CGM (CRT, LCD), MTM (LCD)

* Displays 80×25 or 40×25 characters on one screen
* 8×8 pixels for one character box
* 7×7 pixels for one character
* With character attribute
* Can display 256 different characters
* Video signal: 14.31818MHz maximum
* V-sync signal: 60Hz
* H-sync signal: 15.75kHz

2. MTM (CRT)

* Displays 80×25 characters in one screen
* 9×14 pixels for one character box
* 7×9 pixels for one character
* Can drive an 18kHz-monochrome display monitor
* Video signal: 16.257MHz maximum
* V-sync signal: 720* 350 (H X V), 50Hz
* H-sync signal: 18.432kHz



	HD	HS	HBP	HDISP	HFP	VD	VS	VBP	VDISP	VFP
CGM	64	4	8	45	7	16.5	2	2	11	1.5
(80×25 TEXT)	μs	μs	μs	μs	μs	ms	ms	ms	ms	ms
MTM	54	9	0	45	0	20	1	0	19	0
	μs	μs	μs	μs	μs	ms	ms	ms	ms	ms

*The signal polarity is positive ··· CGM
negative ··· MTM

VIDEO OUTPUT WAVEFORMS

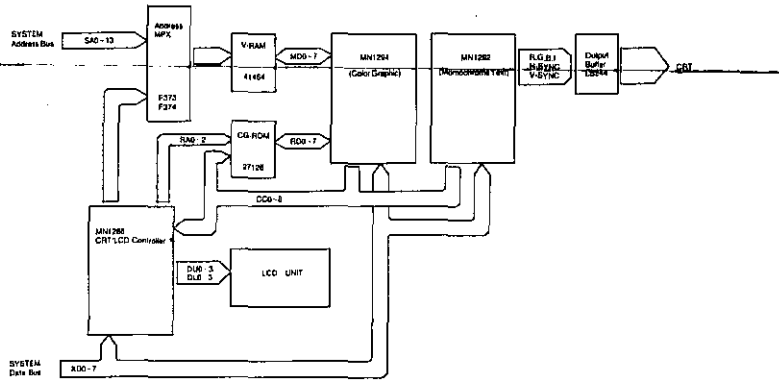


Figure 2-34. Block diagram of display circuit

2-2-17-1. Internal Registers of the MN1288 (Table 2-21)

There are nineteen registers in the MN1288. They are used to define parameters for the CRT monitor. The Index register which is one of those registers, is used for a pointer to the other 18 registers. It is assigned by the CPU at the I/O address 3B4H for the monochrome board or 3D4H for the color board.

The Index register must be first loaded with the necessary register number, and then the Data register is loaded with the information to be placed in the selected register.

The Data register is assigned by the CPU at the I/O address 3B5H for the monchrome board or 3D5H for the color board.

The following table shows the value that must be loaded into the MN1288 internal registers, and Figure 2-35 shows the each value on the CRT monitor.

Table 2-21. Register definition

Reg. #	Description	Read/ Write	MONO.	Color 40×25	board 80×25	GRPH	Item	Unit
R0	HORIZONTAL TOTAL	W	61	38	71	38	Nht	Characters
R1	HORIZONTAL DISPLAYED	W	50	28	50	28	Nht	Characters
R2	HORIZONTAL SYNC POSITION	W	52	2D	5A	2D	Nhsp	Characters
R3	HORIZONTAL SYNC WIDTH	W	0F	0A	0A	0A	Nhsw	Characters
R4	VERTICAL TOTAL	W	19	1F	1F	7F	Nvt	Characters Row
R5	VERTICAL TOTAL ADJUST	W	06	06	06	06	Nadj	Scan Line
R6	VERTICAL DISPLAYED	W	19	19	19	64	Nvd	Characters Row
R7	VERTICAL SYNC POSITION	W	19	1C	1C	70	Nvsp	Characters Row
R8	INTERLACE MODE	W	02	02	02	02		–
R9	MAX. SCAN LINE ADDRESS	W	0D	07	07	01	Nr	Scan Line
R10	CURSOR START	W	0B	06	06	06	Nr	Scan Line
R11	CURSOR END	W	0C	07	07	07	Nr	Scan Line
R12	START ADDRESS (H)	W	–	00	00	00		–
R13	START ADDRESS (L)	W	–	00	00	00		–
R14	CURSOR ADDRESS (H)	R/W	XX	XX	XX	XX		–
R15	CURSOR ADDRESS (L)	R/W	XX	XX	XX	XX		–
R16	LIGHT PEN ADDR. (H)	R	–	XX	XX	XX		–
R17	LIGHT PEN ADDR. (L)	R	–	XX	XX	XX		–

-: Not used the function.

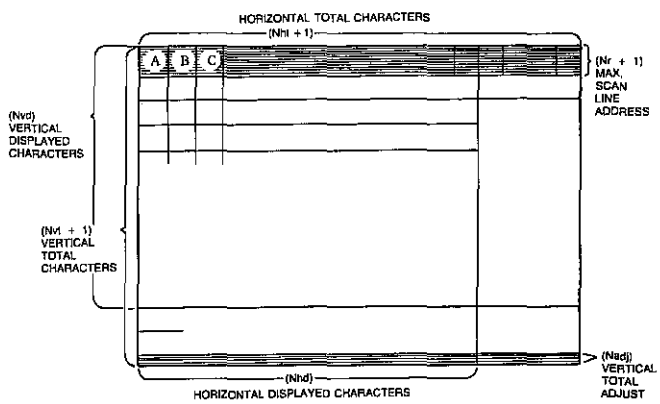


Figure 2-35. Register description

2-2-17-2. I/O Map of MTM

The table below shows the I/O address assignments of the MTM.

Table 2-22. I/O map of MTM

I/O Addr.	Description
3B4	68B45 Index register
3B5	68B45 Data register
3B8	CRT Control register
3BA	CRT Stantus register

*** CRT Control Register**

This write only register is used to control the MTM.

Table 2-23. CRT control register

I/O Addr.	Bit	CRT control register
3B8	0	—
	1	—
	2	—
	3	Video enable
	4	—
	5	Blink enable
	6	—
	7	—

***CRT Status Register**

This read only register is used to check the MTM. That is, whether the H-sync or B/W video signal is output or not can be judged via this register

Table 2-24. CRT status register

I/O Addr.	Bit	Description
3BA	0	H-sync
	1	—
	2	—
	3	B/W video

2-2-17-3. I/O Map of CGM

The table below shows the I/O address assignments of the CGM.

Table 2-25. I/O map of CGM

I/O Addr.	Description
3D4	68B45 Index register
3D5	68B45 Data register
3D8	Mode Select Register
3D9	Color Select Register
3DA	Status Register

***Mode Select Register**

This 6-bit write only register is used to determine the display mode and brinking attribute of the CGM.

Table 2-26. Mode select register

I/O Addr.	Bit	Description
3D8	0	H: 80×25 Text Mode, L: 40×25 Text Mode
	1	H: Graphics Mode, L: Text Mode
	2	H: Black/White Mode, L: color Mode
	3	H: Enable VIDEO Signal, L: Disable VIDEO Signal
	4	H: 640×200 Black/White Graphics Mode
	5	H: Change background intensity to blinking attribute

Table 2-27 shows bit assignments of each display.

Table 2-27. Bit assignments

Mode	Bit 5	4	3	2	1	0
80×25 (MONO.)	1	0	1	0	0	1
(COLOR)	1	0	1	0	0	1
40×25 (MONO.)	1	0	1	1	0	0
(COLOR)	1	0	1	0	0	0
320×200 (MONO.)	X	0	1	1	1	0
(COLOR)	X	0	1	0	1	0
640×200	X	1	1	1	1	0

X: Don't care

*** Color Select Register**

This 6-bit write only register is used to determine the selection of screen colors for the CGM.

Table 2-28. Color select register

I/O Addr.	Bit	Description
3D9	0	Blue
	1	Green — These bits select the border color in
	2	Red — text mode, background color in 320×200
	3	Intensity — mode or foreground color in 640×200 mode.
	4	Select background color in text mode or intensified set of colors in graphics mode.
	5	Select color set 0 or 1 in 320×200 mode When this bit is set to 1, the color set 1 is selected. When this bit is set to 0, the color set 0 is selected.

Table 2-29. Color combinations

COLOR	I	R	G	B
BLACK	0	0	0	0
BLUE	0	0	0	1
GREEN	0	0	1	0
CYAN	0	0	1	1
RED	0	1	0	0
MAGENTA	0	1	0	1
BROWN	0	1	1	0
WHITE	0	1	1	1
GRAY	1	0	0	0
LIGHT BLUE	1	0	0	1
LIGHT GREEN	1	0	1	0
LIGHT CYAN	1	0	1	1
LIGHT RED	1	1	0	0
LIGHT MAGENTA	1	1	0	1
YELLOW	1	1	1	0
WHITE (HI-INTENSITY)	1	1	1	1

Table 2-30. Color setstable

C0	C1	COLOR SET 0 R	G	B	COLOR SET 1 R	G	B
0	0	Background color specified by Color Select Register					
0	1	0	1	0	0	1	1
1	0	1	0	0	1	0	1
1	1	1	1	0	1	1	1

*** CRT Status Register**

This 4-bit read only register is used to check the CGM board. That is, whether the V-sync or Display Enable signal is output or not is judged via this register.

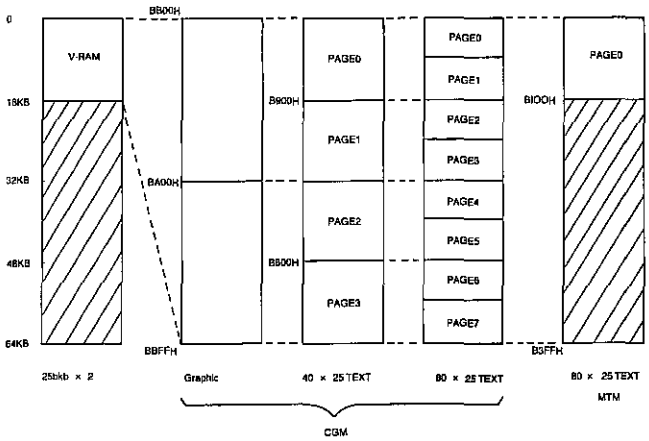
Table 2-31. CRT status register

I/O Addr.	Bit	Description
3DA	0	Display Enable
	1	–
	2	–
	3	V-Sync.

2-2-17-4. V-RAM Map

The Display circuit has two 256KB (64Kbit × 4) D-RAMs as the V-RAM, but it uses only 16Kbytes for the display buffer. The same memory area is used for both MTM and CGM, but its addresses assigned for each mode are fifferent.

Fig.2-36 shows the display buffer memory allocation for each mode. The area marked with shading are not used.



***TEXT MODE**

80×25 TEXT (MTM)
80×25 TEXT (CGM)
40×25 TEXT (CGM)

Figure 2-36. Display buffer memory allocation

Every character to be displayed has one byte of character code and also one byte of attribute code.
An attribute byte can be divided into four functions: blink, intensity, foreground and background. Their assignments are shown as below.

Table 2-32. Attribute assignments

Background			Foreground			Display mode
R	G	B	R	G	B	
0	0	0	0	0	0	Non display
0	0	0	0	0	1	With underline
0	0	0	1	1	1	Normal display
1	1	1	0	0	0	Reverse display

Blink	Display mode	Intensity	Display mode
0	Non blink	0	Normal intensity
1	Blink	1	High intensity

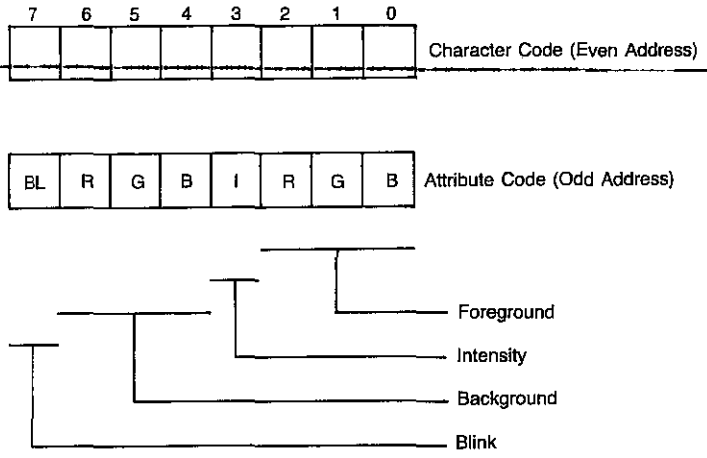


Figure 2-37. Attribute assignments

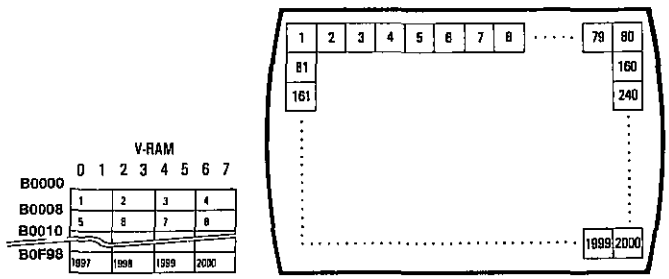


Figure 2-38. V-RAM map in 80 × 25 text mode (MTM)

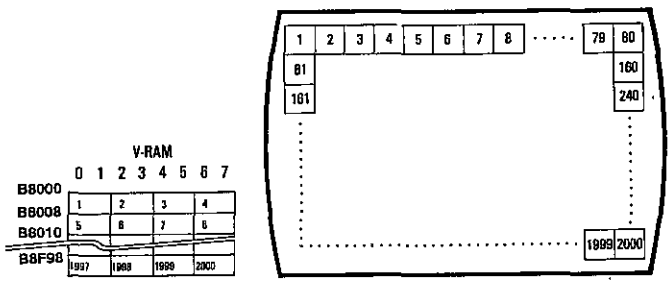


Figure 2-39. V-RAM map in 80 × 25 text mode (CGM)

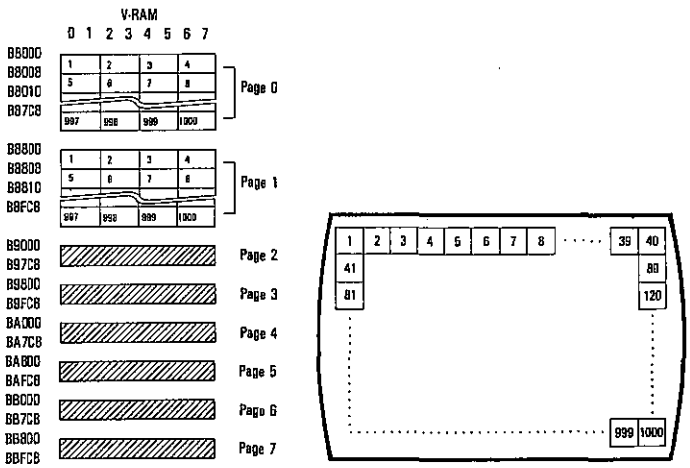


Figure 2-40. V-RAM map in 40 × 25 text mode (CGM)

*** 320×200 Graphics Mode (CGM)**

In this mode, 4 of 16 colors can be displayed.

The C0 and C1 signals select four colors from the color set 0 or 1 corresponding to the bit 5 of the color select register. The color set 1 includes the blue color signal, however the color set 0 does not include the blue color signal.

Functional assignments for every byte are shown below.

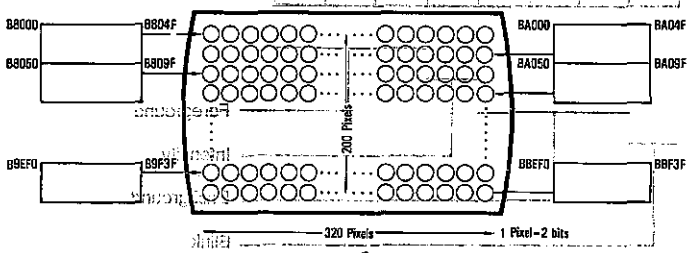


Figure 2-41. V-RAM map in 300 × 200 graphics mode

Table 2-32. Bit assignments

7	6	5	4	3	2	1	0
C1	C0	C1	C0	C1	C0	C1	C0
First display element		Second display element		Third display element		Fourth display element	

*** 640×200 Graphics Mode (CGM)**

In this high resolution mode, every bit of the V-RAM corresponds to every pixel on the screen.

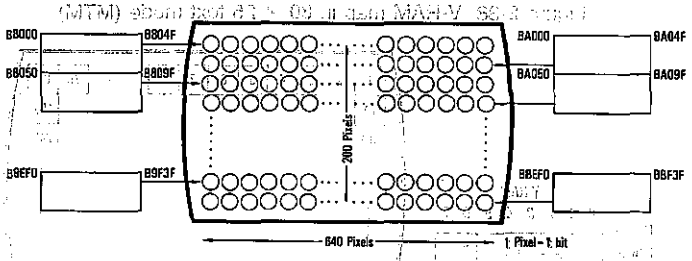


Figure 2-42. V-RAM map in 640 × 200 graphics mode

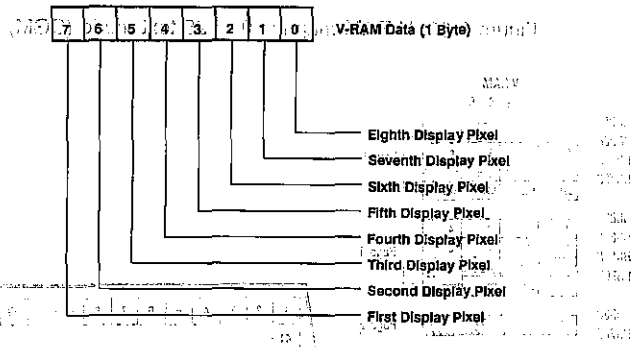


Figure 2-43. Bit assignments

2-2-17-5. CG-ROM Map

The CG-ROM has 16K bytes of memory capacity, the lower 4K bytes (0H~0FFFH) and used for the LCD (MTM & CGM).

This 4K bytes storage area is further divided into half; 256 character font patterns having the single-dot construction are stored in the first 2K bytes, and also 256 character font patterns having the double-dot construction are stored in the remaining area of the CGROM.

The 2K bytes (2800H~2FFFH) are used for CGM. The upper 4K bytes (3000H~3FFFH) are used for MTM.

This 4K-byte storage area is further divided into half; the lower half of 4K-byte stores the upper area of the 8×14 character box, and also the upper half of 4K-byte stores the remaining area of the character box.

Though the CGROM has character font patterns, it is not used in the graphics display mode (CGM). When displaying characters in the graphics mode, the font data stored in the BIOS ROM is used.

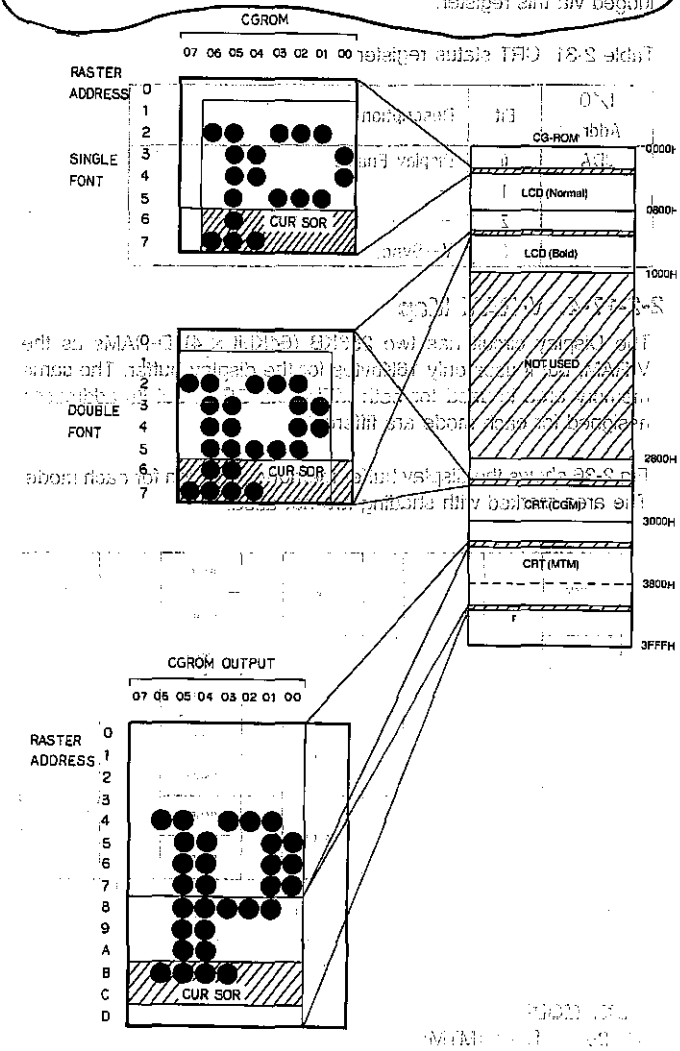


Figure 2-44. CG-ROM map

2-3. KEYBOARD UNIT

Introduction

The keyboard is separated from the main unit and is attached by a modular plug connector on the right side of the main unit. The keyboard cable can be disconnected from both the keyboard and the main unit. The curled, shielded keyboard cable is approximately 0.9" long (260mm).
The interface lines between the keyboard and the system unit consist of a power supply (+5V DC), GND, and two bidirectional signal lines.
The keyboard contains its own microprocessor to implement all functions normally required of a keyboard.

Key Controller

The keyboard employs an 80C49 (8-bit one-chip microprocessor) and a 2464 (64K-byte one time PROM).
The 80C49 has 238-byte RAM which is used as the key buffer.
The 2464 contais the control program including self-diagnostics.
The keyboard is connected to the keyboard interface on the main PCB with the two signal lines, KBDDATA and KBDCLK. Using these lines, a bi-directional data transfer is performed.
With various commands from the keyboard interface, the keyboard mainly performs the following operations:

* Resets the keyboard itself.
* Re-outputs the key scan codes.
* Varies the detection period for the key auto-repeat function.
* Turns the LEDs on the keyboard on or off.

Conversely, the keyboard performs the following for the system unit:

* Requests that a command be reset.
* Tells the result of the self-diagnostic at power on or at reset.
* Denoted that the 16-byte keyboard buffer is full.

Signals P10 through P13 in the figure are used as key scan signals, and DB0 through DB7 are used as key return signals. The interface between the main PCB and the keyboard is performed by P27, P26, T0 and INT terminals.I P27 transmits a key clock signal; P26 also transmits key data. The keyboard CPU checks the T0 and INT terminals to judge whether the keyboard interface on the main PCB is ready to receive data.
When the keyboard CPU is ready to send key data, it first checks these line. If the KBDCLD line is LOW, the key data is stored in the RAM of the keyboard CPU. If the KBDCLK line is HIGH and KBDDATA line is LOW, the key data is stored in the RAM of the keyboard CPU and the keyboard CPU receives data from the 8042.
The keyboard CPU sends the key scan signals to the key matrix and judges conditions for each key by reading the key return signals. When one of the keys is pressed, the keyboard CPU emits a key code signal corresponding to that key, and sends it to the 8042 together with a key clock signal sequentially. At this time, the keyboard CPU sends a start bit, an 8-bit key code, and odd parity bit, and a stop bit.
If the parity bit sent from the keyboard CPU does not match with the one in the keyboard interface, the 8042 sends a resend command "FE" to the keyboard.(Ref. CHAPTER 1 for keylayout.)

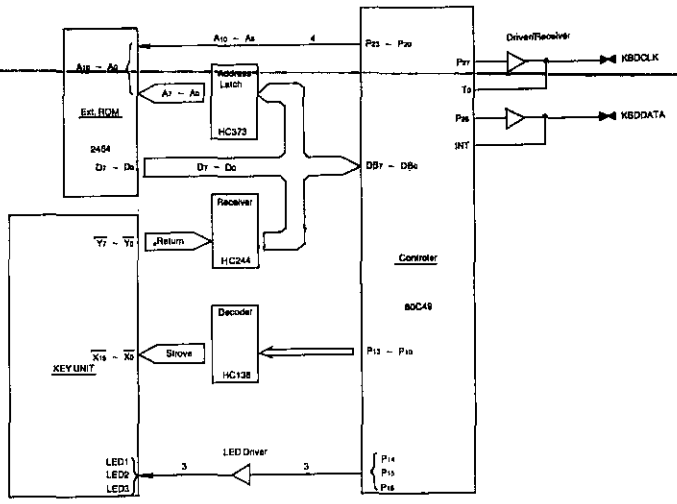
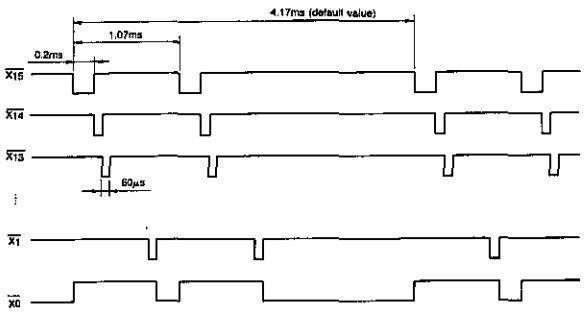


Figure 2-45. Block diagram of keyboard



TIMING CHART OF KEY STROBE

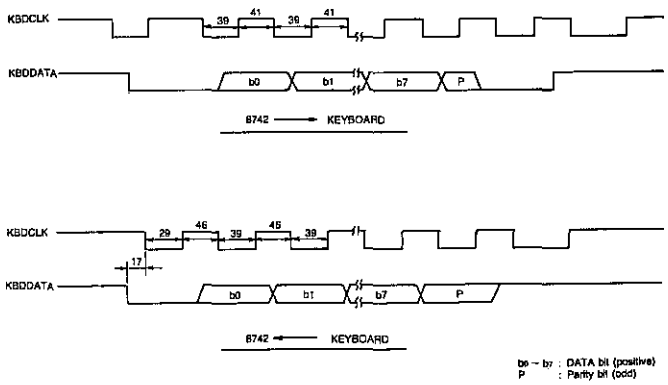


Figure 2-46. Timing chart of data transmission

2-4. POWER SUPPLY UNIT

1) General

Power source unit are energized main supply of single phase 100V-127V a.c (or 200V-240V a.c) 50/60Hz, and +5V output is stabilized by switching control. +12V output and −5V, −12V, −15V output are stabilized by 3 or 5-terminal regulator.
This power source units contains a invertor circuit, ACL signal circuit, and invertor stop output.

2) Theory of operation

2-A) EMC filter

Fig. 2-46 shows EMC (Electro Magnetic Capability) filter circuit.
L1, 2 is RFI (Radio Frequency Interference) suppression choke.
C1, 2, 5 are used for normal mode RFI suppression.
C6, 7, 8, 9 are used for common mode RFI suppression.

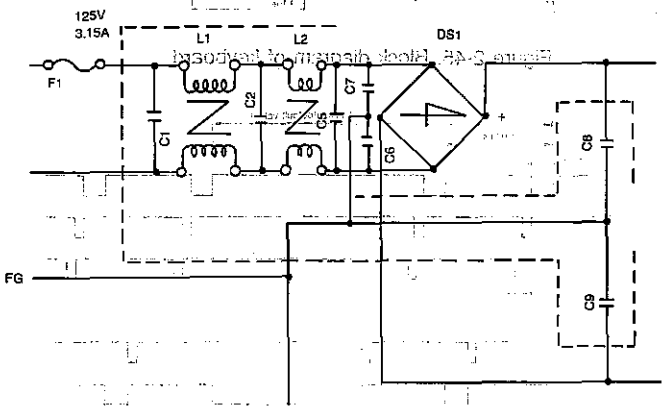


Figure 2-46

2-B) Input detector circuit

Fig. 2-47 (or 2-48) shows input detector circuit.
Main supply that supply through EMC (Electro Magnetic Capability) filter is rectified in bridge DS1 and filtered in C10A, B.
Main supply is changed into DC input.
TH1 A-B power thermistor is used inrush current suppression.

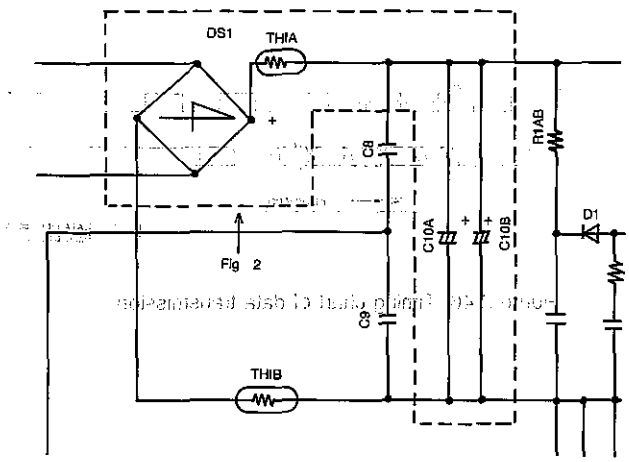


Figure 2-47 (For 100V series)

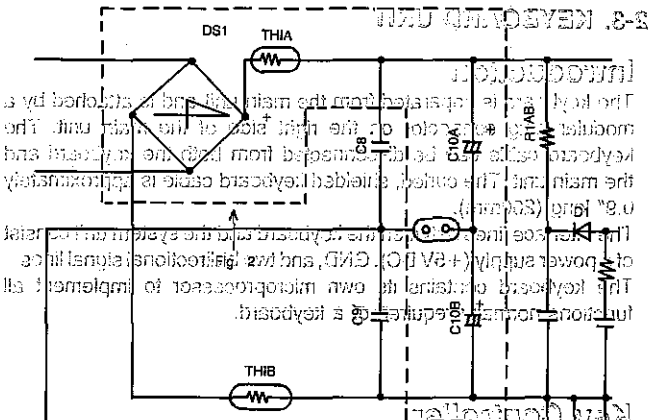


Figure 2-48 (For 200V series)

2-C) Main switching circuit

Fig. 2-49 shows main switching circuit.
The circuit that constructed by C11, C12, R1AB, R2AB, D1 are used to protect TR1 from high volts surge.
TR1 is main switching transistor and produce high frequency square wave.
The circuit that constructed by R7, R6, R32, C15, C41, D2AB are used to drive base of TR1.
Following explanation is theory that TR1 begin to excite.

Turn on input → Exciting current flow to base of TR1 through (1-4) by TR1 → Base current that TR1 needs to operate is applied from (6-7) → The currrent excite TR1 → High frequency square wave apply to T1

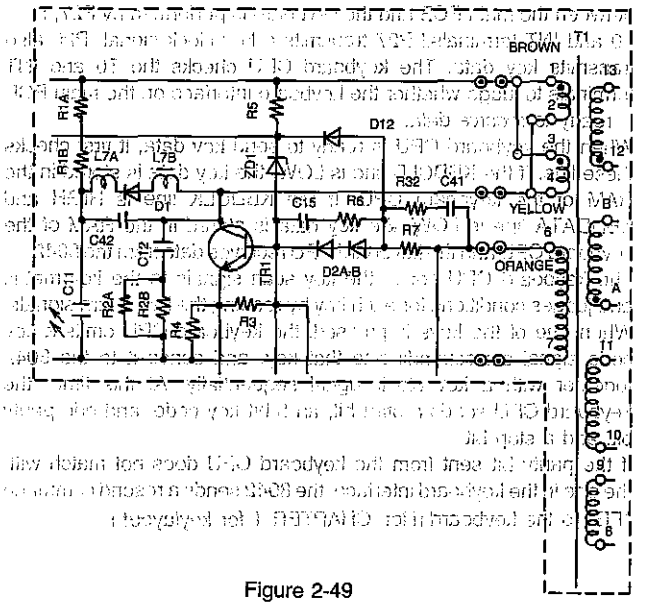


Figure 2-49

2-D)Controll circuit

Fig. 2-50 shows control circuit.
+5V output is stabilized by optical isolator PC1, error amplifier IC2 and transistor TR2.
IC2 detects proportional voltage signal to +5V output.
The signal is amplified by IC2.
The amplified signal is supplied to TR2 through the optical isolator PC 1.
TR2 control pulse width of TR1 and oscillation frequency.

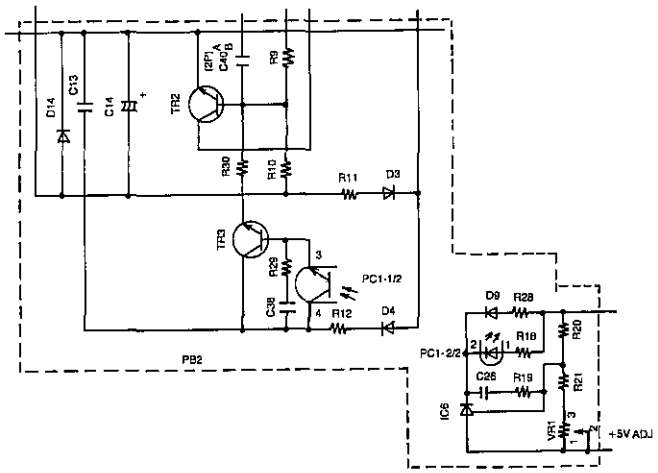


Figure 2-50

2-E) +12V output

Fig. 2-51 shows +12V output circuit.
High frequency output (winding 12,13 of T1) is rectified in bridge DS2 and filtered in C16AB, and to develop the 12 volts output through the 5-terminal regulator IC7.

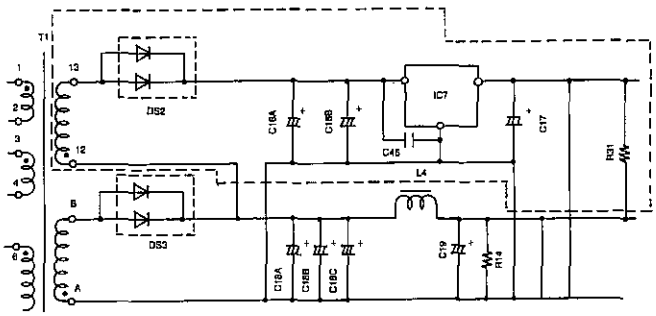


Figure 2-51

2-F) +5V output

Fig. 2-52 shows +5V output circuit.
High frequency output (winding A-B of T1) is rectified in bridge DSW3 and filtered in C18A,B,C and L4 to develop the 5 volts output.

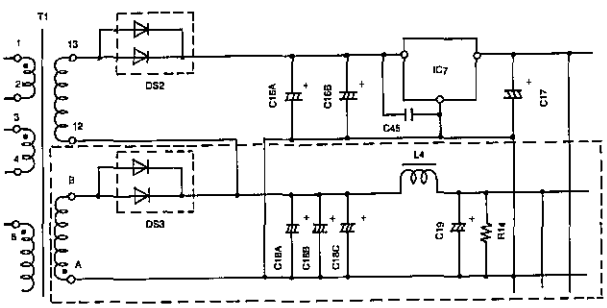


Figure 2-52

2-G)

(a)−5V output

Fig. 2-53-(a) shows −5V output circuit. High frequency output (winding 11-10, of T1) is rectified in diode D5 and filtered in C20, to develop the −5V output through the 3-terminal regulator IC1.

(b) −12V, −15V output

Fig. 2-53-(b) shows −12V, −15V output circuit. High frequency outuput (winding 9-8, of T1) is rectified in diode D6 and filtered in C22, to develop the −12V output through the 3-terminal regulator IC2 and −15V output through the 3-terminal regulator IC2.

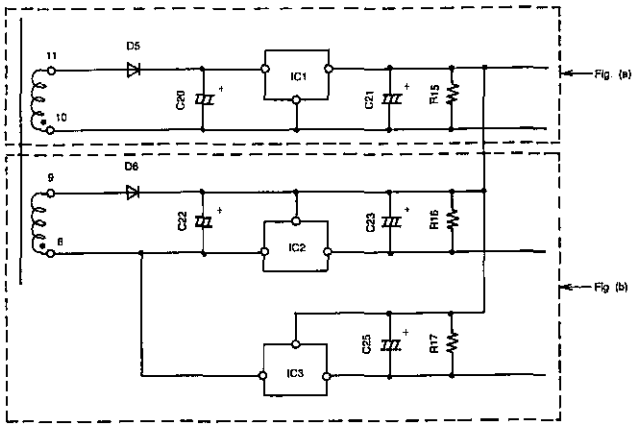


Figure 2-53

2-H) ACL signal circuit

Fig. 2-54 shows $\overline{ACL}$ circuit.
The $\overline{ACL}$ signal is provided with IC4.

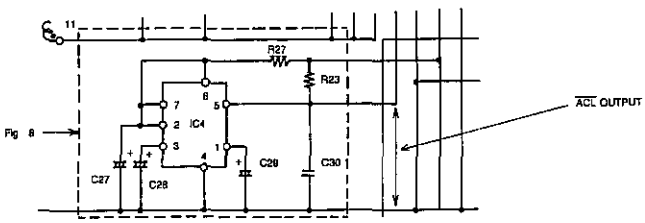


Figure 2-54

The following is operation of IC4.

a)Functional diagram

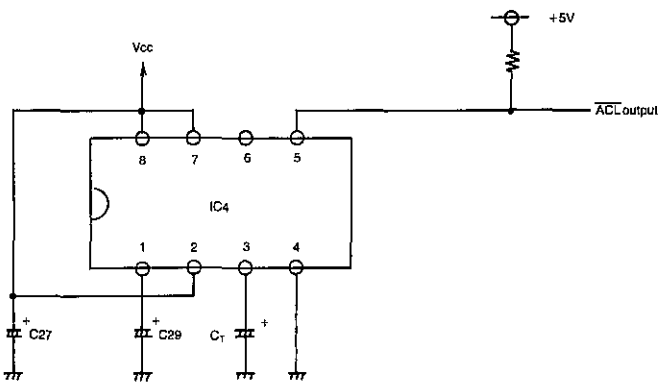


Figure 2-55

C27, C29; Noise & ripple suppression capacitor.
C_T; Capacitor for timing

b)Timing diagram

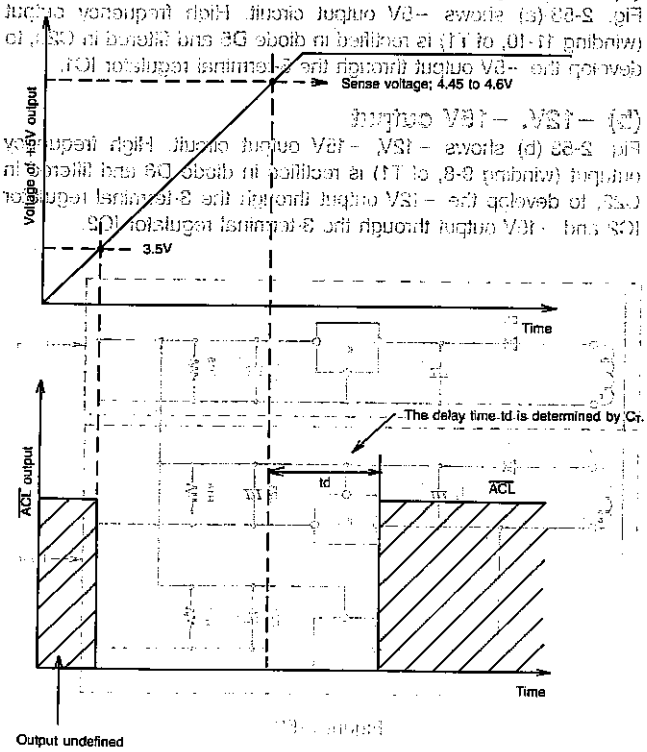


Figure 2-56

2-I) Invertor circuit

Fig. 2-57 shows invertor circuit.
The circuit is self oscillation type switching power supply and energized +12V output through 3-terminal adjustable regulator IC5.
Adjustment of invertor output voltage is performed by a change of IC5 output voltage.
Adjustment of IC5 output voltage can be performed that charge value of external resistor between INV.V ADJ output and GND.
Invertor circuit contains invertor output voltage cut off terminal CN7.

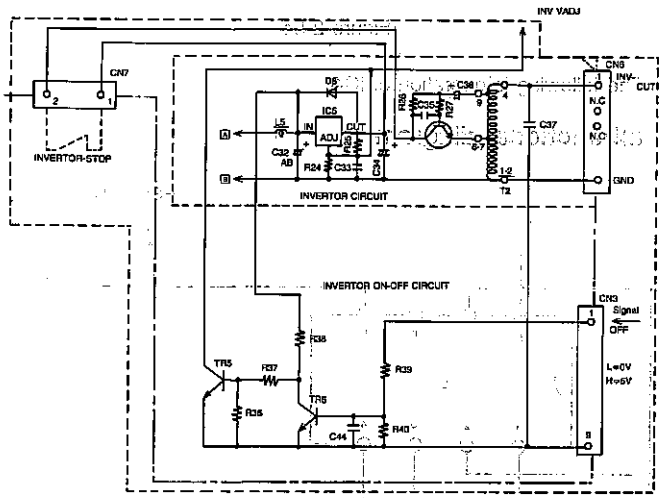


Figure 2-57

2-J) Invertor ON-OFF circuit

Fig. 2-58 shows invertor ON-OFF circuit.
The invertor circuit is controlled by signal of CN3.

CN3. signal→ Low → Invertor circuit stop.
High → Invertor circuit operates.

But this operation is available under CN7-1-2 open condition.

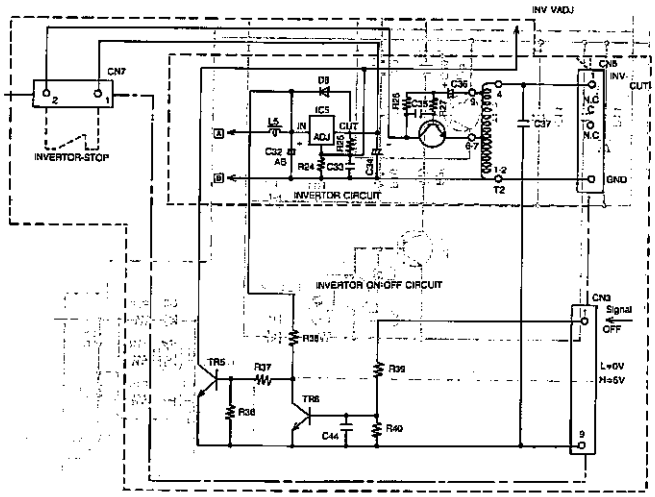


Figure 2-58

2-K) Over voltage protection circuit.

Fig. 2-59 and Fig. 2-59-(a) shows over voltage protection circuit.
When +5V output goes to more than +6 volts.
The circuit become to operate, then switching socillation circuit is stopped.

2-L) Thermal protection circuit

Fig. 2-59 and Fig. 2-59-(b) shows thermal protection circuit.
Abnormal internal temperature rise is detected by this circuit during the power supply operating, and then switching oscillation circuit is stopped by this circuit.

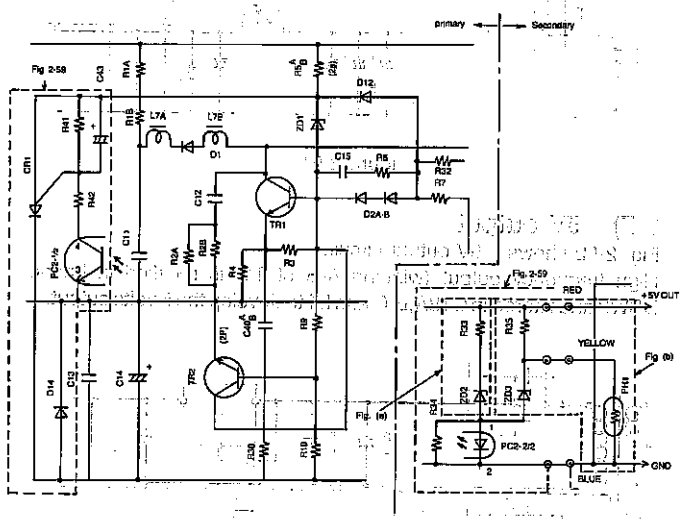


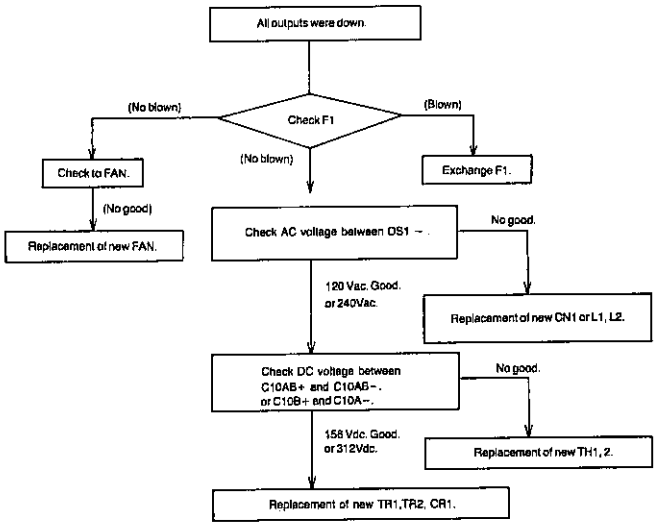
Figure 2-59

3) Troubleshooting guides

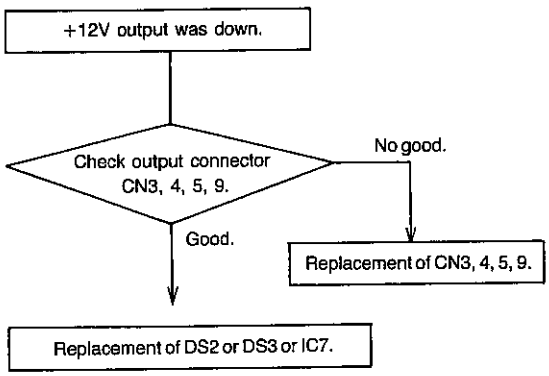
Repair should be performed in according to following Troubleshooting flow chart.

3-B) Troubleshooting flow chart

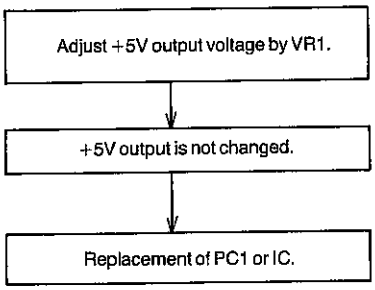
a)When all outputs were down.



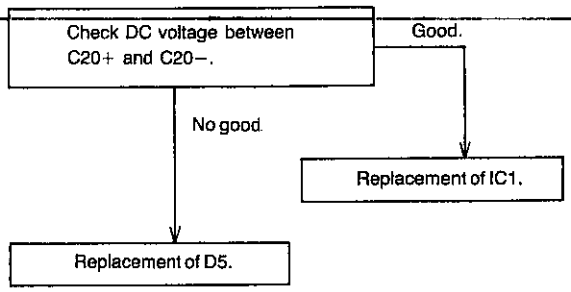
b) When +12V output was down.



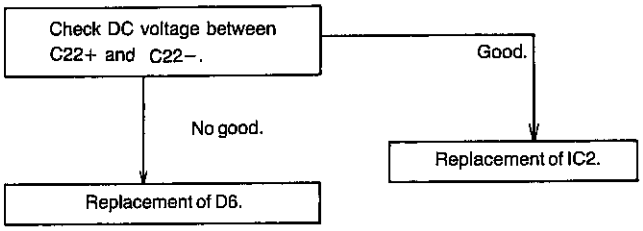
c) When +5V output was gone low voltage or high voltage.



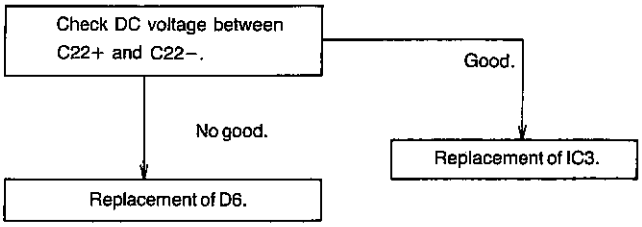
d) When −5V output was down.



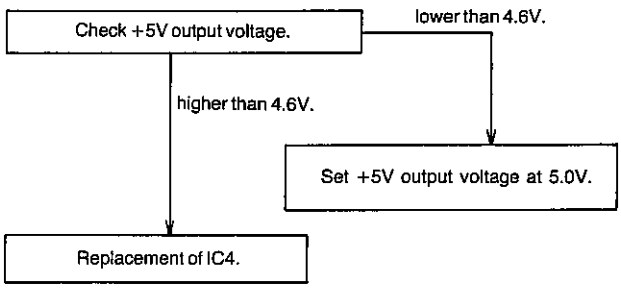
e) When −12V output was down.



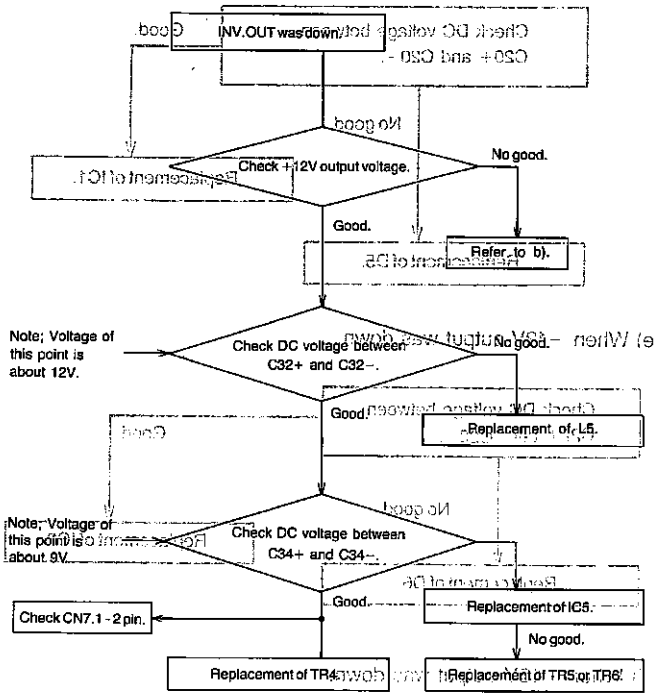
f) When −15V output was down.



g) When $\overline{ACL}$ output was down.



h) When INV.OUT was down.



4) Specification sheets

4-A) Specification of line

a) Line voltage; 100 - 120Vac or 220Vac.

b) Applicable to wide range of line voltage from 87 Vac to 132 Vac or 174 Vac to 271 Vac.

c) Applicable to wide range of line frequency from 48 Hz to 62 Hz.

4-B) Specification of output

Refer to Table-1.

OUTPUT		+5V OUTPUT	+12V OUTPUT	-5V OUTPUT	-15V OUTPUT	-12V OUTPUT
OUTPUT CURRENT	MAX PULSE CURRENT (A)	6.8	2.6			
	STATIC MAX CURRENT (A)	6.0	1.8	0.05	0.2	
	MIN CURRENT (A)	1.5	0.015	0	0.015	0.015
STABILITY (%)		±4%	0.015~0.1A±10% 0.1 ~1.8A±6% 1.8 ~2.6A±10%	±8%	±10%	±10%

Table 2-33

4-C) Specification of output timing

a) Output timing chart.

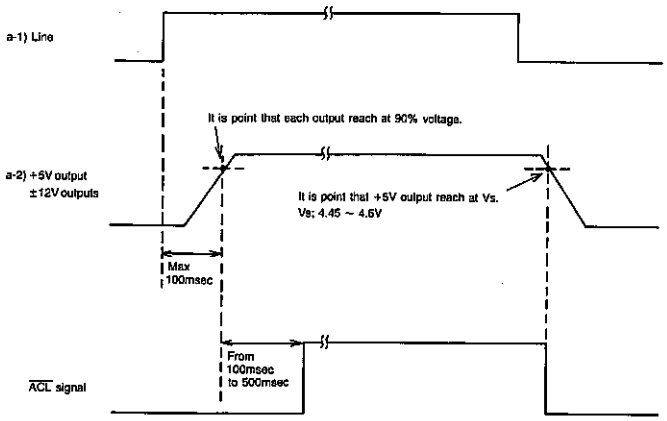


Figure 2-60

b) Ability of ACL

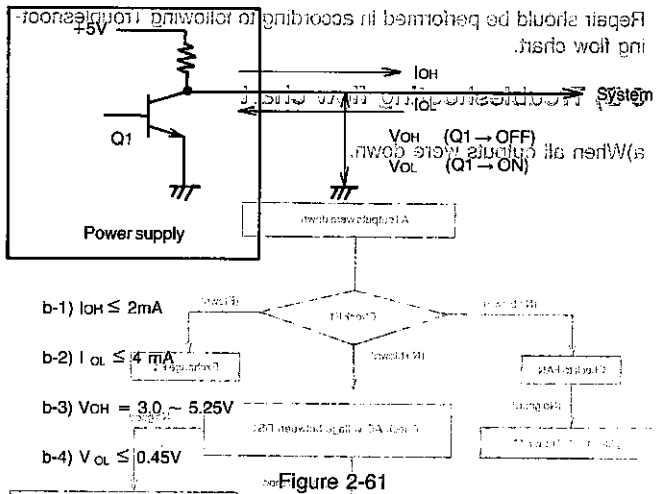


Figure 2-61

5) Theory of connection between PWB1 and PWB2

PWB2 is secured by the 6 screws as shown Fig 12 on PWB1.
It is possible to disassemble by the 6 screws.

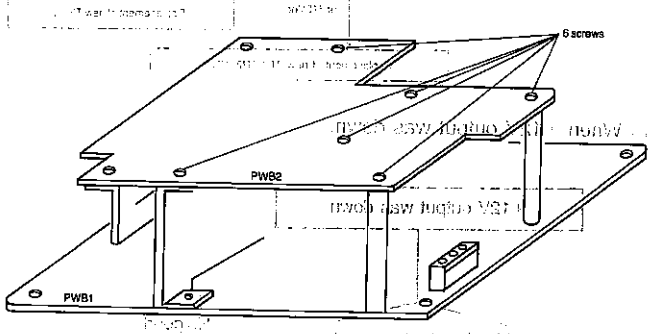


Figure 2-62

2-5. LIQUID CRYSTAL DISPLAY UNIT

2-5-1. Introduction

The LCD unit is the system's master display. It is an ultra-precision unit comprising an LCD panel and control board connected with a film carrier type LSI. Field servicing of this unit is not possible. If it is malfunctioning, the faulty unit component requires replacement. The following provides information required for unit replacement and some operating principles;

2-2-2. Configuration

The LCD unit can be broken down as illustrated in Figure 6.1.

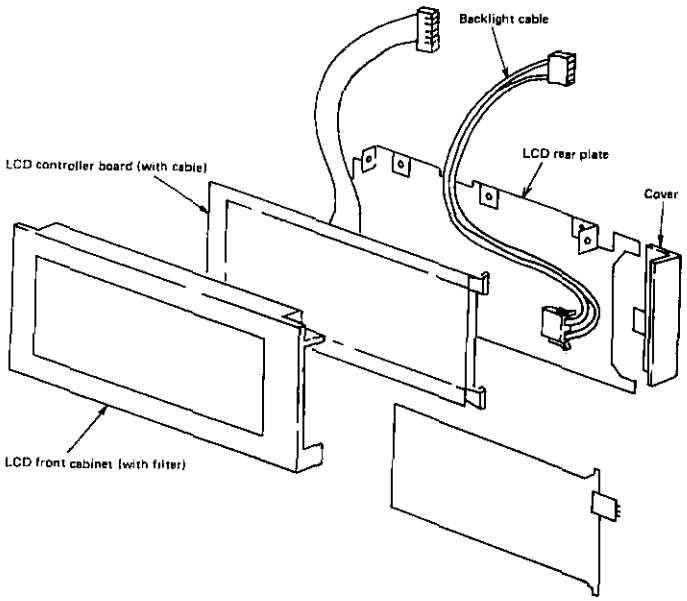


Figure 2-63. Exploded view of LCD unit

2-5-3. Circuit Configuration

The LCD unit can be broken down as illustrated in Figure 2-63.

2-5-4. Screen Configuration

In order to achieve a high contrast with lower duty cycle, the LCD screen is divided into two sections (upper and lower) of 640×100 dots each. Each section is driven at a duty cycle of 1/100.

2-5-5. Input Data and Control Signals

The LCD driver is an 80-pin LSI chip containing shift registers, latches, and LCD drivers.

Input data for each screen section is received line-by-line (640 dots) to the LCD unit. The data is converted by shift registers into parallel 4-bit data, and sequentially transferred to the LCD drivers along with the clock signal CP2, beginning from the top left corner of the screen. When one line (640 dots) of data is transferred, it is latched as parallel data for 640 signal lines at the negative edge of the latch signal, CP1.

The LCD driver drives the 640 signal lines according to the latched data.

The Scan Start signal (S) is pretransferred from the scan signal driver to the first line of the scan electrodes.

The scan electrodes and signal electrodes form a matrix to display the contents of the display data on the first row of each screen section.

While the data is diplayed on the first row., the LCD unit receives the data for the second row. When the 640 dots of data are transferred and latched at the rnegative edge of the CP1, driving is switched from the first row to the sencond row. The sequence is repeated for all the subsequent rows

When data is displayed on the 100th row of each screen section, sacnning returns to the first row again to repeat the same sequence.

The Scan Start signal (S) drives the row of electrodes.

To suppress flickering the LCDs is driven at a frame frequency of 70 to 80 Hz.

If DC voltage is applied to the LCD panel, chemical reaction will cause the liquid crystal in the panel to deteriorate. To prevent this, the driving signal polarity is inverted by a Driving Signal AC Coupling signal (M).

Due to the nature of the CMOS driver, the power consumption of the LCD unit increases with the CP2 clock frequency.

To reduce the CP2 clock rate, the driver LSI contains four shift registers to convert data into 4 bit prallel data.

The shift registers contribute to the reduction of power consumption by the unit.

Four bits of display data are input to the data input pins DU0-DU3A (for uper screen section) and DL0-DL3 (for lower screen section).

To further reduce power consumption, the LCD unit has a data input bus. The bus allows the data inputs of the drivers to function only when appropriate data is applied to them.

The following describes the data input to the signal electrodes for the upper and lower screen sections and driver LSI chip select sequence.

The driver LD1 on the extreme left of the screen is first selected. When 80 bits of data (20 CP2) are input to that driver, the second driver LSI next to the first driver is selected. This sequence is continued until the driver at the extreme right of the screen is selected. Chip select occurs simultaneously for the signal electrode driver LSIs for the upper and lower screen sections.

The data for the upper and lower screen sections is thus transferred through the 4-bit bus starting with the leftmost column of the screen.

The LCD unit contains no refreshing RAM, and requires constant application of display data and timing signals to its inputs, even for still images.

The input signal timing is shown in figure 2-64.

Table 2-34. Interface timing specifications

Item	Symbol	Soecificcations			Unit
		MIN	TYP	MAX	
Frame period	TFRM	12.5		14.3	ns
Clock period	TCP2	710			ns
High level clock pluse width	tCWH	335			ns
Low level clock pluse width	tCWL	335			ns
High level latch clock pluse width	tLWH	450			ns
Data setup time	tSU	70			ns
Data hold time	tH	120			ns
CP1 clock margin time to CP2	tCL	200			ns
CP2 clock margin time to CP1	tLC	20			ns
M clock margin time to CP2	tM	−400		400	ns
CP1 setup time to CP2	ts21	200			ns
Overlap time of Low period of CP2 with High period of CO1	toV	450			ns
Clock rise and fall time	tr, tf			50	ns

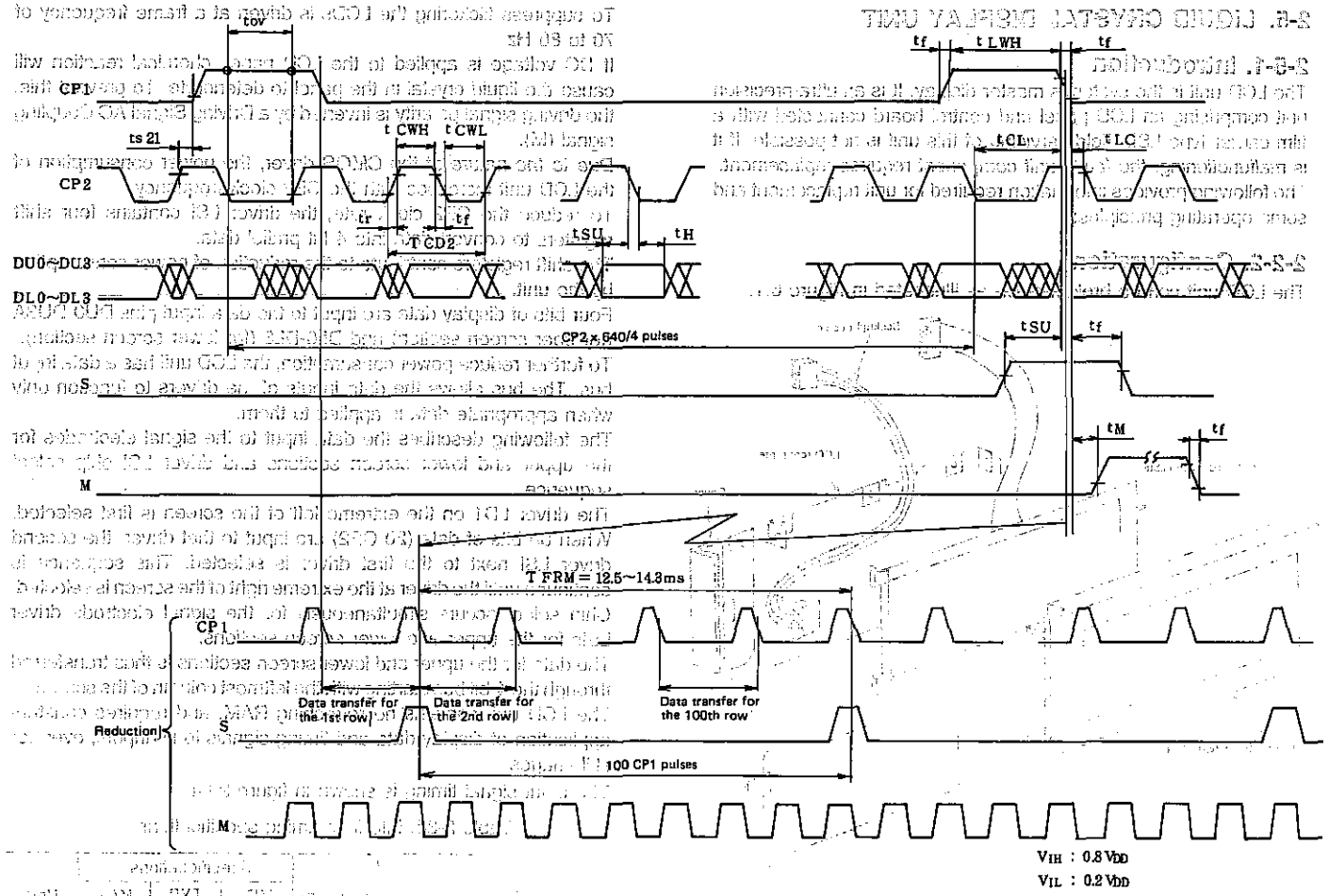


Figure 2-64. Interface timing

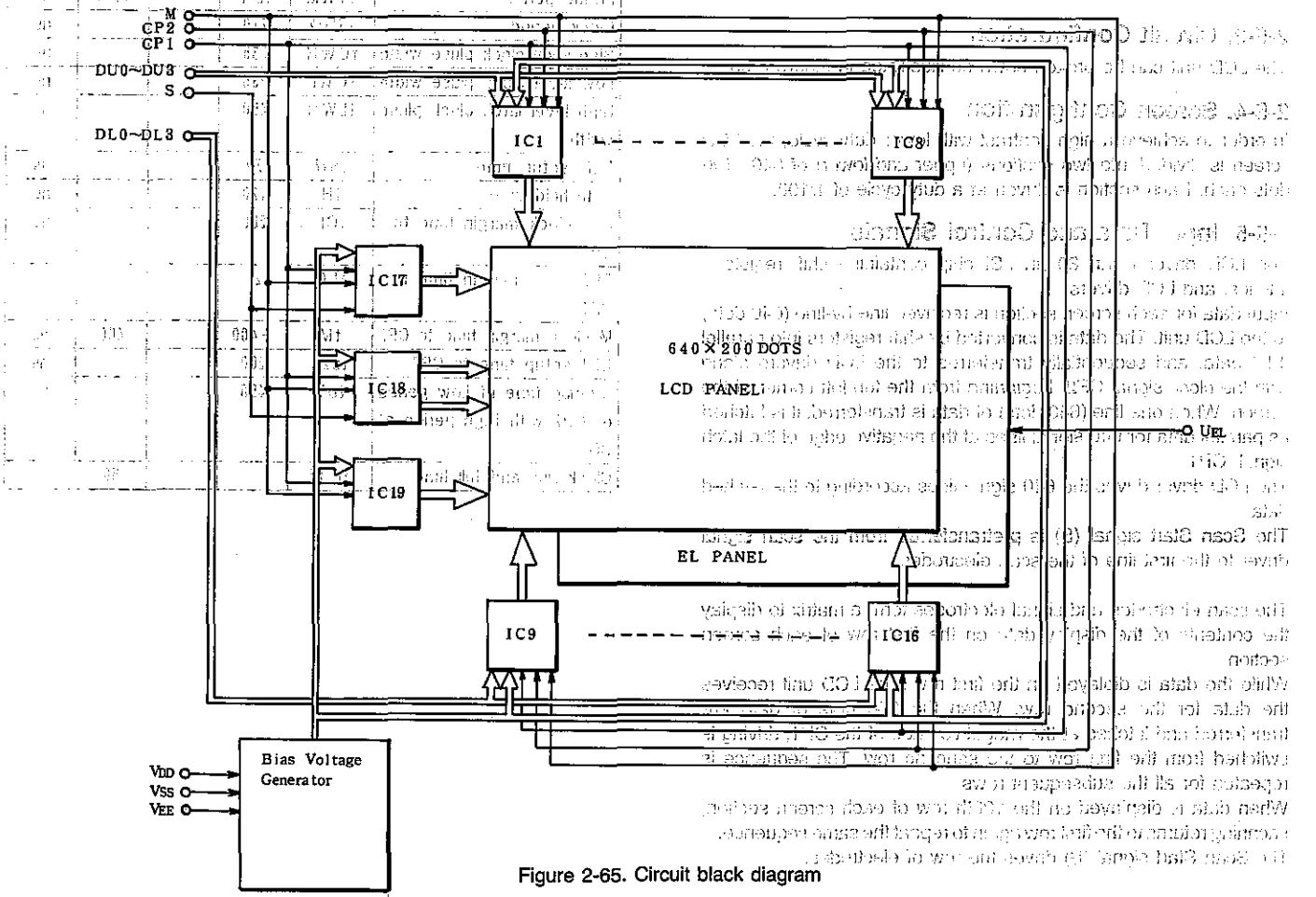


Figure 2-65. Circuit black diagram

CHAPTER 3.
FLOPPY DISK DRIVE UNIT

In this chapter is noted specification only and then other items are refered to GM3505E service manual.

3-1. Specifications

3-1-1. Performance

1) Performance list-1

(1) High density mode

Item		Single recording density	Double recording density
Recording capacity (80 cylinder)	Unformatted	833 K Bytes	1666 K Bytes
	Formatted (26 sectorstrack)	532 K Bytes	1064 K Bytes
Recording density		4935 BPI	9870 BPI
Track density		96TPI	
Cylinders		80	
Tracks		160	
Recording method		FM	MFM
Floppy disk rotating speed		360 RPM±2% (includes ripple)	
Data transfer speed		250K Bits/sec	500K Bits/sec
Average wait time		83.3ms	
Access time Average access time Track to track Setting time		95ms 3ms, min. * 15ms, max.	
Motor startup time		0.6sec, max.	

* Step pulse input may be possible to 0.8ms, as the buffered seek method is adopted (see 4-5-3).

NOTE: The above specifications apply to the high density floppy disk that assured to write and read tracks 0 through 79.

(2)Normal density mode

Item		Single recording density	Double recording density
Recording capacity (80 cylinder)	Unformatted	500K Bytes	1000K Bytes
	Formatted (16 sectorstrack)	327.68K Bytes	655.36K Bytes
Recording density		2961 BPI	5922 BPI
Track density		96TPI	
Cylinders		80	
Tracks		160	
Recording method		FM	MFM
Floppy disk rotating speed		300/360RPM±2% (See 7-4-1.)	
Data transfer speed		125/150K Bits/sec	25.0/300K Bits/sec
Average wait time		100/83.3ms	
Access time Average access time Track to track Setting time		95ms 3ms, min. * 15ms, max.	
Motor startup time		0.6sec, max.	

* Step pulse input may be possible to 0.8ms, as the buffered seek method is adopted (see 4-5-3).

2) Performance list-2

(High density mode)

Item	Limits
Head alignment	±70%, min.
Azimuth	18', max.
Index burst	200 $^{+300}_{-100}$ μs
Head amp output	1F2V, max. 2F0.15V, min. (with Hitachi Maxell MD2-256HD in use)
Modulation	20%, max. (with Hitachi Maxell MD2-256HD in use)
Resolution	60%, min. (with Hitachi Maxell MD2-256HD in use)
Time margin	300ns, min. (measured after write)
Magnetic loss	70%, min. $\frac{V2}{V1}\times 100$ V2: Output after magnetic loss V1: Output after write
Asymmetry	400ns, max.

3-1-2. Performance list-3

Item	Mechanical performance
Eject button operating pressure	1.7kg, max.

3-1-3. Operating conditions

Physical dimensions, except the bezel	146mm (W) × 28.6mm (H) × 202mm (D)		
DC power supply (*3)	+12VDC±5% (RIPPLE 200mVpp, max.) 0.13A; typical, 1.0A; max. But, ±7.5% possible when the motor is on (see 5-1 for more details). +5VDC±5% (ripple 100mVpp, max.), 0.05A; standby, 0.36A; typical, 0.8A; max.		
Power consumption	0.25W (typical during standby)*2		3.4W (typical during operation)
Environmental requirements		Operating	Non-operating
	Temperature	5 to 42℃, (10 to 51℃ for the medium)	-35 to 65℃*1 (-20 to 60℃ during storage)
	Relative humidity	20 to 80% (w/floppy disk) 20 to 85% (w/o floppy disk)	10 to 95%, without moisture condensation
	Maximum wet ball temperature	29℃	Without moisture condensation
	Temperature slope	15℃/H	
	Vibration (except resonance point)	0.25G, max.	2G, max.
	Shock	5G(10ms)	40G(10ms)
	Altitude	500m	12000m
Weight	950g, max. (except the protect sheet)		
Installing direction	Three directions (see Fig.3-2).		
Noise	40dB(A) Conditions Measured at 1 meter in frontof the floppy disk drive unit with the motor in rotationand the head being loaded with the recommendedfloppy disk inserted.		

*1: 72H, except for the floppy disk.
*2: Standby is the condition that the drive unit is not selected and the motor is not on.
*3: Spike voltage is included in the ripple.

3-1-4. Reliability

MTBF (under normal condition)	11,000POH (current carrying time)
MTTR	30 minutes
Expected life	5 years
Error rate	
Soft error	Once per 10^8 bits (up to two retrials)
Hard error	Once per 10^{12} bits
Seek error	Once per 10^5 seeks
Floppy disk life	(With Hitachi Maxell MD2-256HD in use)
Passes on one track	3.5×10^6 passes
Loads	30,000 times (including motor stop)
Seeks on same location	10×10^5 times
Safety standards	UL CSA (conforming)
EMI	FCC class B (conforming) to 51°C for the medium)

3-1-5. Interfacing signal description

1) Input signals (controller to drive)

Pin	Signal name	Description
10 12 14	DRIVE SELECT 0 1	Used to select one of four drive units (maximum) connected to the PC-7200. Unit numbers 0 to 4 correspond to the actual drive unit numbers. Selection is done by means of the dip switch within the drive unit.
6	2	See Para.8 for setting of dip switch. It is also possible to use signal as motor on off control signal using the jumper wire.
8	3	
4	HEAD LOAD This signal is valid only when the head load magnet is in use.	Although it is not possible to use the signal to load the head because the mechanical head loadmode is adopted, it can be used as a data write gate signal. And it requires the same controlas the normal head load signal, there would be no need of controlling this signal when the dip switch 7 or 8 is set on. (See 82.)
16	MOTOR ON	This signal is used to drive the spindle motor. The motor rotates with a low state of this signal. All drives connected are operated by this signal, irrespective of DRIVE SELECT0 to 3. It is possible to control the spindle motor using DRIVE SELECT0 to 3, instead of this signal, when the jumper is used. (See 9-1.)
18	DIRECTION SELECT	This signal is used to select the head moving direction. With a low state of this signal, the head moves towards disk inner side. And, a low on this line moves the head towards disk outer side.
20	STEP	With this signal the head is moved to access the disk. A single pulse of a low state signal moves the head one track towards the direction given by DIRECTION SELECT. Action takes place at a trail edge of the signal.
22	WRITE DATA	Data write signal. At a high to low transition of the signal, the current in the head coil is inverted to write data bits. The data are written when WRITE GATE is at a low. Recording is done in the FM or MFM mode.
24	WRITE GATE	With a low state of this signal, data are enabled to write. When the signal is at a high, data read or disk access is enabled.
32	SIDE ONE SELECT	With this signal is selected the side-0 or side-1. When the signal is at a low, the side-1 is selected. When the signal is at a high, the side-0 is selected.
2	LOW DENSITY	With this signal is slected the high density or normal density mode. When the signal is at a low, the normal density mode is selected. When the signal is at a high, the high density mode is selected.

2) Output signals (controller to drive)

Pin	Signal name	Description
8	INDEX	This signal is issued when the disk index hole is sensed. The signal turns low each time a holeis detected. It is possible by the use of the jumper to change the signal issuing condition. (Refer to 9-2.)
26	TRACK 00	A low on this line shows that the head is on the track 00.
28	WRITE PROTECT	A low on this line shows that the disk is write protected, in other words, the write protect notch is covered.
30	READ DATA	Data read signal which turns low when a magnetic inversion is sensed on the disk. The data are read in the FM or MFM mode. This signal is not sent out until it became internally ready.
34	READY*	This signal goes low when all of the following conditions are met. (1) All dc supplies are on. (2) Disk is inserted properly in the drive unit. (3) Disk must be rotating with a speed of more than 70% of the given rating. The signal is held within the device when DRIVE SELECT is at a high, and it will be sent out when DRIVE SELECT turned low.
34	DISK CHANGE*	This signal goes low when one of the following conditions are met. (1) At power on. (2) When the push-button is depressed or a disk is ejected. The signal goes high when all of the following conditions are met. (1) When a step pulse is received. (2) When a disk is inserted.
7	OPEN*	This signal line is left unconnected.

* These three signals (READY, DISK CHANGE, OPEN) are factory options and one of signals can be selected.

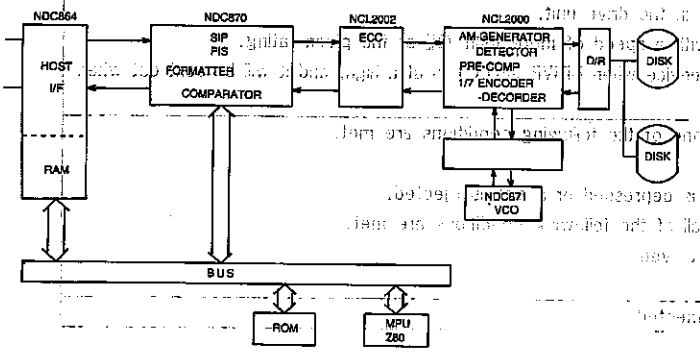
CHAPTER 4.
HARD DISK INTERFACE
(used for the model PC-7200 only)

1. General

This controller is an IBM PC AT controller (for JVC drive) that consists of an NDC864 Host Interface, NDC870 Hard Disk Controller, NCL2000 RLL Modem, NCL2002 ECC, and Z-80 Microprocessor. Discussion will be given about the NDC9008 around the above mentioned microchips.

2. Basic operations

a. Block diagram



b. Host interface

The NDC864 is the IBM AT compatible interfacing microchip.
The NDC864 is directly connected to the host bus and allows easier construction of the disk controller in conjunction with the NDC870 HDC.

b-1. Bus

There are two host buses and two internal buses.

b-1-1. Host interface address bus (A0 to A9)

The host uses this bus to select task file register and control/status register.

b-1-2. Host interface data bus (SD0 to 15)

A 16-bit bidirectional bus is employed to transfer data, command, and status.
For transfer of data between the host and the controller sector buffer (RAM within the NDC864), all 16 bits are directly connected to the RAM.

b-1-3. Interface board bus

When the Z-80 MPU is in action, the firmware program ROM address, NDC864 register address, NDC870 register address, and NCL2002 register address are sent from the Z-80 MPU.
When the NDC870 HDC is in action, the FPU program ROM address is sent from the NDC870. (FPU program: format sequencer microprogram)

b-1-4. Interboard data bus

When the Z-80 MPU is in action, the data bus is used for transfer of the firmware program data and transfer of data between IC registers. When the NDC870 HDC is in action, disk data are transferred by the control of the NDC870.

c. Hard disk startup

Command from the host is first stored in the NDC864 command register which is processed by the Z-80 MPU program. The Z-80 MPU program sets necessary control registers for the NDC870 and the top address is set for necessary microprogram and the control is handed to the NDC870. After the NDC870 acquires the control for the interboard bus (data, address, control signal), it starts to execute the microcommands from the top address of the microprogram to do a series of operations (data transfer, disk drive control). The control is then is handed to the Z-80 MPU after completion of a series of operations.

d. CRC and ECC

CRC and ECC are generated and interrogated by the NDC870 and NCL2002.
A 2-byte CRC is contained in the ID field and 7-byte ECC is contained in the data field.

d-1. CRC

The CRC code is generated and checked in the CRC operation circuit of the NDC870. CRC two bytes are controlled by the NDC870 microprogram so as to attached to the ID field. The CRC bytes are written at a time of FORMAT command.

d-2. ECC

The ECC code is generated and checked in the NCL2002 ECC circuit and recorded in the byte filed that follows the data field, using the NDC870 ECC write signal.
When an error is found during read, the control is returned to the MPU to locate the error location and to produce the bit pattern in error. When no error is found, all registers within the ECC generation circuit are set zero, and when an error is met, a different bit pattern is created according to the number of error bits and location. After this, the data already within the data buffer of the NDC864 are corrected and sent to the host.

e. RLL modulation and demodulation (NCL2000)

The RLL modulator/demodulator (NCL2000) modulates the NRZ serial data into 2-7 code serial data transferred from the NDC870 (NCL2002), to create data to be written on the disk.
On the contrary, the 2-7 code read from the disk are demodulated in to the NRZ serial data to be transferred to the NDC870.
It is connected with the NDC871 hybrid VCO, to select data demodulation VFO control and clock.
Shown below is the table for the NRZ and 2-7 code conversion.

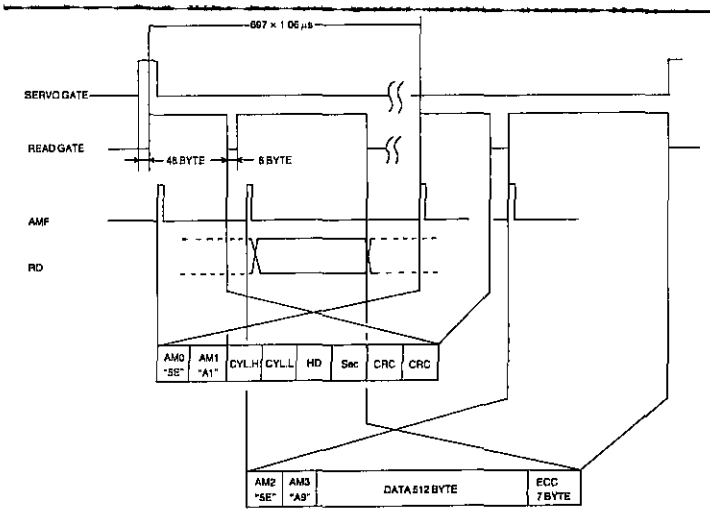
NRZ DATA	2-7 CODE
01	0100
00	1000
111	000100
100	001000
101	100100
1101	00100100
1100	00001000

f. Seek

Step pulse required to seek is created by the NDC870 microprogram under the step rate of 18 microseconds. When the Z-80 MPU recognizes the seek command, information (buffer mode, head moving direction, and number of pulses) for the NDC870 HDC are given by the Z-80 MPU monitor program. Then, the NDC870 microprogram is started to sent step pulses to the disk drive with the direction control signal.

g. Read

After the read gate is enabled by the NDC870 HDC, a sync pattern is sought for by the LS123 (one-shot). The sync pattern is 1001001---, and the LS123 factor is set to the value re-trigger is possible (233±5ns), and the one-shot is kept at "1" (triggered) at all times so long as the sync pattern data are issued from the disk. When the LS123 output is received by the NCL2000, the synchronous field detect circuit counter comes active. As the counter counts 16 pulses, the NCL2000 sets the latch to switch from 2F clock to read data and the CLAMP signal is sent out to suppress a phase difference between the read data and the VCO clock. When 48 pulses are counted, the address mark detect circuit comes active. When the address mark is detected, the address mark found signal is sent from the NCL2000 to the NDC870 HDC. (A unique mark identical to the 2/7 rule is used.) (With this signal, it is found the top location of the data and the byte location.)
The NRZ serial data demodulated in the NCL2000 are converted into parallel form in the NDC870 to be sent to the NDC864 interface microchip.



NOTE-1: READ GATE turns ON after 48 bytes×1.06μs by SERVO GATE and AM is started to search. Assuming from format write, the time that AMF turns ON is 697×1.06μs.

h. Write

When the write command is received from the host, the Z-80 MPU program sets the DMA buffer address transfer counter in the NDC870 HDC, to start the DMA.

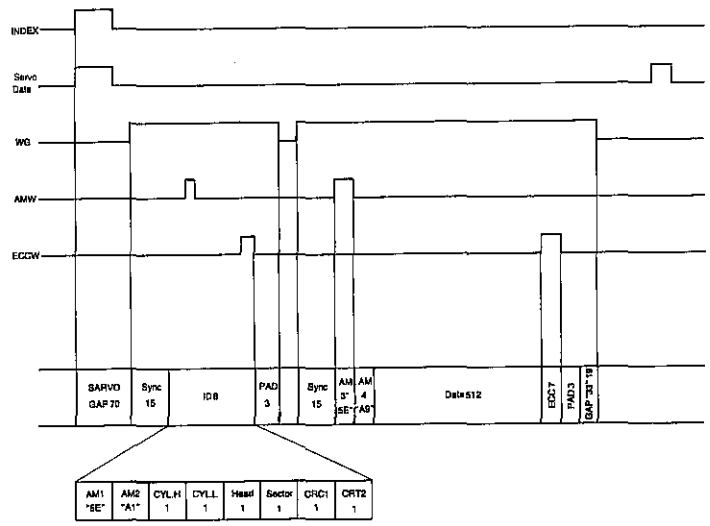
First, the NDC870 microprogram detects the ID field (refer to Read).

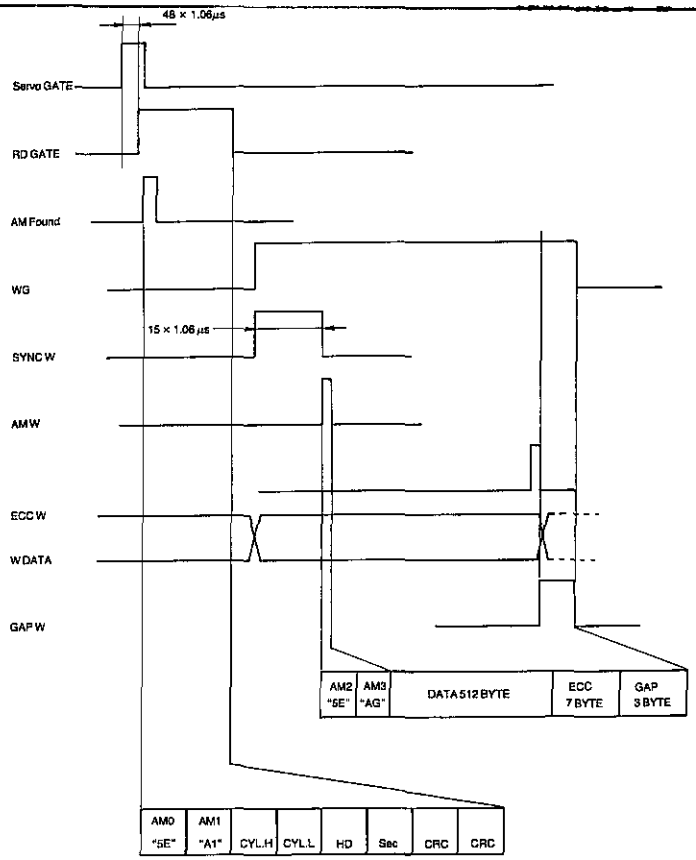
When the ID field is detected, the NDC870 HDC sets WRITE GATE active and the synchronous field is written. (2-7 code sync pattern is generated by the NCL2000.) As long as the NRZ serial data from the NDC870 is at a low, the syncronous field is continued to write.

At a low to high transition of the NRZ serial data, the NCL2000 modulator/demodulator generates the address mark pattern.

Thereafter, the NRZ serial data are demodulated into a 2-7 code by the NCL2000, and the ECC 7 bytes are attached to the data field and the data are written on the disk.

Format Track Write





3. Drive interface

PIN	I/O	SIGNAL	PIN	I/O	SIGNAL
1		GND	2	O	R.DATA
3		GND	4	I	W.DATA
5		GND	6	I	FACTORY OPTION
7	I	POWER SAVE	8	O	(SHIP READY)
9		GND	10	I	READ/WRITE
11	I	MOTOR ON	12	I	HEAD SELECT
13	I	DIRECTION IN	14	I	STEP
15	O	WRITE FAULT	16	O	SEEK COMPLETE
17	O	SERVO GATE	18	O	INDEX
19	O	TRACK 000	20	O	READY
21		GND(Logic)	22		+5V(Logic)
23		GND(MOTOR)	24		+5V(MOTOR)
25		GND	26		+12V

4. Troubleshooting

a. General

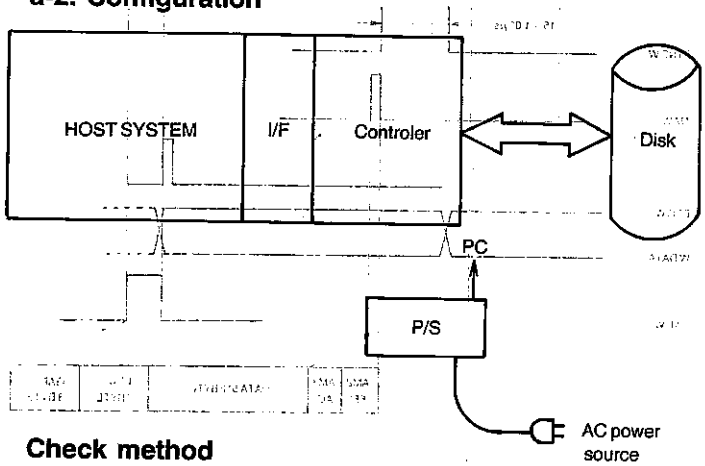
Next is discussed about troubleshooting regarding the NDC9008 magnetic disk controller.

a-1. Tool

The following tools are required for troubleshooting.

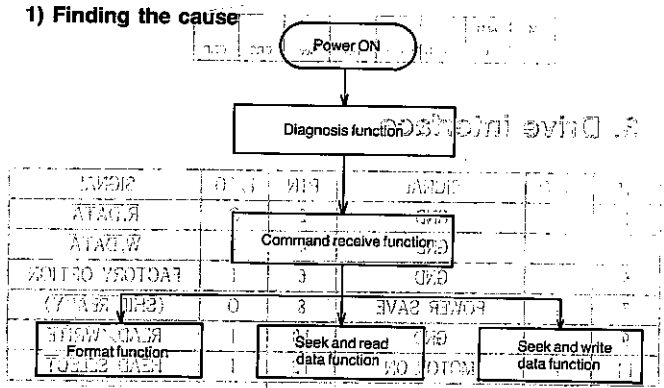
1. Host system
2. Disk in trouble
3. Oscilloscope
4. Diagnostic program

a-2. Configuration



Check method

1) Finding the cause



b. Controller basic functional checks

The controller function is checked to see if power on or reset function is working properly.

a) In case Z-80 MPU (8G) MREQ (pin-15) RD (pin-18) output is not on

Cause: MPU BUSRQ (pin-22) at low-level:

→ NDC864 in failure.

· MPU INT (pin-12) at low level:

→ NDC864 in failure

→ LS04 (4D) in failure

· MPU RESET (pin-23) at low level:

→ NDC864 in failure

→ PST518A in failure

· MPU CLK (pin-1), 5.0MHz not received:

→ Crystal X2 in failure

→ MPU in failure

c. Drive not ready

c-1) Ready signal check

Check the ready signal after power on.

c-2) Power save signal does not turn low

→ 74HCT240 (5C) in failure

→ NDC870 in failure

c-3) Ready signal does not go low even if the power save signal is normal

→ Drive unit or signal cable in failure.

c-4) If the ready signal is normal

→ 74HCT240 (9H) in failure

d. Error status appears after successful command transfer or no response from the controller

d-1. Check the JP4 and JP5 jumper plug setups

d-2. Command transfer not enabled even if setup is normal

→ CN1 or NDC864 in failure

If the NDC864 is normal, read the I/O address in 1F7 (177) after power on to check that the [50H] is in the status register.

→ NDC870 in failure

e. Trouble at data seek and read command

An error evokes after a successful startup.

e-1. Seek error

→ Check the step pulse (CN2, 3, pin-14).

If not appeared:

·NDC870 in failure

·74HTC240 (5C) in failure

→ If step pulse is normal:

·Drive unit in failure

e-2. Record not found or data error

→ Check TP5 if 15MHz is oscillated.

If not oscillated:

·NDC871 in failure

·Crystal (x1) in failure

→ Check if sync is found.

If 200ns±5ns is not found from TP2 (one-shot output):

·V1 in maladjustment

·VS123 (6F) in failure

If both are normal but sync write not found:

→ Drive unit in failure

NCL2000 in failure

→ CN2, 3-READ/WRITE (pin-10) does not change high and low:

·NDC870 in failure (pin-22 does not turn high and low).

·PST518A in failure (pin-3 does not turn high).

·MC3487P in failure

→ If READ/WRITE is normal, but read data are not produced:

·Drive unit in failure

→ If read data are produced but an error is caused:

·If ECC error is seen: NCL2002 in failure.

·If address mark not found: NCL2000 in failure

Check method

Read TRIG INDEX (CN2, 3, pin-18) of the sector 1 only from the host.

g. Trouble at data seek and write

1. Seek error

Refer to Paragraph e.

2. Record not found

Refer to Paragraph e.

In regard to a write failure, there is a good possibility that the drive unit is in failure.

CHAPTER 5.
HARD DISK DRIVE

Specification of the hard disk drive

1-1. Model name
JD3824R0-0D1 (w/o shield case)

1-2. Disk
Disk: 1
Cylinders: 615+1
Tracks: 1230

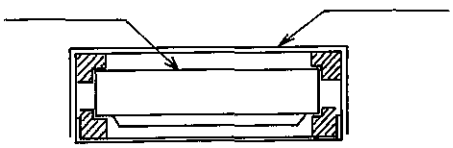
1-3. Storage capacity
Unformatted: 26.6MB
Formatted: 21.44MB

1-4. Recording method
Method: 2-7 RLL
Data transfer rate: 7.5M bits/sec

1-5. Formatting
Sectors per track: 34
Capacity per sector: 512 bytes

1-6. Average access time including settling time
24ms (track to track)
78ms average (1/3 track)
130ms full stroke

1-7. Environmental requirements
Operating temperature (in the test temperature compartment)
0 to 55°C, where the temperature is measured at the top plate of the drive unit.
Operating temperature: −20 to 60°C
Operating humidity: 20 to 80%RH, with moisture ball temperature at 29°C, max.
Non-operating humidity 5 to 90%RH, with moisture ball temperature at 29°C, max.
*The above specifications are for the drive unit only.



1-8. Reliability
MTBF: 20,000 hours
MTTR: 30 minutes
P.M: Not required
Life: 5 years
CSS: 10,000D start/stop
Medium defect: 20 max., except for the cylinder 0.
Defect length: 11 bits, max.
Error rate:
Soft error (NOTE): 10-10, max.
Hard error: 10-12, max.
Seek error: 10-5, max.
NOTES:
(1) In regard to a soft error, recovery is attained after eight times of retrials.
(2) In regard to a hard error, recovery is not attained after eight times of retrials.

1-9. Shock resistance
Operating: 3G, 10ms, during write (5G, actual)
7G, 10ms, during read (sinusoidal halfwave)
Non-operating: 70G, 10ms (all axial direction) (sinusoidal halfwave)

1-10. Vibration resistance
Operating: 5 to 10Hz, 1.245mm, full amplitude
10 to 500Hz, 0.25G, peak
Transit: • Vertical (axis Y)
8 to 27Hz: 1.3G, peak
27 to 33Hz: deviation, 0.9144mm
33 to 500Hz: 2.0G, peak
• Longitudinal (axis Z) and horizontal (axis X)
7 to 27Hz: 0.75G, peak
27 to 33H: deviation, 0.508mm
33 to 500Hz: 1.1G, peak

1-11. Weight
860 grams, HDD only

1-12. Physical dimensions
See the table.

1-13. DC power supply (HDD only)

	Allowable error	Allowable ripple	Consumption current (max)
+12V	±5%	100mVp−p	250mA
+5V(MOTOR)	±10%	150mVp−p	1,500mA
+5V(LOGIC)	±5%	100mVp−p	150mA

Ripple shall be 20Hz to 120Hz and 10Hz to 1MHz white noise.

1-14. Power consumption (rated voltage at 25±2°C
• Motor ON:
Read: 3.8W, max.
Write; 3.6W, max.
Seek: 5.7W, max. (9.7W, peak)
Waiting:3.3W, max.
• Motor starting (5msec max.): 8.8W, peak

1-15. Format
(1) Physical format
Cylinders 0 through 614 are physically formatted.
Hard track formatting is done for hard sectors.
(2) Interleave 2

1-16. Drive interface specification

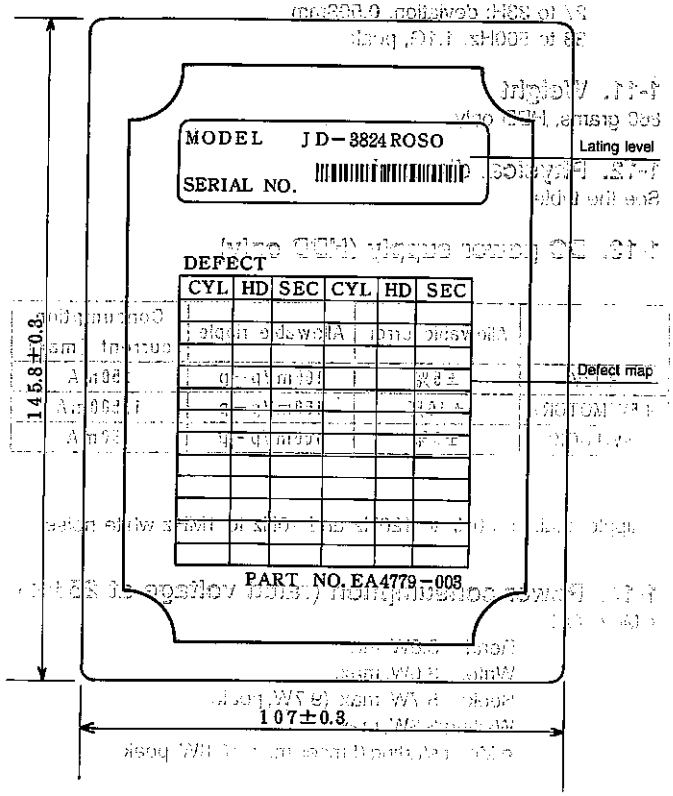
PIN	I/O	SIGNAL	PIN	I/O	SIGNAL
1		GND	2	O	R.DATA
3		GND	4	I	W.DATA
5		GND	6	I	FACTORY OPTION
7		POWER SAVE	8	O	(SHIP READY)
9		GND	10	I	READ/WRITE
11	I	MOTOR ON	12	I	HEAD SELECT
13	I	DIRECTION IN	14	I	STEP
15	O	WRITE FAULT	16	O	SEEK COMPLETE
17	O	SERVO GATE	18	O	INDEX
19	O	TRACK 000	20	O	READY
21		GND(Logic)	22		+5V(Logic)
23		GND(MOTOR)	24		+5V(MOTOR)
25		GND	26		+12V

NOTE-1: The following applies to the pin-12, head select logic.
Head 0/head 1
NOTE-2: No connection should be made to the pin-6, for, it is a factory option input which is not used by this model.
NOTE-3: The pin-8 is an output that turn low when the head has moved to the shipping position and it is possible to drive the red LED.

NOTE-4: Except for the power supply and pin-8, input and output are 74HC compatible. (2K pullup resistance is attached to input.)

1-17. Drive marginal value

1±8ns, max.
(Jitter of less than 6ns is preferable for the controller to be used used in conjunction.)

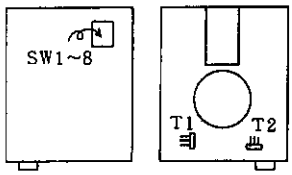


CHAPTER 6.
ADJUSTMENT

PC-7200 series MFD setup

The following settings are required to use the MFD for the PC-7200.

	o PC-7201 o PC-7202 (Drive A) o PC-7221	o PC-7202 (Drive B) o CE-720F	o CE-721F
SW1	ON	OFF	←
SW2	OFF	←	←
SW3	OFF	ON	←
SW4	ON	OFF	←
SW5	OFF	←	←
SW6	OFF	←	←
SW7	ON	←	←
SW8	OFF	←	←
T1	SS	←	
T2	DC	←	



NOTE1: Use a fine tipped item such as a pair of tweezers to set SW1 to SW8.

PC-7200 timer error adjustment

[Purpose]

To adjust timer accuracy, the timer basic clock frequency may be adjusted using the trimmer capacitor.

[Instrument required]

Type UT-300 or UT300A error adjusting tool or frequency counter.

[Measuring method]

1. Connect the power cable of the instrument with the wall outlet and turn power on after a lapse of more than 15 minutes which is required for the instrument to become stable.
2. Apply probes to test pins, TP1 and TP7 (GND) of the main board.
3. Connect power supply, MFD, LCD, or CRT to the main board and turn power on. Insert the test disk in the MFD.
4. After ensuring that "LOADING OK" appeared in the display, adjust the timer error to the room temperature using the trimmer capacitor, in reference to the table below.

Room temperature	Daily error (sec/day)	Nominal value
14 ~ 16°C	−0.25 ~ +0.65	(+0.25)
16 ~ 18°C	−0.20 ~ +0.85	(+0.35)
18 ~ 20°C	+0.20 ~ +1.00	(+0.45)
20 ~ 30°C	−0.20 ~ +1.15	(+0.55)

7-1. 80287 80-Bit HMOS NUMERIC PROCESSOR EXTENSION (80287-8)

- **High Performance 80-Bit Internal Architecture**
- **Implements Proposed IEEE Floating Point Standard 754**
- **Expands iAPX 286/10 Datatypes to Include 32-, 64-, 80-Bit Floating Point, 32-, 64-Bit Integers and 18-Digit BCD Operands**
- **Object Code Compatible with 8087**
- **Built-in Exception Handling**
- **Operates in Both Real and Protected Mode iAPX 286 Systems**
- **8x80-Bit, Individually Addressable, Numeric Register Stack**
- **Protected Mode Operation Completely Conforms to the iAPX 286 Memory Management and Protection Mechanisms**
- **Directly Extends iAPX 286/10 Instruction Set to Trigonometric, Logarithmic, Exponential and Arithmetic Instructions for All Datatypes**
- **Compatible with 80386 CPU**
- **Available in EXPRESS—Standard Temperature Range**

Available in 40 pin-Cerdip package (see Packaging Spec: Order #231369)

The Intel® 80287 is a high performance numerics processor extension that extends the iAPX 286/10 architecture with floating point, extended integer and BCD data types. The iAPX 186/20 computing system (80286 with 80287) fully conforms to the proposed IEEE Floating Point Standard. Using a numerics oriented architecture, the 80287 adds over fifty mnemonics to the iAPX 286/20 instruction set, making the iAPX 286/20 a complete solution for high performance numeric processing. The 80287 is implemented in N-channel, depletion load, silicon gate technology (HMOS) and packaged in a 40-pin cerdip package. The iAPX 286/20 is object code compatible with the iAPX 86/20 and iAPX 88/20.

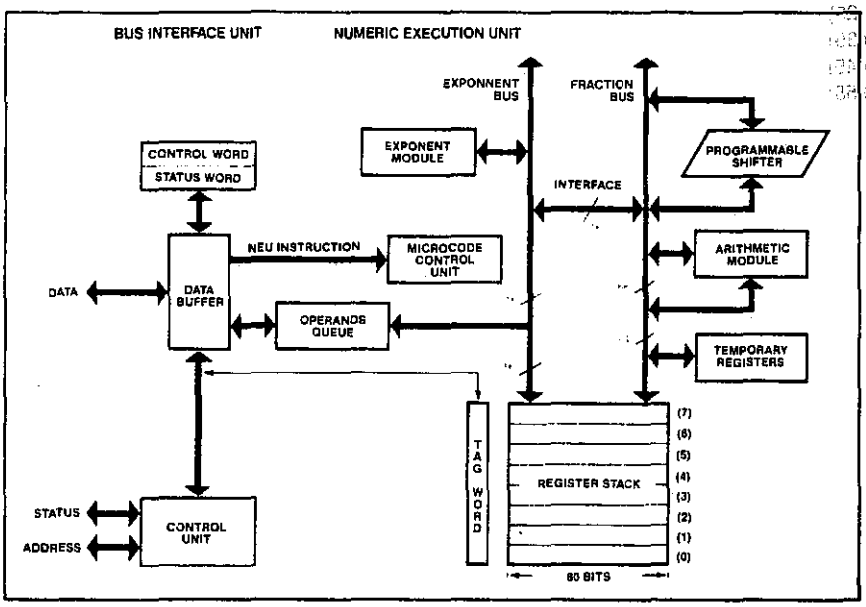
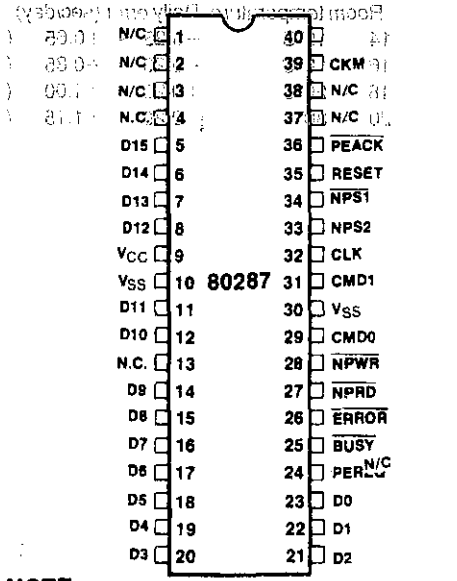


Figure 1. 80287 block diagram



NOTE:
N.C. PINS MUST NOT BE CONNECTED.

Figure 2. 80287 pin configuration

Table 1. 80287 pin description

Symbols	Type	Name and Function
CLK	I	Clock input: this clock provides the basic timing for internal 80287 operations. Special MOS level inputs are required. The 82284 or 8284A CLK outputs are compatible to this input.
CKM	I	Clock Mode signal: indicates whether CLK input is to be divided by 3 or used directly. A HIGH input will cause CLK to be used directly. This input may be connected to V_{CC} or V_{SS} as appropriate. This input must be either HIGH or LOW 20 CLK cycles before RESET goes LOW.
RESET	I	System Reset: causes the 80287 to immediately terminate its present activity and enter a dormant state. RESET is required to be HIGH for more than 4 80287 CLK cycles. For proper initialization the HIGH-LOW transition must occur no sooner than 50 μs after V_{CC} and CLK meet their D.C. and A.C. specifications.
D15-D0	I/O	Data: 16-bit bidirectional data bus. Inputs to these pins may be applied asynchronous to the 80287 clock.
$\overline{\text{BUSY}}$	O	Busy status: asserted by the 80287 to indicate that it is currently executing a command.
$\overline{\text{ERROR}}$	O	Error status: reflects the ES bit of the status word. This signal indicates that an unmasked error condition exists.
PEREQ	O	Processor Extension Data Channel operand transfer request: a HIGH on this output indicates that the 80287 is ready to transfer data. PEREQ will be disabled upon assertion of $\overline{\text{PEACK}}$ or upon actual data transfer, whichever occurs first, if no more transfers are required.
$\overline{\text{PEACK}}$	I	Processor Extension Data Channel operand transfer ACKnowledge: acknowledges that the request signal (PEREQ) has been recognized. Will cause the request (PEREQ) to be withdrawn in case there are no more transfers required. $\overline{\text{PEACK}}$ may be asynchronous to the 80287 clock.
$\overline{\text{NPRD}}$	I	Numeric Processor Read: Enables transfer of data from the 80287. This input may be asynchronous to the 80287 clock.
$\overline{\text{NPWR}}$	I	Numeric Processor Write: Enables transfer of data to the 80287. This input may be asynchronous to the 80287 clock.
$\overline{\text{NPS1}}$, NPS2	I	Numeric Processor Selects: indicate the CPU is performing an ESCAPE instruction. Concurrent assertion of these signals (i.e., $\overline{\text{NPS1}}$ is LOW and NPS2 is HIGH) enables the 80287 to perform floating point instructions. No data transfers involving the 80287 will occur unless the device is selected via these lines. These inputs may be asynchronous to the 80287 clock.
CMD1, CMD0	I	Command lines: These, along with select inputs, allow the CPU to direct the operation of the 80287. These inputs may be asynchronous to the 80287 clock.

7-2. TM-42: 8042/8742AH UNIVERSAL PERIPHERAL INTERFACE 8-BIT SLAVE MICROCONTROLLER

- **UPI-42: 12 MHz**
- **Pin, Software and Architecturally Compatible with 8041A/8741A**
- **8-Bit CPU plus ROM, RAM, I/O, Timer/Counter and Clock in a Single Package**
- **2048 x 8 ROM/EPROM, 128 x 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins**
- **One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface**
- **DMA, Interrupt, or Polled Operation Supported**
- **Fully Compatible with all Intel and Most Other Microprocessor Families**
- **Interchangeable ROM and EPROM Versions**
- **Expandable I/O**
- **Sync Mode Available**
- **Over 90 Instructions: 70% Single Byte**
- **Available in EXPRESS — Standard Temperature Range**
- **inteligent Programming™ Algorithm — Fastest EPROM Programming**
- **8742AH Available in 40-Lead Cerdip Package**
- **8042 Available in both 40-Lead Plastic and 44-Lead Plastic Leaded Chip Carrier Packages**

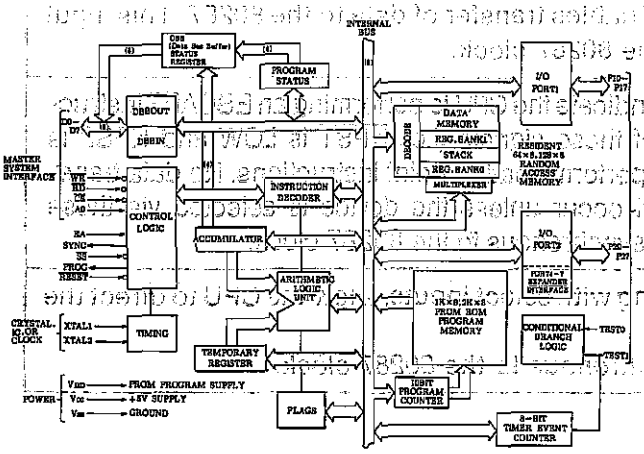
(See Packaging Spec., Order #231369)

The Intel UPI-42 is a general-purpose Universal Peripheral Interface that allows the designer to develop customized solution for peripheral device control.

It is essentially a "slave" microcontroller, or a microcontroller with a slave interface included on the chip. Interface registers are included to enable the UPI device to function as a slave peripheral controller in the MCS™ Modules and iAPX family, as well as other 8-, 16-bit systems.

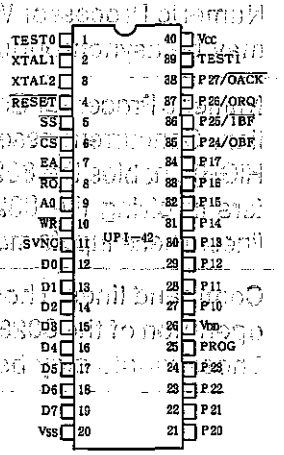
To allow full user flexibility, the program memory is available in either ROM or UV-erasable EPROM. All UPI-42 devices are fully pin compatible for easy transition from prototype to production level designs. These are the memory configurations available.

UPI Device	ROM	EPROM	RAM	Programming Voltage
8042	2K	—	256	—
8742AH	—	2K	256	12.5V



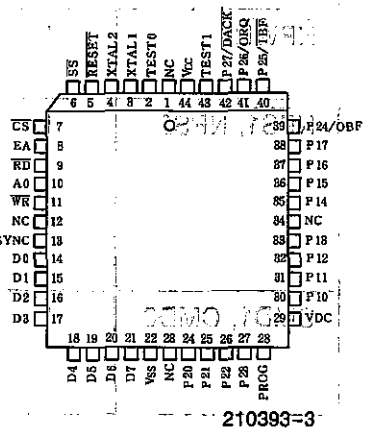
210393-1

Figure 1. Block diagram



210393-2

Figure 2. DIP pin configuration



210393-3

Figure 3. PLCC pin configuration

Table 1. Pin Description

Symbol	DIP Pin No.	PLCC Pin No.	Type	Name and Function
TEST 0, TEST 1	1 39	2 43	I	**TEST INPUTS:** Input pins which can be directly tested using conditional branch instructions. **FREQUENCY REFERENCE:** TEST 1 (T_1) also functions as the event timer input (under software control). TEST 0 (T_0) is used during PROM programming and verification in the 8742AH. It is also used during "sync mode" to reset the instruction state to S1 and synchronize the internal clock to PH1. See the Sync Mode Section.
XTAL 1, XTAL 2	2 3	3 4	I	**INPUTS:** Inputs for a crystal, LC or an external timing signal to determine the internal oscillator frequency.
$\overline{RESET}$	4	5	I	**RESET:** Input used to reset status flip-flops and to set the program counter to zero. $\overline{RESET}$ is also used during PROM programming and verification.
$\overline{SS}$	5	6	I	**SINGLE STEP:** Single step input used in conjunction with the SYNC output to step the program through each instruction (8742AH). This should be tied to +5V when not used. This pin is also used to put the device in synch mode by applying 12.5V to it.
$\overline{CS}$	6	7	I	**CHIP SELECT:** Chip select input used to select one UPI microcomputer out of several connected to a common data bus.
EA	7	8	I	**EXTERNAL ACCESS:** External access input which allows emulation, testing and PROM/ROM verification. This pin should be tied low if unused.
$\overline{RD}$	8	9	I	**READ:** I/O read input which enables the master CPU to read data and status words from the OUTPUT DATA BUS BUFFER or status register.
A_0	9	10	I	**COMMAND/DATA SELECT:** Address Input used by the master processor to indicate whether byte transfer is data (A_0 = 0, F1 is reset) or command (A_0 = 1, F1 is set).
$\overline{WR}$	10	11	I	**WRITE:** I/O write input which enables the master CPU to write data and command words to the UPI INPUT DATA BUS BUFFER.
SYNC	11	13	O	**OUTPUT CLOCK:** Output signal which occurs once per UPI-42 instruction cycle. SYNC can be used as a strobe for external circuitry; it is also used to synchronize single step operation.
D_0-D_7 (BUS)	12-19	14-21	I/O	**DATA BUS:** Three-state, bidirectional DATA BUS BUFFER lines used to interface the UPI-42 microcomputer to an 8-bit master system data bus.
P_{10}-P_{17}	27-34	30-33 35-38	I/O	**PORT 1:** 8-bit, PORT 1 quasi-bidirectional I/O lines. P_{10}-P_{14} and P_{17} access the signature row and security bit on the 8742AH.
P_{20}-P_{27}	21-24 35-38	24-27 39-42	I/O	**PORT 2:** 8-bit, PORT 2 quasi-bidirectional I/O lines. The lower 4 bits (P_{20}-P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4-7 access. The upper 4 bits (P_{24}-P_{27}) can be programmed to provide interrupt Request and DMA Handshake capability. Software control can configure P_{24} as Output Buffer Full (OBF) interrupt, P_{25} as Input Buffer Full ($\overline{IBF}$) interrupt, P_{26} as DMA Request (DRQ), and P_{27} as DMA ACKnowledge ($\overline{DACK}$).
PROG	25	28	I/O	**PROGRAM:** Multifunction pin used as the program pulse input during PROM programming. During I/O expander access the PROG pin acts as an address/data strobe to the 8243. This pin should be tied high if unused.
V_{CC}	40	44		**POWER:** +5V main power supply pin.
V_{DD}	26	29		**POWER:** +5V during normal operation. +12.5V during programming operation. Low power standby pin in EPROM and ROM versions.
V_{SS}	20	22		**GROUND:** Circuit ground potential.

7-3. MC146818

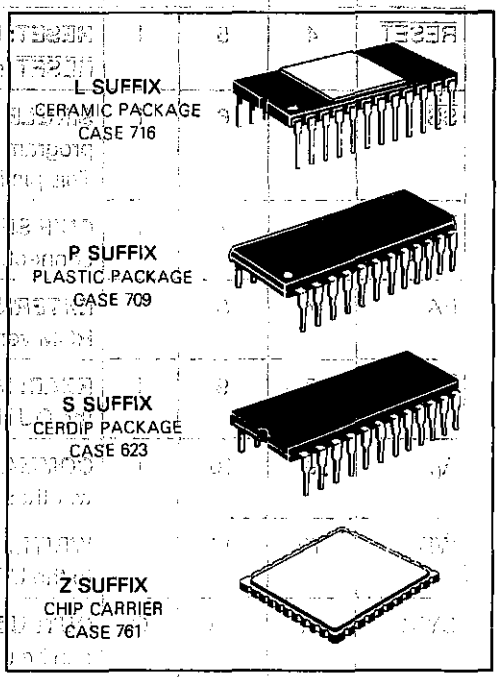
Advance Information

REAL-TIME CLOCK PLUS RAM (RTC)

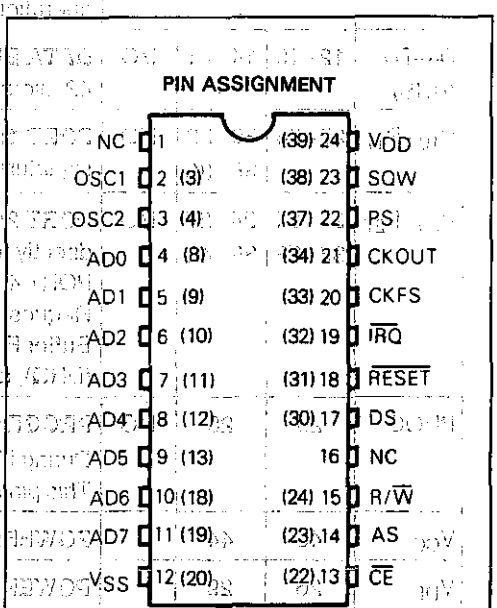
The MC146818 Real-Time Clock plus RAM is a peripheral device which includes the unique MOTEL concept for use with various microprocessors, microcomputers, and larger computers. This part combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The MC146818 uses high-speed CMOS technology to interface with 1-MHz processor buses, while consuming very little power.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS part (in an otherwise NMOS/TTL system) including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the MC146818 may be used with a CMOS microprocessor to relieve the software of the timekeeping workload and to extend the available RAM of an MPU such as the MC146805E2.

- Low-Power, High-Speed, High-Density CMOS
- Internal Time Base and Oscillator
- Counts Seconds, Minutes, and Hours of the Day
- Counts Days of the Week, Date, Month, and Year
- 3 V to 6 V Operation
- Time Base Input Options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz
- Time Base Oscillator for Parallel Resonant Crystals
- 40 to 200 μW Typical Operating Power at Low Frequency Time Base
- 4.0 to 20 mW Typical Operating Power at High Frequency Time Base
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24-Hour Clock with AM and PM in 12-Hour Mode
- Daylight Savings Time Option
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Microprocessor Bus Compatible
- MOTEL Circuit for Bus Universality
- Multiplexed Bus for Pin Efficiency
- Interfaced with Software as 64 RAM Locations
- 14 Bytes of Clock and Control Registers
- 50 Bytes of General Purpose RAM
- Status Bit Indicates Data Integrity
- Bus Compatible Interrupt Signals ($\overline{IRQ}$)
- Three Interrupts are Separately Software Maskable and Testable
  - Time-of-Day Alarm, Once-per-Second to Once-per-Day
  - Periodic Rates from 30.5 μs to 500 ms
  - End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Clock Output May Be Used as Microprocessor Clock Input
  - At Time Base Frequency ÷1 or ÷4
- 24-Pin Dual-In-Line Package
- Chip Carrier Also Available



PIN ASSIGNMENT



Pin numbers in parentheses represent equivalent Z suffix chip carrier pins. Pins that have not been designated for the chip carrier are not connected.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Figure 1. Block diagram

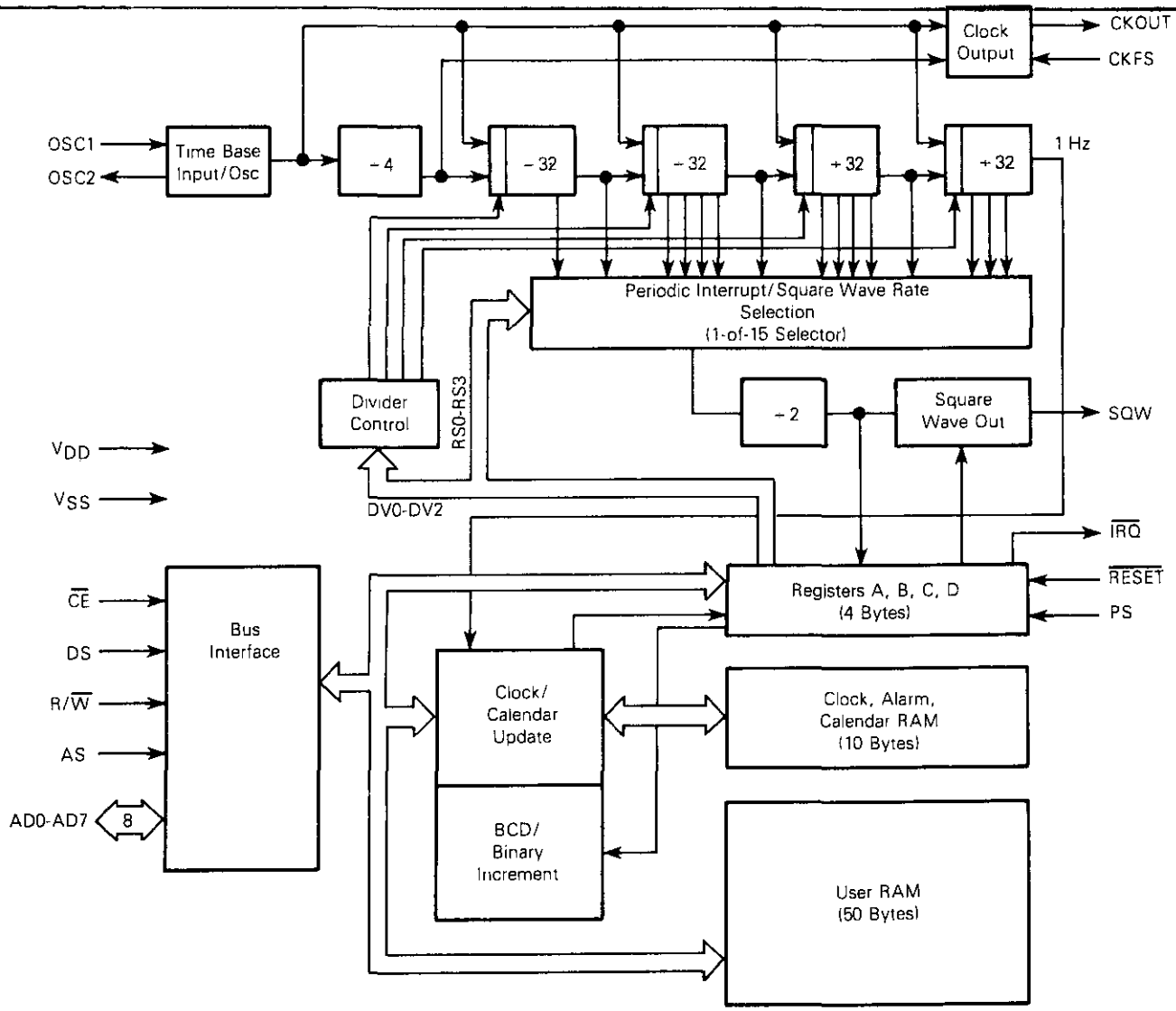
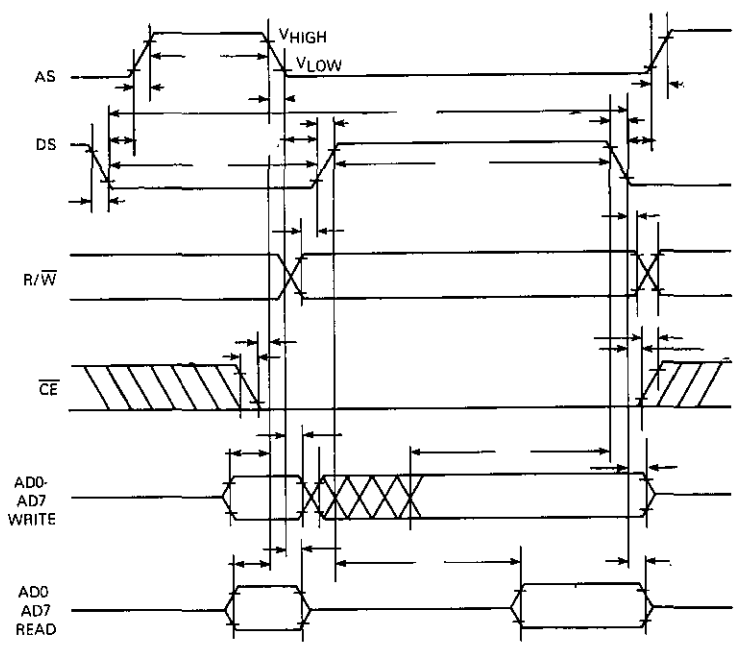


Figure 2. MC146818 bus timing



NOTE: $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 10%

SIGNAL DESCRIPTIONS

The block diagram in Figure 1 shows the pin connection with the major internal functions of the MC146818 Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

V_{DD}, V_{SS}

DC power is provided to the part on these two pins, V_{DD} being the more positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

OSC1, OSC2 — TIME BASE, INPUTS

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC1 as shown in Figure 10. The internal time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant AT cut crystal at 4.194304 MHz or 1.048576 MHz frequencies. The crystal connections are shown in Figure 11 and the crystal characteristics in Figure 12.

CKOUT — CLOCK OUT, OUTPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 2.

CKFS — CLOCK OUT FREQUENCY SELECT, INPUT

When the CKFS pin is tied to V_{DD} it causes CKOUT to be the same frequency as the time base at the OSC1 pin. When CKFS is tied to V_{SS}, CKOUT is the OSC1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS.

Table 2. Clock output frequencies

Time Base (OSC1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4.194304 MHz	High	4.194304 MHz
4.194304 MHz	Low	1.048576 MHz
1.048576 MHz	High	1.048576 MHz
1.048576 MHz	Low	262.144 kHz
32.768 kHz	High	32.768 kHz
32.768 kHz	Low	8.192 kHz

SQW — SQUARE WAVE, OUTPUT

The SQW pin can output a signal from one of the 15 taps provided by the 22 internal-divider stages. The frequency of the SQW may be altered by programming Register A, as shown in Table 5. The SQW signal may be turned on and off using the SQWE bit in Register B.

AD0-AD7 — MULTIPLEXED BIDIRECTIONAL ADDRESS/DATA BUS

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the MC146818 since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the MC146818 latches the address from AD0 to AD5. Valid write data must be presented and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle, the MC146818 outputs eight bits of data during the latter portion of the DS or $\overline{RD}$ pulses, then ceases driving the bus (returns the output drivers to the high-impedance state) when DS falls in the Motorola case of MOTEL or $\overline{RD}$ rises in the other case.

AS — MULTIPLEXED ADDRESS STROBE, INPUT

A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the MC146818. The automatic MOTEL circuit in the MC146818 also latches the state of the DS pin with the falling edge of AS or ALE.

DS — DATA STROBE OR READ, INPUT

The DS pin has two interpretations via the MOTEL circuit. When emanating from a Motorola type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and $\phi 2$ ($\phi 2$ clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.

The second MOTEL interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ emanating from the competitor type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

The MOTEL circuit, within the MC146818, latches the state of the DS pin on the falling edge of AS/ALE. When the Motorola mode of MOTEL is desired DS must be low during AS/ALE, which is the case with the Motorola multiplexed bus processors. To ensure the competitor mode of MOTEL, the DS pin must remain high during the time AS/ALE is high.

R/$\overline{W}$ — READ/WRITE, INPUT

The MOTEL circuit treats the R/$\overline{W}$ pin in one of two ways. When a Motorola type processor is connected, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high, whereas a write cycle is a low on R/$\overline{W}$ during DS.

The second interpretation of R/$\overline{W}$ is as a negative write pulse, $\overline{WR}$, $\overline{MEMW}$, and $\overline{I/OW}$ from competitor type processors. The MOTEL circuit in this mode gives R/$\overline{W}$ pin the same meaning as the write ($\overline{W}$) pulse on many generic RAMs.

$\overline{CE}$ — CHIP ENABLE, INPUT

The chip-enable ($\overline{CE}$) signal must be asserted (low) for a bus cycle in which the MC146818 is to be accessed. $\overline{CE}$ is not latched and must be stable during DS and AS (Motorola case of MOTEL) and during $\overline{RD}$ and $\overline{WR}$ (in the other MOTEL case). Bus cycles which take place without asserting $\overline{CE}$ cause no actions to take place within the MC146818. When $\overline{CE}$ is high, the multiplexed bus output is in a high-impedance state.

When $\overline{CE}$ is high, all address, data, DS, and R/$\overline{W}$ inputs from the processor are disconnected within the MC146818. This permits the MC146818 to be isolated from a powered-down processor. When $\overline{CE}$ is held high, an unpowered device cannot receive power through the input pins from the real-time clock power source. Battery power consumption can thus be reduced by using a pullup resistor or active clamp on $\overline{CE}$ when the main power is off. When $\overline{CE}$ is not used, it should be grounded.

$\overline{IRQ}$ — INTERRUPT REQUEST, OUTPUT

The $\overline{IRQ}$ pin is an active low output of the MC146818 that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the processor program normally reads Register C. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state. Multiple interrupting devices may thus be connected to an $\overline{IRQ}$ bus with one pullup at the processor.

$\overline{RESET}$ — RESET, INPUT

The $\overline{RESET}$ pin does not affect the clock, calendar, or RAM functions. On powerup, the $\overline{RESET}$ pin must be held low for the specified time, t_{RLH}, in order to allow the power supply to stabilize. Figure 13 shows a typical representation of the $\overline{RESET}$ pin circuit.

When $\overline{RESET}$ is low the following occurs:

a) Periodic Interrupt Enable (PIE) bit is cleared to zero,
b) Alarm Interrupt Enable (AIE) bit is cleared to zero,
c) Update ended Interrupt Enable (UIE) bit is cleared to zero,
d) Update ended Interrupt Flag (UF) bit is cleared to zero,
e) Interrupt Request status Flag (IRQF) bit is cleared to zero,
f) Periodic Interrupt Flag (PF) bit is cleared to zero,
g) The part is not accessible.

7-4. MN1288 LCD CONTROL LSI

The MN1288 is a multi-function LSI to control both liquid crystal dot matrix graphic displays and raster scan cathode ray tube displays.
It is suitable for controlling the display of transportable computers.

1. FEATURES

1. The MN1288 is suitable for personal computers using LCDs and CRTs.
2. Large screen LCDs can be used.
3. In the LCD mode, the software for the CRT can be used without difficulty.
4. Scrolling and external synchronization are possible.
5. 84-Pin flat package, using CMOS technology.

2. FUNCTIONS

2-1. LCD and CRT Control Common Functions

- Display character capacity (Programmable) : 214 (16384) characters
- VRAM addressing : 16K words
- Scrolling, paging : Scrolling scan line by scan line
  Scrolling character row by character row
- Cursor display (Programmable) : The cursor format and blinking
- External synchronization : In the non-interfaced mode
- Bus interface : 6800 family and 8080 family
- Floating address function

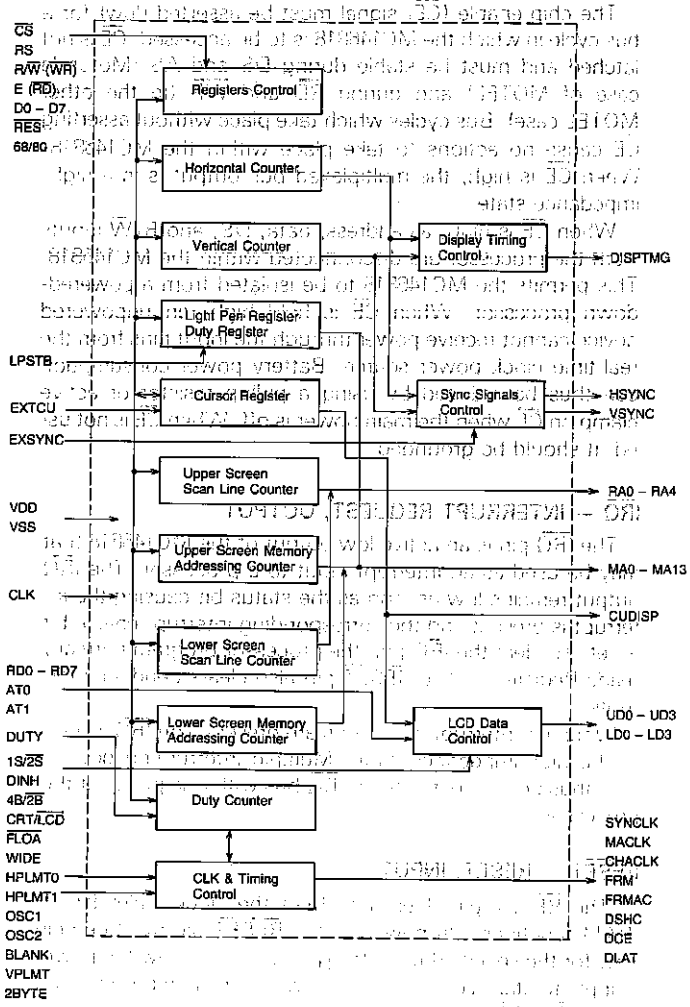
2-2. LCD Control Functions

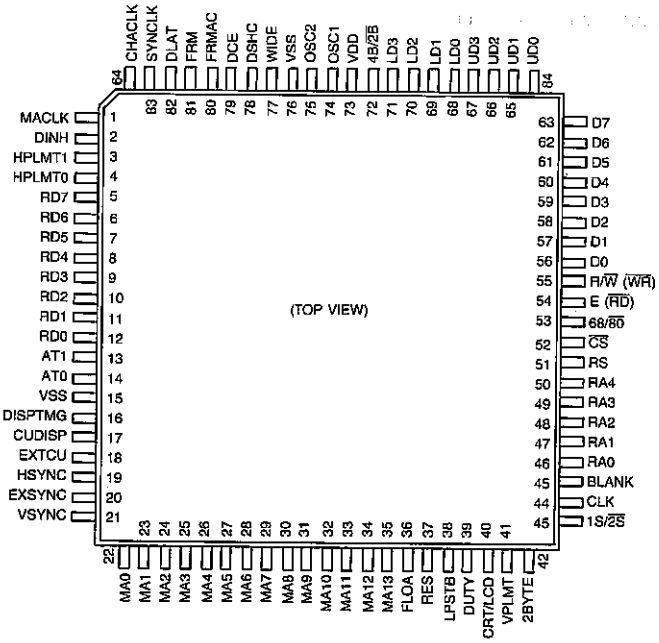
- Display format : Full display (non-divided screen)
  Upper and lower display (divided screen)
- Data outputs : 2 bits, 4 bits
- Duty (Programmable) : 1/2 – 1/256
- Front composition : Horizontal 4, 6, 8 dots
  Vertical 1-32 dots
- Sync signals : HSYNC (Horizontal synchronization)
  VSYNC (Vertical synchronization)
- Artibute control
- Built-in oscillator circuit

2-3. CRT Control Functions

- Scanning modes : Non-interlaced mode
  Interlaced-sync mode
  Interlaced-sync with video mode
- Skew funtion : Display timing
  Cursor display timing
- Light pen

MN1288 Block Diagram





Pin Configuration

Pin Description

PIN No.	Symbol	TYPE	C/L *1	Function
1	MACLK	O	L	Clock output from the memory addressing counter
2	DINH	I	L	LCD Data control input DINH is HIGH : Data (UD0-UD3.LD0-LD3) are LOW.
3 4	HPLMT1 HPLMT0	I	L	Input signals to determine the number of horizontal dots of a character HPLMT1 L L H H HPLMT0 L H L H HORIZONTAL DOTS 8 4 6 8
5 { 12	RD7 { RD0	I	L	Input data to display in the LCD mode
13 14	AT1 AT0	I	L	Input signals to control the attributes AT1 L L H H AT0 L H L H ATTRIBUTE EXTINGUISH REVERSAL NORMAL LIGHT
15	VSS			System ground
16	DISPTMG	O	C/L	Output signal to indicate the active display arealt is an active high signal.
17	CUDISP	O	C	Output signal to indicate a valid cursor address in the CRT mode. It is an active high signal. In the LCDmode, this output is not effective-kept LOW.
18	EXTCU	I	C/L	Input signal to enable the external cursor control. It is an active high signal. EXTCU is LOW : Extinguish EXTCU is HIGH : The cursor position is determined by the value of the Cursor Scan Line Register.
19	HSYNC	O	C/L	Output signal which is active during the horizontal retrace interval
20	EXSYNC	I	C/L	Input signal to enable the external sync mode. It is an active high signal. ESYNC is High : External Sync Mode
21	VSYNC	I/O	C/L	Bi-directional signal which is active during the vertical retrace interval. EXSYNC is LOW : (VSYNC) output EXSYNC is HIGH : (VSYNC) input
22 { 35	MA0 { MA13	O	C/L	Output signal to provide refresh memory addresses.
36	$\overline{FLOA}$	I	C/L	Input signal to float MA0-MA13 and RA0-RA4 outputs. It is an active low signal.
37	$\overline{RES}$	I	C/L	Input signal to reset this LSI. It is an active low signal.
38	LPSTB	I	C	Input signal from the light pen detecting a character position
39	DUTY	I	L	Input signal to determine the duty of the LCD. High : 1/100, Low : 1/200
40	CRT/$\overline{LCD}$	I		Input signal to select the display device, the CRT or the LCD. High : CRT mode, Low : LCD mode
41	VPLMT	I	L	Input signal to limit the number of vertical dots of a character.
42	2BYTE	I	L	Input signal to enable horizontal 16-dot characters. 2BYTE is LOW : Horizontal 8-dot character 2BYTE is HIGH : Horizontal 16-dot character
43	1S/$\overline{2S}$		L	Input signal to select the LCD format, the non-divided display format or the divided display format 1S/$\overline{2S}$ is HIGH : non-divided display format 1S/$\overline{2S}$ is LOW : divided display format
44	CLK	I	C	Clock input in the CRT mode. It is used to synchronize all CRT functions.
45	BLANK	I	L	input signal to generate HSYNC and VSYNC in the LCD mode. BLANK is HIGH : Generation of HSYNC and VSYNC BLANK is LOW : Non-genertion of HSYNC and VSYNC
46 { 50	RA0 { RA4	O	C/L	Output signals provide the row address of a character.
51	RS	I	C/L	Input signal to select the internal registers RS is LOW : Selection of the address registers RS is HIGH : Selection of the control registers
52	$\overline{CS}$	I	C/L	Chip select signal input. It is an active low signal.

53	68/$\overline{80}$	I	C/L	Input signal to determine the bus interface. 68/$\overline{80}$ is LOW : 8080 family bus interface. 68/$\overline{80}$ is HIGH : 6800 family bus interface
54	E($\overline{RD}$)	I	C/L	In the 6800 family mode, Enable Sync signal input from the CPU. In the 8080 family mode, Read Control signal input from the CPU
55	R/$\overline{W}$($\overline{WR}$)	I	C/L	In the 6800 family mode R/W select signal input from the CPU. In the 8080 family mode Write contrl signal input from the CPU
56 { 63	D0 { D7	I/O	C/L	Bi-directional data with the CPU
64 { 67	UD0 { UD3	O	L	In the divided display format of the LCD, parallel output data to provide the upper data for the LCD row drivers. In the non-divided display format mod, parallel output data to provide for the LCD row drivers. UD2.UD3 : 2bit outputs UD0-UD3 : 4bit outputs
68 { 71	LD0 { LD3	O	L	Parallel output data to provide the lower data for the row drivers in the divided display format mode ofthe LCD LD2, LD3 : 2bit outputs LD0-LD3 : 4bit outputs In the non-divided display format these outputs are not used.
72	4B/$\overline{2B}$	I	L	Input signal to select the type of the LCD data outputs, the 2-bit or the 4-bit data outputs. 4B/$\overline{2B}$ is LOW : 2-bit outputs 4B/$\overline{2B}$ is HIGH : 4-bit outputs
73	VDD			+5V Power supply
74 75	OSC1 OSC2	I O	L L	These are the pins to which a crystal is attached in the internal oscillation on mode of LCD. On the use of external clock, OSC1 is the external CLK input.
76	VSS			System ground
77	WIDE	I	L	In the wide mode, the horizontal width of a character is widened twice. WIDE is Low : normal WIDE is High : wide
78	DSHC	O	L	Output signal to shift the data for the LCD row drivers
79	DSHC	O	L	Output signal to enable the LCD row drivers
80	FRMAC	O	L	Alternate output signal for the LCD column and row drivers
81	FRM	O	L	Fram signal to initialize the LCD column drivers
82	DLAT	O	L	Output signal for the LCD column and row drivers to latch the data
83	SYNCLK	O	L	Symchronous signal to provide for the external system.
84	CHACLK	O	L	Character clock output

*1) C/L indicates the CRT or the LCD mode: C is the LCD mode
L is the CRT mode
C/L is the CRT and the LCD mode

Description of the Programmable Registers

Address Register	Register Number	Register Type	Read/ Write	Display Mode CRT/LCD	Data Bits 7	6	5	4	3	2	1	0
×	AR	Address Register	W	CRT/LCD	×	×	×					
00	R0	Hrixontal Total *1	W	CRT/LCD *2								
01	R1	Hrixontal Displayed	W	CRT/LCD								
02	R2	HSYNC Position *1	W	CRT/LCD *2								
03	R3	HSYNC/VSYNC Width	W	CRT/LCD *2	V3	V2	V1	V0	H3	H2	H1	H0
04	R4	Vertical Total *1	W	CRT/LCD *2	×							
05	R5	Vertical Total Adjust	W	CRT	×	×	×					
06	R6	Vertical Displayed	W	CRT	×							
07	R7	VSYNC Position *1	W	CRT/LCD *2	×							
08	R8	Interlace mode & Skew	W	CRT	C1	C0	D1	D0	×	×	V	S
09	R9	Maximun Scan Line Address	W	CRT/LCD	×	×	×					
0A	R10	Cursor Start Scan Line	W	CRT/LCD	×	B	P					
0B	R11	Cursor End Scan Line	W	CRT/LCD	×	×	×					
0C	R12	Start Address (H)	R/W	CRT/LCD	×	×						
0D	R13	Start Address (L)	R/W	CRT/LCD								
0E	R14	Cursor Address (H)	R/W	CRT/LCD	×	×						
0F	R15	Cursor Address (L)	R/W	CRT/LCD								
10	R16	Light Pen (H)	R	CRT	×	×						
11	R17	Light Pen (L), Duty Register *1	R/W	CRT/LCD								
1D	R29	Start Scan Line Address	R/W	CRT/LCD	×	×						
1F	R31	Vertical Blanking Flag	R	CRT/LCD *2	×	×	×	×	×	×	VF	×

*1: The register value = The required value – 1 *2: In the LCD mode, the register is effective when BLANK is High.

7-5. MN1292 VIDEO SIGNAL CONTROL LSI

The systems using both the CRT (720×350) and the LCD (640×200) without difficulty.

This LSI is packed in a 100-pin flat package and uses CMOS technorogy.

1. FEATURES

1-1. Both LCD and CRT Mode

Display Format	Character Mode (80×25)
Colors	Monochrome

1-2. LCD Mode

LCD Panel	640×200 (1-Panel, 2-Panel)
Panel Image	Normal, Reverse
Character Font	8×8 dots
Attribute Types	Mode 1, Mode 2
Intensity Types	Half-Tone, Alternate Font

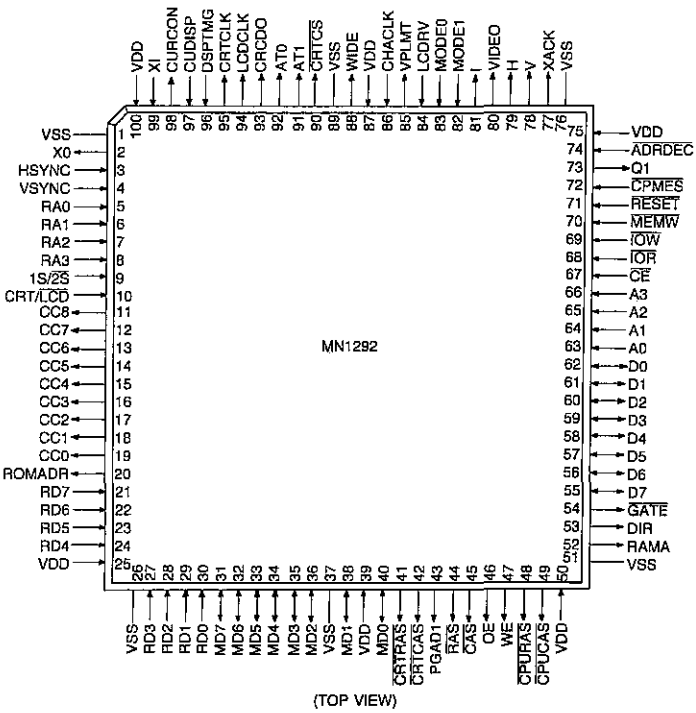
1-3. CRT Mode

Display Monitor	720×350
Character Font	9×14 dots

Note: The MN1288 is a LCD/CRT controller.

2. PIN DESCRIPTIONS

2-1. Pin Assignment



(TOP VIEW)

Figure 2-1. Pin assignment

2-2. Pin Descriptions

Pin No.	Pin Name	I/O	Functions
1	VSS		System ground
2	XO	O	Output osc
3	HSYNC	I	Input HSYNC signal
4	VSYNC	I	Input VSYNC signal
5~8	RA0~RA3	I	Input raster addresses to control underline
9	1S/$\overline{2S}$	I	Input signal to select the LCD format 1S/$\overline{2S}$ is HIGH : 1-Panel format 1S/$\overline{2S}$ is LOW : 2-Panel format
10	CRT/$\overline{LCD}$	I	Input signal to select the CRT and theLCD CRT/$\overline{LCD}$ is HIGH : CRT mode CRT/$\overline{LCD}$ is LOW : LCD mode
11~19	CC8~CC0	O *2	Output address to the C.G.ROM
20	ROMADR	O *1	Output address to the C.G.ROM CRT mode : ROMADR is HIGH LCD mode : ROMADR is LOW
21~24 27~30	RD7~RD0	I	Input data from the C.G.ROM
25	VDD		+5V Power supply
26	VSS		System ground
31~36 38,40	MD7~MD0	I/O *2	Bi-directional data with the video RAM
37	VSS		System ground
39	VDD		+5V Power supply
41	$\overline{CRTRAS}$	O *2	Output signal to enable row address of the MN1288
42	$\overline{CRTRAS}$	O *2	Output signal to enable column address of the MN1288
43	PGAD1	O *2	Output address to the video RAM
44	$\overline{RAS}$	I/O *2	Output $\overline{RAS}$ signal to the video RAM
45	$\overline{CAS}$	O *2	Output $\overline{CAS}$ signal to the video RAM
46	$\overline{OE}$	O *2	Output $\overline{OE}$ signal to the video RAM
47	$\overline{WE}$	O *2	Output $\overline{WE}$ signal to the video RAM
48	$\overline{CPURAS}$	O *2	Output signal to enable row address of the CPU
49	$\overline{CPUCAS}$	O *2	Output signal to enable column addressof the CPU
50	VDD		+5V Power supply
51	VSS		System ground
52	RAMA	O *2	Output address to the video RAM
53	DIR	O *2	Output signal to control the data bus
54	$\overline{GATE}$	O *2	Output signal to control the data bus
55~62	D7~D0	I/O *2	Bi-directional data with the CPU
63~66	A3~A0	I	Input address from the CPU
67	$\overline{CE}$	I	Input signal to enable the MN1292 $\overline{CE}$ is LOW : the MN1292 is active
68	$\overline{IOR}$	I	Input signal to read internal registers
69	$\overline{IOW}$	I	Input signal to write internal registers
70	$\overline{MEMW}$	I	Input signal to write the video RAM
71	$\overline{RESET}$	I	Input signal to reset the system
72	$\overline{CPMES}$	I	Input signal to control the video RAM access by the CPU
73	Q1	O	Output latch signal to the address MPX
74	$\overline{ADRDEC}$	I	Input signal to address the internalregisters by the CPU
75	VDD		+5V Power supply
76	VSS		System ground
77	XACK	O *2	Output write signal to the CPU
78	V	O *2	Output vertical sync signal
79	H	O *2	Output horizontal sync signal
80	VIDEO	O *2	Output video signal

81	I	O *2	Output internsity signal
82	MODE1	I	Input signals to control the attribute in
83	MODE0	I	the LCD mode
84	LCDRV	I	Input signal to reverse the LCD panel LCDRV is LOW : Normal image LCDRV is HIGH : Reverse image
85	VPLMT	O *2	Output signal to control the VPLMT of the MN1288 LCD mode : VPLMT is HIGH CRT mode : VPLMT is LOW (connect to the VPLMT of theMN1288)
86	CHACLK	I	Input signal to control diplay timings (connect to the CHACLK of the MN1288)
87	VDD		+5V Power supply
88	WIDE	O *2	Output signal to control the WIDE of the MN1288 When CE is LOW, WIDE is always LOW. (connect to the WIDE of the MN1288)
89	VSS		System ground
90	$\overline{CRTCS}$	O *2	Output signal to select the MN1288 (connect to the CS of the MN1288)
91	AT1	O *2	Output signal to control the attribute inthe
92	AT0		LCD mode (connect to the AT0, AT1 of the MN1288)
93	CRLCO	O	Output signal to select the LCD and the CRT
94	LCDCLK	O *2	Output clock signal in the LCD mode (connect to the OSC1 of the MN1288)
95	CRTCLK	O *2	Output clock signal in the CRT mode (connect to the CLK of the MN1288)
96	DSPTMG	I	Input DSPTMG signal from the MN1288
97	CUDISP	I	Input CUDISP signal from the MN1288
98	CURCON	O *2	Output signal to control cursor blinkingin the LCD mode. In the CRT mode this signal is HIGH. (connect to the EXTCU of the MN1288)
99	X1	I	Input osc
100	VDD		+5V Power supply

Figure 2-2. Pin descriptions (Part 1 of 4)

Notes: *1: These pins are 'LOW' when the $\overline{CE}$ is 'HIGH'.
*2: These pins are 'High-Z' when the $\overline{CE}$ is 'HIGH'.
When the $\overline{CE}$ is 'HIGH', only osc continue to operate.

3. MN1292 BLOCK DIAGRAM

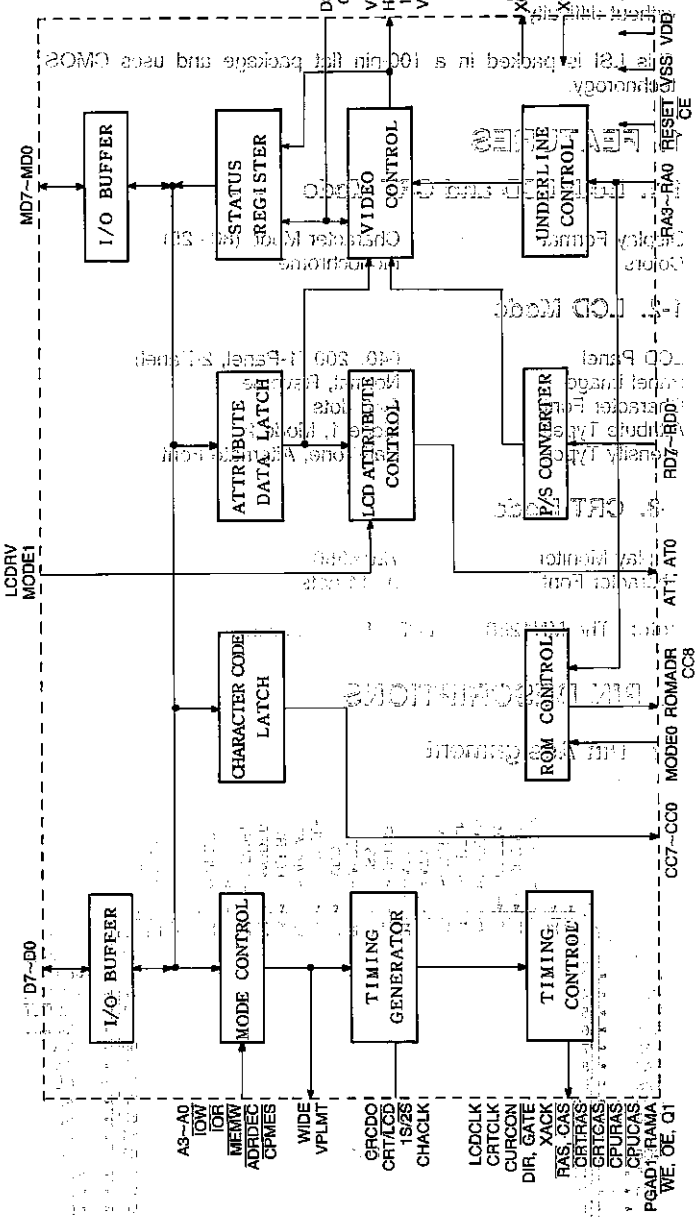


Figure 3-1. MN1292 block diagram

4. I/O ADDRESS MAP

ADRDEC	A3~A0	READ/WRITE	Functions
H	×		Not Decoded
L	0, 2, 4, 6	WRITE ONLY	MN1288 Address Register
L	1, 3, 5, 7	READ/WRITE	MN1288 Data Registers
L	8	WRITE ONLY	Mode Control Register
L	9	—	Not Used
L	A	READ ONLY	Status Register
L	B~F	—	Not Used

Figure 4-1. I/O address map

7-6. MN1294 LCD CONTROL LSI

The MN1294 is a video signal synthesizing LSI with the graduation display feature that has been developed for personal computer display. When used in combination with the MN1288 LCD/CRT controller, it will enhance to establish a display feature that has both the LCD and CRT displaying functions. While the color display function is furnished for the CRT, the color display function is furnished for the LCD with attribute and graduation features.

1. Features

1. When used in conjunction with the MN1288, a compact LCD/CRT display CGA can be established, which is about one third of the conventional CGA.

2. As RGB output and composite video signal outputs are furnished for the CRT display, it is possible to do monochrome or color display.

3. For the LCD display, it enhances to operate in the color CRT display mode using the attribute or graduation feature.

4. There are three kinds of attributes for the LCD display.

5. There are two modes of four and eight tones for the LCD display.

6. In the LCD 8-graduation mode, it is possible to choose any pattern of tone.

7. For the LCD display attribute, it is possible to choose intensity based emphasize by font selection or graduation (halftone).

8. In the LCD graphic 320×200 dots color mode, there are choices of pseudo 3-tone and 4-tone.

9. In the LCD display mode, black and white of the display data can be inverted.

10. It is possible to connect the following four types of display units, when a color graphic board is composed using the MN1294 and MN1288.

    a) RGB monitor (640×200 dots, 8 colors, 2 tones)
    b) Home television that has the composite video input
    c) LCD panel (640×200 dots, 2 screen)
    d) LCD panel (640×200 dots, 1 screen)

11. CMOS, 124-pin flat package

2. PIN DESCRIPTIONS

2-1. Pin Assignment

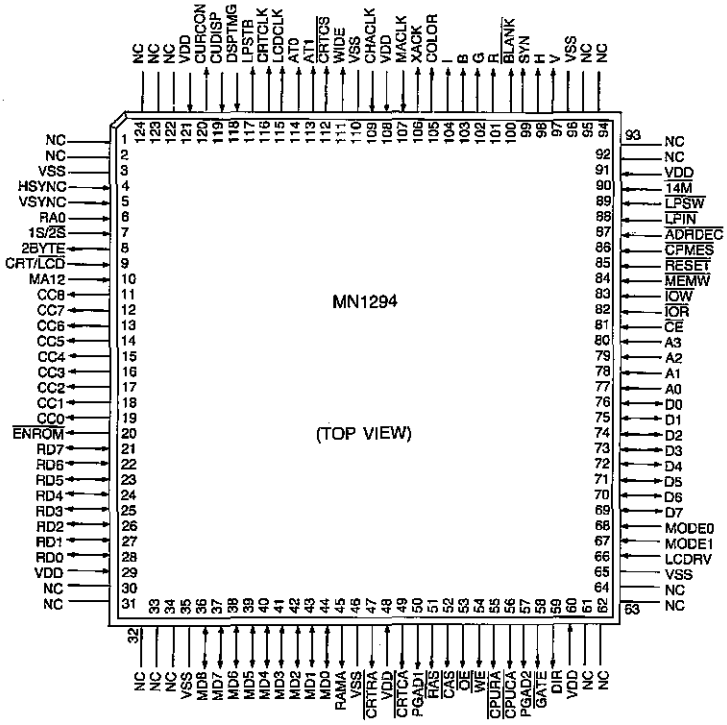


Figure 2-1. Pin assignment

2-2. Pin Descriptions

Pin No.	Pin Name	I/O	Functions
1~2	NC		Not Connected
3	VSS		System ground
4	HSYNC	I	Input HSYNC Signal
5	VSYNC	I	Input VSYNC Signal
6	RA0	I	Input RA0 signal of the MN1288
7	1S/$\overline{2S}$	I	Input signal to select the LCD format. 1S/$\overline{2S}$ is HIGH : 1-Panel format 1S/$\overline{2S}$ is LOW : 2-Panel format
8	2BYTE	O *1	Output signal to enable horizontal 16-dots characters. 2BYTE is HIGH : 8-dots characters 2BYTE is LOW : 16-dots characters
9	CRT/$\overline{LCD}$	I	Input signal to select the CRT or the LCD. HIGH : CRT mode LOW : LCD mode
10	MA12	I	Input MA12 signal from the MN1288
11~19	CC8~CC0	O *2	Output address to the C.G.ROM
20	$\overline{ENROM}$	O *1	Output signal to enable the C.G.ROM
21~28	RD7~RD0	I/O *2	Bi-directical data with C.G.ROM
29	VDD		+5V Power supply
30~34	NC		Not Connected
35	VSS		System ground
36~44	MD8~MD0	I/O *2	Bi-directical data with video RAM
45	RAMA	O *2	Output address to the video RAM
46	VSS		System ground
47	$\overline{CRTRA}$	O *2	Output signal to enable row address ofthe MN1288
48	VDD		+5V Power supply
49	$\overline{CRTCA}$	O *2	Output signal to enable column addressof the MN1288
50	PGAD1	O *2	Output signal to video RAM
51	$\overline{RAS}$	O *2	Output $\overline{RAS}$ signal to video RAM
52	$\overline{CAS}$	O *2	Output $\overline{CAS}$ signal to video RAM
53	$\overline{OE}$	O *2	Output $\overline{OE}$ signal to video RAM
54	$\overline{WE}$	O *2	Output $\overline{WE}$ signal to video RAM
55	$\overline{CPURA}$	O *2	Output signal to enable row address ofthe CPU
56	$\overline{CPUCA}$	O *2	Output signal to enable column addressof the CPU
57	PGAD2	O *2	Output signal to video RAM
58	$\overline{GATE}$	O *2	Output signal to coutrol data bus
59	DIR	O *2	Output signal to coutrol data bus.
60	VDD		+5V Power supply
61~64	NC		Not connected
65	VSS		System ground
66	LCDRV	I	Input signal to reverse the LCD panel
67	MODE1	I	Input signal to control attribute andshading
68	MODE0	I	functions in the LCD mode
69~76	D7~D0	I/O *2	Bi-directional data with the CPU
77~80	A3~A0	I	Input address from the CPU
81	$\overline{CE}$	I	Input signal to enable the MN1294 $\overline{CE}$ is LOW, the MN1294 is active.
82	$\overline{IOR}$	I	Input signal to read infernal registers
83	$\overline{IOW}$	I	Input signal to write infernal registers
84	$\overline{MEMW}$	I	Input signal to write video RAM
85	$\overline{RESET}$	I	Input signal to reset system
86	$\overline{CPMES}$	I	Input signal to control video RAM access by the CPU
87	$\overline{ADRDEC}$	I	Input signal to access the internal registers by the CPU
88	$\overline{LTIN}$	I	Input strobe signal of light pen
89	$\overline{LPSW}$	I	Input signal to show light pen condition $\overline{LPSW}$ is HIGH : Light pen not connected $\overline{LPSW}$ is LOW : Light pen connected
90	14M	I	Input clock signal of 14MHz
91	VDD		+5V Power supply
92~95	NC		Not connected
96	VSS		System ground
97	V	O *2	Output vertical sync signal to CRT
98	H	O *2	Output Horizontal sync signal to CRT
99	SYN	O *2	Output composite sync signal
100	$\overline{BLANK}$	O *2	Output signal of black level
101	R	O	Output RED signal to CRT
102	G	O	Output GREEN signal to CRT
103	B	O	Output BLUE signal to CRT
104	I	O *2	Output intensity signal to CRT
105	COLOR	O *2	Output color signal to composite monitor
106	XACK	O *2	Output wait signal to the CPU
107	MACLK	I	Input signal to control the LCD outputdata from the MN1288
108	VDD		+5V Power supply
109	CHACLK	I	Input signal to synchronize with theMN1288
110	VSS		System ground
111	WIDE	O *2	Output signal to control wide mode (connect to WIDE pin of the MN1288)
112	$\overline{CRTCS}$	O *2	Output chip select signal to the MN1288
113	AT1	O *2	Output signal to control the attribute inthe
114	AT0	O *2	LCD mode
115	LCDCLK	O *2	Output clock signal to the MN1288 in the LCD mode (connect to OSC1 pin of the MN1288)

Figure 2-2. Pin descriptions (Part 1 of 4)

Notes: *1: These pins are 'LOW' when the $\overline{CE}$ is 'HIGH'.
*2: These pins are 'High-Z' when the $\overline{CE}$ is 'HIGH'.

116	CRTCLK	O *2	Output clock signal to the MN1288 in the CRT mode (connect to CLK pin of the MN1288)
117	LPSTB	O *1	Output light pen strobe signal to the MN1288 This signal is LOW in LCD mode.
118	DSPTMG	I	Input signal of DISPTMG from the MN1288
119	CUDISP	I	Input signal of CUDISP from the MN1288
120	CURCON	O *2	Output signal to control the cursor blinking (connect to EXTCU of the MN1288)
121	VDD		+5V Power supply
122~124	NC		Not connected

Figure 2-2. Pin descriptions (Part 3 of 4)

Notes: *1: These pins are 'LOW' when the $\overline{CE}$ is 'HIGH'.
*2: These pins are 'High-Z' when the $\overline{CE}$ is 'HIGH'.

3. MN1294 BLOCK DIAGRAM

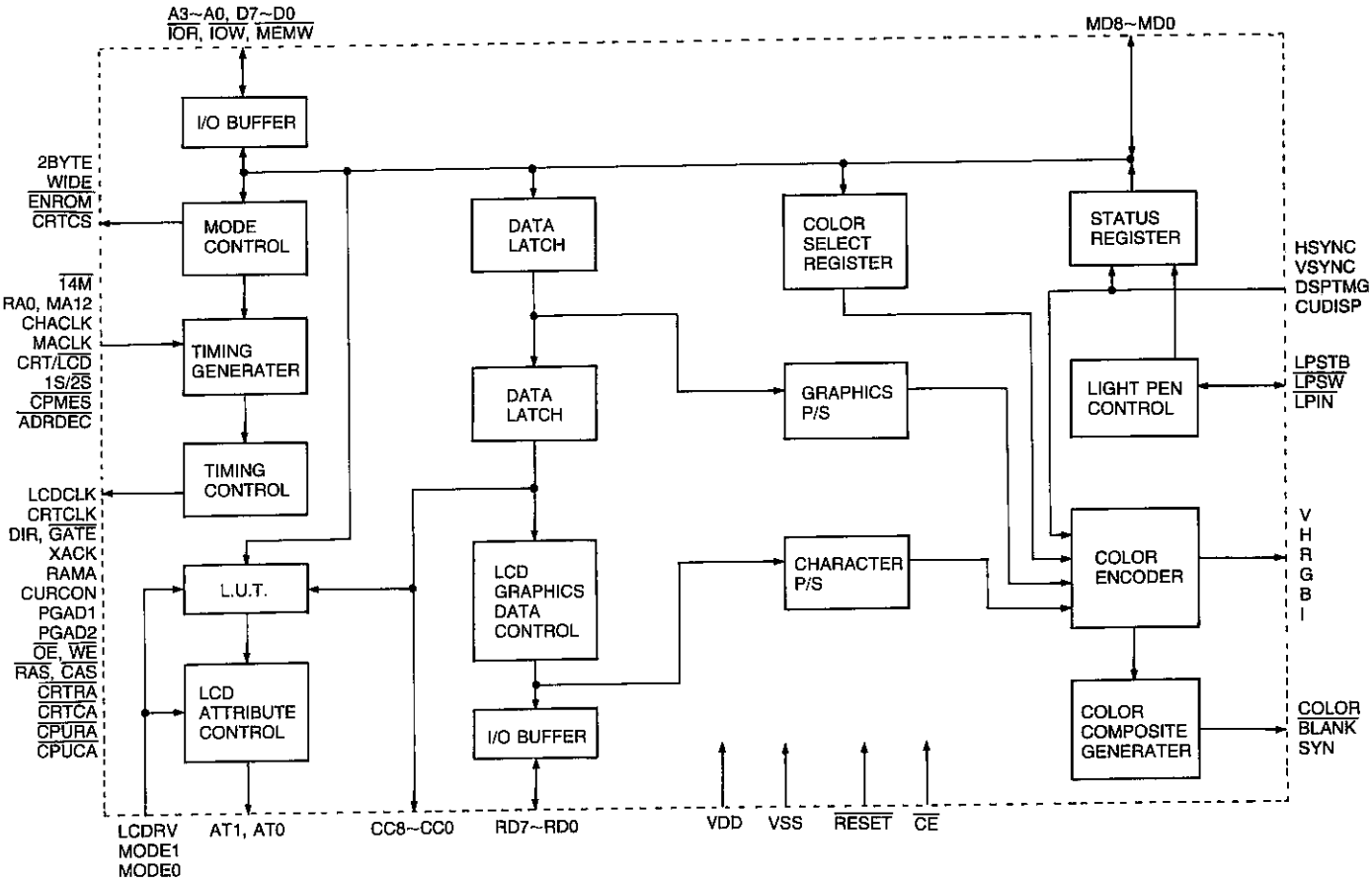


Figure 3-1. MN1294 block diagram

4. INTERNAL REGISTERS

ADREC	A3～A0	READ/WRITE	Registers
H	–	–	Not Decoded
L	0 2 4 6	WRITE ONLY	MN1288 Address Register
L	1 3 5 7	READ/WRITE	MN1288 Data Registers
L	8 *	WRITE ONLY	Mode Control Register
L	9 *	WRITE ONLY	Color Select Register
L	A	READ/WRITE	READ : Status Register Write : Shading Pattern Select Enable Register
L	B *	WRITE ONLY	Light Pen Latch Reset Register
L	C *	WRITE ONLY	Light Pen Latch Set Register

Figure 4-1. Internal registers

Note: *: If this register is read, the value will change.

4-1. The MN1288 Address Register and Data Registers

These are internal registers in the MN1288.

4-2. Mode Control Register

This register controls displaying modes as follows.

Bit	Function
7～6	Not Used
5	Background Intensity or Blink Bit
4	High-Resolution(640×200) Mode
3	Enable Video
2	Color Mode Select
1	Graphics Select
0	80×25 Character Mode

Table 4-2. Mode control register

Bit 5 Background Intensity or Blink Bit
When this bit is 1 (0), bit 7 of the attribute data functions as a blinking (background intensity) bit.

Bit 4 High-Resolution (640×200) Mode
When this bit is a 1, high-resolution (640×200) monochrome graphics mode is selected. The foreground color (only one color) can be selected out of the 16 colors.

Bit 3 Enable Video
When this bit is a 1, the video outputs are enabled.

Bit 2 Color Mode Select
When this bit is a 1, monochrome mode is selected.
When this bit is a 0, color mode is selected.

Bit 1 Graphics Select
When this bit is a 1, graphics mode is selected.
When this bit is a 0, character mode is selected.

Bit 0 80×25 Character Mode
When this bit is a 1, 80×25 character mode is selected.

4-3. Color Select Register

This register selects the displaying color in the CRT mode.
This register does not affect the LCD mode.

Bit	Function
7～6	Not Used
5	Selects Active Color Set in 320×200 Graphics Mode
4	Selects Intensified Set of Colors in 320×200 Graphics Mode
3	Selects Intensified Border Color in Character Mode Selects Intensified Background Color in 320×200 Graphics Mode Selects Intensified Foreground Color in 640×200 Graphics Mode
2	Selects Red Border Color in Graphics Mode Selects Red Background Color in 320×200 Graphics Mode Selects Red Foreground Color in 640×200 Graphics Mode
1	Selects Green Border Color in Character Mode Selects Green Background Color in 320×200 Graphics Mode Selects Green Foreground Color in 640×200 Graphics Mode
0	Selects Blue Border Color in Character Mode Selects Blue Background Color in 320×200 Graphics Mode Selects Blue Foreground Color in 640×200 Graphics Mode

Figure 4-3. Color select register

Bit 5 When this bit is a 1, color set 2 is selected.
When this bit is a 0, color set 1 is selected.
(See page 19 on color sets)

Bit 4 When this bit is a 1, foreground colors are intensified in 320×200 graphics mode.

Bit 3, 2, 1, 0
These bits select the border color of the screen in character mode, background color in 320×200 graphics mode and foreground color in 640×200 graphics mode. When these bits are set, the colors are selected.

4-4. Status Register

This register shows displaying conditions and light pen conditions.

Bit	Function	
7～4	Not Used	
3	Vertical Sync	Active High
2	Light Pen Switch	Active Low
1	Light Pen Strobe	Active High
0	Display Enable	Active Low

Figure 4-5. Status register

Bit 3 Vertical Sync
This bit is active during vertical retrace period.

Bit 2 Light Pen Switch
When this bit is active, light pen switch is ON.

Bit 1 Light Pen Strobe
This bit indicates light pen strobe signal.

Bit 0 When this bit is inactive, the MN1288 is either in a horizontal or vertical retrace period.
If the video RAM is accessed when this bit is active, it will cause flickers in the 80×25 character mode.

4-5. Shading Pattern Select Enable Register

When the value of this register is 90H～9FH, it enables to select shading patterns.

* The shading pattern can be changed as follows:
1. Write 90H～9FH to shading pattern select enable register. (Disable to write the MN1288 registers)
2. Write the values to shading pattern select register.
3. Write 00H to shading pattern select enable register. (Return to normal I/O mapping)

4-6. Light Pen Latch Reset Register

When the CPU writes to this register, the light pen latch is cleared.

4-7. Light Pen Latch Set Register

When the CPU writes to this register, the light pen latch is set.

4-8. Shading Pattern Select Register

This is a write only register and is used to select the shading pattern.

ADRDEC	A3~A0	READ/WRITE	Bit							
			7	6	5	4	3	2	1	0
L	0	WRITE ONLY	*	R2	R1	R0	*	G2	G1	G0
L	1	WRITE ONLY	*	B2	B1	B0	*	H2	H1	H0

Figure 4-6. Shading pattern select register

Notes: 1. '*' means Don't Care
2. When H2=H1=H0='1', the 8-shade mode is selected.

The shading is determind by decoding the values of this register.

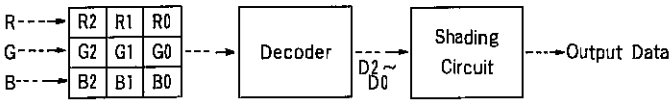


Figure 4-7. Shading data decoded diagram

The shading numbers are calculated by the logic below.

$$Dn=(R\cdot Rn)+(G\cdot Gn)+(B\cdot Bn) \qquad (n=0, 1, 2)$$

The default values of this register is shown in Figure 4-8.

R2	R1	R0	G2	G1	G0	B2	B1	B0
0	1	0	1	0	0	0	0	1

Figure 4-8. Default data

4-9. The Relation Between Shading Patterns and Numbers

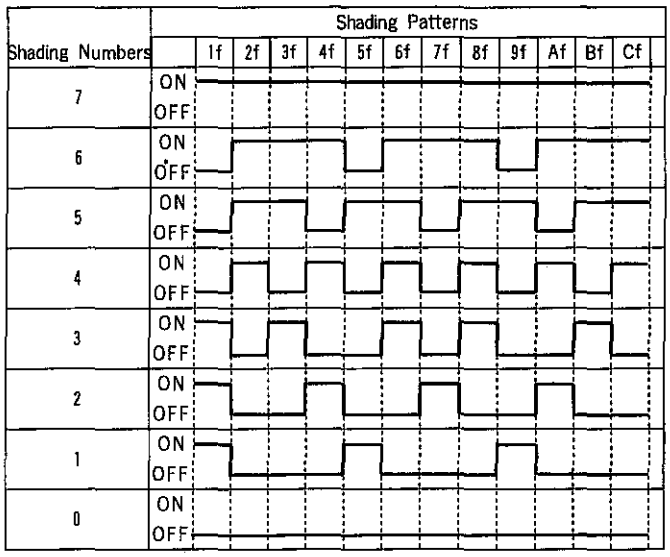


Figure 4-9. Shading pattern
(1f~Cf are the frame numbers of the LCD.)

According to the shading number, the shading pattern is determined. Data are outputed when the shading patterns are 'ON'. The MN1294 controls the shading function using these patterns.

5. THE MN1294 FUNCTIONS

Mode Control Register						CRT Mode	LCD Mode			
5	4	3	2	1	0		Mode 1	Mode 2	Mode 3	Mode 4
1	0	1	1	0	0	Character Monochrome * 40×25	Character Mode 1 40×25	Character Mode 2 40×25	Character Mode 3 40×25	Character Mode 4 40×25
1	0	1	0	0	0	Character Color 40×25				
1	0	1	1	0	1	Character Monochrome * 80×25	Character Mode 1 80×25	Character Mode 2 80×25	Character Mode 3 80×25	Character Mode 4 80×25
1	0	1	0	0	1	Character Color 80×25				
–	0	1	1	1	0	Graphics Monochrome * 320×200	Graphics Monochrome 320×200	Graphics Monochrome 320×200	Graphics Monochrome 320×200	Graphics Monochrome 320×200
–	0	1	0	1	0	Graphics Color 320×200	Graphics 3-shade 320×200	Graphics 4-shade 320×200	Graphics 3-shade 320×200	Graphics 4-shade 320×200
–	1	1	1	1	0	Graphics Monochrome 640×200	Graphics Monochrome 640×200	Graphics Monochrome 640×200	Graphics Monochrome 640×200	Graphics Monochrome 640×200

Note: * RGB : color
Composite : monochrome

Figure 5-1. The MN1294 displaying function table

5-1. Displaying Mode

5-1-1. Character Mode

Every character position in the character mode is defined by two bytes in the video RAM. Data format is shown in Figure 5-2.

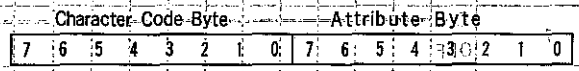


Figure 5-2. Data format in character mode

5-1-2. Graphics Mode

Every data in the video RAM defines the graphics pattern on the screen. There is no attribute code in this mode.

5-2. CRT Mode

5-2-1. Character Color Mode

The character attribute format is shown in Figure 5-3.

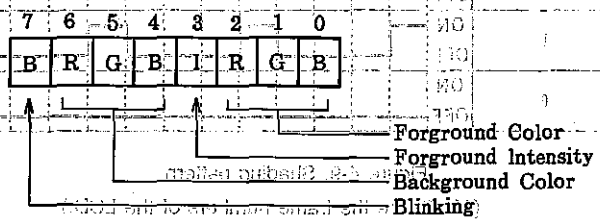


Figure 5-3. Attribute format

The blink bit functions as background intensity when bit 5 of the mode control register is a 0.
The color values are given in the Figure 5-4.

I	R	G	B	Displaying Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	Light Gray
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White

Figure 5-4. Displayed color

5-2-2. Character Monochrome Mode

The character attribute format is shown in Figure 5-5.

7	6	5	4	3	2	1	0	Attribute Function
B	0	0	0	I	1	1	1	Normal
B	1	1	1	I	0	0	0	Reverse
B	0	0	0	I	0	0	0	Non desplay(Black)
B	1	1	1	I	1	1	1	Non desplay(White)

Figure 5-5. Character attribute in monochrome mode

Note: I: Intensity B: Blink

5-2-3. Graphics Mode (320×200 Mode)

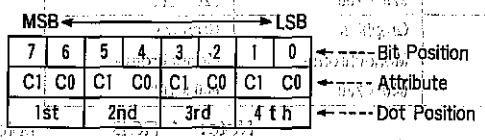


Figure 5-6. 320 × 200 graphics bit mapping

In 320× graphics mode, 1 byte in the video RAM represents 4 dots on the CRT. Each 20bit of attribute indicates the color of each dot. The color is defined by color select register. Bit 5 of color select register selects the color set in 320×200 graphics mode. When bit 2 of mode control register is a 0, the color set is defined by bit 5 of the color select register as shown in Figure 5-7. When bit 2 of mode control register is a 1, the color set is as below.

Attribute		Bit 2 of the mode control register		
		= '0'		= '1'
C1	C0	Color set 1	Color set 2	
0	0	Background Color	Background Color	Background Color
0	1	Green	Cyan	Cyan
1	0	Red	Magenta	Red
1	1	Brown	Light Gray	Light Gray

Figure 5-7. 320 × 200 graphics mode color sets

5-2-4. Graphics Mode (640×200 Mode)

In 640×200 graphics mode, 1 byte in the video RAM represents 8 dots on the CRT. MSB of the video RAM data is left most dot on the screen, and LSB is right most dot. Only 2 colors including background color can be used in this mode.

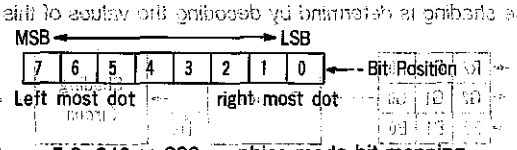
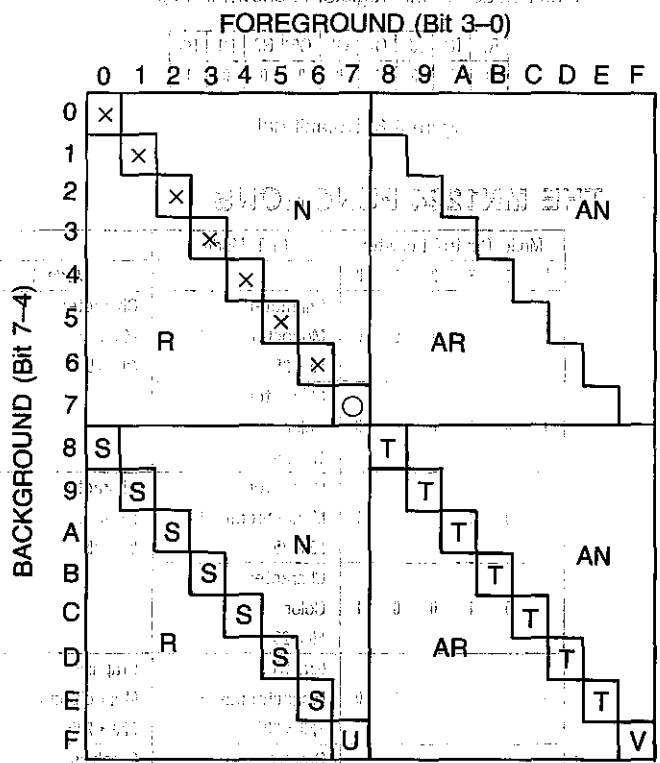


Figure 5-8. 640 × 200 graphics mode bit mapping

5-3. LCD Mode

5-3-1. Character Mode 1

In this mode, character intensity is represented by alternate font. The character intensity is available when the C.G. ROM has alternate fonts.



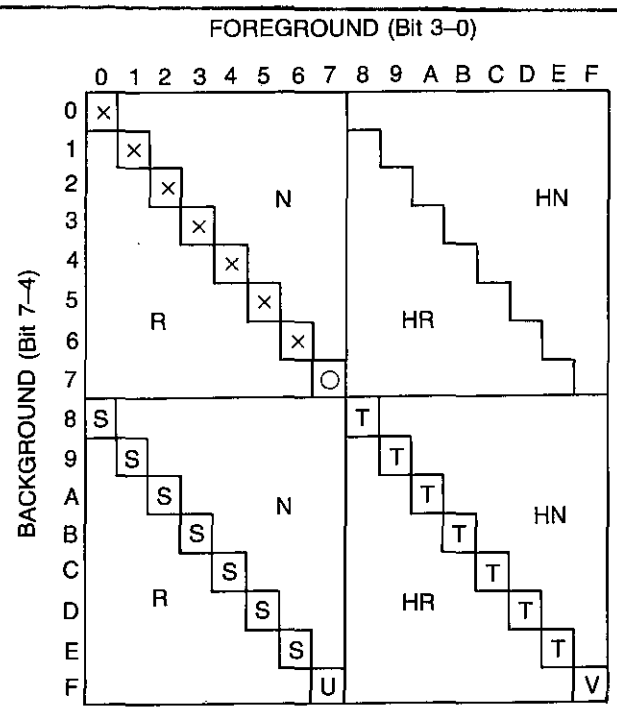
Bit 5 of Mode Control Register	S	T	U	V
1	×	AN	○	AN
0	N	×	N	○

× Non Display
○ All Dots on
N Normal
R Reverse
A Alternate Font

Figure 5-9. Character mode 1

5-3-2. Character Mode 2

In this mode, the character intensity is represented by shading.



Bit 5 of Mode Control Register	S	T	U	V
1	×	HN	○	HN
0	N	×	N	○

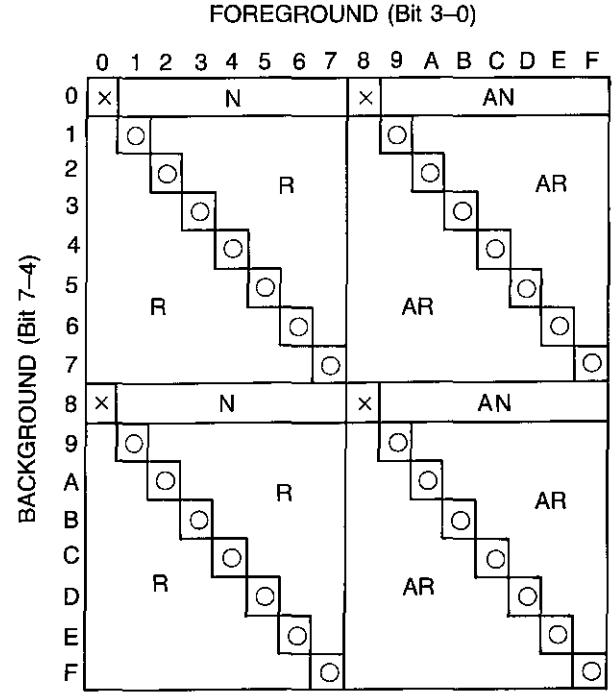
× Non Display
○ All Dots on
N Normal
R Reverse
H Half Tone

Figure 5-10. Character mode 2

Note: 'Half Tone' is a No. 4 shading of the shading numbers. (See page 14 on the shading numbers)

5-3-3. Character Mode 3

In this mode, character intensity is represented by alternate font. The character intensity is available when the C.G. ROM has alternate fonts.

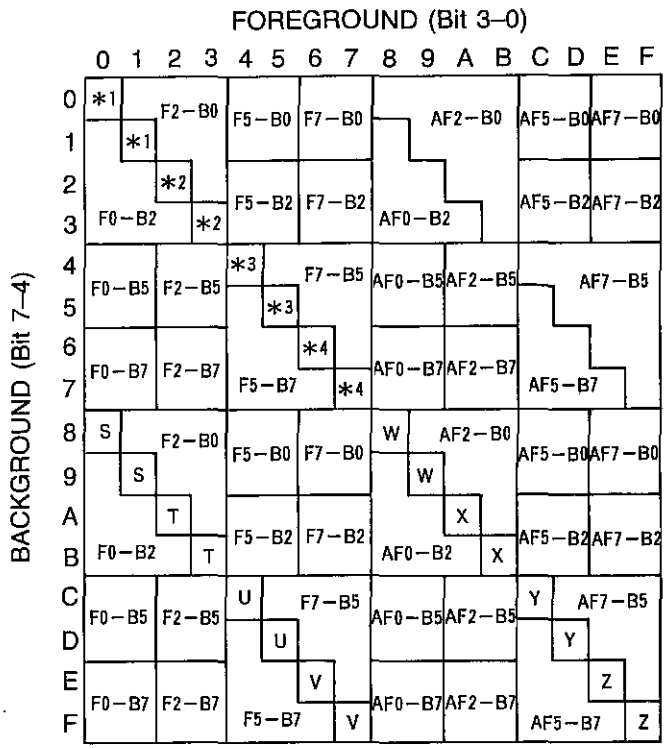


× Non Display
○ All Dots on
N Normal
R Reverse
A Alternate Font

Figure 5-11. Character mode 3

5-3-4. Character Mode 4

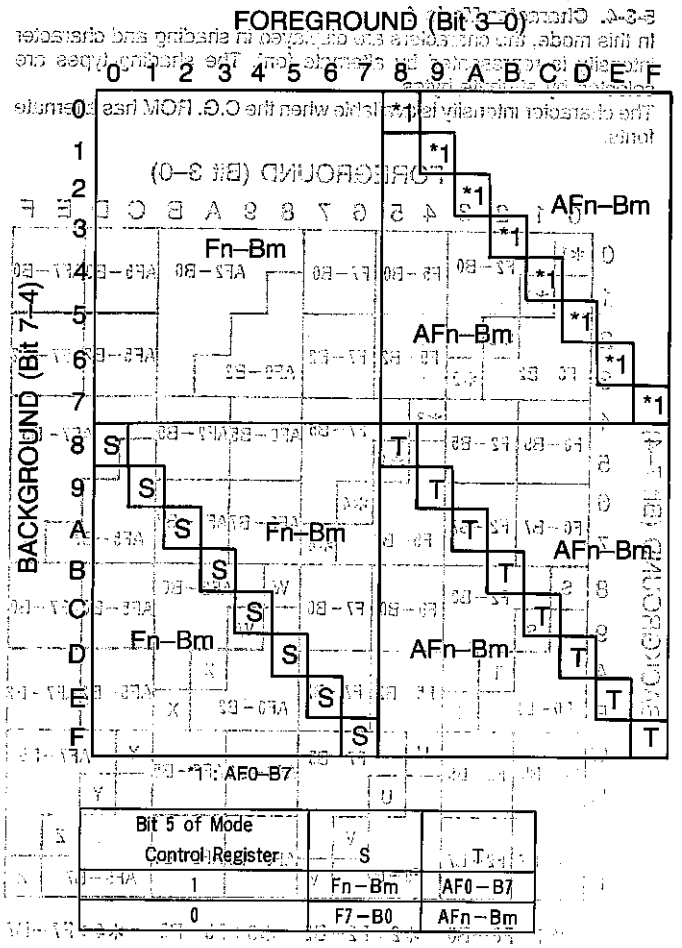
In this mode, the characters are displayed in shading and character intensity is represented by alternate font. The shading types are selected by attribute bytes.
The character intensity is available when the C.G. ROM has alternate fonts.



Bit 5 of Mode Control Register	S	T	U	V	W	X	Y	Z
1	F0–B0	F2–B2	F5–B5	F7–B7	AF2–B0	AF2–B0	AF7–B5	AF7–B5
0	F0–B2	F0–B2	F5–B7	F5–B7	AF0–B0	AF2–B2	AF5–B5	AF7–B7

Figure 5-12. Character mode 4 (4-shade mode)

Fn–Bm	F	Foreground
	B	Background
	n	Shading Number of Foreground
	m	Shading Number of Background
AFn–Bm	A	Alternate Font



Bit 5 of Mode Control Register	S	T
1	Fn–Bm	AF0–B7
0	F7–B0	AFn–Bm

Fn–Bm	F	Foreground
	B	Background
	n	Shading Number of Foreground
	m	Shading Number of Background
AFn–Bm	A	Alternate Font

Figure 5-13. Character mode 4 (8-shade mode)

5-3-5. Graphics Mode

MSB						LSB		
7	6	5	4	3	2	1	0	Bit Position
C1	C0	C1	C0	C1	C0	C1	C0	Attribute
1st		2nd		3rd		4 t h		Dot Position

Figure 5-13. 320 × 200 graphics bit mapping

In 320×200 graphics mode, 1 byte in the video RAM represents 4 dots on the LCD.
Each 2-bit of the attribute indicates the condition of each dot.
When the bit 2 of the mode control register is a 0 (color mode), 2 types of shading are available. One is the 3-shade mode and the other is the 4-shade mode. The input of the MODE0 pin selects the shading modes.
When the MODE0 is a 0, the 3-shade mode is selected. When the MODE0 is a 1, the 4-shade mode is selected

C1	C0	Dot Condition
0	0	□□
0	1	■■
1	0	■■
1	1	■■

Monochrome Mode

C1	C0	Dot Condition
0	0	□□
0	1	■□
1	0	□■
1	1	■■

3-Shade Mode

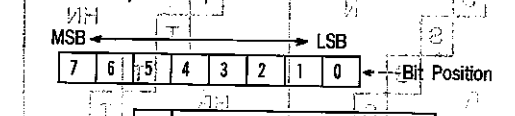
C1	C0	Dot Condition
0	0	□□
0	1	□■ (Half Tone)
1	0	■□
1	1	■■

4-Shade Mode

Figure 5-15. 320 × 200 graphics mode dot conditions

■ Dot is 'off' □ Dot is 'on'

640×200 Graphics Mode



Bit	Dot Condition
0	□
1	■

Figure 5-16. 620 × 200 graphics mode dot conditions

■ Dot is 'off' □ Dot is 'on'

In this mode, 1 byte in the video RAM represents 8 dots on the LCD. MSB of the display data is left most dot on the screen, and LSB is right most dot on the screen.
When the bits of the display data are 1, the dots are 'on'.
When the bits of the display data are 0, the dots are 'off'.

5. INTERNAL REGISTERS

5-1. MN1288 Address Register and Data Registers

These I/O addresses are used to access the MN1288 registers. When these I/O addresses are accessed, the CRTCS falls to low level.

5-2. Mode Control Register

This is a 2-bit write only register. This register controls video outputs and blinking.

BITS	Function
7~6	Not Used
5	Blink Enable
4	Not Used
3	Video Enable
2~0	Not Used

Figure 5-1. Mode control register

Bit 5 Blink Enable
When this bit is set to 1 (0), the bit 7 of attribute data functions as a blink (background intensity) bit.

Bit 3 Video Enable
When this bit is set to 1, display data are enabled to output.

5-3. Status Register

This is a 2-bit read only register. This register shows display conditions.

BITS	Function
7~4	Not Used
3	Video Signal Check
2~1	Not Used
0	Horizontal Retrace Period

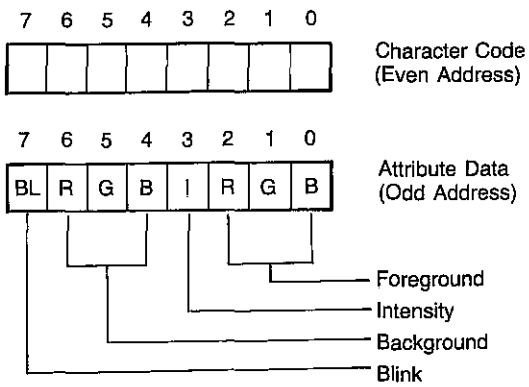
Figure 5-2. Status register

Bit 3 Video Signal Check
This bit has the value of video data.

Bit 0 Horizontal Retrace Period
This bit become 'H' during horizontal retrace period.

6. DISPLAY FUNCTIONS

Every character position is defined by two bytes in the video RAM. The character code must be an even address, and the attribute data must be an odd address in the video RAM.



6-1. LCD Mode

In the LCD mode, there are 4 types of display conditions according to the attribute data as below. The MODE1 and the MODE0 control the character modes.

MODE1	MODE0	Display Conditions	
		R.G.B Bits	1 bit
0	0	Mode 1	Alternate Font
0	1	Mode 1	Shading
1	0	Mode 2	Alternate Font
1	1	Mode 2	Shading

Figure 6-3. Character display format in the LCD mode

Notes:

1. Alternate Font
When the MODE0 is 'L' and the 1 bit is 'H', the MN1292 outputs high level to the CC8 (address bit of C.G. ROM). It changes the character font patterns to the alternate font.

2. Shading
When the MODE0 is 'H' and the 1 bit is 'H', the character is displayed in half-tone.

7. OPERATION

7-1. Display Operation

7-1-1. CRT (CRT/LCD='H')
In the CRT mode, the addresses from the MN1288 are latched by CRTRAS and CRTCAS signals. Their addresses are RAS address and CAS address respectively. The MN1292 uses a page mode to access the DRAM. The data from the DRAM flow into the MD7~MD0. The first data is a character code and the next is an attribute data.
The character data are transfered to the C.G. ROM through the CC7~CC0. The CC8 data has the same value as the RA3 from the MN1288. The CC8~CC0 addresses the C.G. ROM which then outputs the character dot pattern data to the MN1292 through RD7~RD0.
The timing diagram is shown in Figure 7-7.

7-1-2. LCD (CRT/LCD='L')
In the LCD mode, the CRTRAS and CRTCAS signals control RAS address and CAS address respectively as same as the CRT mode. The character codes are transfered to the CC7~CC0. The CC8 is always at low level except when MODE0 is 'L' and the intensity bit (bit 3 of the attribute code) is 'H'. (See display functions in the LCD mode) The C.G. ROM outputs the character dot pattern according to the C.G. ROM address (CC8~CC0). These patterns are transfered to RD7~RD0 of the MN1288.
The attribute data are decoded in the MN1292 and transfered to AT0 and AT1.
The shading function (half-tone) is controlled by AT1 and AT0.
The timing diagram in the LCD mode is shown in Figure 7-8.

*1 C.G. ROM Format

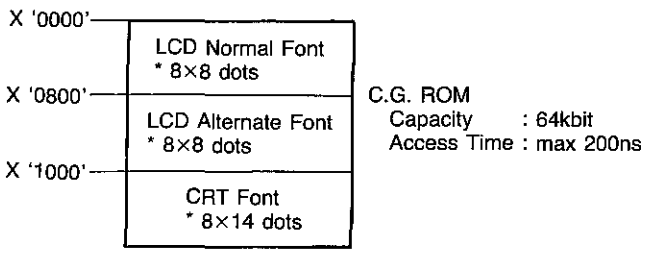


Figure 7-1. C.G. ROM format

Note: * : Character Box Size

CRT/LCD	MODE1	MODE0	CC8	ROMADR
H(CRT)	–	–	RA3	H
L(LCD)	L	L	MD3.7	L
	L	H		
	H	L	MD3.7	
	H	H	L	

* MD3 : Fore Ground Intensity bit
MD7 : Back Ground Intensity bit

Figure 7-2. CC8 and ROMADR in the various modes

*2 In the CRT mode, the 9th dot of the character font is generated by decoding the CC5~CC7 and RD0. The decoding circuit is shown in Figure 7-3.

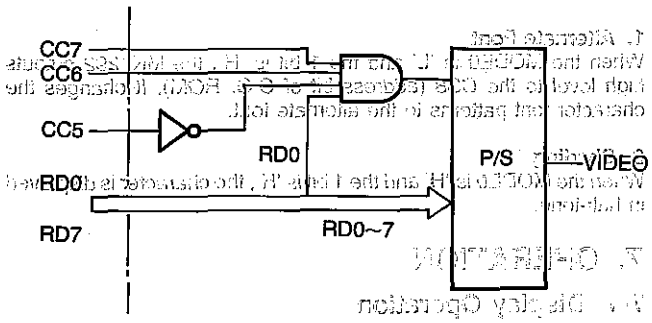


Figure 7-3. The decoding circuit in the MN1292

*3 The underline is displayed when raster address is hex 0CH in the CRT mode, and hex 07H in the LCD mode.

7-2. Video RAM access of the CPU

The MN1292 accesses the video RAM using the cycle steal technique. When the CPU accesses the video RAM, no flikers will appear in the display images of either the CRT or the LCD modes.
The video RAM access timings are shown in Figure 7-9.~7-12.

7-3. Reset Sequence

The MN1292 starts to operate when the reset is inactive.
The MN1292 synchronizes with the MN1288 (LCD/CRT Controller) and fits the video RAM access timing, memory address output timing, and data input timing.
When the operation starts, the MN1292 outputs LCDCLK to the MN1288 and the CHACLK (which is a divided by 8 signal of LCDCLK) is then fed back to the MN1292. The video RAM access signals are generated from the first falling edge of CHACLK. (Timing diagrams are shown in Figure 7-13.~7-14.)
When the display mode (CRT or LCD) is changed while the MN1292 is operating, the MN1292 will reset itself and synchronize with the MN1288 using the CHACLK.

7-4. Display Size and Operating Frequency of the MN1288

7-4-1. CRT Mode

The 720×350 dots monochrome CRT can be connected in the CRT mode.
The operating frequency of the MN1288 is calculated below.

$$\text{CRTCLK} = \frac{16.257\text{MHz}}{9} = 1.806\text{MHz}$$

The MN1292 outputs 9 bits data to the VIDEO pin during the 1 character clock period.
The values to set to the MN1288 registers are shown in Figure 7-4.

Register No.	Register Name	value to set<HEX>
R0	Horizontal Total	61
R1	Horizontal Displayed	50
R2	HSYN Position	52
R3	HSYNC/VSYNC Width	0F
R4	Vertical Total	19
R5	Vertical Total Adjust	06
R6	Vertical Displayed	19
R7	VSYNC Position	19
R8	Interlace mode & Skew	02
R9	Maximun Scan Line Address	0D
R10	Cursor Start Scan Line	0B
R11	Cursor End Scan Line	0C
R12	Start Address<H>	00
R13	Start Address<L>	00
R14	Cursor Address<H>	00
R15	Cursor Address<L>	00
R16	Light Pen<H>	–
R17	Light Pen<L>	–

Figure 7-4. The values to set to the MN1288

The display size calculated by the values of Figure 7-4 is shown in Figure 7-5.

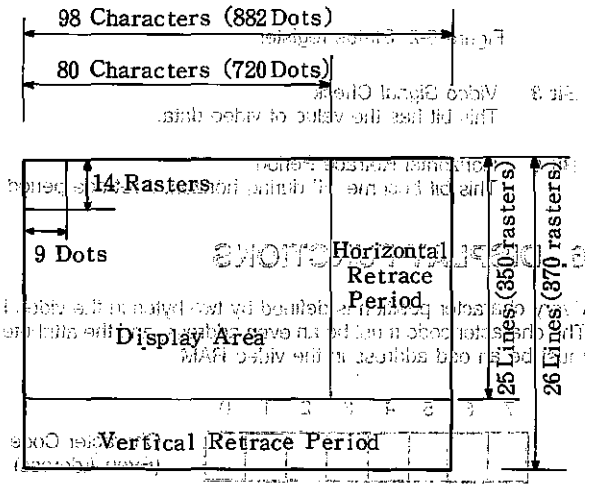


Figure 7-5. Display size in CRT mode

$$\text{Horizontal Frequency} = \frac{1.806\text{MHz}}{98} = 18.43\text{KHz}$$

$$\text{Vertical Frequency} = \frac{18.43\text{KHz}}{370} = 49.8\text{Hz}$$

The underline is displayed when the raster address is hex 0CH. The underline is overlapped by cursor when the values in Figure 7-4. are set to the MN1288 registers.

7-4-2. LCD Mode

The 640×200 dots LCD panel can be connected.
The operating frequency of the MN1288 is calculated as follows.

1-Panel LCD
LCDCLK=16.257MHz×2/3=10.84MHz
CHACLK=10.84MHz / 8=1.355MHz
2-Panel LCD
LCDCLK=16.257MHz×2/3÷2=5.42MHz
CHACLK=5.42MHz / 8=677.5KHz

The values to set to the MN1288 registers are the same as CRT mode. (Figure 7-4) When the VPLMT is 'H', the number of vertical raster is 200 rasters.
The ROMADR signal controls the character font patterns.

The display size calculated by the values of Figure 7-4 is shown in Figure 7-6.

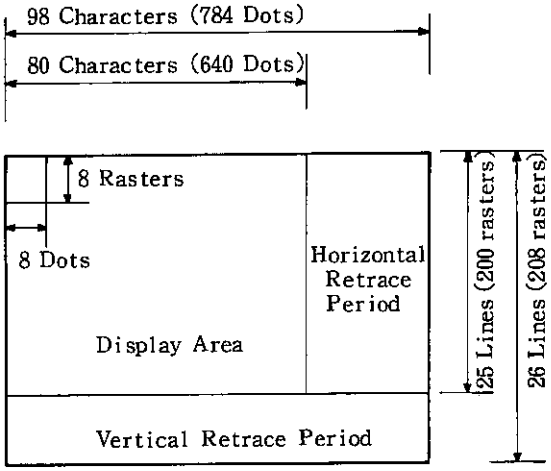


Figure 7-6. Display size in the LCD mode

The frame frequency=66.5Hz
The underline is displayed when the raster address is hex 07H.
The underline is overlapped by cursor when the values in Figure 7-4 are set to the MN1288 registers.

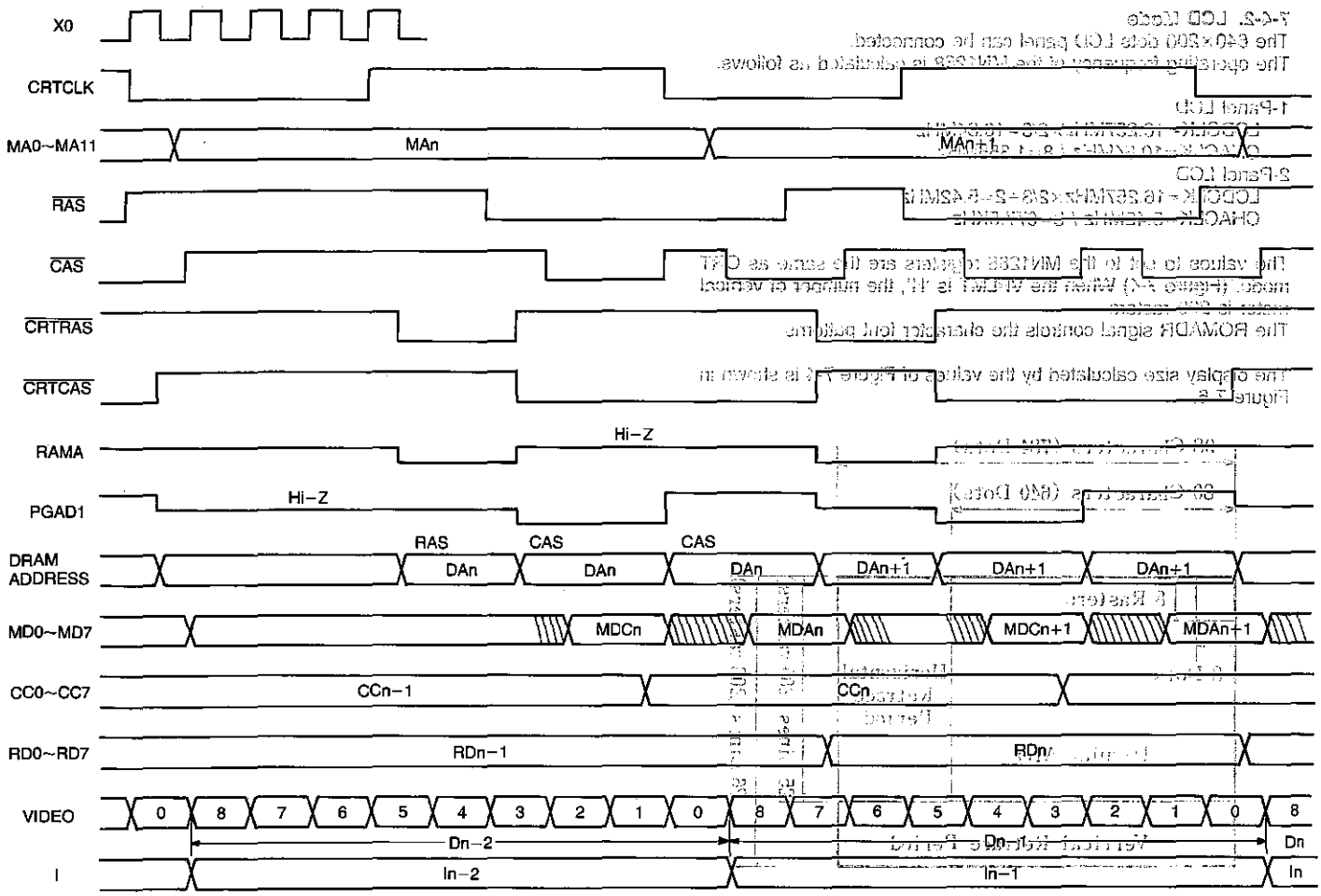


Figure 7-7. Timing diagram in the CRT mode

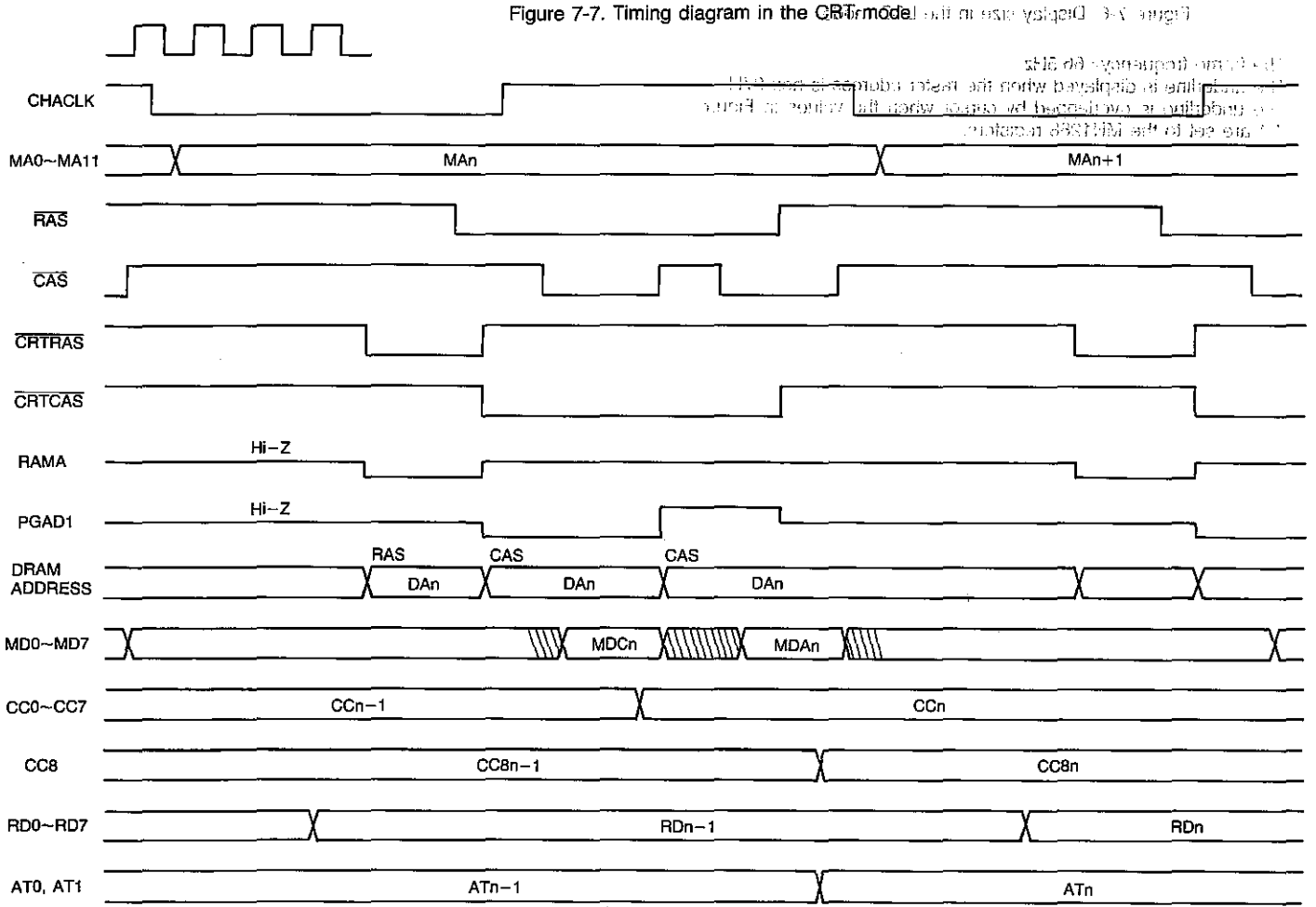


Figure 7-8. Timing diagram in the LCD mode

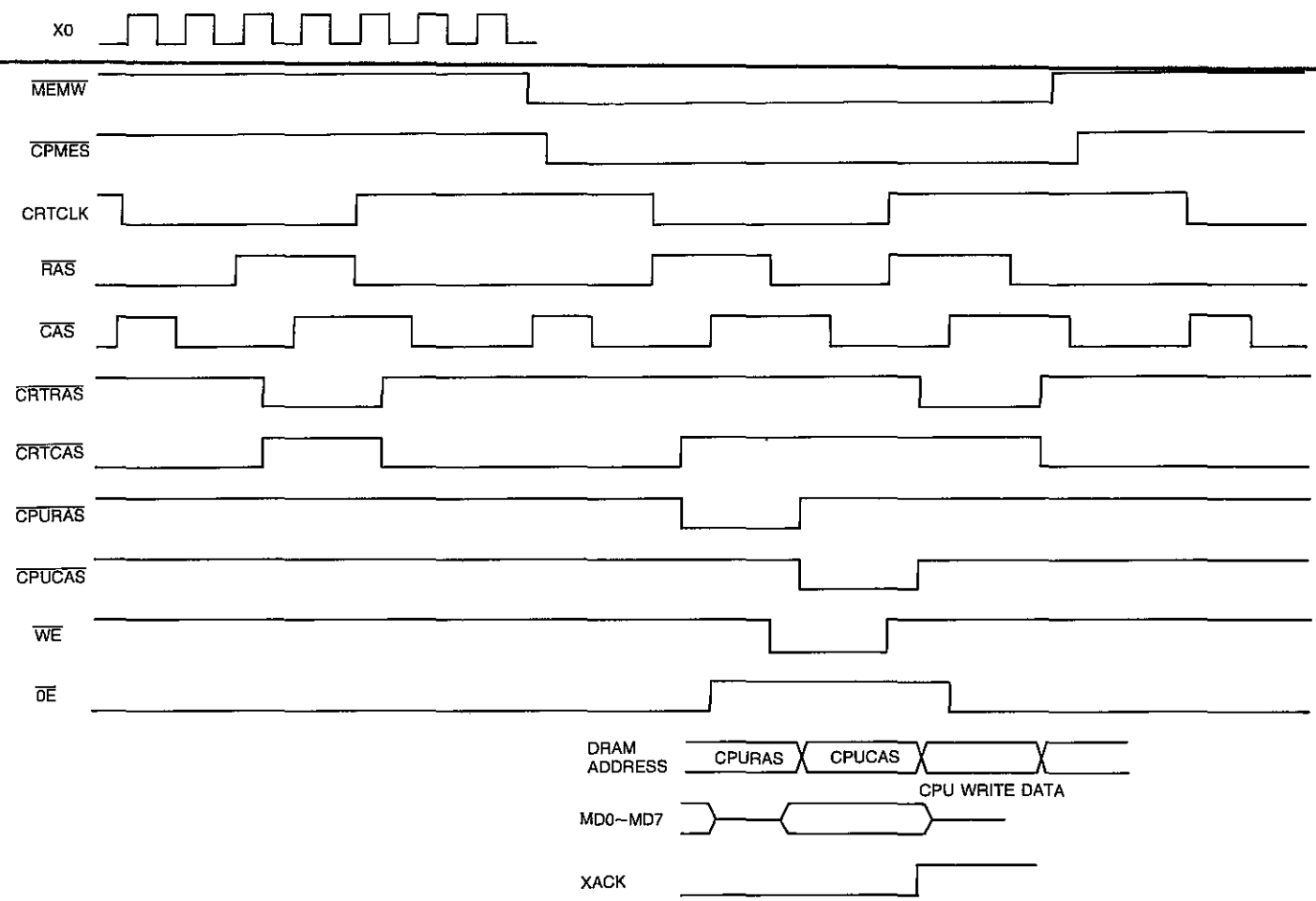


Figure 7-9. Video RAM access by the CPU in the CRT mode (Write)

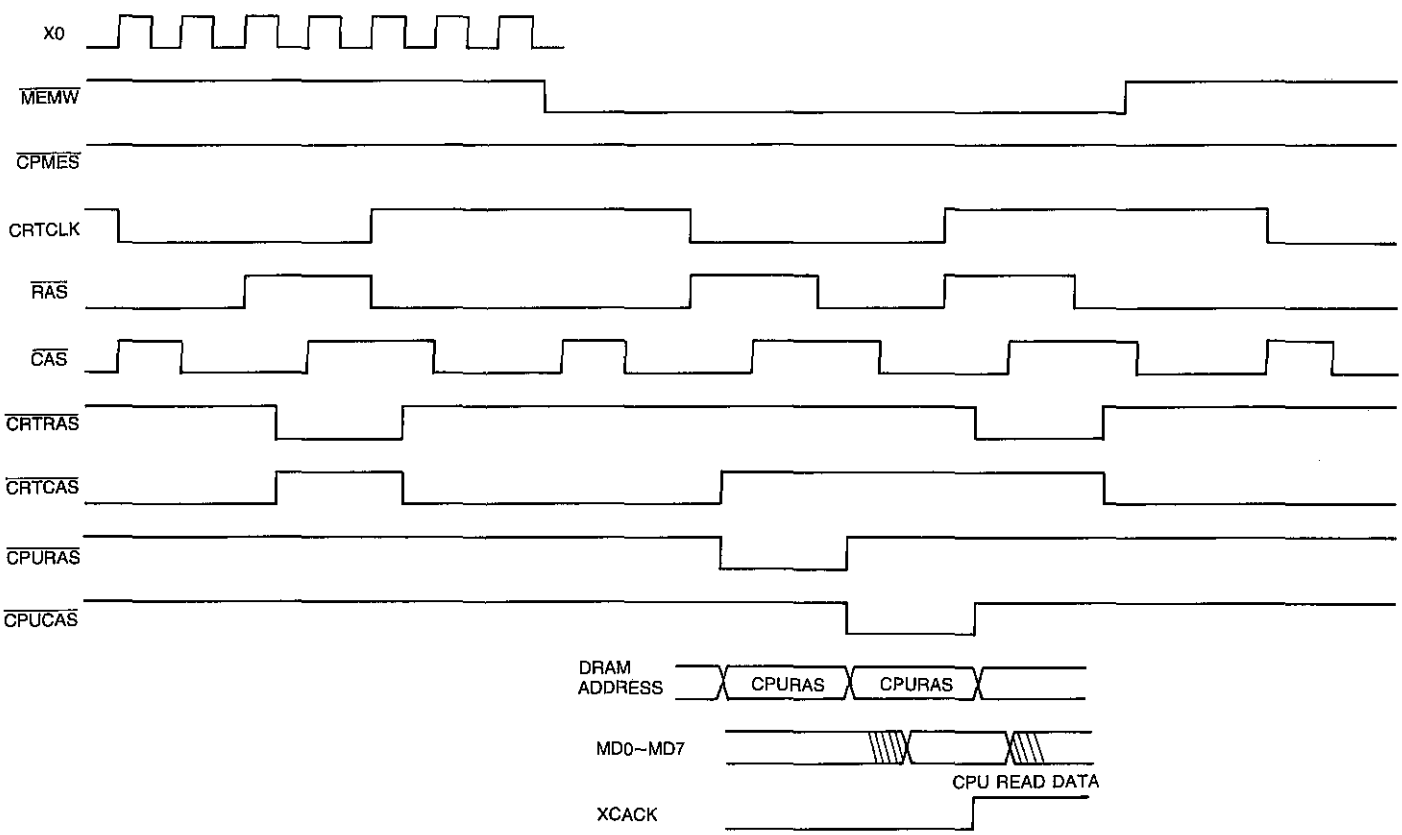


Figure 7-10. Video RAM access by the CPU in the CRT mode (Read)

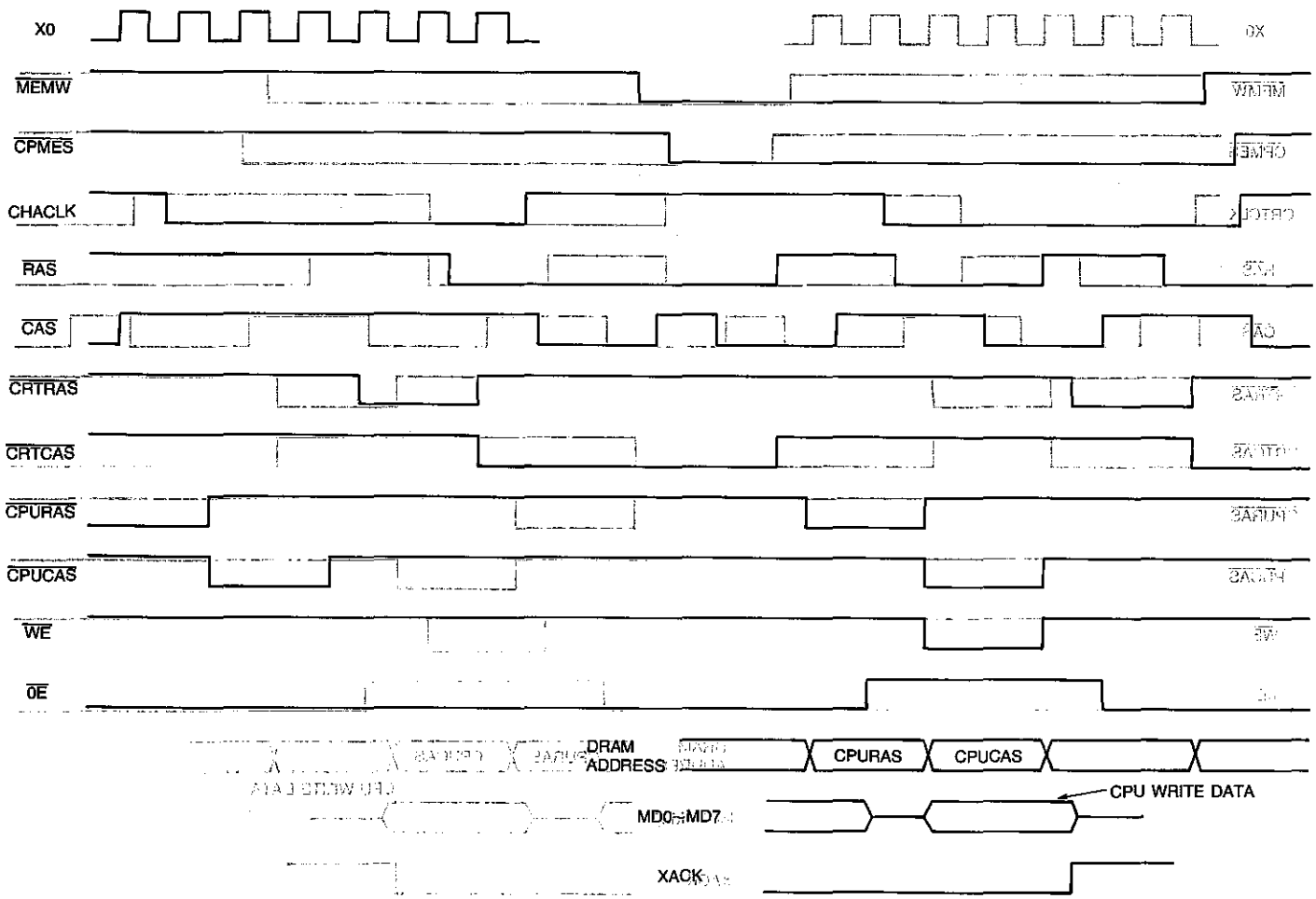


Figure 7-11. Video RAM access by the CPU in the LCD mode (Write)

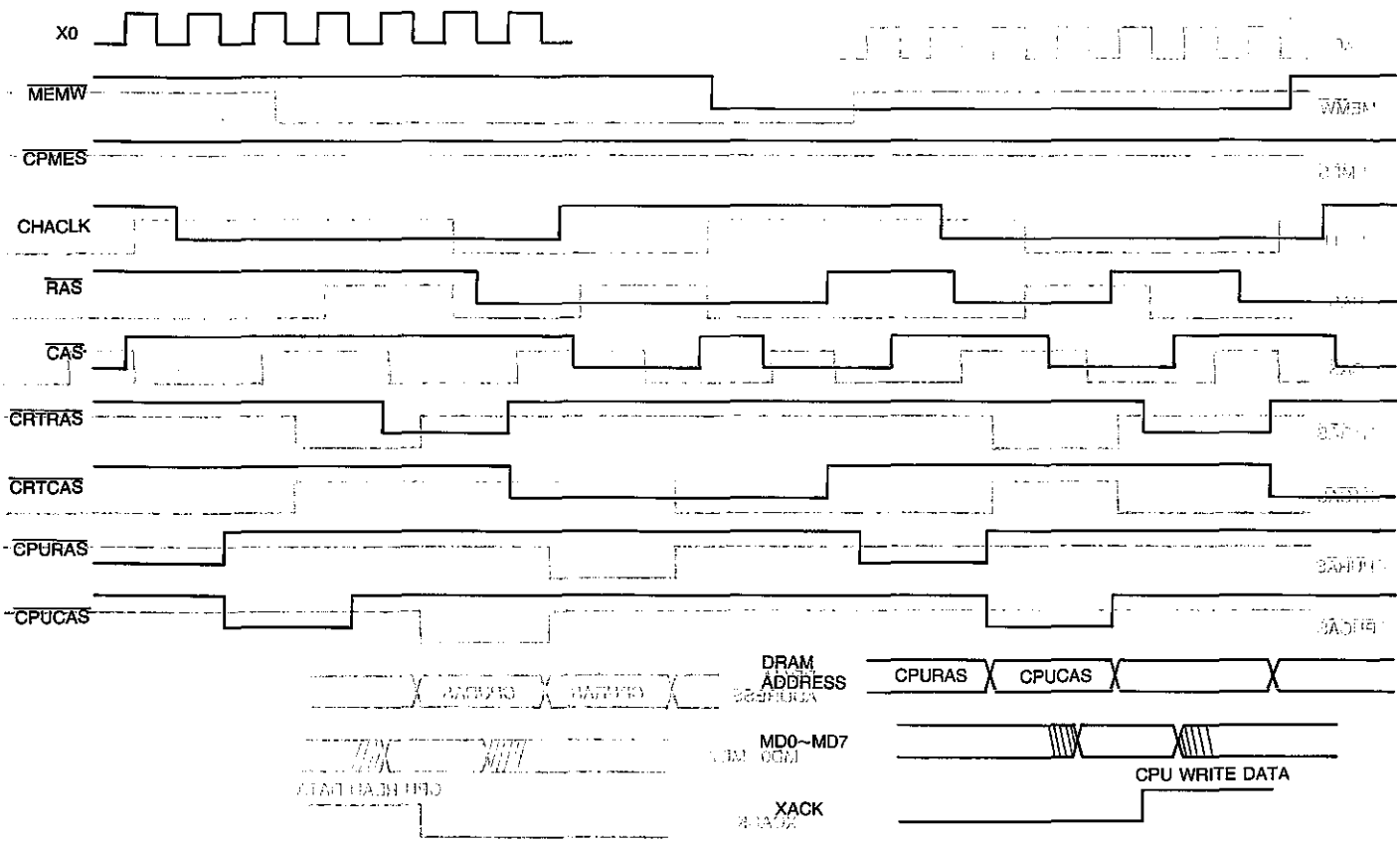


Figure 7-12. Video RAM access by the CPU in the LCD mode (Read)

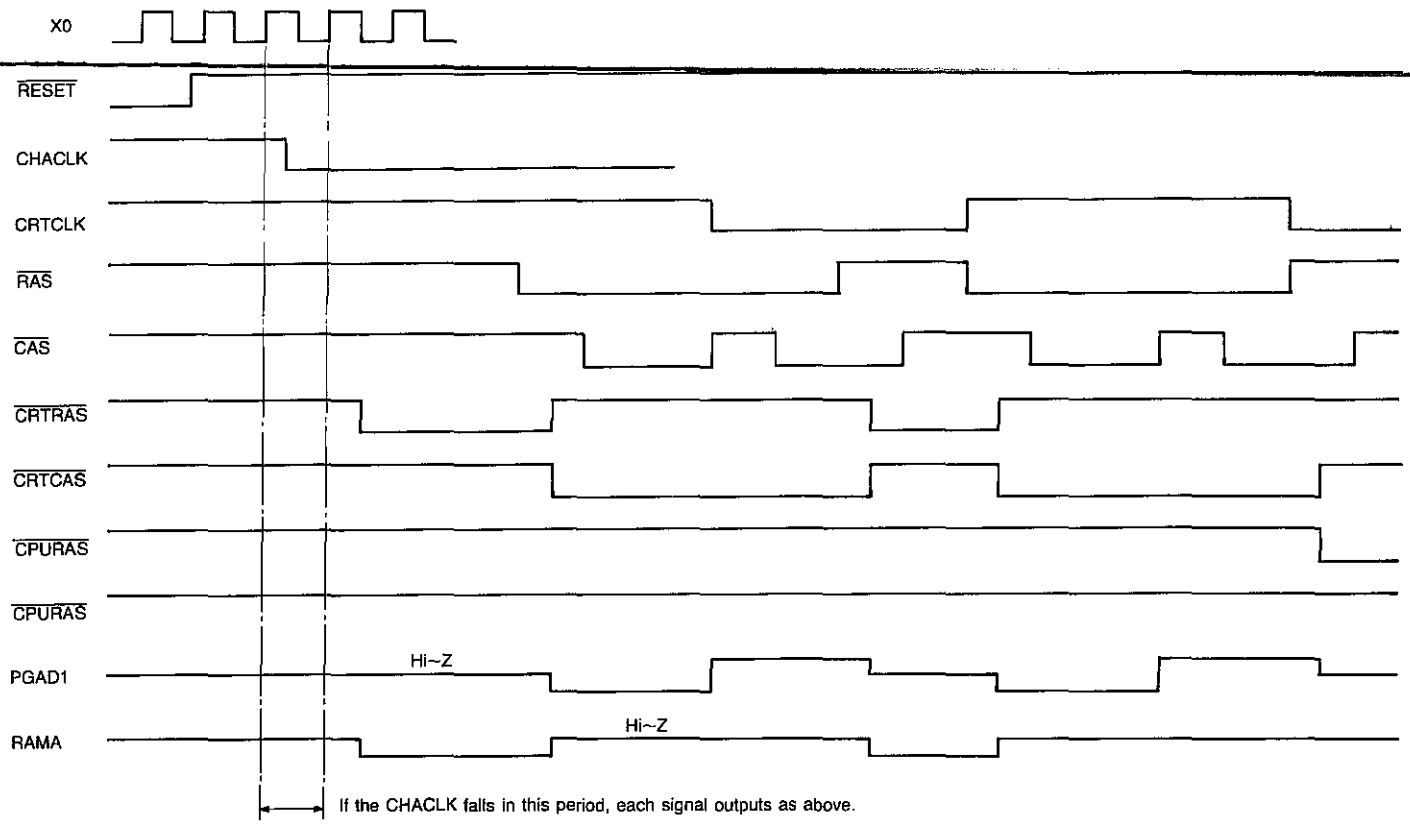


Figure 7-13. Reset sequence in the CRT mode

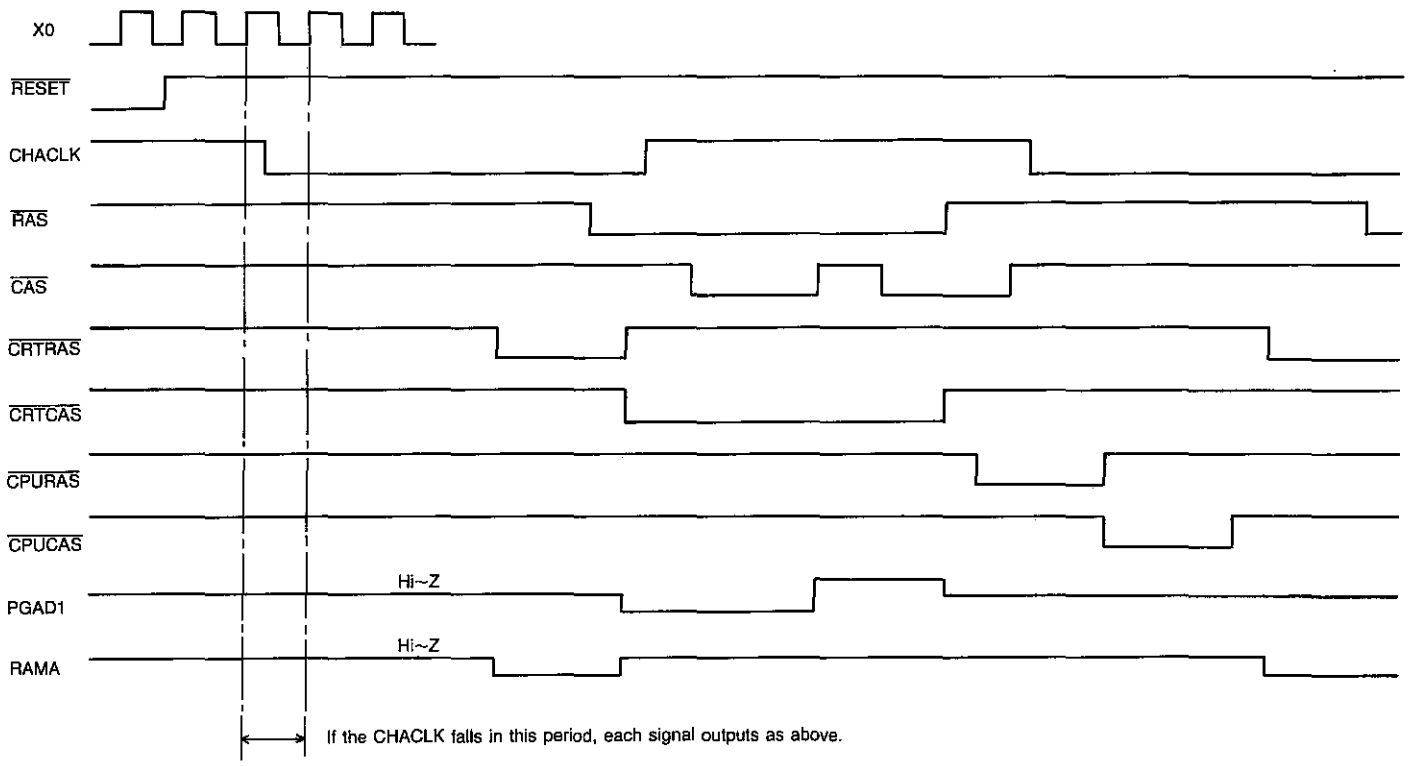
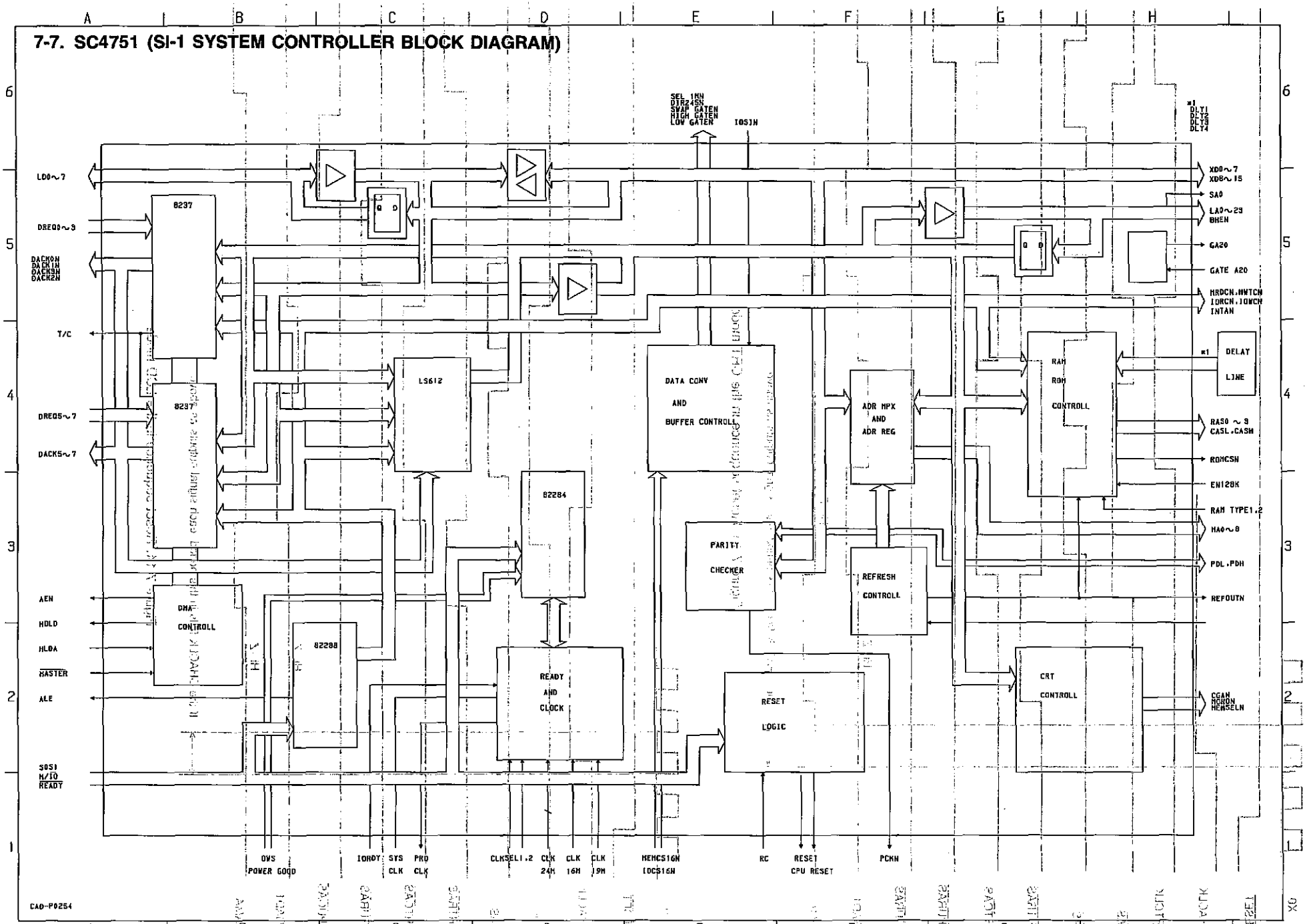
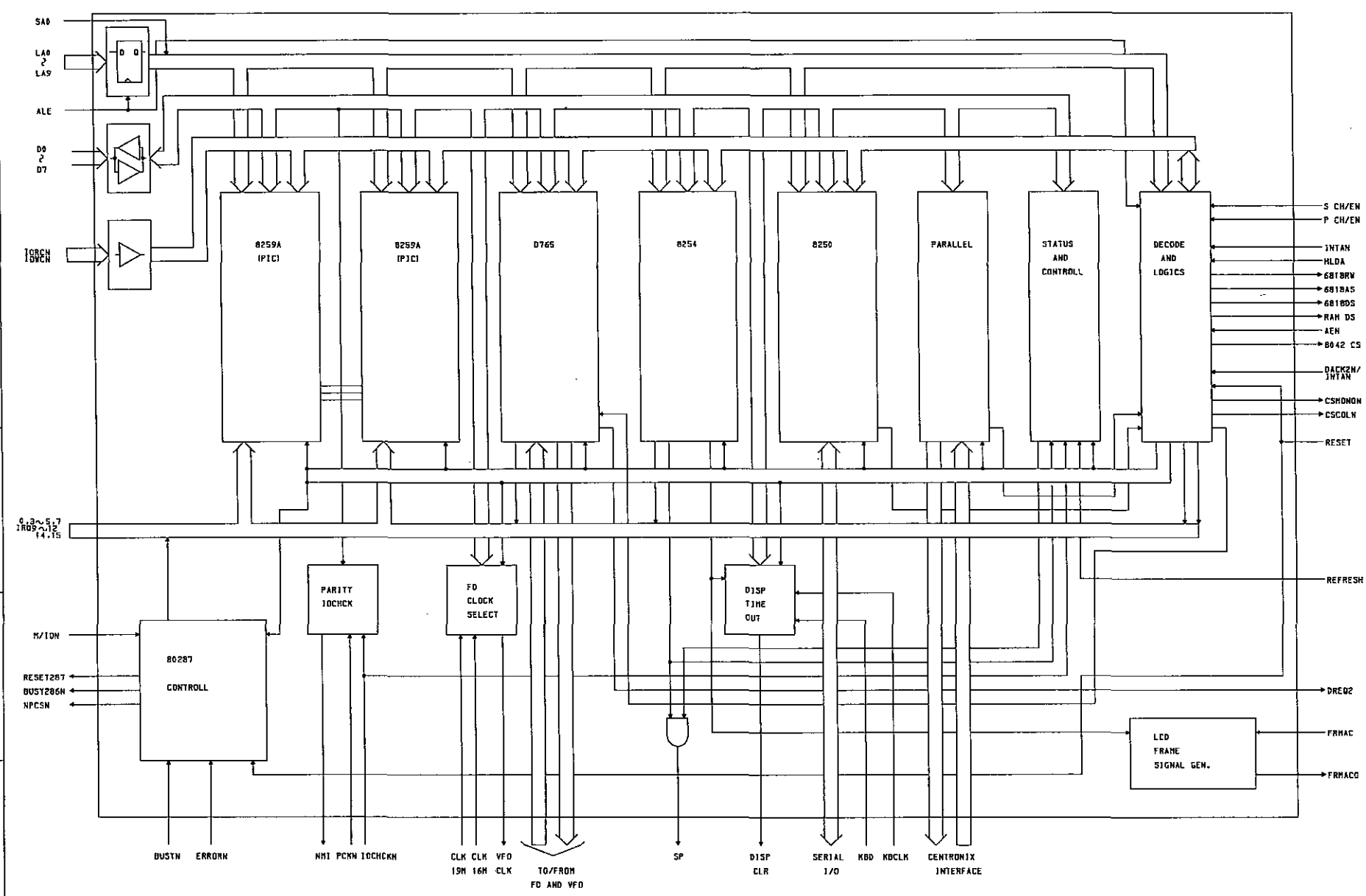


Figure 7-14. Reset sequence in the LCD mode

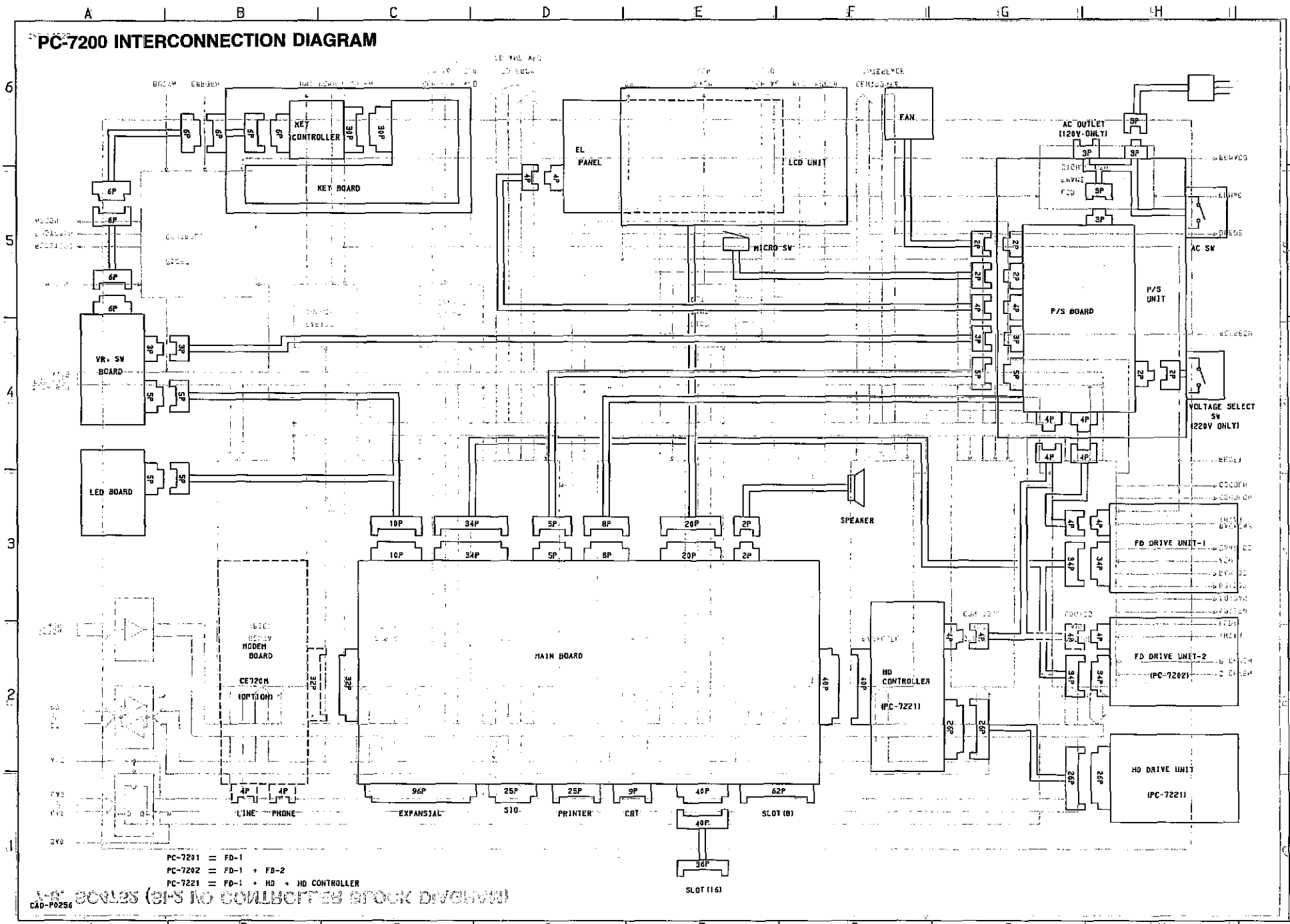
7-7. SC4751 (SI-1 SYSTEM CONTROLLER BLOCK DIAGRAM)



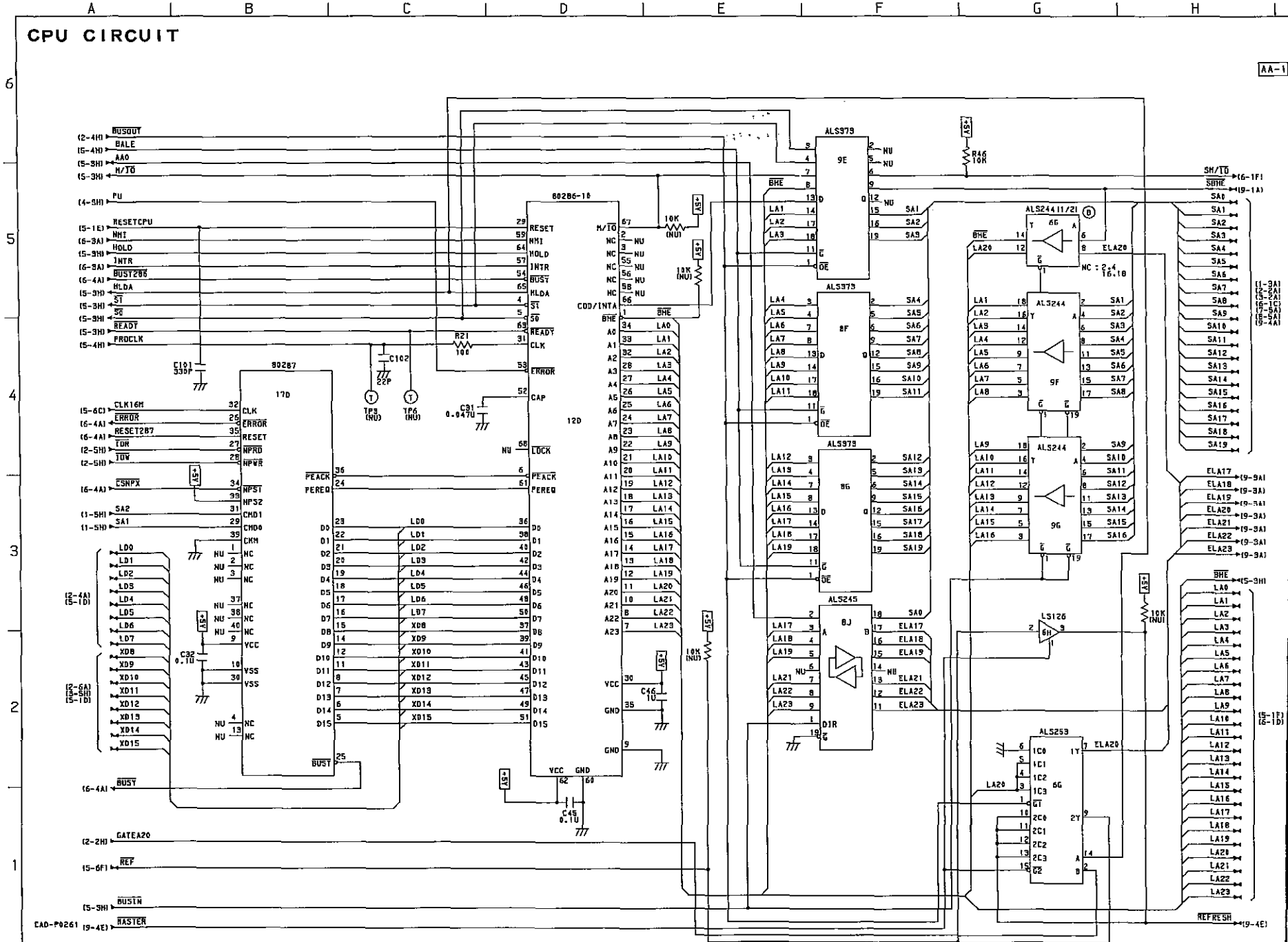
7-8. SC4752 (SI-2 I/O CONTROLLER BLOCK DIAGRAM)



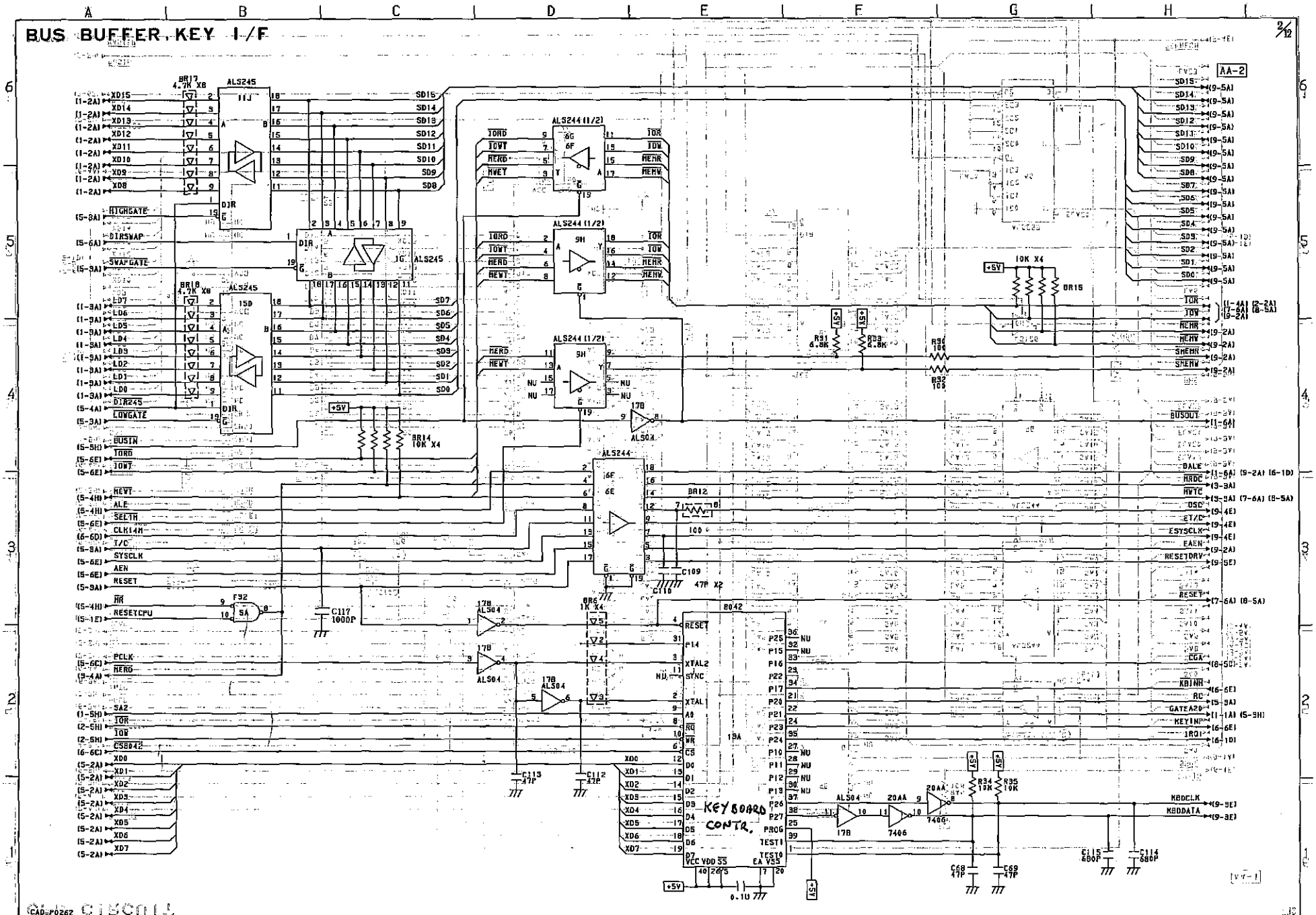
PC-7200 INTERCONNECTION DIAGRAM



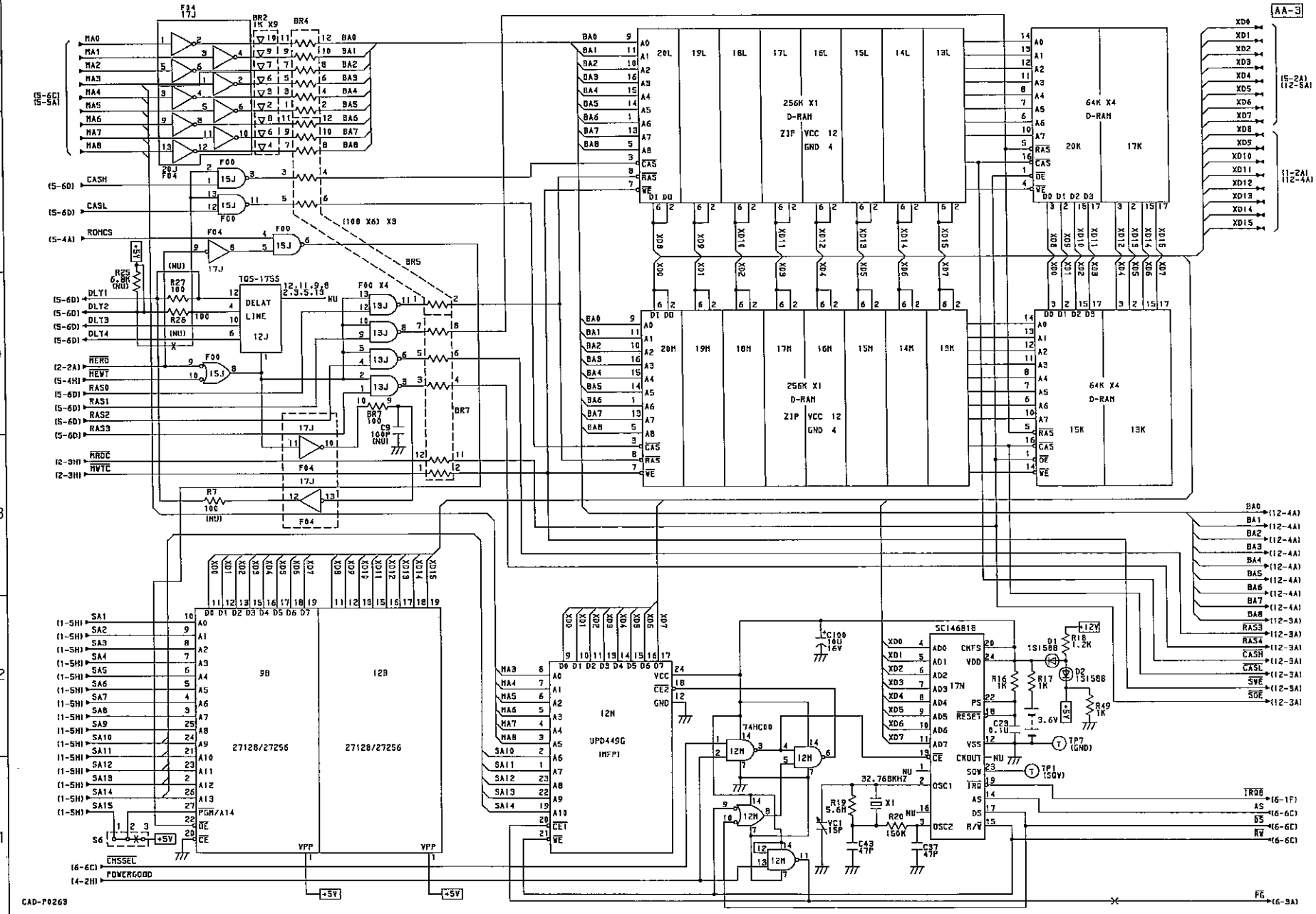
CPU CIRCUIT

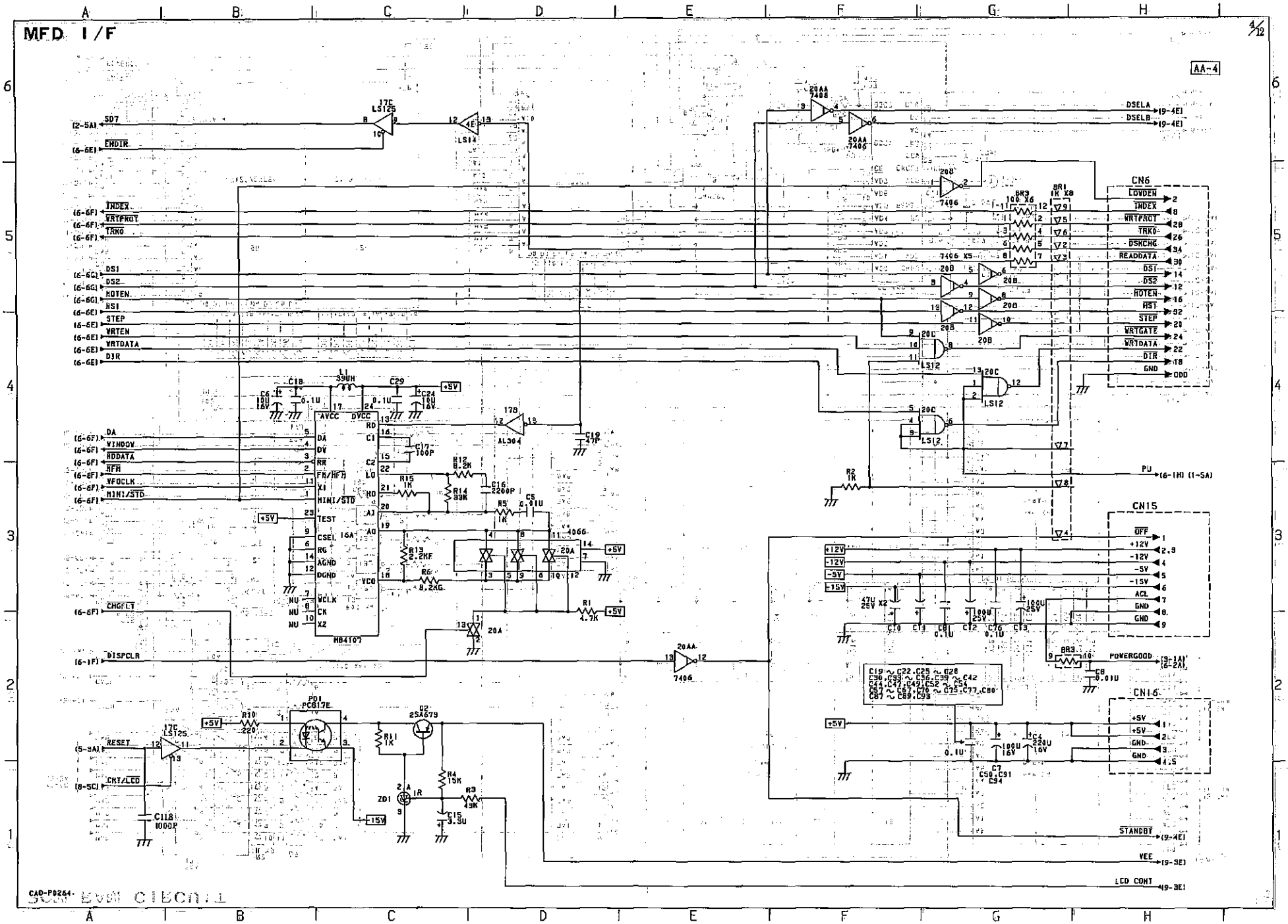

80286-10
80287
ALS373
ALS244
ALS245
ALS253
LS126
BUSOUT
BALE
AA0
M/IO
PU
RESETCPU
NMI
HOLD
INTR
BUST286
HLDA
ST
SO
READY
PROCLK
CLK16M
ERROR
RESET287
IOR
IOW
CSNPX
BUSY
GATEA20
REF
BUSIN
MASTER
CAD-P0261
REFRESH
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SA19
LA0
LA1
LA2
LA3
LA4
LA5
LA6
LA7
LA8
LA9
LA10
LA11
LA12
LA13
LA14
LA15
LA16
LA17
LA18
LA19
LA20
LA21
LA22
LA23
ELA17
ELA18
ELA19
ELA20
ELA21
ELA22
ELA23
BHE
R46 10K
R21 100
C101 330P
C102 22P
C31 0.047U
C32 0.1U
C45 0.1U
C46 10U
10K (NU)
TP3 (NU)
TP6 (NU)

BUS BUFFER, KEY I/F

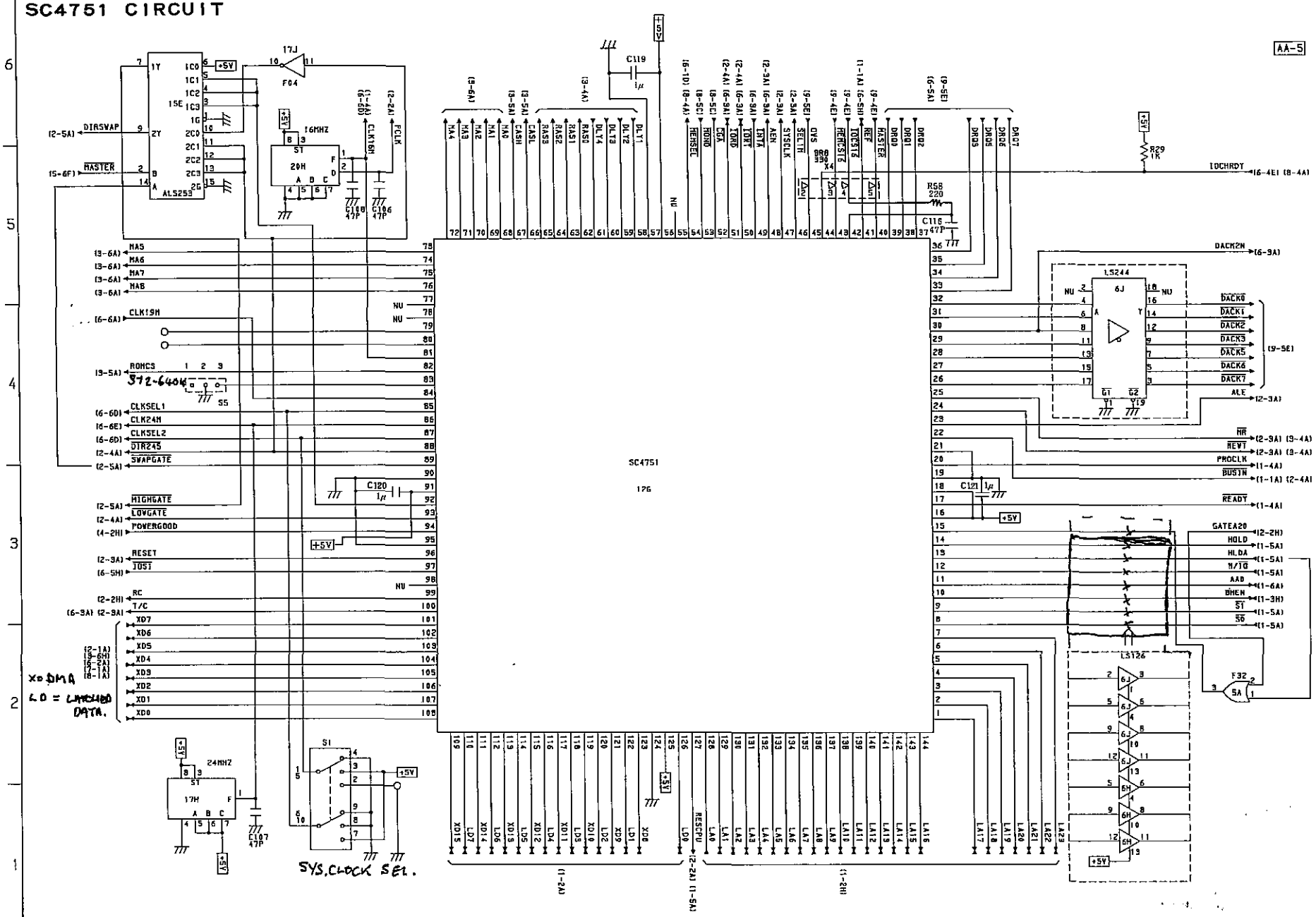


ROM, RAM CIRCUIT

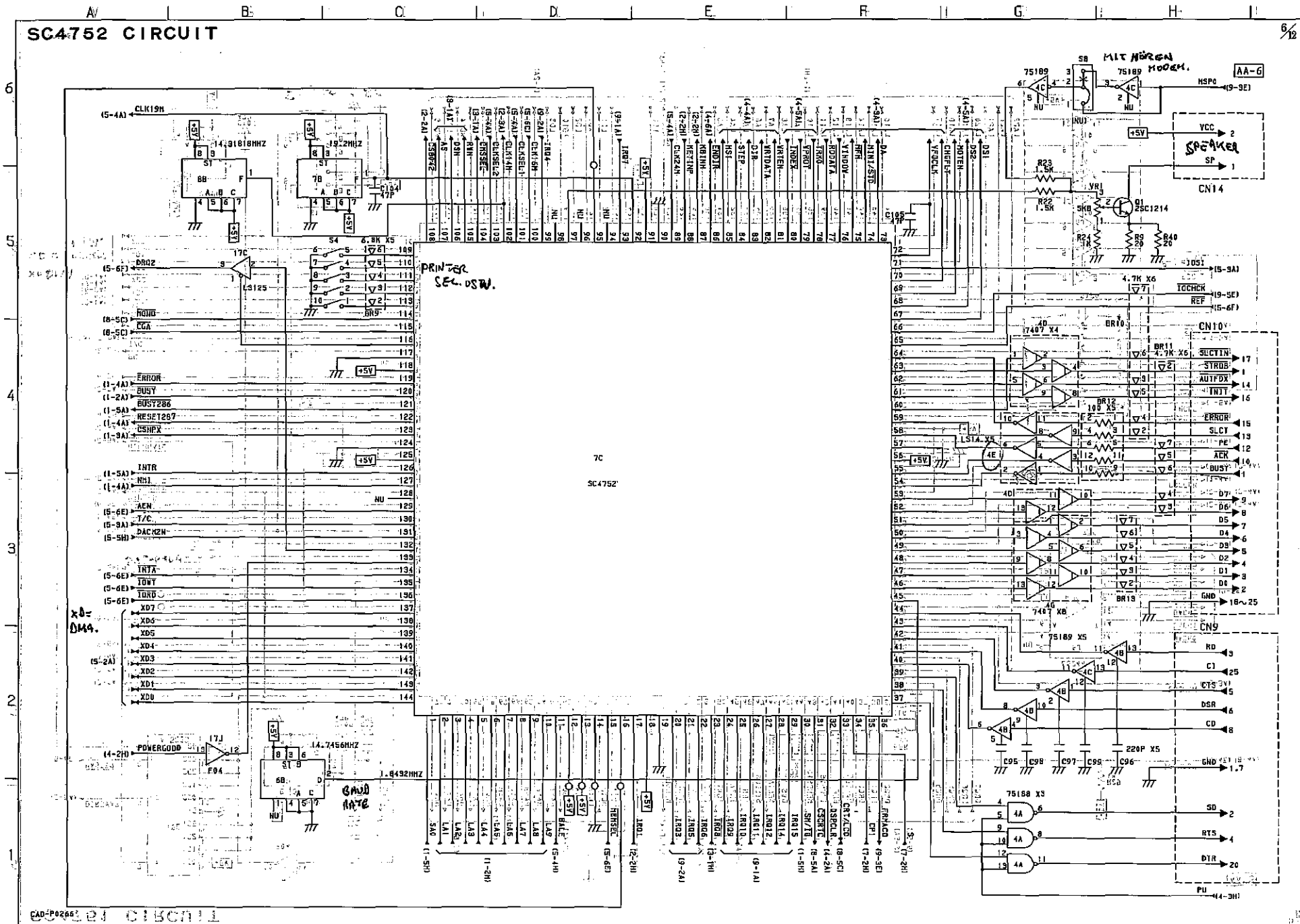



MFD I/F
4/12
AA-4
CN6
CN15
CN16
SD7
ENDIR
INDEX
WRTPROT
TRK0
DSI
DS2
MOTEN
HSI
STEP
WRTEN
WRTDATA
DIR
DA
WINDOW
RDDATA
HFH
VFOCLK
MINI/STD
CHGFLT
DISPCLR
RESET
CRT/LCD
DSELA
DSELB
DSKCHG
READDATA
WRTGATE
GND
PU
OFF
+12V
-12V
-5V
-15V
ACL
POWERGOOD
STANDBY
VEE
LCD CONT
MB4107
PC817E
2SA679
AL304
LS125
LS14
LS12
7406
7408
4066
CAD-P0264

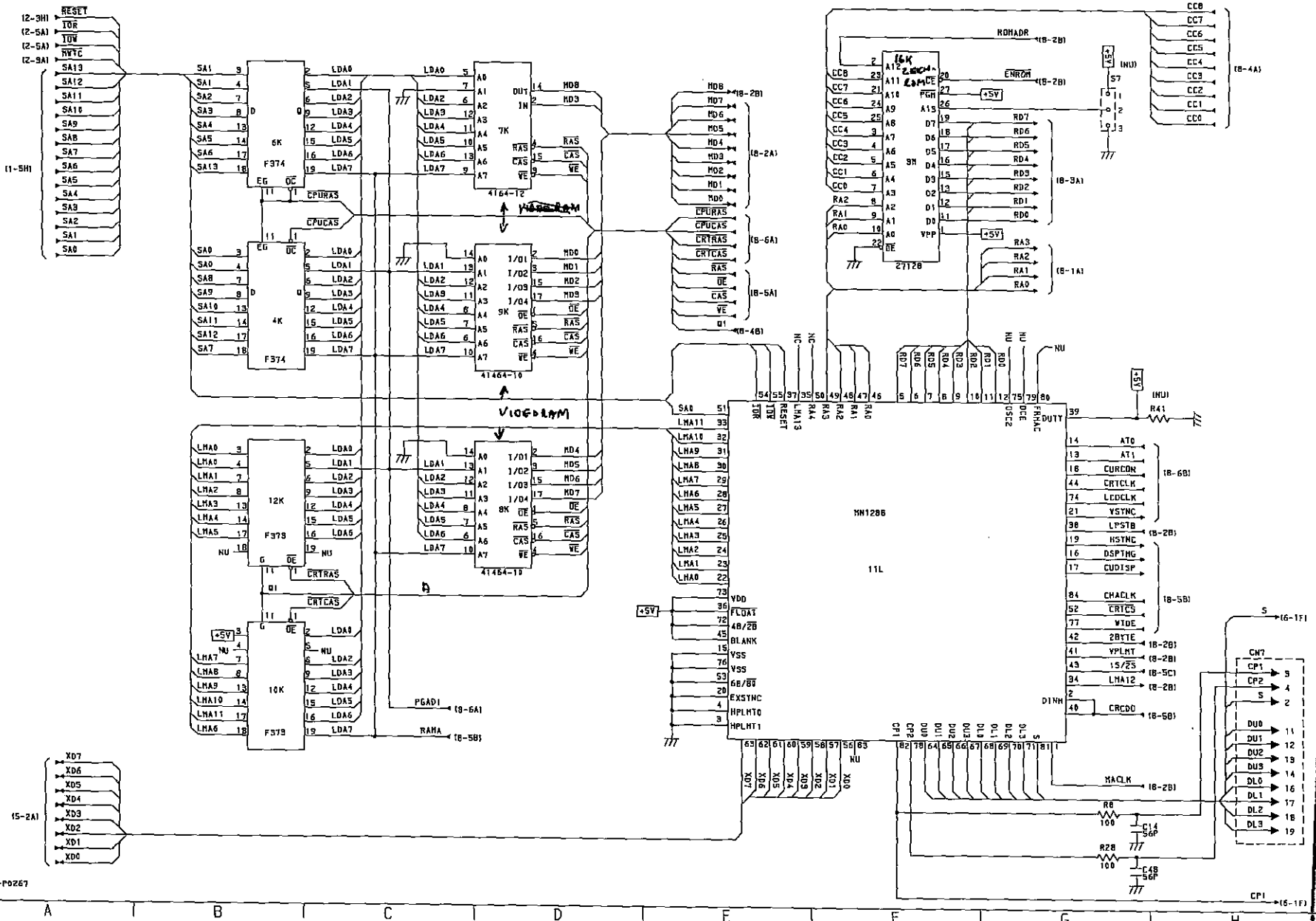
SC4751 CIRCUIT

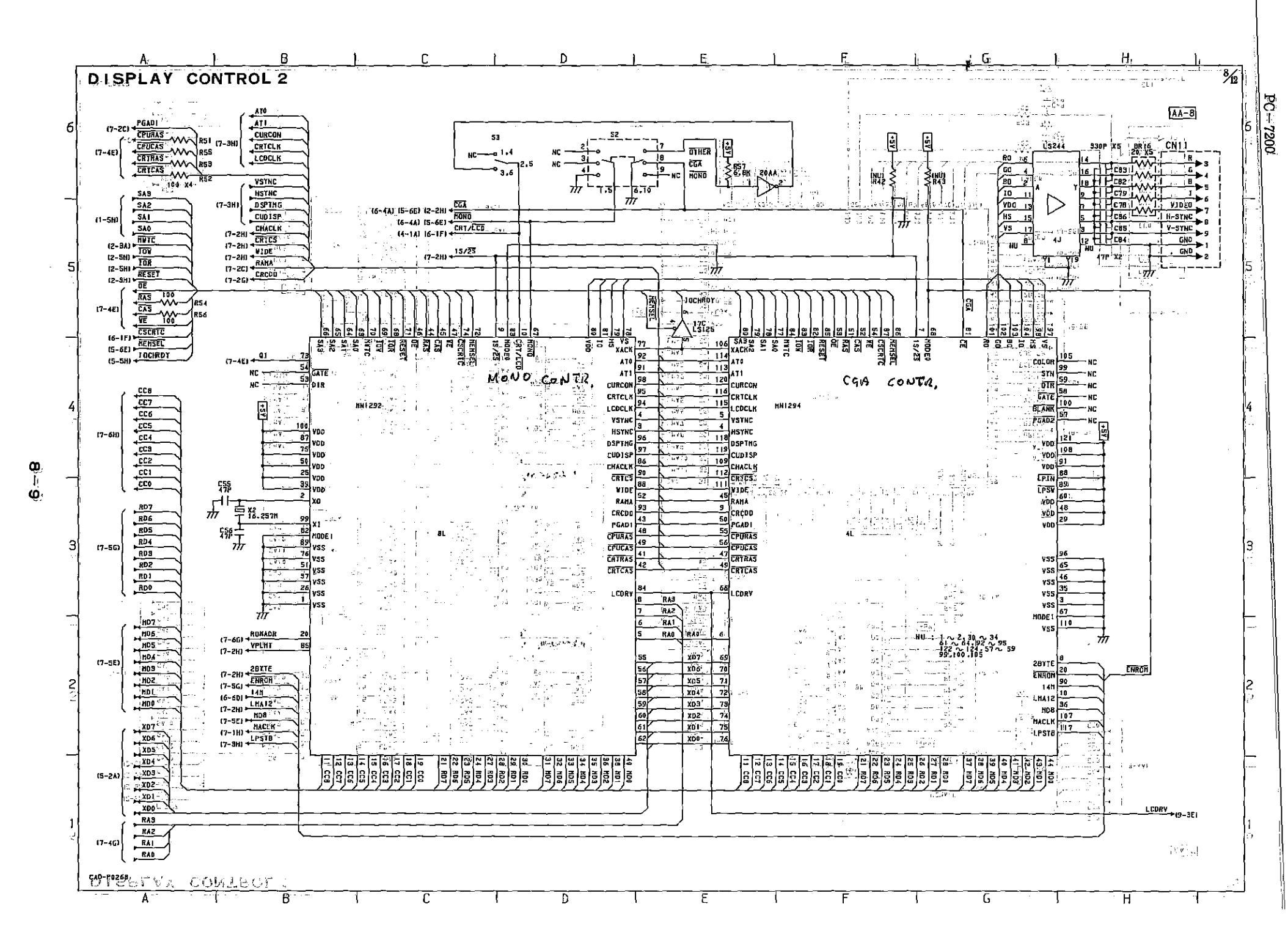


SC4752 CIRCUIT



DISPLAY CONTROL 1



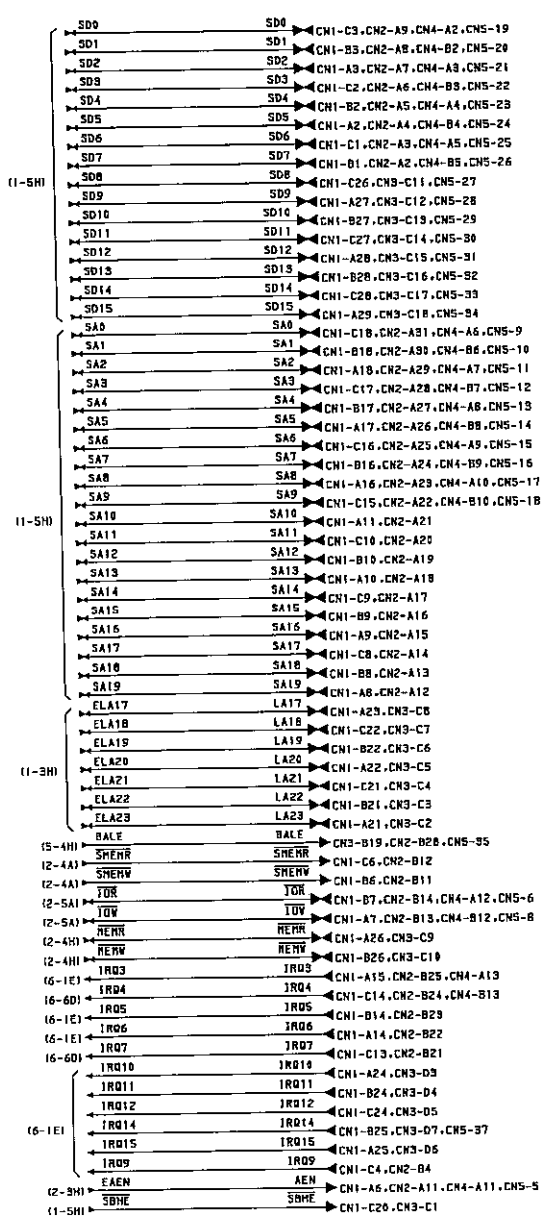

DISPLAY CONTROL 2
8/12
AA-8
MONO CONTR.
CGA CONTR.
HN1292
HN1294
8L
4L
S3
S2
LS244
930P X5
CN11
R51
R55
R53
R52
R54
R56
R57
20AA
CS5 47P
CS6 47P
X2 16.257M
17C LS125
PGADI
CPURAS
CPUCAS
CRTRAS
CRTCAS
VSYNC
HSYNC
DSPTMG
CUDISP
CHACLK
CRTCS
WIDE
RAMA
CRCDD
RESET
IOCHRDY
RENSEL
CGA
MOND
CRT/LCD
LCDRV
ENROM
2BYTE
14M
LHA12
MD8
HACLK
LPSTB
VPLHT
ROMADR
R
G
B
I
VIDEO
H-SYNC
V-SYNC
GND
NU
DISPLAY CONTROL 2

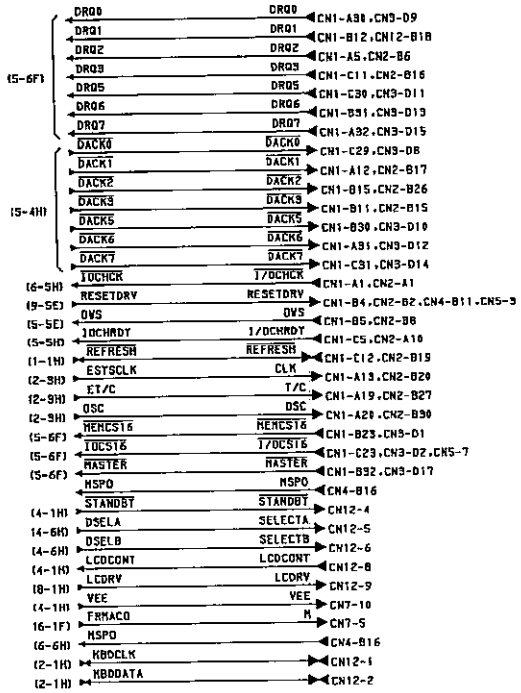
PC-7200

6-8

LINE CONNECTION

AA-9





CAD-F0269

CONNECTOR TABLE 1

AA-110

1. Expansion I/O Bus

Pin NO	Signal	Pin NO	Signal	Pin NO	Signal
A1	I/OCHCK	B1	SD7	C1	SD6
A2	SD5	B2	SD4	C2	SD3
A3	SD2	B3	SD1	C3	SD0
A4	GND	B4	RESETDRV	C4	IRQ9
A5	DRQ2	B5	OWS	C5	I/OCHRDY
A6	AEN	B6	SMEMW	C6	SMEMR
A7	IOW	B7	IOR	C7	GND
A8	SA19	B8	SA18	C8	SA17
A9	SA16	B9	SA15	C9	SA14
A10	SA13	B10	SA12	C10	SA11
A11	SA10	B11	DACK3	C11	DRQ3
A12	DACK1	B12	DRQ1	C12	REFRESH
A13	CLK	B13	GND	C13	IRQ7
A14	IRQ6	B14	IRQ5	C14	IRQ4
A15	IRQ3	B15	DACK2	C15	SA9
A16	SA8	B16	SA7	C16	SA6
A17	SA5	B17	SA4	C17	SA3
A18	SA2	B18	SA1	C18	SA0
A19	T/C	B19	BALE	C19	GND
A20	OSC	B20	GND	C20	SBHE
A21	LA23	B21	LA22	C21	LA21
A22	LA20	B22	LA19	C22	LA18
A23	LA17	B23	MEMCS16	C23	I/OCS16
A24	IRQ10	B24	IRQ11	C24	IRQ12
A25	IRQ15	B25	IRQ14	C25	GND
A26	MEMR	B26	MEMW	C26	SD8
A27	SD9	B27	SD10	C27	SD11
A28	SD12	B28	SD13	C28	SD14
A29	SD15	B29		C29	DACK0
A30	DRQ0	B30	DACK5	C30	DRQ5
A31	DACK6	B31	DRQ6	C31	DACK7
A32	DRQ7	B32	MASTER	C32	+5V

2. I/O Slot 1

Pin NO	Signal	Pin NO	Signal
A1	I/OCHCK	B1	GND
A2	SD7	B2	RESETDRV
A3	SD6	B3	+5V
A4	SD5	B4	IRQ9
A5	SD4	B5	−5V
A6	SD3	B6	DRQ2
A7	SD2	B7	−12V
A8	SD1	B8	OWS
A9	SD0	B9	+12V
A10	I/OCHRDY	B10	GND
A11	AEN	B11	SMEMW
A12	SA19	B12	SMEMR
A13	SA18	B13	IOW
A14	SA17	B14	IOR
A15	SA16	B15	DACK3
A16	SA15	B16	DRQ3
A17	SA14	B17	DACK1
A18	SA13	B18	DRQ1
A19	SA12	B19	REFRESH
A20	SA11	B20	CLK
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	DACK2
A27	SA4	B27	T/C
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	OSC
A31	SA0	B31	GND

3. I/O Slot 2

Pin NO	Signal	Pin NO	Signal
C1	SBHE	D1	MEMCS16
C2	LA23	D2	I/OCS16
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	DACK0
C9	MEMR	D9	DRQ0
C10	MEMW	D10	DACK5
C11	SD8	D11	DRQ5
C12	SD9	D12	DACK6
C13	SD10	D13	DRQ6
C14	SD11	D14	DACK7
C15	SD12	D15	DRQ7
C16	SD13	D16	+5V
C17	SD14	D17	MASTER
C18	SD15	D18	GND
C19		D19	
C20		D20	

4. Modem

Pin NO	Signal	Pin NO	Signal
A1	GND	B1	GND
A2	SD0	B2	SD1
A3	SD2	B3	SD3
A4	SD4	B4	SD5
A5	SD6	B5	SD7
A6	SA0	B6	SA1
A7	SA2	B7	SA3
A8	SA4	B8	SA5
A9	SA6	B9	SA7
A10	SA8	B10	SA9
A11	AEN	B11	RESETDRV
A12	IOR	B12	IOW
A13	IRQ3	B13	IRQ4
A14	+5V	B14	+5V
A15	+12V	B15	−12V
A16	GND	B16	MSPO

5. Hard Disk

Pin NO	Signal	Pin NO	Signal
1	DSELB	2	GND
3	RESETDRV	4	+5V
5	AEN	6	IOR
7	IOCS16	8	IOW
9	SA0	10	SA1
11	SA2	12	SA3
13	SA4	14	SA5
15	SA6	16	SA7
17	SA8	18	SA9
19	SD0	20	SD1
21	SD2	22	SD3
23	SD4	24	SD5
25	SD6	26	SD7
27	SD8	28	SD9
29	SD10	30	SD11
31	SD12	32	SD13
33	SD14	34	SD15
35	BALE	36	−5V
37	IRQ14	38	+5V
39	GND	40	GND

6. Floppy Disk

Pin NO	Signal	Pin NO	Signal
1	GND	2	LOW DEN
3	GND	4	
5	GND	6	
7	GND	8	INDEX
9	GND	10	
11	GND	12	DS2
13	GND	14	DS1
15	GND	16	MOTEN
17	GND	18	DIR
19	GND	20	STEP
21	GND	22	WRT DATA
23	GND	24	WRT GATE
25	GND	26	TRK0
27	GND	28	WRT PROT
29	GND	30	READ DATA
31	GND	32	HSI
33	GND	34	DSKCHG

7. LCD

Pin NO	Signal	Pin NO	Signal
1	GND	2	S
3	CP1	4	CP2
5	M	6	GND
7		8	+5V
9	GND	10	VEE
11	DU0	12	DU1
13	DU2	14	DU3
15	GND	16	DL0
17	DL1	18	DL2
19	DL3	20	GND

CONNECTOR TABLE 2

AA-11

8. RS232C

Pin NO	Signal	Pin NO	Signal
1	GND	14	
2	SD	15	
3	RD	16	
4	RTS	17	
5	CTS	18	
6	DSR	19	
7	GND	20	DTR
8	CD	21	
9		22	CI
10		23	
11		24	
12		25	
13			

9. Printer

Pin NO	Signal	Pin NO	Signal
1	STROB	14	AUTFDX
2	D0	15	ERROR
3	D1	16	INIT
4	D2	17	SLCTIN
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

10. CRT

Pin NO	Signal	Pin NO	Signal
1	GND	6	I
2	GND	7	VIDEO
3	R	8	H-SYNC
4	G	9	V-SYNC
5	B		

11. LED

Pin NO	Signal
1	KBD CLK
2	KBD DATA
3	+5V
4	STAND BY
5	SELECT A
6	SELECT B
7	GND
8	LCD CONT
9	LCD RV
10	GND

12. Speaker

Pin NO	Signal
1	SP
2	Vcc

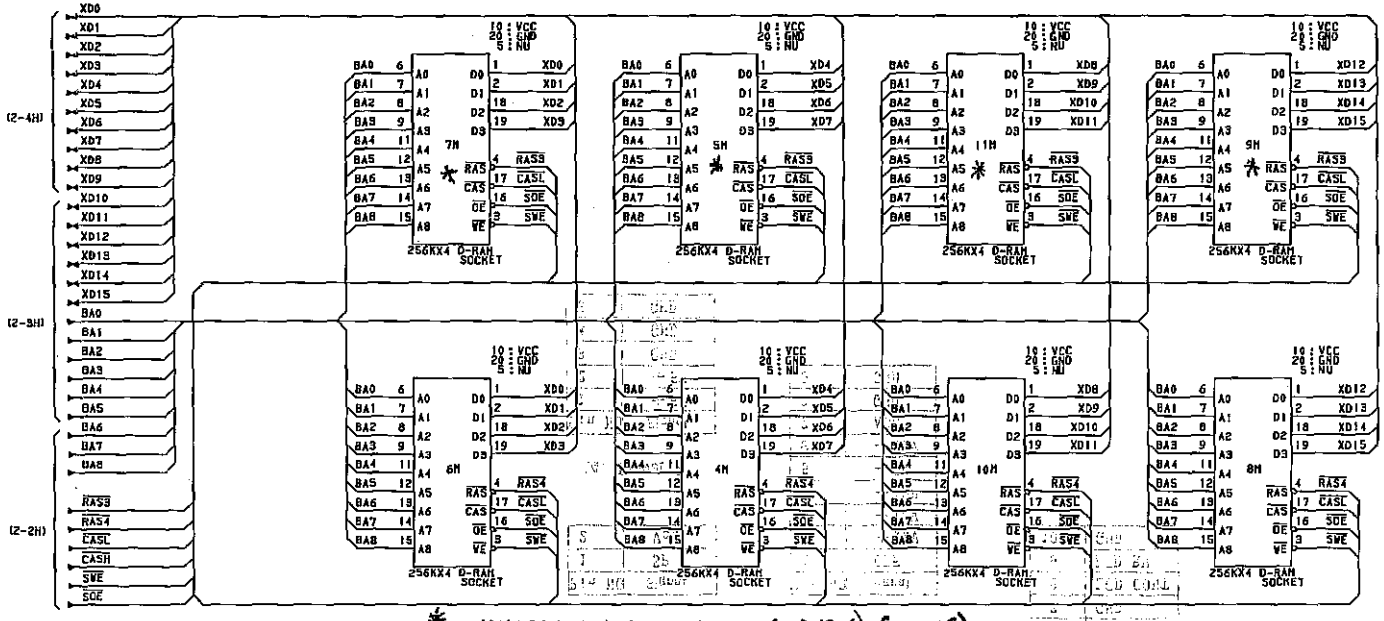
13. Power 1

Pin NO	Signal
1	OFF
2	+12V
3	+12V
4	-12V
5	-5V
6	-15V
7	ACL
8	GND
9	GND

14. Power 2

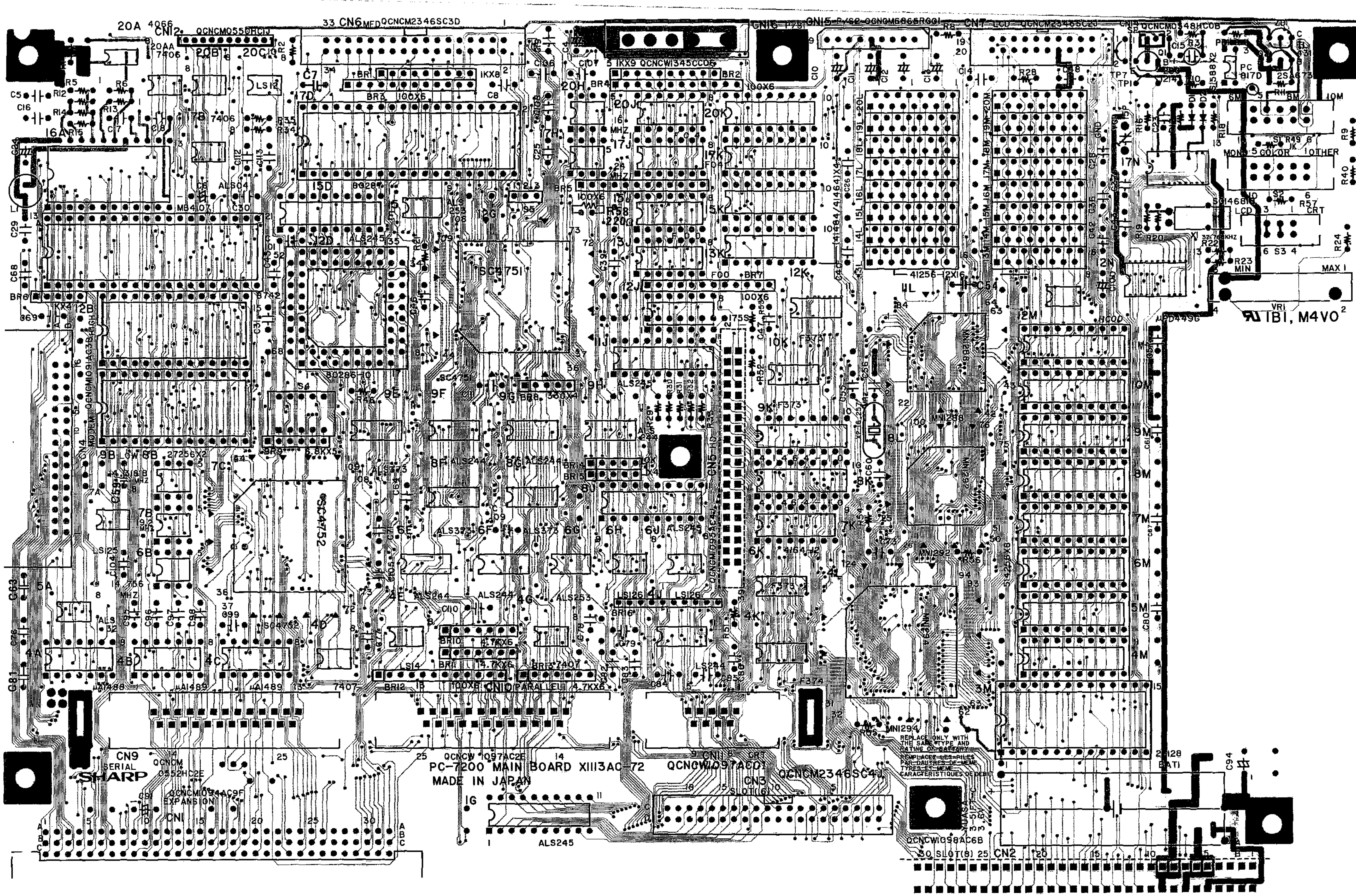
Pin NO	Signal
1	+5V
2	+5V
3	GND
4	GND
5	GND

EXPANSION RAM

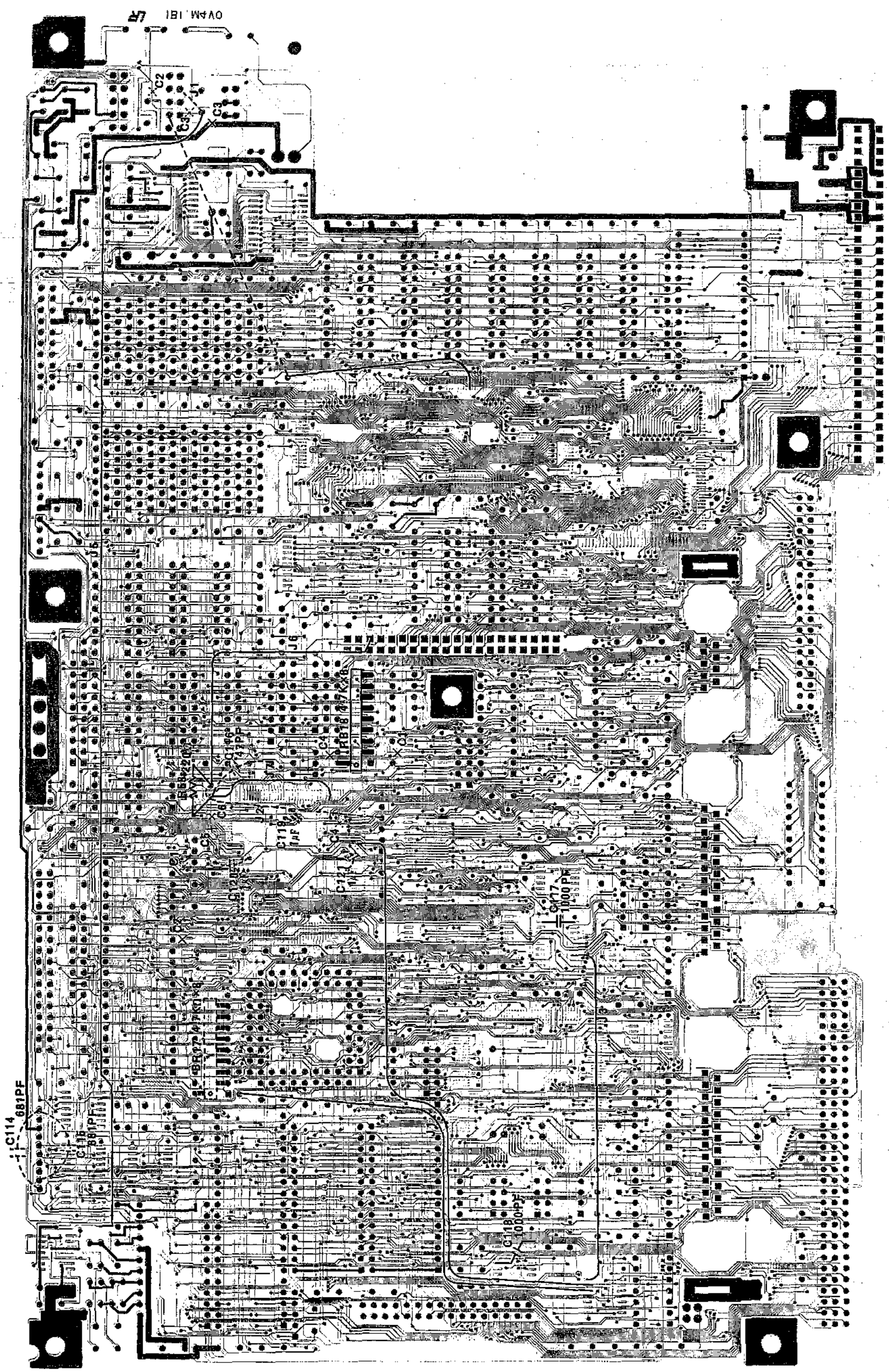


* UNCERTAIN 4256KBX4 (+512K) (120NS)

MAIN P.W.B.

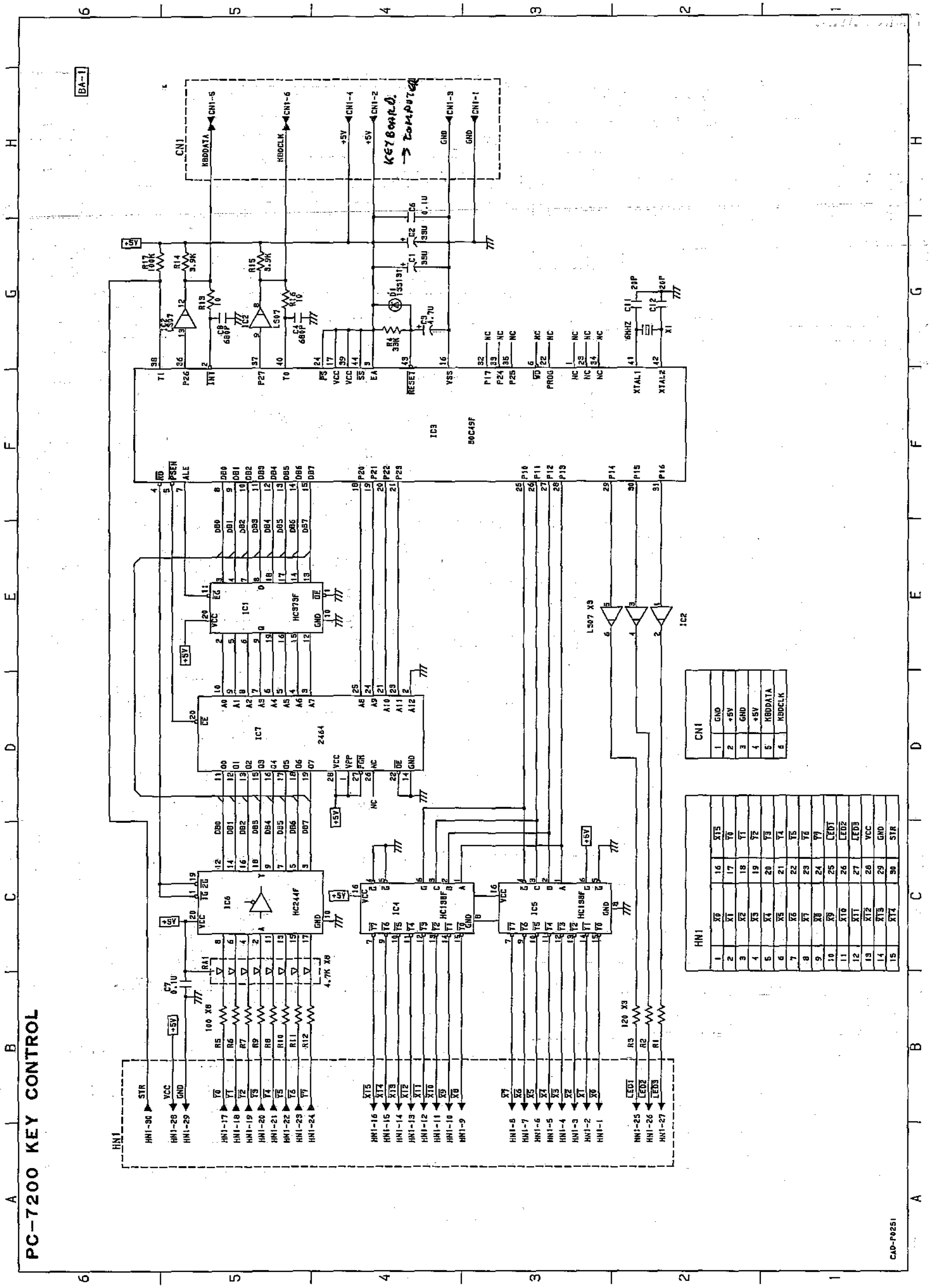

PC-7200 MAIN BOARD XIII3AC-72
MADE IN JAPAN
SHARP
CN9 SERIAL
CN1 EXPANSION
CN10 PARALLEL
CN3 SLOT(16)
CN2 SLOT(8)
CN4 MODEM
CN5 HD
CN6 MFD
CN7 LCD
CN12
80286-10
SC4751
SC4752
ALS245
ALS244
ALS373
ALS253
LS126
41256-12X16
MONO COLOR OTHER
LCD CRT
MAX MIN
BAT1
REPLACE ONLY WITH THE SAME TYPE AND RATING OF BATTERY
REMPLACER LES PILES PAR D'AUTRES DE MEME TYPES ET DE MEME CARACTERISTIQUES DE DEBIT

MAIN P.W.B.



※ Lines(——) parts are on the parts side.
Blocked lines(---) parts are on the solder side.

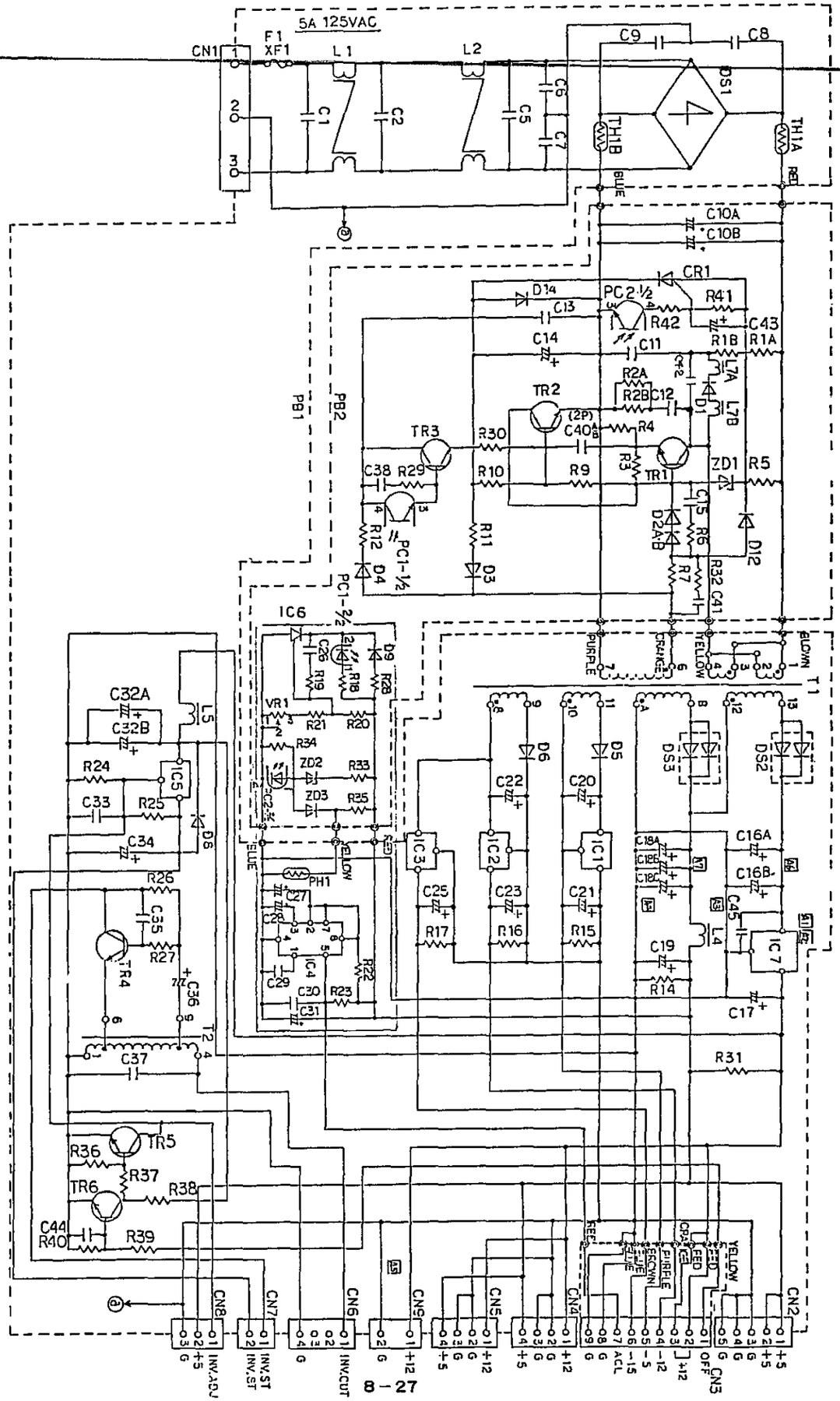
PC-7200 KEY CONTROL

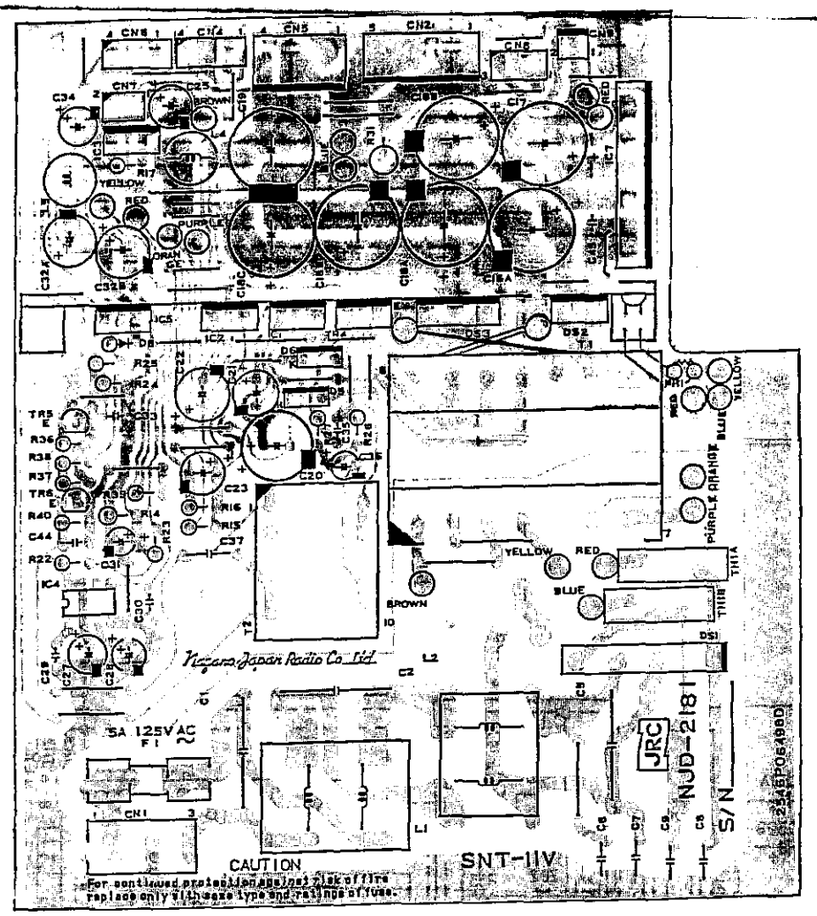


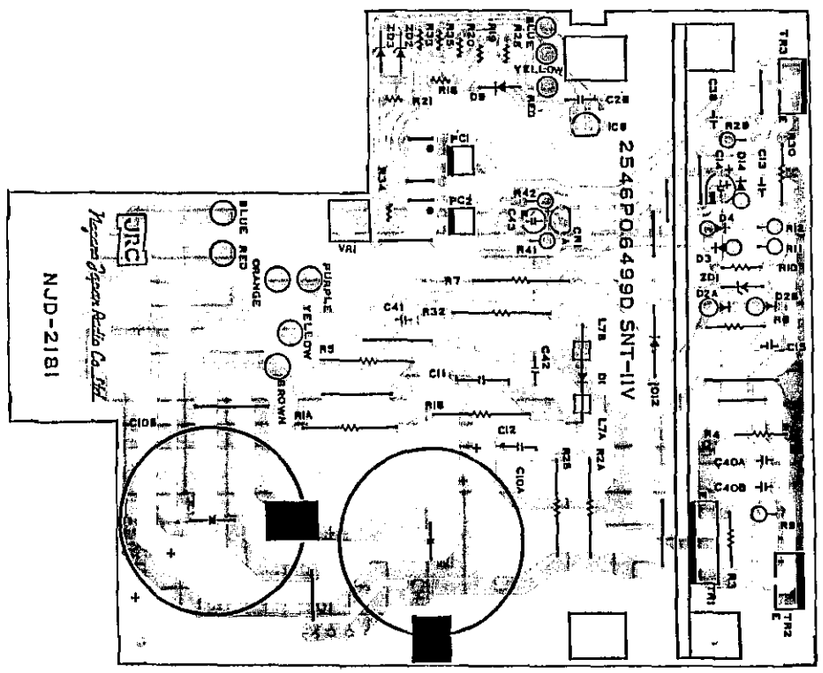
CN1	
1	GND
2	+5V
3	GND
4	+5V
5	KBDDATA
6	KBDCLK

HN1			
1	X0	16	X15
2	X1	17	Y0
3	X2	18	Y1
4	X3	19	Y2
5	X4	20	Y3
6	X5	21	Y4
7	X6	22	Y5
8	X7	23	Y6
9	X8	24	Y7
10	X9	25	LED1
11	X10	26	LED2
12	X11	27	LED3
13	X12	28	VCC
14	X13	29	GND
15	X14	30	STR

POWR SUPPLY P.W.B. 100V SERIES

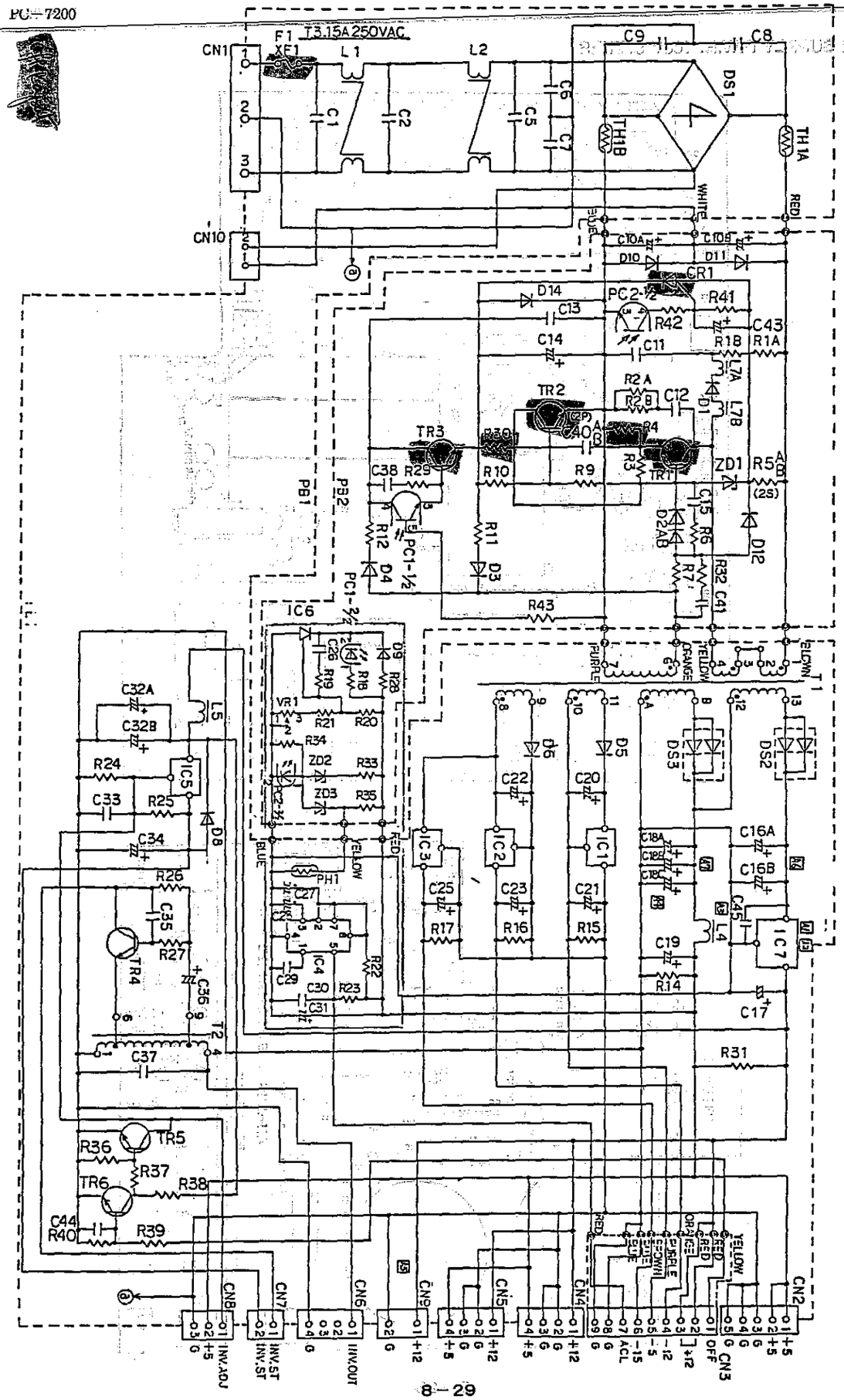




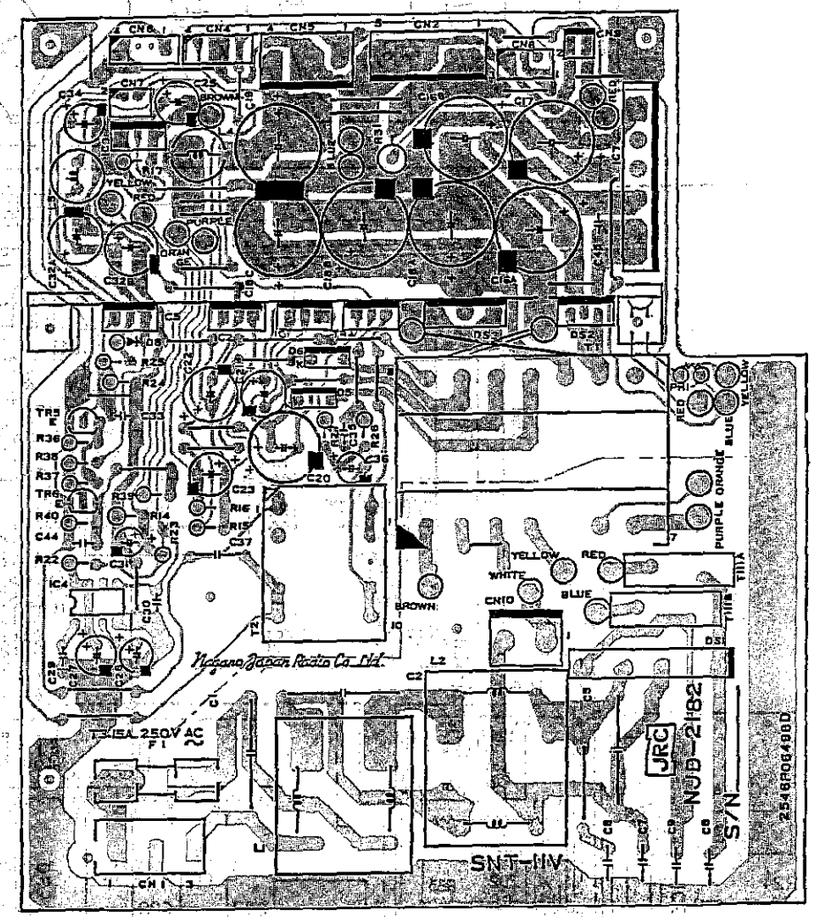


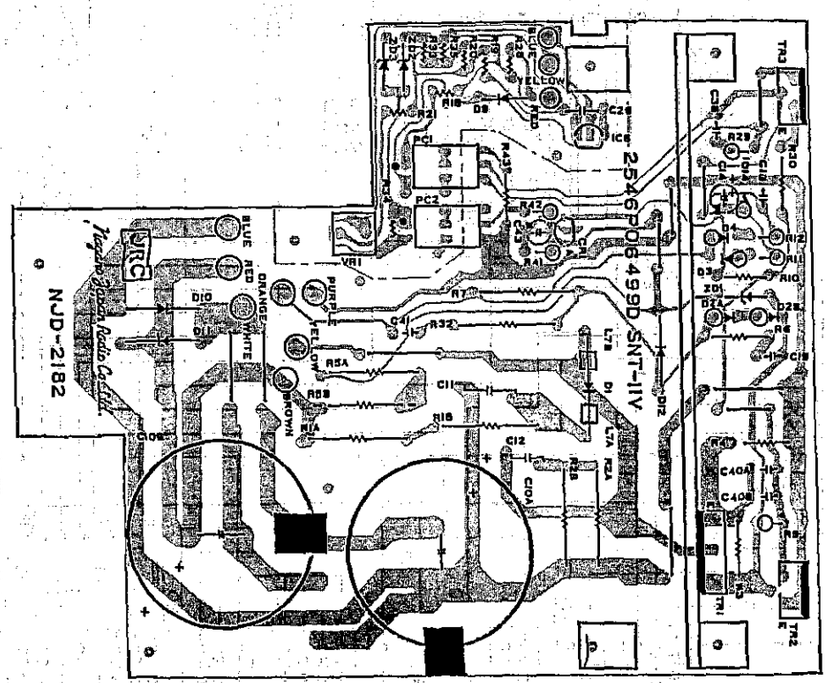
POWER SUPPLY CIRCUIT 100V SERIES

POWER SUPPLY CIRCUIT 200V SERIES



POWR SUPPLY P.W.B. 200V SERIES





PC7202/7221 PARTS LIST

1 Exteriors

2 Main frame unit

3 Packing material & Accessories · CE720K

4 Key exteriors · CE720K

5 Keyboard unit · CE720K

6 LED PWB unit

7 Key PWB unit

8 Main PWB unit

9 Valiable resistor PWB unit

10 Power supply unit - - - 100V series

11 Power supply unit - - - 200V series

12 Hard disk interface PWB unit - - - PC7221 only

Please note that some of components were replace by new types, which are marked with an asterisk (*). While the parts code of the new type is given in Parts List, the parts code of the old type is not. Since the old types were used up to the 301st production unit whose machine serial numbers are listed below, all those three components marked with an asterisk must be replaced by the old types altogether, even if only a component needs to be replaced.

79101263 ~ 79101353	10 sets
79100013 ~ 79100203	20 sets
79108395 ~ 79108845	46 sets
79110405 ~ 79111315	92 sets
79109355 ~ 79110395	105 sets
79101665 ~ 79101785	13 sets
79101365 ~ 79101505	15 sets
TTL	301 sets

DESTINATION TABLE

U	USA		KD	Denmark
Y	CANADA		KE	Netherland, Austria
G	EUROPE		KF	France
H	U. Kingdom		KG	W Germany
Q	Australia		Ki	Italy
T	TJ	Korea, Venezuela	KN	Norway
	TSC	Taiwan	KS	Sweden, Finland
E	EH	Malaysia; Singapore		
	EQ	New Zealand	KW	Switzerland (E)
	ESB	Saudi Arabia	KX	Switzerland (F)
	ESG	Indonesia, Thailand, Philippine		
		Lebanon, Jorday, W-Africa		
		Hong Kong		
	ESGI	Pakistan, Argentine		
		Iraq, U.A.E.		

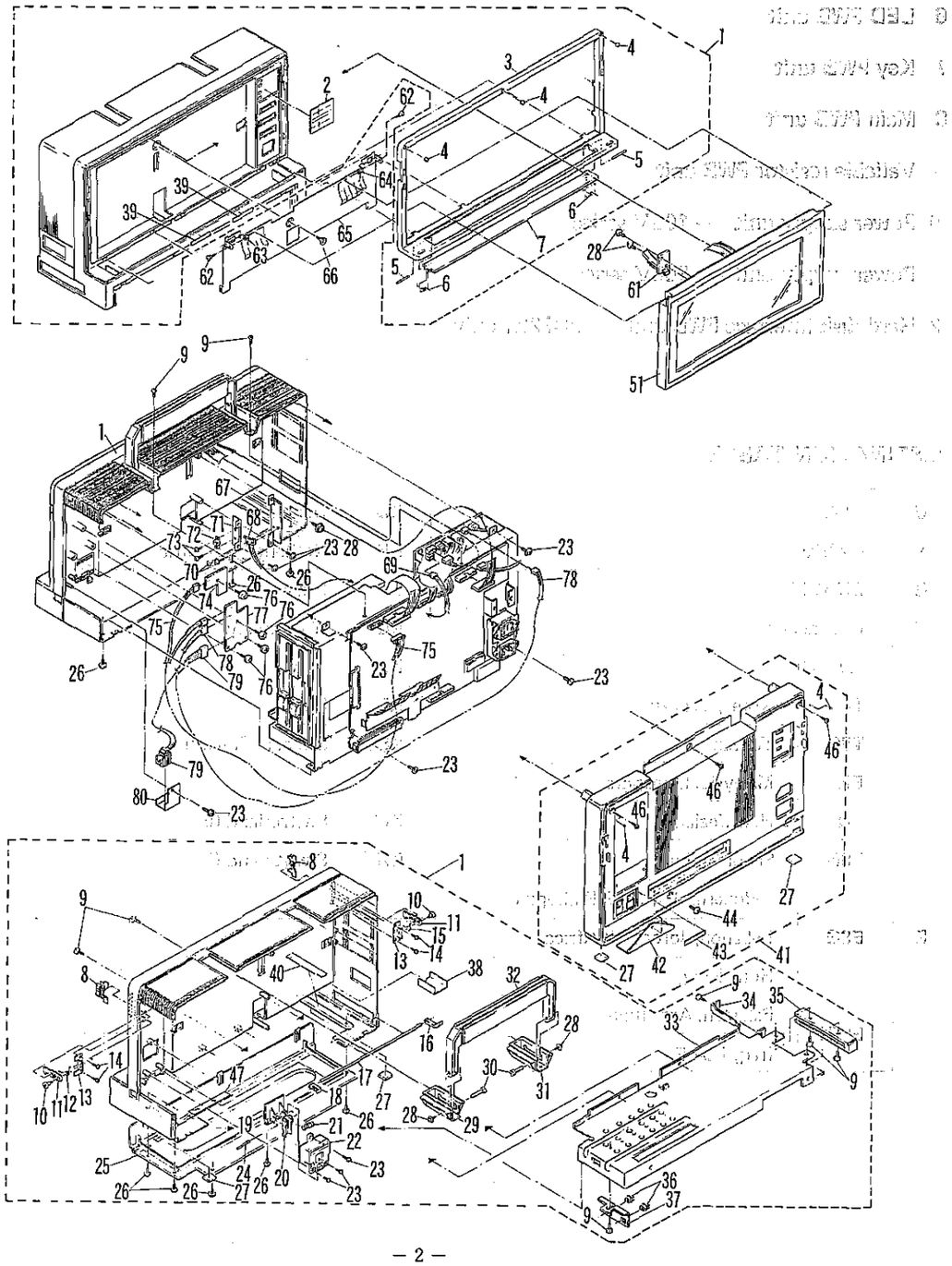
Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
*** 1	CCABA1047AC02	BZ	N	E	Front housing unit (№2~24,26~40)	(U,Y)(PC-7202)
	CCABA1047AC11	BZ	N	E	Front housing unit (№2~24,26~40)	(other countries)(PC-7202)
	CCABA1047AC03	BZ	N	E	Front housing unit (№2~24,26~40)	(U,Y)(PC-7221)
	CCABA1047AC12	BZ	N	E	Front housing unit (№2~24,26~40)	(other countries)(PC-7221)
2	PFiLW1003ACSB	AL	N	C	LED filter	(U,Y)(PC-7202)
	PFiLW1003ACZZ	AL	N	C	LED filter	(Other countries)(PC-7202)
	PFiLW1003ACSA	AL	N	C	LED filter	(PC-7221)
3	HPNLC2140HCSA	AV	N	D	Front panel	(U,Y)
	HPNLC2140HCZZ	AP		D	Front panel	(Other countries)
4	GLEGG1024CCZZ	AA		C	Rubber foot	
5	LPiNS2032HCZZ	AC		C	Key cable pin	
6	MSPRC2025HCZZ	AA		C	Key cable spring	
7	CPLTP2060HC04	AM	N	C	Key cable plate	(U,Y)
	CPLTP2060HC02	AH		C	Key cable plate	(Other countries)
8	JKNBZ1876CCSA	AB	N	C	Cabinet lock button	(U,Y)
	JKNBZ1876CC01	AB		C	Cabinet lock button	(Other countries)
9	XBBSC30P06000	AA		C	Screw (3×6)	
10	LX-BZ1159CCZZ	AA		C	Screw	
11	MLEVP1044CCSA	AB	N	C	Cabinet lock lever	(U,Y)
	MLEVP1044CC01	AB		C	Cabinet lock lever	(Other countries)
12	MSPRC2029HCZZ	AC		C	Cabinet lock spring 1	
13	LANGF1530CCZZ	AC		C	Lock lever angle	
14	XCPSD26P06000	AA		C	Screw (2.6×6)	
15	MSPRC2030HCZZ	AC		C	Cabinet lock spring 2	
16	PTME-2001HCZZ	AC		C	LCD rutch pawl	
17	PBAR-2011HCZZ	AL		C	Push button bar	
18	LSTPP2004HCZZ	AC		C	Push bar stopper	
19	JBTN-2048HCSC	AE	N	D	Push button	(U,Y)
	JBTN-2048HCSB	AC	N	D	Push button	(Other countries)
20	PBAR-1001ACZZ	AC	N	C	Push bar	
21	MSPRC2024HCZZ	AA		C	Push button spring	
22	GCASP1007ACSA	AC	N	C	Button case	(U,Y)
	GCASP1007ACZZ	AC	N	C	Button case	(Other countries)
23	XBBSD30P06000	AA		C	Screw (3×6)	
24	LPiNS2031HCZZ	AD		C	Push button pin	
** 25	GFTAU1040ACZZ	AY	N	C	Bottom housing	(U,Y)
**	GFTAU1040ACSA	AY	N	C	Bottom housing	(Other countries)
26	XBBSD30P05000	AA	N	C	Screw (3×5)	
27	GLEGG1009HCSA	AB	N	C	Rubber foot	(Other countries)
	GLEGG1009HCZZ	AC		C	Rubber foot	(U,Y)(PC-7202)
	GLEGP1009ACZZ	AC	N	C	Rubber foot	(U,Y)(PC-7221)
28	XBPSD40P08KS0	AA		C	Screw (4×8KS)	
29	MLEVP2023HCS1	AF	N	C	Handle fixing lever L	(U,Y)
	MLEVP2023HCZ1	AF	N	C	Handle fixing lever L	(Other countries)
30	LPiNS2030HCZZ	AH		C	Pin for handle	
31	MLEVP2024HCS1	AF	N	C	Handle fixing lever R	(U,Y)
	MLEVP2024HCZ1	AF	N	C	Handle fixing lever R	(Other countries)
32	JHNDP2004HCSA	AY	N	C	Handle	(U,Y)
	JHNDP2004HCZZ	AY		C	Handle	(Other countries)
33	CFRM-1005AC02	AV	N	E	Frame B unit (№9,34~37)	(U,Y)
	CFRM-1005AC01	AW	N	E	Frame B unit (№9,34~37)	(Other countries)
34	GFTAZ2030HCZZ	AF		C	Connector Cover	
35	GCOVH1026ACZZ	AG	N	C	Connector food	
36	LBSHC5020BCZZ	AB		C	PWB guide bushing	
37	LANGT1124ACZZ	AC	N	C	Guide rail angle	
38	GCOVH1032ACZZ	AD	N	D	Blank cover	
39	PSPAZ2037HCZZ	AE		C	Spacer A	
40	PZETZ1026ACZZ	AC	N	C	Insulator sheet 2	
*** 41	CCABB1041AC40	BG	N	E	Rear housing unit (№4,27,42~44)	(U,Y)
***	CCABB1041AC41	BE	N	E	Rear housing unit (№4,27,42~44)	(TJ only)
***	CCABB1041AC42	BE	N	E	Rear housing unit (№4,27,42~44)	(TSC only)
***	CCABB1041AC50	BE	N	E	Rear housing unit (№4,27,42~44)	(G,H,Q,E)
42	GFTAZ1034ACZZ	AL	N	C	Box cover	
43	TLABZ1275ACSA	AB	N	C	Modem label	(U,Y)
44	XBTSC40P06000	AA		C	Screw (4×6)	
46	LX-BZ2058HCZZ	AA		C	Screw	
47	PZETZ1024ACZZ	AD	N	C	Housing insulator sheet 1	(G,H,Q,E)(PC-7221)
51	DUNT-1790ACZZ	CV	N	E	LCD unit	(U only)
	DUNT-1786ACZZ	CV	N	E	LCD unit	(Other countries)
61	MLOK-1004ACZZ	AD	N	C	LCD lock	
62	LX-BZ2055HCZZ	AB		C	Screw	
63	MSPRC2027HCZZ	AA		C	LCD spring	
64	MSPRD2028HCZZ	AA		C	LCD spring R	
65	LANGT2302HCZC	AQ		C	LCD angle	
66	XBSSD40P06000	AA		C	Screw (4×8)	
67	LANGQ2349HCZZ	AD		C	Microswitch fixing angle	
68	QSW-M2043HCZZ	AL		B	Microswitch	
69	QCNW-1219ACZZ	AC	N	C	Microswitch cable	
70	XBPSD20P08000	AA		C	Screw	
71	LANGG2301HCZZ	AD		C	LCD damper angle	

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
72	PDMPO1001ACZZ	AE		C	Damper	
73	XBPSD20P04000	AA		C	Screw (2×4)	
74	CPWBF1115AC01	AD	N	E	LED PWB unit	
75	QCNW-1191ACZZ	AH	N	C	LED cable	
76	XUBSD30P08000	AA		C	Screw (3×8)	
77	CPWBF1116AC03	AE	N	E	Valiable resistor PWB unit	(U only)
	CPWBF1116AC02	AE	N	E	Valiable resistor PWB unit	(Y only)
	CPWBF1116AC01	AE	N	E	Valiable resistor PWB unit	(Other countries)
78	QCNW-1196ACZZ	AE	N	C	INV. VR cable	
79	QCNW-1236ACSA	AL	N	C	Key interface cable + Core	(U,Y)
	QCNW-1197ACZZ	AL		C	Key cable	(Other countries)
80	LANGT2309HCZA	AC	N	C	Key connector angle	

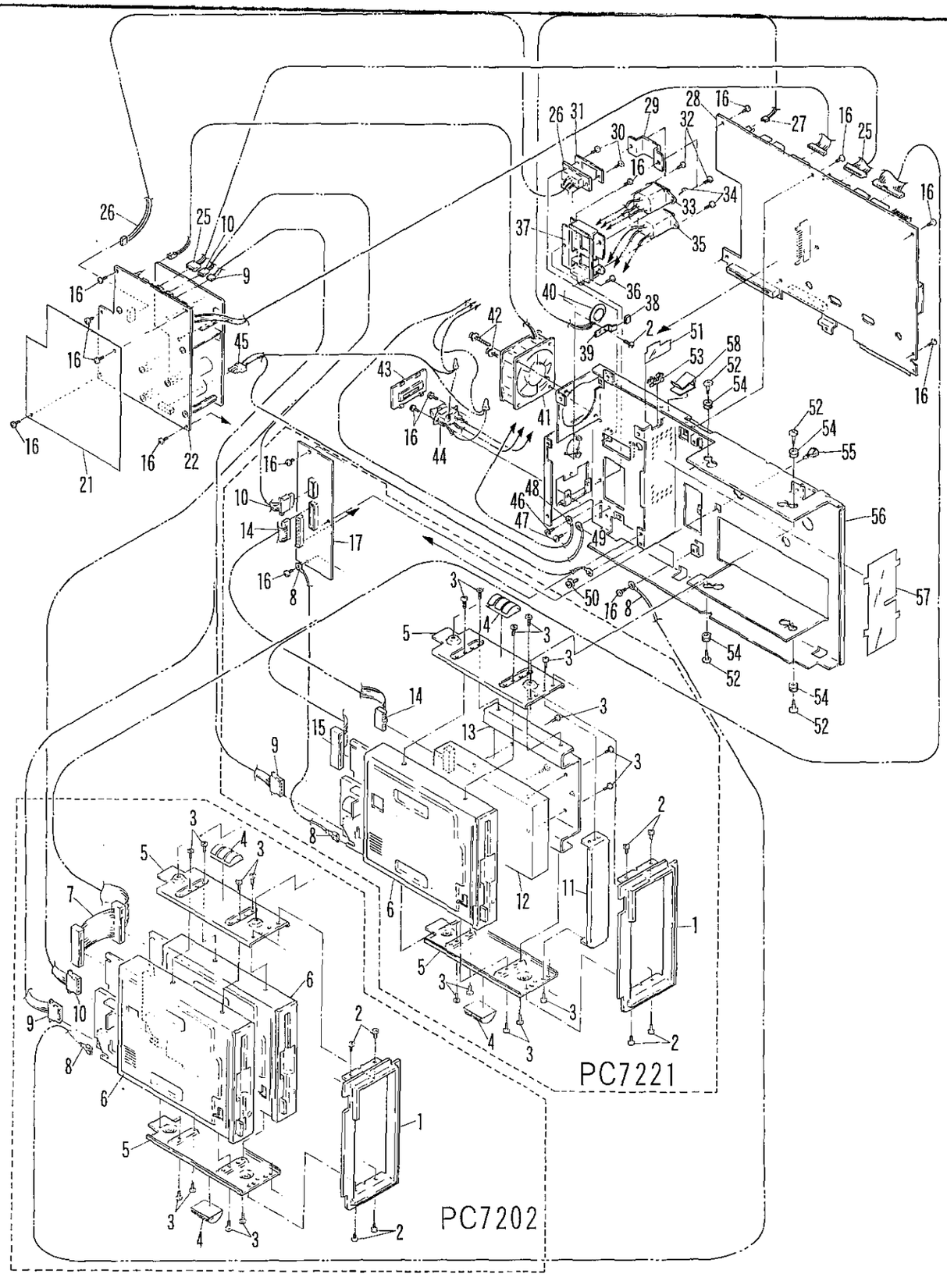


2 Main frame unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GCOVH1024ACS1	AG	N	D	FD blank panel (U,Y)
	GCOVH1024ACZ1	AG	N	D	FD blank panel (Other countries)
2	XBBSD30P05000	AA	N	C	Screw
3	XBPSD30P06K00	AA		C	Screw (3×6K)
4	LPLTP1015ACZZ	AH	N	C	Earth band Plate
5	LANGT1127ACZZ	AF	N	C	FD angle
6	DUNT-1695ACSA	CG	N	E	FD unit (U,Y)
※	DUNT-1695ACZZ	CG	N	E	FD unit (Other countries)
7	QCNW-1217ACZZ	AX	N	C	FD2 cable (34pin) (PC-7202)
8	QCNW-1188ACZZ	AC	N	C	FD earth cable
9	QCNW-1187ACZZ	AH	N	C	FD-PS cable
10	QCNW-1218ACZZ	AK	N	C	FD1-P/S cable
11	HPNLC1026ACSA	AF	N	D	FD panel (U,Y)(PC-7221)
	HPNLC1026ACZZ	AF	N	D	FD panel (Other countries)(PC-7221)
12	DUNT-1694ACZZ	**	N	E	HD unit CP (PC-7221)
13	LANGT1123ACZZ	AH	N	C	HD angle (PC-7221)
14	QCNW-1199ACZZ	AP	N	C	HD cable (PC-7221)
15	QCNW-1186ACZZ	AU	N	C	FD cable (PC-7221)
16	XBBSD30P06000	AA		C	Screw (3×6)
17	DUNTK1693ACZZ	CK	N	E	HD interface PWB unit (PC-7221)
21	PZETY1020ACZZ	AK	N	C	PS insulator sheet
22	RDENC1006ACZZ	BX	N	E	Power supply unit (100V series) (U,Y,T)
	RDENC1007ACZZ	BY	N	E	Power supply unit (200V series) (G,H,Q,E)
25	QCNW-1189ACZZ	AH	N	C	PS cable (5pin)
26	QCNW-1200ACZZ	AQ	N	C	Maltch switch cable (200V series) (G,H,Q,E)
27	QCNW-1215ACZZ	AC	N	B	Speaker cable (2pin)
28	DUNTK1796ACZZ	**	N	E	Main PWB unit (U,Y)
	DUNTK1878ACZZ	**	N	E	Main PWB unit (G only)
	DUNTK1700ACZZ	**	N	E	Main PWB unit (Other countries)
29	GFTAZ1039ACZZ	AL	N	C	Outlet cover (200V series) (G,H,Q,E)
30	XBBSD30P06000	AA		C	Screw (3×6)(200V series) (G,H,Q,E)
31	GCOVH1025ACZZ	AK	N	C	Maltch switch cover (200V series) (G,H,Q,E)
32	XBSSD30P08000	AA		C	Screw (3×8)(100V series) (U,Y,T)
	XBPSD30P06000	AA		C	Screw (3×6)(200V series) (G,H,Q,E)
33	QPLGA2005HCZZ	AP		C	Plug (100V series) (U,Y,T)
34	XBSSD30P08000	AA		C	Screw (3×8)
35	QPLGZ1003ACZZ	AX	N	C	Plug (100V series) (U,Y,T)
	CSOCA1017CCZZ	BE		D	Socket (FN322-3/01) (200V series) (G,H,Q,E)
36	XBBSC30P08000	AA		C	Screw (3×8)
37	LANGQ2303HCZB	AK	N	D	AC switch angle
38	PCUSG1006ACZZ	AB		C	Rubber cushion
39	LANGT1147ACZZ	AF	N	C	Speaker fixing angle
40	RALMB1007HCZZ	AK		B	Speaker (CS-29B)
41	NFANP1011ACZZ	BA	N	B	DC Fan
42	XBPSD40P28KS0	AA		C	Screw (4×28KS)
43	HPNLC2141HCSA	AE	N	D	AC switch panel (U,Y)
	HPNLC2141HCZZ	AE		D	AC switch panel (Other countries)
44	QSW-C9221QCZZ	AK		B	Seesaw switch
45	QCNW-1193ACZZ	AF	N	C	Inlet cable (U,T)
	QCNW-1223ACZZ	AG	N	C	Inlet cable (Y only)
	QCNW-1222ACZZ	AE	N	C	Inlet cable (G,H,Q)
	QCNW-1194ACZZ	AE	N	C	Inlet cable (E only)
46	XBPBZ40P06K00	AA		C	Screw (4×6K)
47	XBPBZ40P06K00	AA		C	Screw (4×6K)(100V series) (U,Y,T)
48	QCNW-1216ACZZ	AC	N	C	P/S earth cable
49	QCNW-1216ACZZ	AC	N	C	P/S earth cable (100V series) (U,Y,T)
50	XBPSD40P06K00	AA		C	Screw (4×6K)
51	PSHEZ1010ACZZ	AC	N	C	PS insulator sheet
52	LX-BZ1022ACZZ	AB		C	Screw
53	LBSHZ2037SCZZ	AD		C	Bushing
54	PGUMM1004ACZZ	AE		C	Rubber
55	PSPAZ1018ACZZ	AB	N	C	Spacer (KGLS-7R) (PC-7221)
** 56	CFRM-1004AC01	AZ	N	E	Main frame unit (№53,54,58) (PC-7202)
**	CFRM-1004AC02	BA	N	E	Main frame unit (№53~55,58) (PC-7221)
57	PSHEZ1009ACZZ	AD	N	C	Sheet
58	LHLDW2045SCZZ	AC		C	Wire holder (MFS-1000)

PC7200

2 Main frame unit

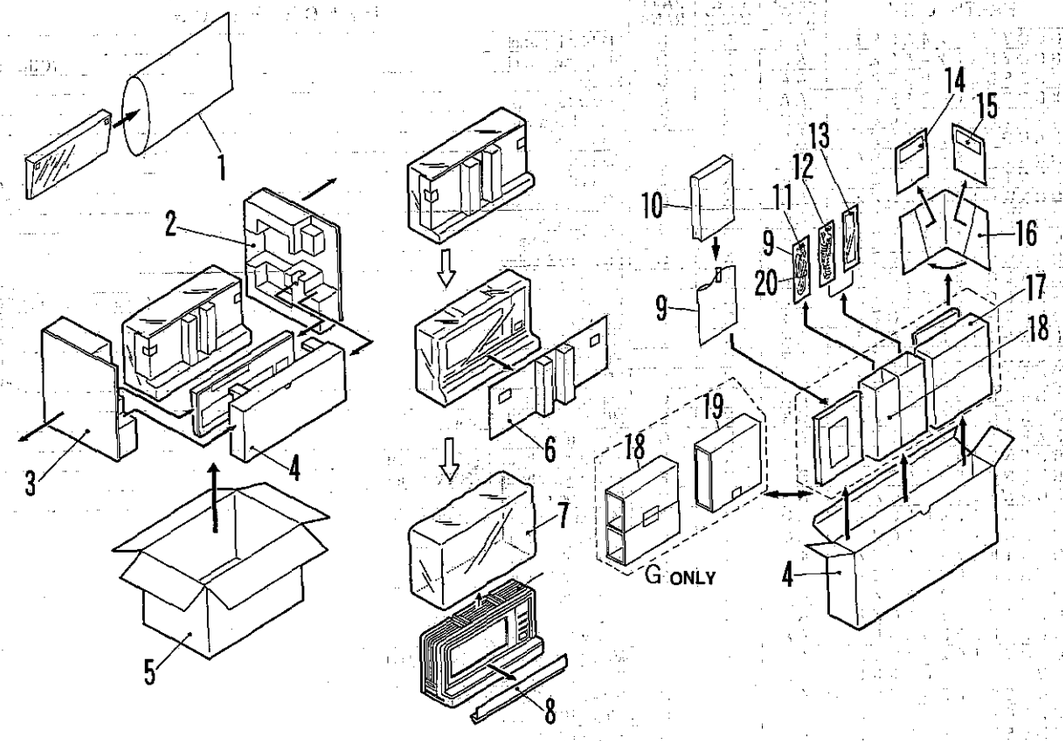


3 Packing material & Accessories • CE720K

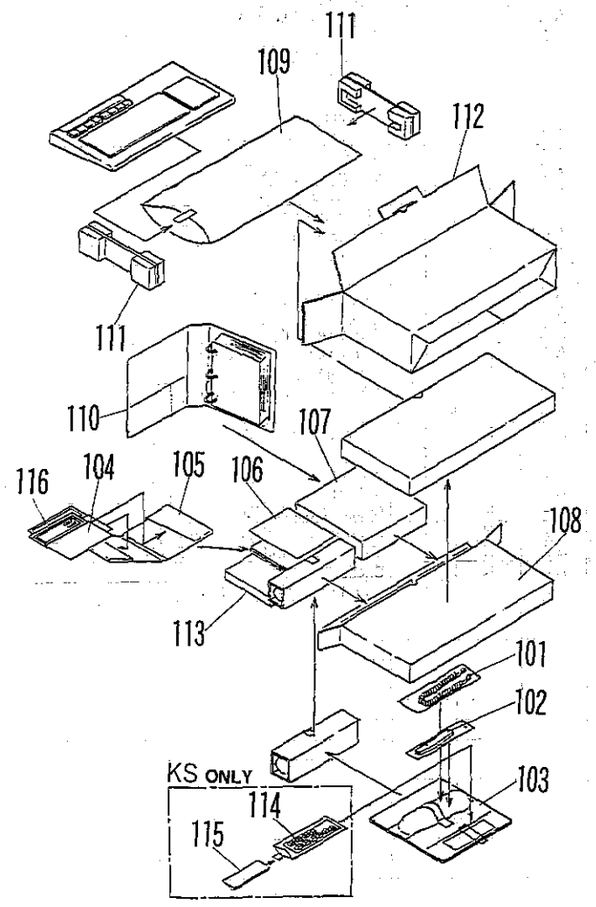
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	SPAKP2397SCZZ	AC		D	Antistatic bag for key	(Except G)
2	SPAKA1835ACZZ	BC	N	D	Packing cushion B (Right)	
3	SPAKA1834ACZZ	AX	N	D	Packing cushion A (Left)	
4	SPAKA1836ACZZ	AK	N	D	Accessories case	
5	SPAKC1855ACZZ	AS	N	D	Packing case	(U,Y)(PC−7202)
	SPAKC1857ACZZ	AS	N	D	Packing case	(H,Q,E,T)(PC−7202)
	SPAKC1856ACZZ	AT	N	D	Packing case	(G only)(PC−7202)
	SPAKC1837ACZZ	AS	N	D	Packing case	(U,Y)(PC−7221)
	SPAKC1853ACZZ	AT	N	D	Packing case	(H,Q,E,T)(PC−7221)
	SPAKC1851ACZZ	AS	N	D	Packing case	(G only)(PC−7221)
6	SPAKA1899ACZZ	AH	N	D	LCD packing cushion	
7	SPAKP2370HCZZ	AF		D	CPU vinyl bag	
8	SPAKA2530HCZZ	AB		D	LCD fixing packing cushion	
9	SSAKA0005WCZZ	AA		D	Vinyl bag (160×260mm)	
10	TiNSE1401ACZZ	BG	N	D	Operation manual for GW−BASIC	(Y,H,Q,T,EH,EQ,ESG,ESG1)
	TiNSE1396ACZZ	AY	N	D	Operation manual for GW−BASIC	(U,ESB)
⚠ 11	QACCD7611QCN2	AQ	N	B	AC cord	(U only)
⚠	QACCD7611QCZZ	AT		B	AC cord	(Y,T)
⚠	QACCB0002PAZZ	AY		B	AC cord	(H only)
⚠	QACCV6620QCZZ	AV		B	AC cord	(G,ESG,ESG1)
⚠	QACCL7620QCZZ	AW		B	AC cord	(Q,EQ)
⚠	QPLGA0010UCZZ	AM		C	3P AC cord adaptor	(T only)
⚠	QPLGA1001ACZZ	AH		B	AC cord adaptor plug	(ESG1 only)
⚠	CCNW−2814SC01	AX		B	AC cord	(ESB only)
⚠	QACCF7320QCZZ	AX	N	B	AC cord	(EH only)
12	QCNW−2330HCSA	AT	N	C	Key cable	(U,Y)
	QCNW−2330HCZZ	AT		C	Key cable	(Other countries)
13	LPLTP1013ACZZ	AC	N	D	Key ten plate	(Except G)
14	DFLP−1086ACZZ	AZ	N	D	MS−DOS/GW−BASIC disket	(U,Y,E,T)
	DFLP−1085ACZZ	AZ	N	D	MS−DOS/GW−BASIC disket	(H,Q)
15	DFLP−1088ACZZ	AZ	N	D	DIAG disket	(U,Y,E,T)
	DFLP−1087ACZZ	AZ	N	D	DIAG disket	(H,Q)
16	SPAKC2612HCZZ	AH		D	Packing case for media	(Except G)
17	CBDRP1020AC0U	BP	N	E	Binder unit (This includes №61~65)	(U,ESB)
	CBDRP1020AC0Y	BP	N	E	Binder unit (This includes №61~65)	(Y,T)
	CBDRP1020AC0H	BP	N	E	Binder unit (This includes №61~65)	(H only)
	CBDRP1020AC0E	BM	N	E	Binder unit (This includes №61~65)	(Q,EH,EQ,ESG,ESG1)
18	SPAKA1897ACZZ	AE	N	D	AC cord sleeve	
19	SPAKA2531HCZZ	AD		D	Accessories sleeve	(G only)
20	UBNDA1008CCZZ	AA		C	AC cord band	
61	GCASP2023HCZZ	AP		D	Binder case	
62	SPAKA1838ACZZ	AK	N	D	Binder add	(U,Y,H,T,ESB)
	SPAKA2529HCZZ	AF		D	Binder add	(Q,EH,EQ,ESG,ESG1)
63	TiNSE1393ACZZ	BD	N	D	Operation manual	(H,Q,EH,EQ,ESG,ESG1)
	TiNSE1390ACZZ	BD	N	D	Operation manual	(U,ESB)
	TiNSE1391ACZZ	BD	N	D	Operation manual	(Y,T)
64	TiNSE1395ACZZ	AX	N	D	Operation manual for MS−DOS	(Y,H,Q,T,EH,EQ,ESG,ESG1)
	TiNSE1394ACZZ	AX	N	D	Operation manual for MS−DOS	(U,ESB)
65	UBDRP1020ACZZ	AW	N	D	Binder	
101	QCNW−2330HCZZ	AT		C	Key cable	
102	LPLTP1013ACZZ	AC	N	D	Key ten plate	
103	SPAKA2433HCZZ	AE		D	Packing cushion C	
104	DFLP−1085ACZZ	AZ	N	D	MS−DOS/GW−BASIC disket	(G only)
105	SPAKC2612HCZZ	AH		D	Packing case for media	
106	TCADZ1056ACZZ	AG	N	D	Tag card	(KF,KG,KI,KW,KX)
107	SPAKA1891ACZZ	AC	N	D	Dummey packin for inst. book	
108	SPAKA2430HCZZ	AL		D	Accessory case	
109	SPAKP2397SCZZ	AC		D	Antistatic bag for key	
110	CBDRP1020AC0E	BM	N	E	Binder unit (This includes №201~205)	(KE,KS)
	CBDRP1022AC0F	BP	N	E	Binder unit (This includes №201~205)	(KF,KX)
	CBDRP1021AC0G	BP	N	E	Binder unit (This includes №201~205)	(KG,KW)
	CBDRP1023AC0i	BP	N	E	Binder unit (This includes №201~206)	(KI only)
111	SPAKA2604HCZZ	AU		D	Packing cushion for key	
112	SPAKC1845ACZZ	AL	N	D	Packing case	
113	TiNSE1401ACZZ	BG	N	D	Operation manual for GW−BASIC	
114	SSAKA0231QCZZ	AA		D	Vinyl bag (80×220mm)	(KS only)
115	TiNSE1420ACZZ	BD	N	D	Operation manual for key	(KS only)
116	DFLP−1087ACZZ	AZ	N	D	DIAG disket	(G only)
201	GCASP2023HCZZ	AP		D	Binder case	
202	SPAKA2529HCZZ	AF		D	Binder add	
203	TiNSE1393ACZZ	BD	N	D	Operation manual	(KE,KS)
	TiNSF1398ACZZ	BD	N	D	Operation manual	(KF,KX)
	TiNSG1399ACZZ	BD	N	D	Operation manual	(KG,KW)
	TiNSi1400ACZZ	BD	N	D	Operation manual	(KI only)
204	TiNSE1395ACZZ	AX	N	D	Operation manual for MS−DOS	
205	UBDRP1020ACZZ	AW	N	D	Binder	(KE,KS)
	UBDRP1022ACZZ	AW	N	D	Binder	(KF,KX)
	UBDRP1021ACZZ	AW	N	D	Binder	(KG,KW)
	UBDRP1023ACZZ	AW	N	D	Binder	(KI only)

PC7200

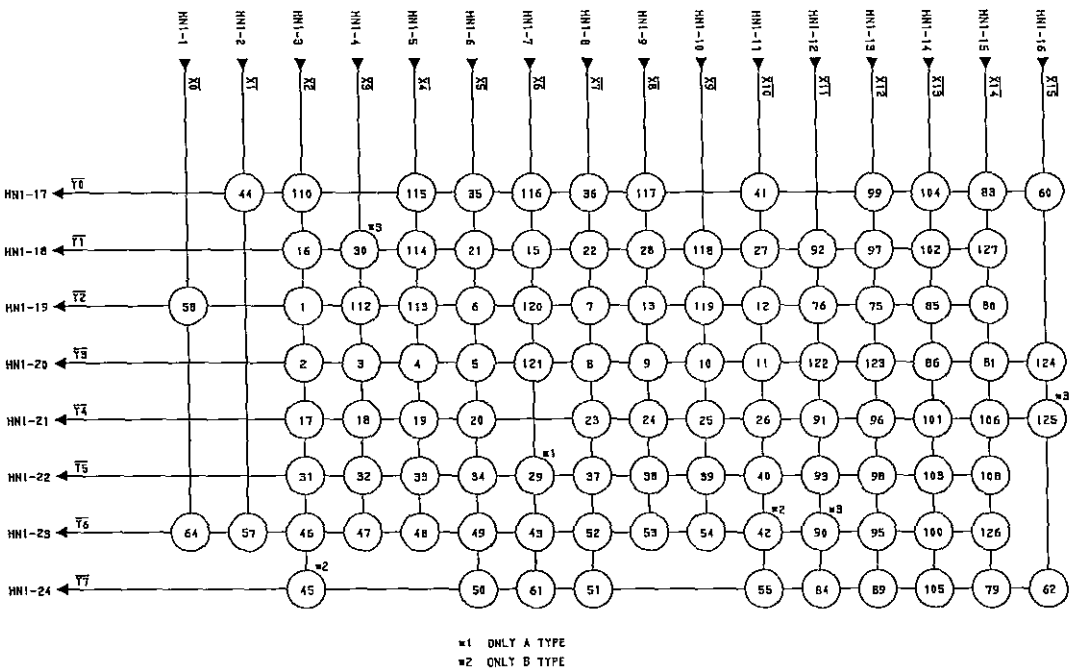
3 Packing material & Accessories • CE720K

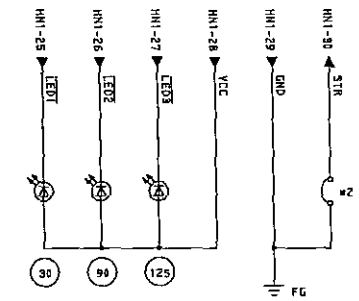


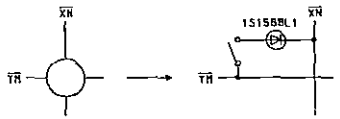
CE720K



KEY MATRIX DIAGRAM

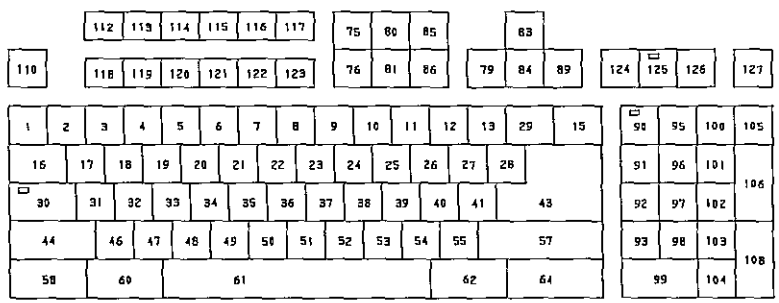




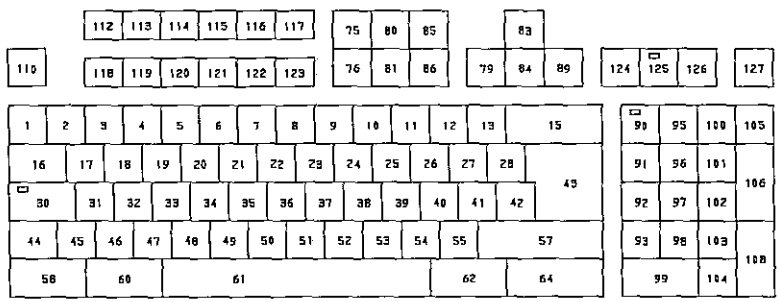


HN1

	SIGNAL NAME
1	$\overline{X0}$
2	$\overline{X1}$
3	$\overline{X2}$
4	$\overline{X3}$
5	$\overline{X4}$
6	$\overline{X5}$
7	$\overline{X6}$
8	$\overline{X7}$
9	$\overline{X8}$
10	$\overline{X9}$
11	$\overline{X10}$
12	$\overline{X11}$
13	$\overline{X12}$
14	$\overline{X13}$
15	$\overline{X14}$
16	$\overline{X15}$
17	$\overline{Y0}$
18	$\overline{Y1}$
19	$\overline{Y2}$
20	$\overline{Y3}$
21	$\overline{Y4}$
22	$\overline{Y5}$
23	$\overline{Y6}$
24	$\overline{Y7}$
25	$\overline{LED1}$
26	$\overline{LED2}$
27	$\overline{LED3}$
28	VCC
29	GND
30	STR

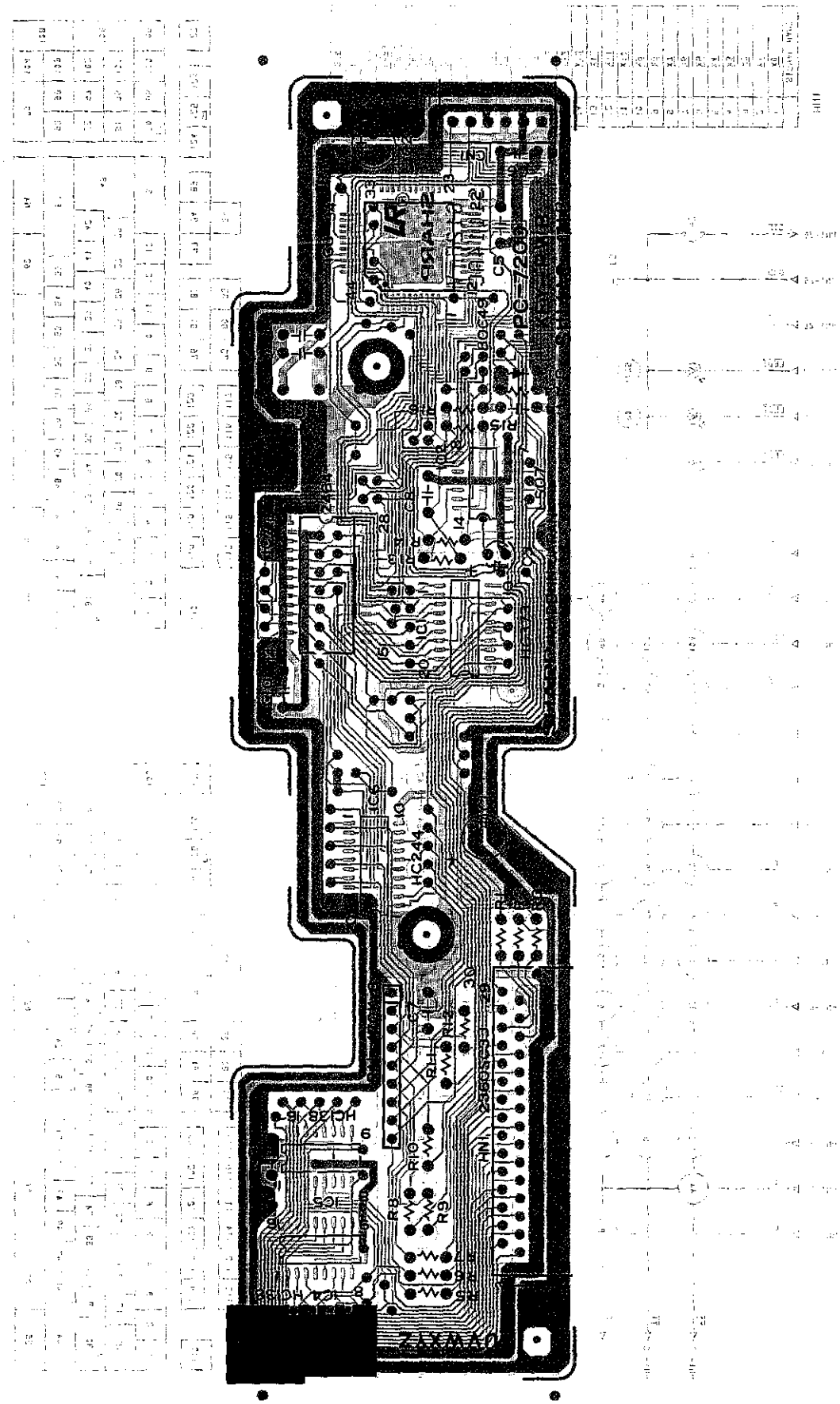


A TYPE (ASCII)



B TYPE (DIN)

CA0-F0253



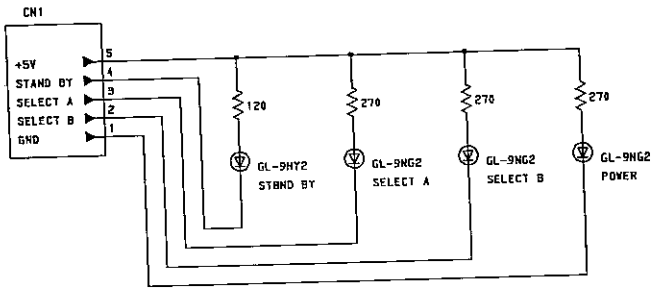
KEY P.W.B.

KEY MATRIX DIAGRAM

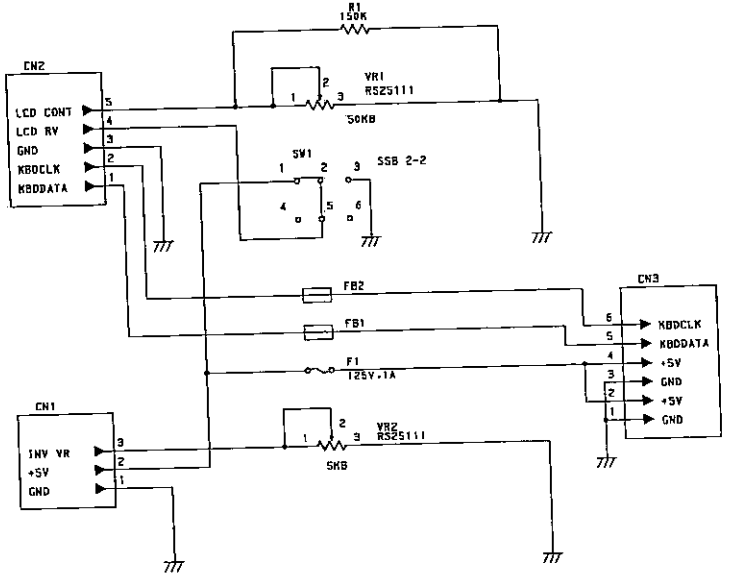
LED PWB/SW, VR PWB

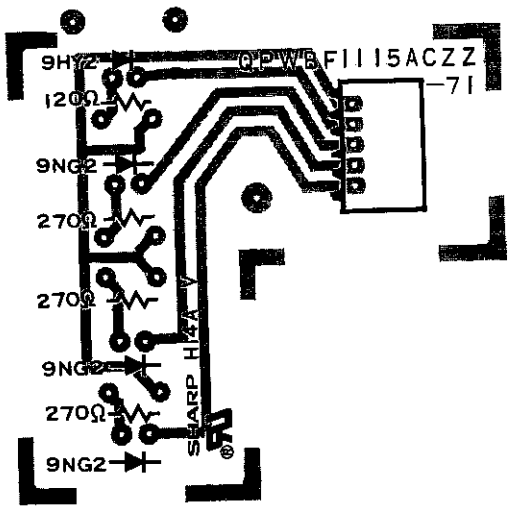
CA-1

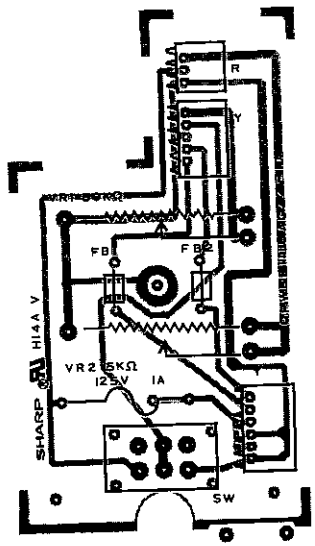
LED PWB



SWVR PWB

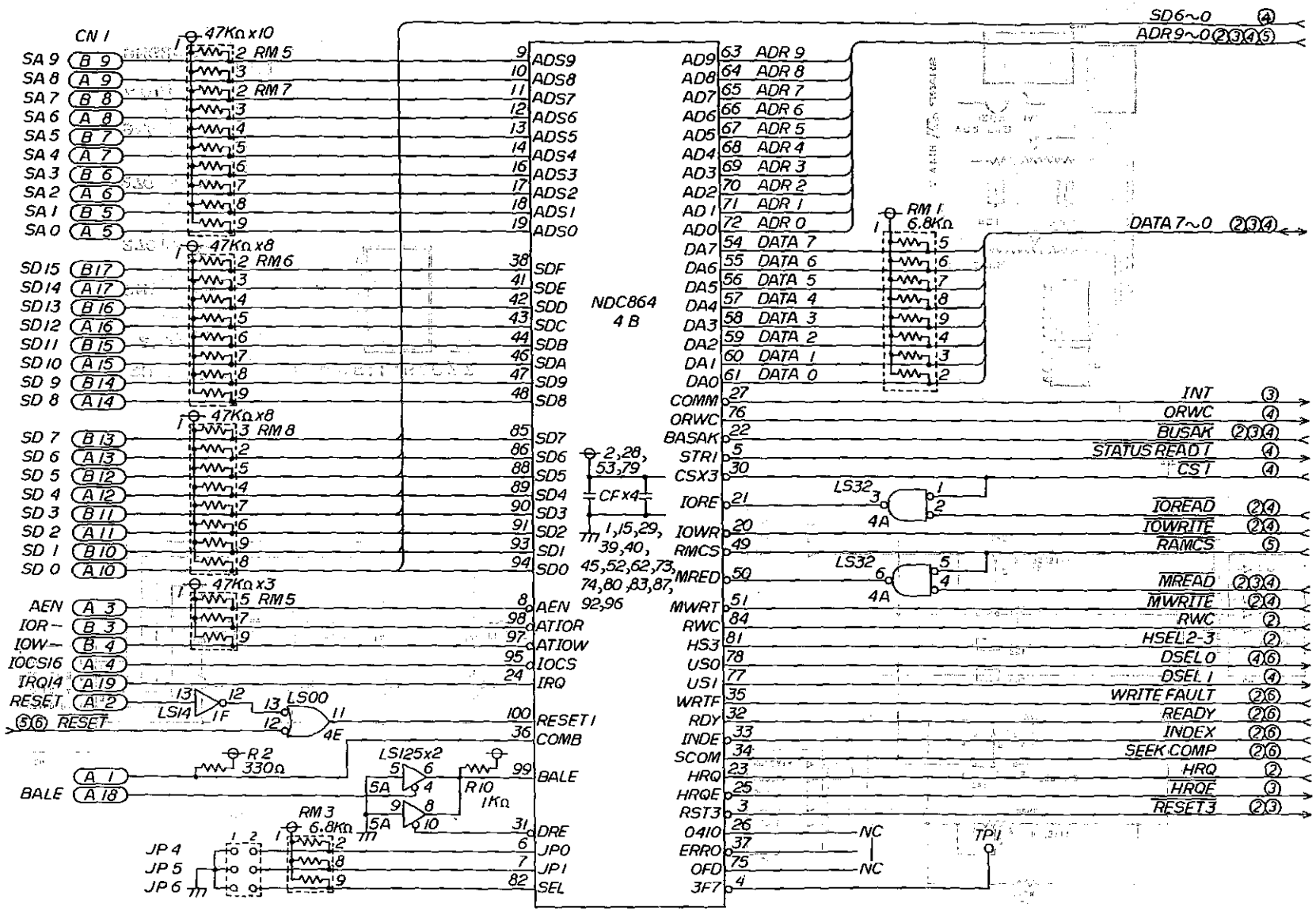




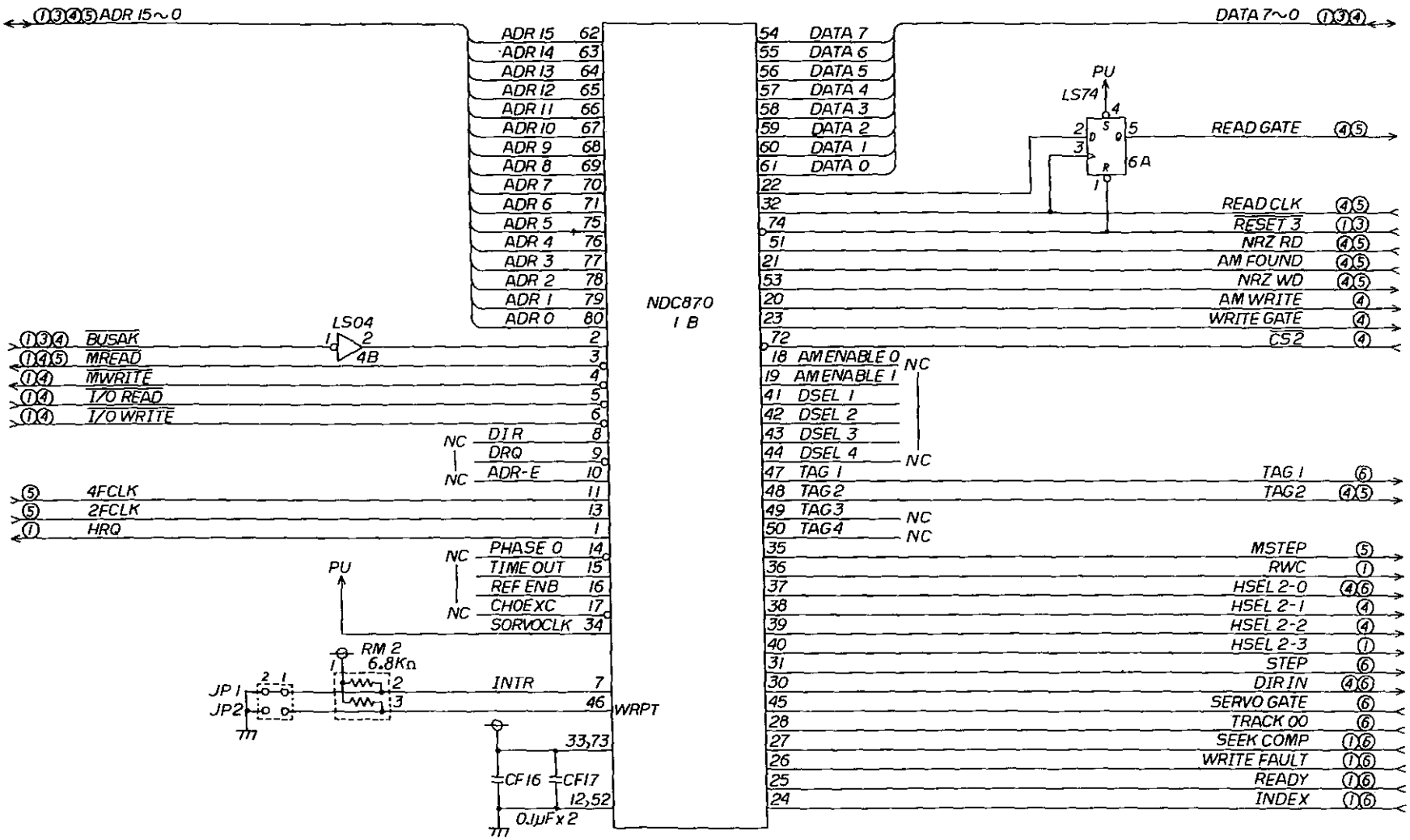


CAD-P0252

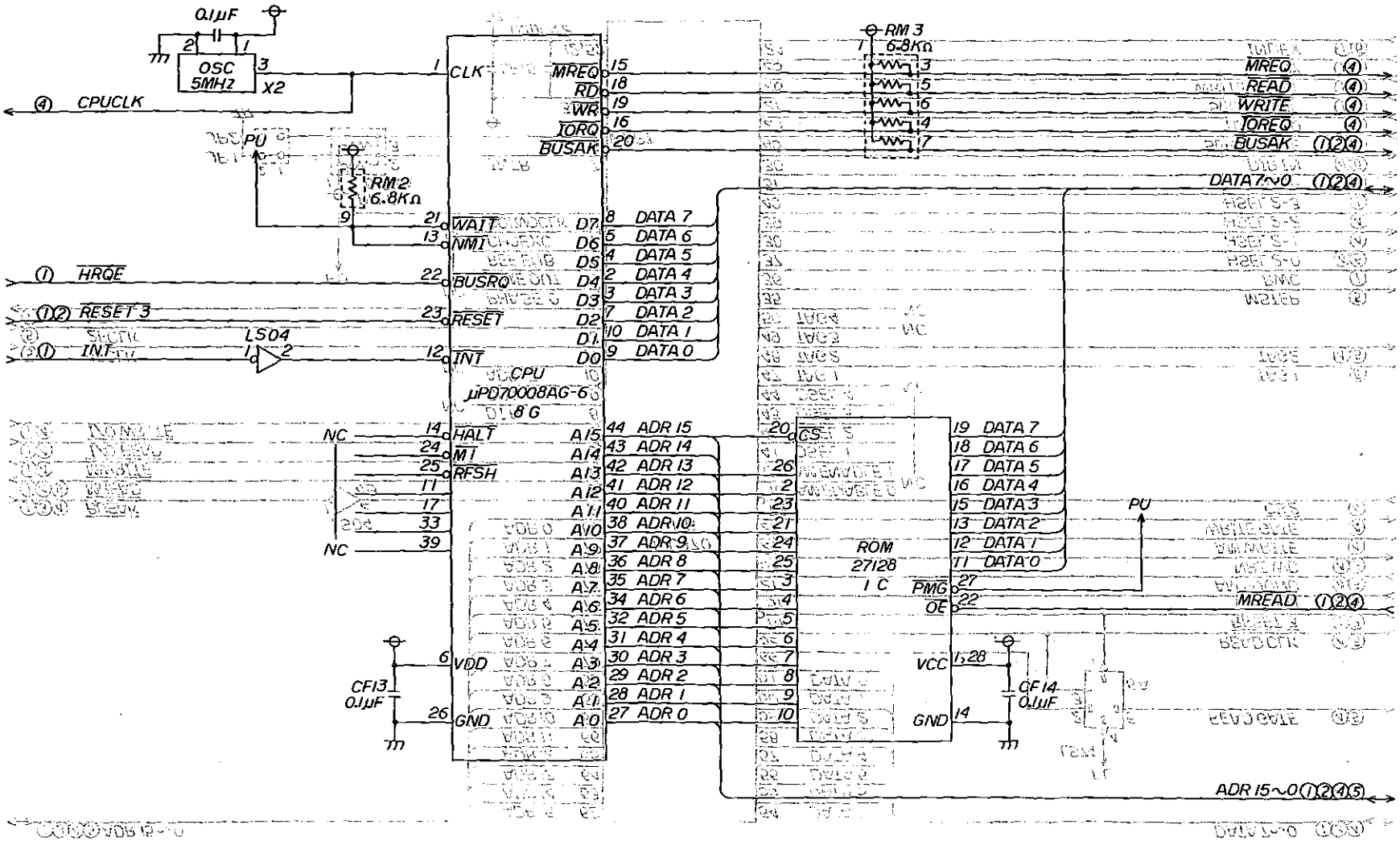
HARD DISK I/F CIRCUIT



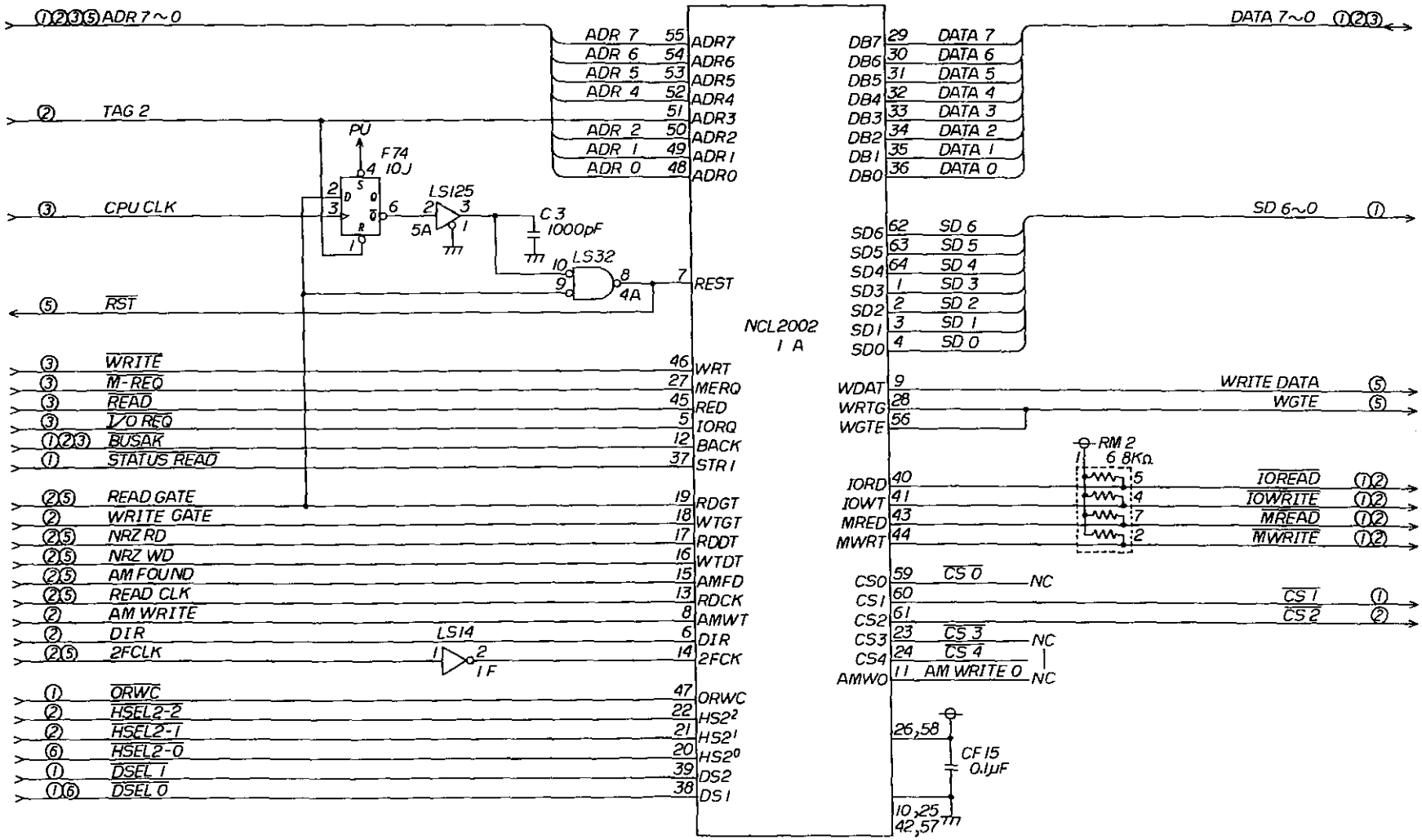
HARD DISK I/F CIRCUIT



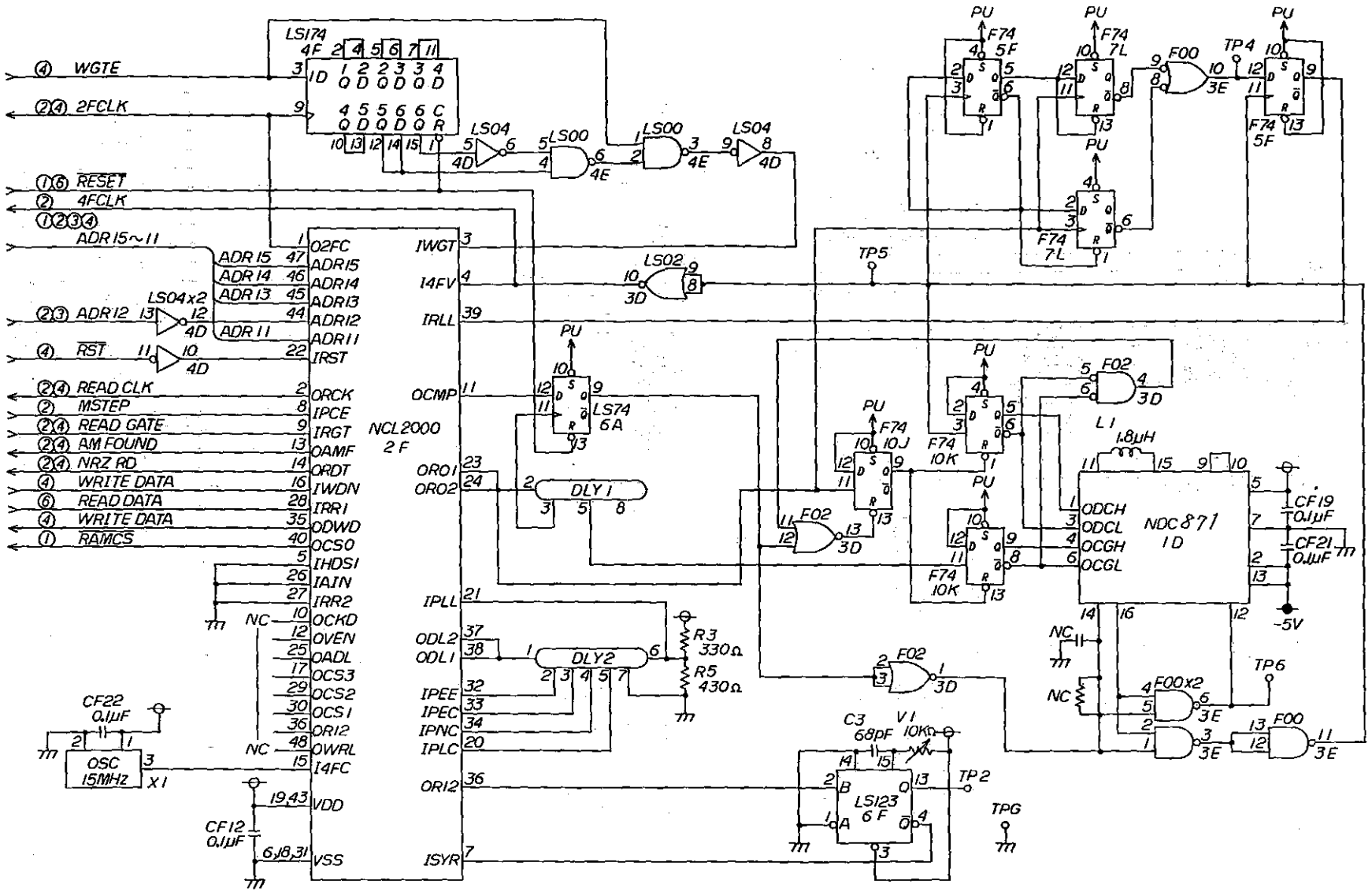
HARD DISK I/F CIRCUIT



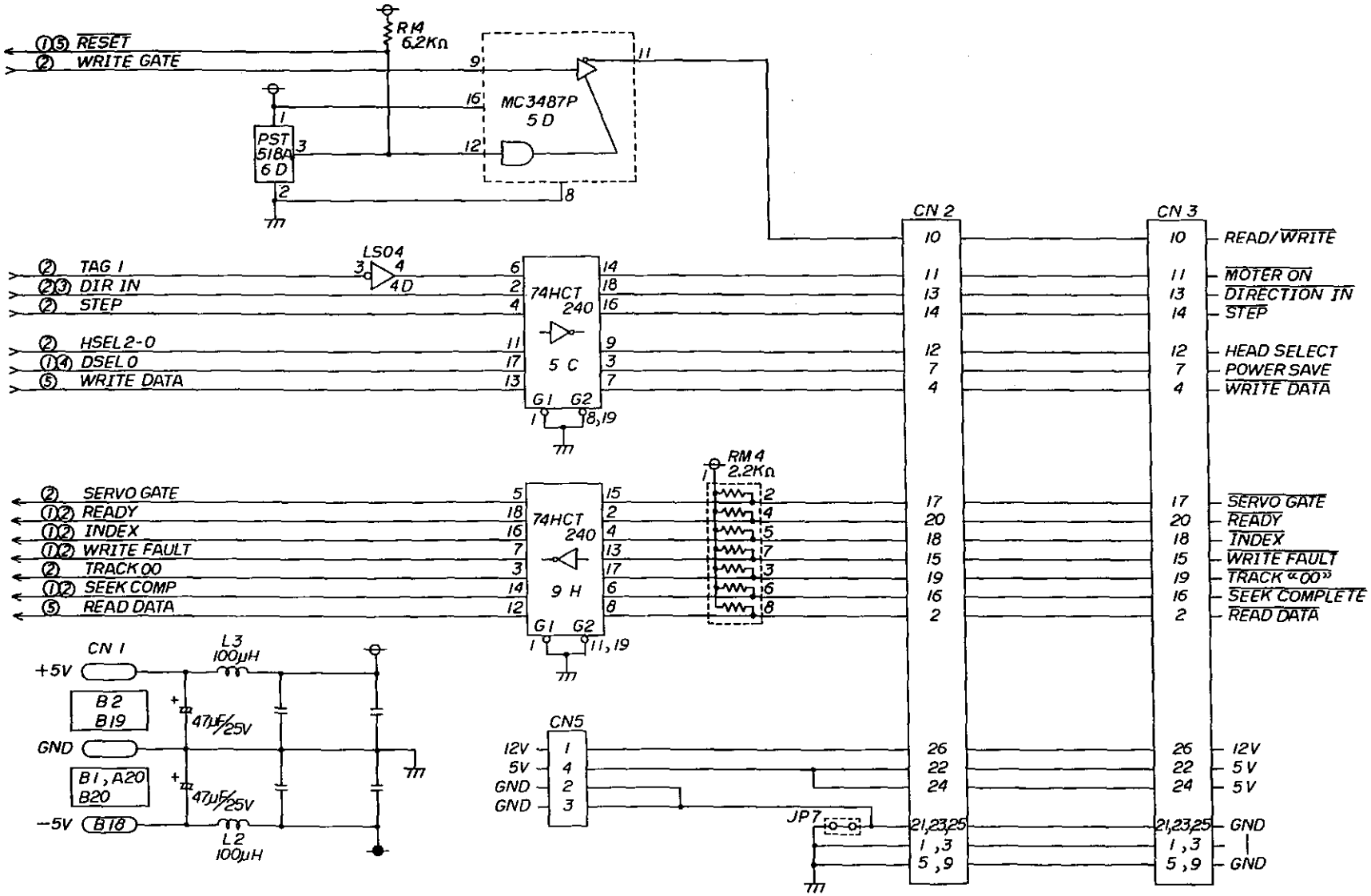
HARD DISK I/F CIRCUIT



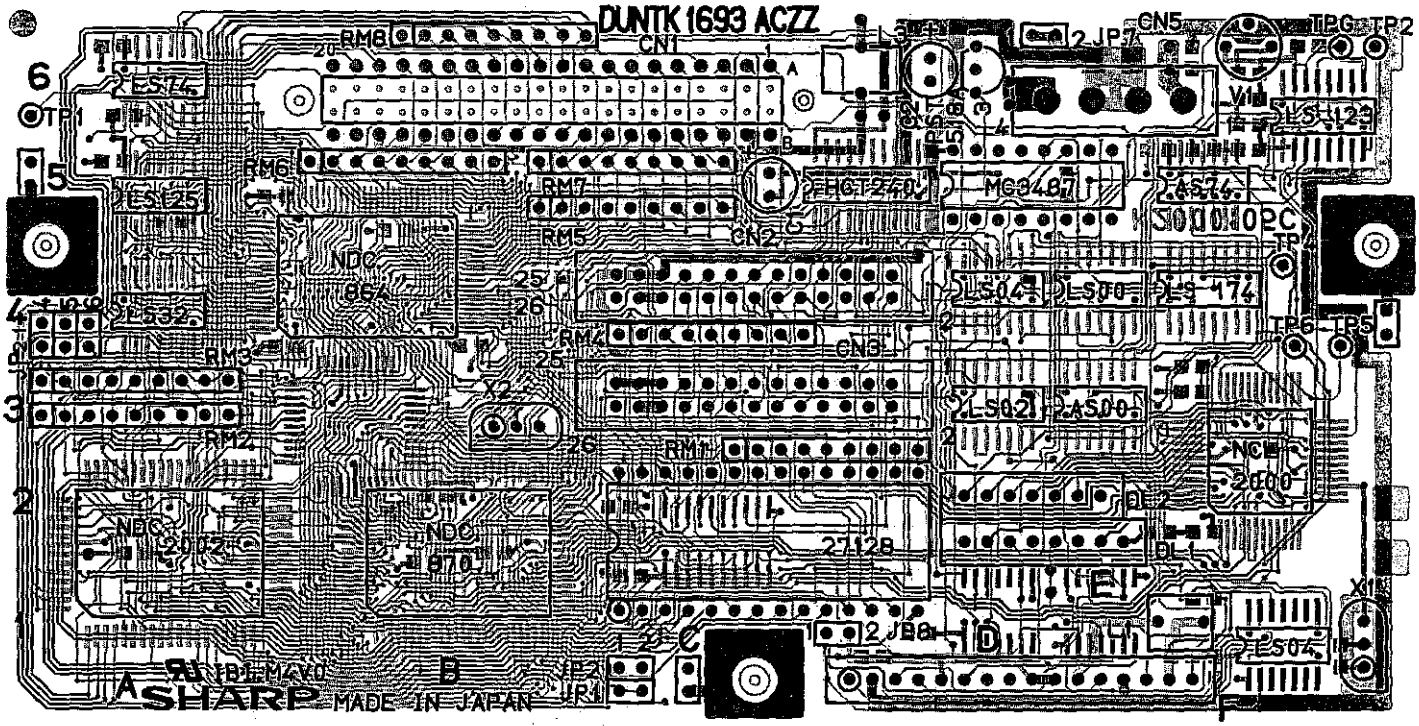
HARD DISK I/F CIRCUIT

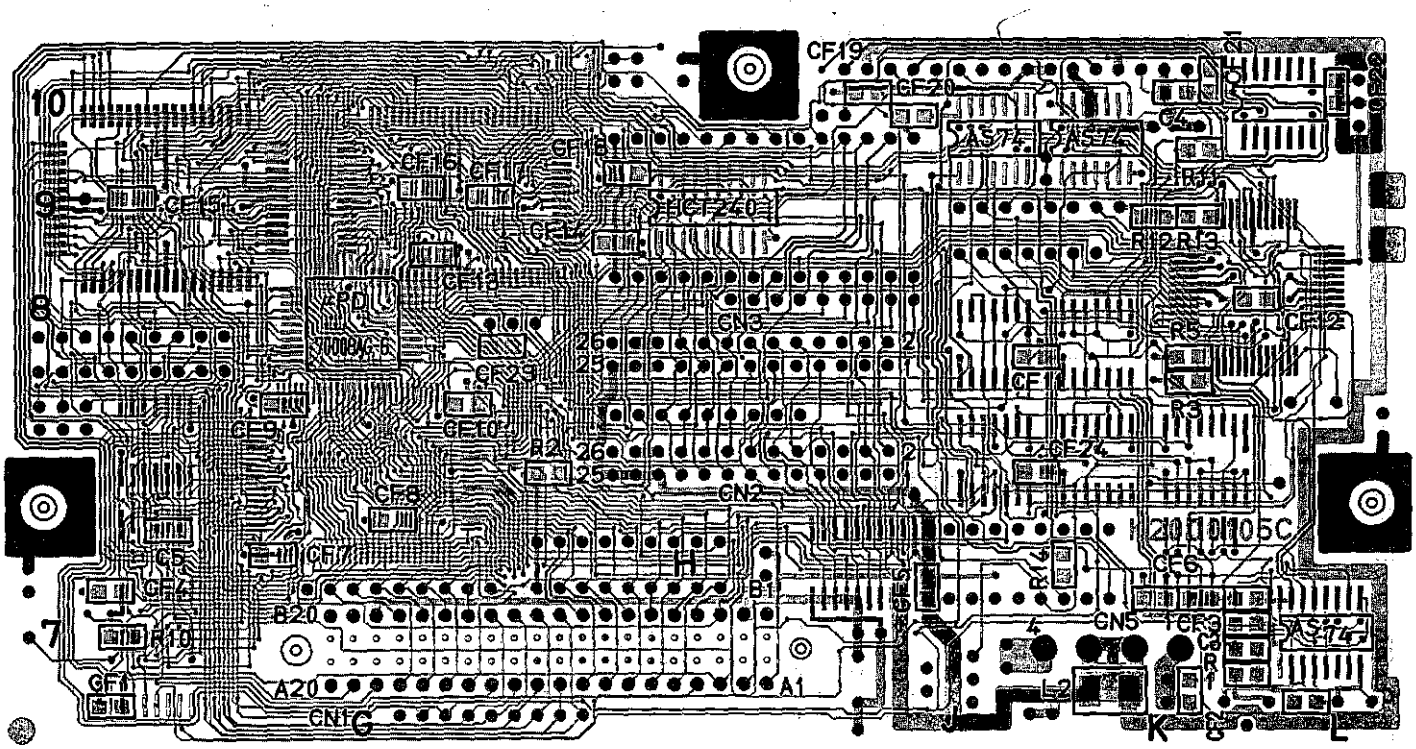


HARD DISK I/F CIRCUIT



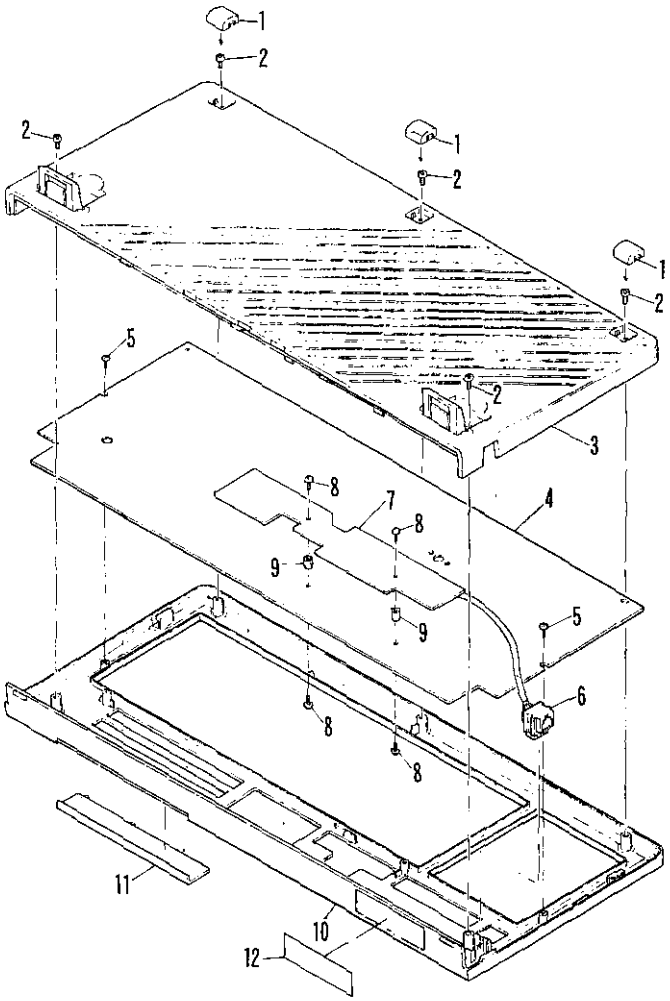
HARD DISK I/F P.W.B.





4 Key exteriors • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	GLEGG2008HCSC	AC	N	C	Key rubber foot	(U,Y)
	GLEGG2008HCSA	AC		C	Key rubber foot	(Other countries)
2	XUBSF30P10000	AA		C	Screw (3×10)	(U,Y)
	XUBSC30P10000	AA	N	C	Screw (3×10)	(Other countries)
3	CCABF2116HC03	AW	N	D	Key bottom housing	(U,Y)
	CCABF2116HC01	AX		D	Key bottom housing	(Other countries)
4	QSW-K1065ACZZ	BS	N	E	Keyboard unit	(U,Y)
	QSW-K1048ACZZ	BS	N	E	Keyboard unit	(H only)
	QSW-K1047ACZZ	BS	N	E	Keyboard unit	(Q,E,T,KE)
	QSW-K1054ACZZ	BS	N	E	Keyboard unit	(KF only)
	QSW-K1053ACZZ	BS	N	E	Keyboard unit	(KG only)
	QSW-K1055ACZZ	BS	N	E	Keyboard unit	(KI only)
	QSW-K1057ACZZ	BS	N	E	Keyboard unit	(KS only)
	QSW-K1058ACZZ	BS	N	E	Keyboard unit	(KW,KX)
5	XUPSD30P08000	AA		C	Screw	
6	QCNW-1235ACZZ	AL	N	C	Key control cable	(U,Y)
	QCNW-1195ACZZ	AL	N	C	Key control cable	(Other countries)
7	CPWBS1114AC02	BQ	N	E	Key PWB unit	(U,Y)
	CPWBS1114AC01	BQ	N	E	Key PWB unit	(Other countries)
8	XBPSD30P04000	AA		C	Screw (3×4)	
9	LX-BZ1020ACZZ	AA	N	C	Screw	
10	GCABE1042ACSA	AN	N	D	Key upper housing	(U,Y)
	GCABE1042ACZZ	AN	N	D	Key upper housing	(Other countries)
11	GCOVH1022ACZZ	AC	N	D	Cover	
12	TLABM1280ACZZ	AC	N	C	Model label	(U,Y)
	TLABM1245ACZZ	AC	N	C	Model label	(H,Q,E,T)
	TLABM1251ACZZ	AC	N	C	Model label	(KE only)
	TLABM1249ACZZ	AC	N	C	Model label	(KF only)
	TLABM1248ACZZ	AC	N	C	Model label	(KG only)
	TLABM1250ACZZ	AC	N	C	Model label	(KI only)
	TLABM1252ACZZ	AC	N	C	Model label	(KS only)
	TLABM1253ACZZ	AC	N	C	Model label	(KW only)
	TLABM1254ACZZ	AC	N	C	Model label	(KX only)
	(Unit)					
901	DUNT-1791ACZZ	CM	N	E	Key unit (U,Y)	(Ref.block 4,5)
	DUNT-1715ACZZ	CM	N	E	Key unit (H only)	(Ref.block 4,5)
	DUNT-1697ACZZ	CM	N	E	Key unit (Q,T,E)	(Ref.block 4,5)



5 Keyboard unit • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	00PA7KEC33A01	AK	N	C	Key top [U,Y]
	00PA7KEC26A01	AK	N	C	Key top [H]
	00PA7KEB99C01	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A01	AK	N	C	Key top [KG]
	00PA7KEC24A01	AK	N	C	Key top [KF]
	00PA7KEC32A01	AK	N	C	Key top [KI]
	00PD2KE042A01	AQ	N	C	Key top [KW,KX]
	00PD2KE041A01	AQ	N	C	Key top [KS]
	00PD2KE041AD7	AQ	N	C	Key top [KD]
	00PD2KE041AE1	AQ	N	C	Key top [KN]
2	00PA7KEC33A02	AK	N	C	Key top [U,Y]
	00PA7KEC26A02	AK	N	C	Key top [H]
	00PA7KEB99C02	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A02	AK	N	C	Key top [KG]
	00PA7KEC24A02	AK	N	C	Key top [KF]
	00PA7KEC32A02	AK	N	C	Key top [KI]
	00PC5KE209B02	AQ	N	C	Key top [KW,KX]
	00PA7KEC23A02	AK	N	C	Key top [KS,KD,KN]
3	00PA7KEC33A03	AK	N	C	Key top [U,Y]
	00PA7KEC26A03	AK	N	C	Key top [H]
	00PA7KEB99C03	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A03	AK	N	C	Key top [KG]
	00PC5KE207A03	AQ	N	C	Key top [KF]
	00PA7KEC32A03	AK	N	C	Key top [KI]
	00PC5KE209B03	AQ	N	C	Key top [KW,KX]
	00PC5KE208A03	AQ	N	C	Key top [KS,KD,KN]
4	00PA7KEC33A04	AK	N	C	Key top [U,Y]
	00PA7KEC26A04	AK	N	C	Key top [H]
	00PA7KEB99C04	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A04	AK	N	C	Key top [KG]
	00PC5KE207A04	AQ	N	C	Key top [KF]
	00PA7KEC32A04	AK	N	C	Key top [KI]
	00PC5KE209B04	AQ	N	C	Key top [KW,KX]
	00PC5KE208A04	AQ	N	C	Key top [KS,KD,KN]
5	00PA7KEC33A05	AK	N	C	Key top [U,Y]
	00PA7KEC26A05	AK	N	C	Key top [H]
	00PA7KEB99C05	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A05	AK	N	C	Key top [KG]
	00PC5KE207A05	AQ	N	C	Key top [KF]
	00PA7KEC32A05	AK	N	C	Key top [KI]
	00PA7KEC28A05	AK	N	C	Key top [KW,KX]
	00PD2KE041A05	AQ	N	C	Key top [KS,KD,KN]
6	00PA7KEC33A06	AK	N	C	Key top [U,Y]
	00PA7KEC26A06	AK	N	C	Key top [H]
	00PA7KEB99C06	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A06	AK	N	C	Key top [KG]
	00PC5KE207A06	AQ	N	C	Key top [KF]
	00PA7KEC32A06	AK	N	C	Key top [KI]
	00PA7KEC28A06	AK	N	C	Key top [KW,KX]
	00PA7KEC23A06	AK	N	C	Key top [KS,KD,KN]
7	00PA7KEC33A07	AK	N	C	Key top [U,Y]
	00PA7KEC26A07	AK	N	C	Key top [H]
	00PA7KEB99C07	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A07	AK	N	C	Key top [KG]
	00PC5KE207A07	AQ	N	C	Key top [KF]
	00PA7KEC32A07	AK	N	C	Key top [KI]
	00PC5KE209B07	AQ	N	C	Key top [KW,KX]
	00PA7KEC23A07	AK	N	C	Key top [KS,KD,KN]
8	00PA7KEC33A08	AK	N	C	Key top [U,Y]
	00PA7KEC26A08	AK	N	C	Key top [H]
	00PA7KEB99C08	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A08	AK	N	C	Key top [KG]
	00PC5KE207A08	AQ	N	C	Key top [KF]
	00PA7KEC32A08	AK	N	C	Key top [KI]
	00PC5KE209B08	AQ	N	C	Key top [KW,KX]
	00PC5KE208A08	AQ	N	C	Key top [KS,KD,KN]
9	00PA7KEC33A09	AK	N	C	Key top [U,Y]
	00PA7KEC26A09	AK	N	C	Key top [H]
	00PA7KEB99C09	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A09	AK	N	C	Key top [KG]
	00PC5KE207A09	AQ	N	C	Key top [KF]
	00PA7KEC32A09	AK	N	C	Key top [KI]
	00PC5KE209B09	AQ	N	C	Key top [KW,KX]
	00PC5KE208A09	AQ	N	C	Key top [KS,KD,KN]
10	00PA7KEC33A10	AK	N	C	Key top [U,Y]
	00PA7KEC26A10	AK	N	C	Key top [H]
	00PA7KEB99C10	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A10	AK	N	C	Key top [KG]
	00PC5KE207A10	AQ	N	C	Key top [KF]
	00PA7KEC32A10	AK	N	C	Key top [KI]

5 Keyboard unit • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
10	00PA7KEC28A10	AK	N	C	Key top	[KW,KX]
	00PC5KE208A10	AQ	N	C	Key top	[KS,KD,KN]
11	00PA7KEC33A11	AK	N	C	Key top	[U,Y]
	00PA7KEC26A11	AK	N	C	Key top	[H]
	00PA7KEB99C11	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A11	AK	N	C	Key top	[KG]
	00PC5KE207A11	AQ	N	C	Key top	[KF]
	00PA7KEC32A11	AK	N	C	Key top	[KI]
	00PA7KEC28A11	AK	N	C	Key top	[KW,KX]
	00PC5KE208A11	AQ	N	C	Key top	[KS,KD,KN]
12	00PA7KEC33A12	AK	N	C	Key top	[U,Y]
	00PA7KEC26A12	AK	N	C	Key top	[H]
	00PA7KEB99C12	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A12	AK	N	C	Key top	[KG]
	00PC5KE207A12	AQ	N	C	Key top	[KF]
	00PA7KEC32A12	AK	N	C	Key top	[KI]
	00PC5KE209B12	AQ	N	C	Key top	[KW,KX]
	00PC5KE208A12	AQ	N	C	Key top	[KS]
	00PA7KEC23AD9	AK	N	C	Key top	[KD,KN]
13	00PA7KEC33A13	AK	N	C	Key top	[U,Y]
	00PA7KEC26A13	AK	N	C	Key top	[H]
	00PA7KEB99C13	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A13	AK	N	C	Key top	[KG]
	00PC5KE207A13	AQ	N	C	Key top	[KF]
	00PA7KEC32A13	AK	N	C	Key top	[KI]
	00PC5KE209B13	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A13	AK	N	C	Key top	[KS]
	00PC5KE208AD8	AQ	N	C	Key top	[KD]
	00PD2KE041AE2	AT	N	C	Key top	[KN]
15	00PA7KEC33A15	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A15	AQ	N	C	Key top	[H]
	00PA7KEB99C15	AQ	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A15	AQ	N	C	Key top	[KG]
	00PA7KEC24A15	AQ	N	C	Key top	[KF]
	00PA7KEC32A15	AQ	N	C	Key top	[KI]
	00PA7KEC28A15	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A15	AQ	N	C	Key top	[KS,KD,KN]
16	00PA7KEC33A16	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A16	AQ	N	C	Key top	[H]
	00PA7KEB99C16	AQ	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A16	AQ	N	C	Key top	[KG]
	00PA7KEC24A16	AQ	N	C	Key top	[KF]
	00PA7KEC32A16	AQ	N	C	Key top	[KI]
	00PA7KEC28A16	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A16	AQ	N	C	Key top	[KS,KD,KN]
17	00PA7KEC33A17	AK	N	C	Key top	[U,Y]
	00PA7KEC26A17	AK	N	C	Key top	[H]
	00PA7KEB99C17	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A17	AK	N	C	Key top	[KG]
	00PA7KEC24A17	AK	N	C	Key top	[KF]
	00PA7KEC32A17	AK	N	C	Key top	[KI]
	00PA7KEC28A17	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A17	AK	N	C	Key top	[KS,KD,KN]
18	00PA7KEC33A18	AK	N	C	Key top	[U,Y]
	00PA7KEC26A18	AK	N	C	Key top	[H]
	00PA7KEB99C18	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A18	AK	N	C	Key top	[KG]
	00PA7KEC24A18	AK	N	C	Key top	[KF]
	00PA7KEC32A18	AK	N	C	Key top	[KI]
	00PA7KEC28A18	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A18	AK	N	C	Key top	[KS,KD,KN]
19	00PA7KEC33A19	AK	N	C	Key top	[U,Y]
	00PA7KEC26A19	AK	N	C	Key top	[H]
	00PA7KEB99C19	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A19	AK	N	C	Key top	[KG]
	00PA7KEC24A19	AK	N	C	Key top	[KF]
	00PA7KEC32A19	AK	N	C	Key top	[KI]
	00PA7KEC28A19	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A19	AK	N	C	Key top	[KS,KD,KN]
20	00PA7KEC33A20	AK	N	C	Key top	[U,Y]
	00PA7KEC26A20	AK	N	C	Key top	[H]
	00PA7KEB99C20	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A20	AK	N	C	Key top	[KG]
	00PA7KEC24A20	AK	N	C	Key top	[KF]
	00PA7KEC32A20	AK	N	C	Key top	[KI]
	00PA7KEC28A20	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A20	AK	N	C	Key top	[KS,KD,KN]
21	00PA7KEC33A21	AK	N	C	Key top	[U,Y]
	00PA7KEC26A21	AK	N	C	Key top	[H]
	00PA7KEB99C21	AK	N	C	Key top	[Q,T,E,KE]

5 Keyboard unit • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
21	00PA7KEC25A21	AK	N	C	Key top [KG]
	00PA7KEC24A21	AK	N	C	Key top [KF]
	00PA7KEC32A21	AK	N	C	Key top [KI]
	00PA7KEC28A21	AK	N	C	Key top [KW,KX]
	00PA7KEC23A21	AK	N	C	Key top [KS,KD,KN]
22	00PA7KEC33A22	AK	N	C	Key top [U,Y]
	00PA7KEC26A22	AK	N	C	Key top [H]
	00PA7KEB99C22	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A22	AK	N	C	Key top [KG]
	00PA7KEC24A22	AK	N	C	Key top [KF]
	00PA7KEC32A22	AK	N	C	Key top [KI]
	00PA7KEC28A22	AK	N	C	Key top [KW,KX]
	00PA7KEC23A22	AK	N	C	Key top [KS,KD,KN]
23	00PA7KEC33A23	AK	N	C	Key top [U,Y]
	00PA7KEC26A23	AK	N	C	Key top [H]
	00PA7KEB99C23	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A23	AK	N	C	Key top [KG]
	00PA7KEC24A23	AK	N	C	Key top [KF]
	00PA7KEC32A23	AK	N	C	Key top [KI]
	00PA7KEC28A23	AK	N	C	Key top [KW,KX]
	00PA7KEC23A23	AK	N	C	Key top [KS,KD,KN]
24	00PA7KEC33A24	AK	N	C	Key top [U,Y]
	00PA7KEC26A24	AK	N	C	Key top [H]
	00PA7KEB99C24	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A24	AK	N	C	Key top [KG]
	00PA7KEC24A24	AK	N	C	Key top [KF]
	00PA7KEC32A24	AK	N	C	Key top [KI]
	00PA7KEC28A24	AK	N	C	Key top [KW,KX]
	00PA7KEC23A24	AK	N	C	Key top [KS,KD,KN]
25	00PA7KEC33A25	AK	N	C	Key top [U,Y]
	00PA7KEC26A25	AK	N	C	Key top [H]
	00PA7KEB99C25	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A25	AK	N	C	Key top [KG]
	00PA7KEC24A25	AK	N	C	Key top [KF]
	00PA7KEC32A25	AK	N	C	Key top [KI]
	00PA7KEC28A25	AK	N	C	Key top [KW,KX]
	00PA7KEC23A25	AK	N	C	Key top [KS,KD,KN]
26	00PA7KEC33A26	AK	N	C	Key top [U,Y]
	00PA7KEC26A26	AK	N	C	Key top [H]
	00PA7KEB99C26	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A26	AK	N	C	Key top [KG]
	00PA7KEC24A26	AK	N	C	Key top [KF]
	00PA7KE032A26	AK	N	C	Key top [KI]
	00PA7KEC28A26	AK	N	C	Key top [KW,KX]
	00PA7KEC23A26	AK	N	C	Key top [KS,KD,KN]
27	00PA7KEC33A27	AK	N	C	Key top [U,Y]
	00PA7KEC26A27	AK	N	C	Key top [H]
	00PA7KEB99C27	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A27	AK	N	C	Key top [KG]
	00PA7KEC24A27	AK	N	C	Key top [KF]
	00PC5KE210A27	AQ	N	C	Key top [KI]
	00PC5KE209B27	AQ	N	C	Key top [KW,KX]
	00PA7KEC23A27	AK	N	C	Key top [KS,KD,KN]
28	00PA7KEC33A28	AK	N	C	Key top [U,Y]
	00PA7KEC26A28	AK	N	C	Key top [H]
	00PA7KEB99C28	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A28	AK	N	C	Key top [KG]
	00PD2KE039A28	AT	N	C	Key top [KF]
	00PD2KE044A28	AT	N	C	Key top [KI]
	00PC5KE209B28	AQ	N	C	Key top [KW,KX]
	00PC5KE208A28	AQ	N	C	Key top [KS,KD,KN]
29	00PA7KEC33A29	AK	N	C	Key top [U,Y]
	00PA7KEB99C29	AK	N	C	Key top [Q,T,E,KE]
30	00PD2KE045A30	AT	N	C	Key top [U,Y]
	00PD2KE043A30	AT	N	C	Key top [H]
	00PD2KE037A30	AT	N	C	Key top [Q,T,E,KE]
	00PD2KE038A30	AT	N	C	Key top [KG]
	00PD2KE039A30	AT	N	C	Key top [KF]
	00PD2KE044A30	AT	N	C	Key top [KI]
	00PD2KE042A30	AT	N	C	Key top [KW,KX]
	00PD2KE041A30	AT	N	C	Key top [KS,KD,KN]
31	00PA7KEC33A31	AK	N	C	Key top [U,Y]
	00PA7KEC26A31	AK	N	C	Key top [H]
	00PA7KEB99C31	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A31	AK	N	C	Key top [KG]
	00PA7KEC24A31	AK	N	C	Key top [KF]
	00PA7KE032A31	AK	N	C	Key top [KI]
	00PA7KEC28A31	AK	N	C	Key top [KW,KX]
	00PA7KEC23A31	AK	N	C	Key top [KS,KD,KN]
32	00PA7KEC33A32	AK	N	C	Key top [U,Y]

5 Keyboard unit • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
	00PA7KEC26A32	AK	N	C	Key top [H]
	00PA7KEB99C32	AK	N	C	Key top [Q,T,E,KE]
	00PA7KEC25A32	AK	N	C	Key top [KG]
32	00PA7KEC24A32	AK	N	C	Key top [KF]
	00PA7KE032A32	AK	N	C	Key top [KI]
	00PA7KEC28A32	AK	N	C	Key top [KW,KX]
	00PA7KEC23A32	AK	N	C	Key top [KS,KD,KN]
	00PA7KEC33A33	AK	N	C	Key top [U,Y]
	00PA7KEC26A33	AK	N	C	Key top [H]
	00PA7KEB99C33	AK	N	C	Key top [Q,T,E,KE]
33	00PA7KEC25A33	AK	N	C	Key top [KG]
	00PA7KEC24A33	AK	N	C	Key top [KF]
	00PA7KE032A33	AK	N	C	Key top [KI]
	00PA7KEC28A33	AK	N	C	Key top [KW,KX]
	00PA7KEC23A33	AK	N	C	Key top [KS,KD,KN]
	00PA7KEC33A34	AK	N	C	Key top [U,Y]
	00PA7KEC26A34	AK	N	C	Key top [H]
	00PA7KEB99C34	AK	N	C	Key top [Q,T,E,KE]
34	00PA7KEC25A34	AK	N	C	Key top [KG]
	00PA7KEC24A34	AK	N	C	Key top [KF]
	00PA7KE032A34	AK	N	C	Key top [KI]
	00PA7KEC28A34	AK	N	C	Key top [KW,KX]
	00PA7KEC23A34	AK	N	C	Key top [KS,KD,KN]
	00PA7KEC33A35	AK	N	C	Key top [U,Y]
	00PA7KEC26A35	AK	N	C	Key top [H]
	00PA7KEB99C35	AK	N	C	Key top [Q,T,E,KE]
35	00PA7KEC25A35	AK	N	C	Key top [KG]
	00PA7KEC24A35	AK	N	C	Key top [KF]
	00PA7KE032A35	AK	N	C	Key top [KI]
	00PA7KEC28A35	AK	N	C	Key top [KW,KX]
	00PA7KEC23A35	AK	N	C	Key top [KS,KD,KN]
	00PA7KEC33A36	AK	N	C	Key top [U,Y]
	00PA7KEC26A36	AK	N	C	Key top [H]
	00PA7KEB99C36	AK	N	C	Key top [Q,T,E,KE]
36	00PA7KEC25A36	AK	N	C	Key top [KG]
	00PA7KEC24A36	AK	N	C	Key top [KF]
	00PA7KE032A36	AK	N	C	Key top [KI]
	00PA7KEC28A36	AK	N	C	Key top [KW,KX]
	00PA7KEC23A36	AK	N	C	Key top [KS,KD,KN]
	00PA7KEC33A37	AK	N	C	Key top [U,Y]
	00PA7KEC26A37	AK	N	C	Key top [H]
	00PA7KEB99C37	AK	N	C	Key top [Q,T,E,KE]
37	00PA7KEC25A37	AK	N	C	Key top [KG]
	00PA7KEC24A37	AK	N	C	Key top [KF]
	00PA7KE032A37	AK	N	C	Key top [KI]
	00PA7KEC28A37	AK	N	C	Key top [KW,KX]
	00PA7KEC23A37	AK	N	C	Key top [KS,KD,KN]
	00PA7KEC33A38	AK	N	C	Key top [U,Y]
	00PA7KEC26A38	AK	N	C	Key top [H]
	00PA7KEB99C38	AK	N	C	Key top [Q,T,E,KE]
38	00PA7KEC25A38	AK	N	C	Key top [KG]
	00PA7KEC24A38	AK	N	C	Key top [KF]
	00PA7KE032A38	AK	N	C	Key top [KI]
	00PA7KEC28A38	AK	N	C	Key top [KW,KX]
	00PA7KEC23A38	AK	N	C	Key top [KS,KD,KN]
	00PA7KEC33A39	AK	N	C	Key top [U,Y]
	00PA7KEC26A39	AK	N	C	Key top [H]
	00PA7KEB99C39	AK	N	C	Key top [Q,T,E,KE]
39	00PA7KEC25A39	AK	N	C	Key top [KG]
	00PA7KEC24A39	AK	N	C	Key top [KF]
	00PA7KE032A39	AK	N	C	Key top [KI]
	00PA7KEC28A39	AK	N	C	Key top [KW,KX]
	00PA7KEC23A39	AK	N	C	Key top [KS,KD,KN]
	00PA7KEC33A40	AK	N	C	Key top [U,Y]
	00PA7KEC26A40	AK	N	C	Key top [H]
	00PA7KEB99C40	AK	N	C	Key top [Q,T,E,KE]
40	00PA7KEC25A40	AK	N	C	Key top [KG]
	00PA7KEC24A40	AK	N	C	Key top [KF]
	00PD2KE044A40	AT	N	C	Key top [KI]
	00PA7KEC28A40	AK	N	C	Key top [KW,KX]
	00PA7KEC23A40	AK	N	C	Key top [KS]
	00PA7KEC23AD6	AK	N	C	Key top [KD,KN]
	00PA7KEC33A41	AK	N	C	Key top [U,Y]
	00PD2KE043A41	AQ	N	C	Key top [H]
	00PA7KEB99C41	AK	N	C	Key top [Q,T,E,KE]
41	00PA7KEC25A41	AK	N	C	Key top [KG]
	00PA7KEC24A41	AK	N	C	Key top [KF]
	00PD2KE044A41	AT	N	C	Key top [KI]
	00PC5KE209B41	AQ	N	C	Key top [KW,KX]
	00PA7KEC23A41	AK	N	C	Key top [KS]

5 Keyboard unit • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
41	00PA7KEC23AD5	AK	N	C	Key top	[KS,KD,KN]
42	00PA7KEC26A42	AK	N	C	Key top	[H]
	00PA7KEC25A42	AK	N	C	Key top	[KG]
	00PA7KEC24A42	AK	N	C	Key top	[KF]
	00PA7KE032A42	AK	N	C	Key top	[KI]
	00PD2KE042A42	AT	N	C	Key top	[KW,KX]
	00PD2KE041A42	AQ	N	C	Key top	[KS,KD,KN]
43	00PA7KEC33A43	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A43	AQ	N	C	Key top	[H]
	00PA7KEB99C43	AQ	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A43	AQ	N	C	Key top	[KG]
	00PA7KEC24A43	AQ	N	C	Key top	[KF]
	00PA7KE032A43	AQ	N	C	Key top	[KI]
	00PA7KEC28A43	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A43	AQ	N	C	Key top	[KS,KD,KN]
44	00PA7KEC33A44	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A44	AQ	N	C	Key top	[H]
	00PA7KEB99C44	AQ	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A44	AQ	N	C	Key top	[KG]
	00PA7KEC24A44	AQ	N	C	Key top	[KF]
	00PA7KEC32A44	AQ	N	C	Key top	[KI]
	00PA7KEC28A44	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A44	AQ	N	C	Key top	[KS,KD,KN]
45	00PA7KEC26A45	AK	N	C	Key top	[H]
	00PA7KEC25A45	AK	N	C	Key top	[KG]
	00PA7KEC24A45	AK	N	C	Key top	[KF]
	00PA7KEC32A45	AK	N	C	Key top	[KI]
	00PC5KE209B45	AQ	N	C	Key top	[KW,KX]
	00PC5KE208A45	AQ	N	C	Key top	[KS]
	00PC5KE208AD3	AQ	N	C	Key top	[KD]
	0,0PA7KEC23AD4	AK	N	C	Key top	[KN]
46	00PA7KEC33A46	AK	N	C	Key top	[U,Y]
	00PA7KEC26A46	AK	N	C	Key top	[H]
	00PA7KEB99C46	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A46	AK	N	C	Key top	[KG]
	00PA7KEC24A46	AK	N	C	Key top	[KF]
	00PA7KEC32A46	AK	N	C	Key top	[KI]
	00PA7KEC28A46	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A46	AK	N	C	Key top	[KS,KD,KN]
47	00PA7KEC33A47	AK	N	C	Key top	[U,Y]
	00PA7KEC26A47	AK	N	C	Key top	[H]
	00PA7KEB99C47	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A47	AK	N	C	Key top	[KG]
	00PA7KEC24A47	AK	N	C	Key top	[KF]
	00PA7KEC32A47	AK	N	C	Key top	[KI]
	00PA7KEC28A47	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A47	AK	N	C	Key top	[KS,KD,KN]
48	00PA7KEC33A48	AK	N	C	Key top	[U,Y]
	00PA7KEC26A48	AK	N	C	Key top	[H]
	00PA7KEB99C48	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A48	AK	N	C	Key top	[KG]
	00PA7KEC24A48	AK	N	C	Key top	[KF]
	00PA7KEC32A48	AK	N	C	Key top	[KI]
	00PA7KEC28A48	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A48	AK	N	C	Key top	[KS,KD,KN]
49	00PA7KEC33A49	AK	N	C	Key top	[U,Y]
	00PA7KEC26A49	AK	N	C	Key top	[H]
	00PA7KEB99C49	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A49	AK	N	C	Key top	[KG]
	00PA7KEC24A49	AK	N	C	Key top	[KF]
	00PA7KEC32A49	AK	N	C	Key top	[KI]
	00PA7KEC28A49	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A49	AK	N	C	Key top	[KS,KD,KN]
50	00PA7KEC33A50	AK	N	C	Key top	[U,Y]
	00PA7KEC26A50	AK	N	C	Key top	[H]
	00PA7KEB99C50	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A50	AK	N	C	Key top	[KG]
	00PA7KEC24A50	AK	N	C	Key top	[KF]
	00PA7KEC32A50	AK	N	C	Key top	[KI]
	00PA7KEC28A50	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A50	AK	N	C	Key top	[KS,KD,KN]
51	00PA7KEC33A51	AK	N	C	Key top	[U,Y]
	00PA7KEC26A51	AK	N	C	Key top	[H]
	00PA7KEB99C51	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A51	AK	N	C	Key top	[KG]
	00PA7KEC24A51	AK	N	C	Key top	[KF]
	00PA7KEC32A51	AK	N	C	Key top	[KI]
	00PA7KEC28A51	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A51	AK	N	C	Key top	[KS,KD,KN]
52	00PA7KEC33A52	AK	N	C	Key top	[U,Y]

5 Keyboard unit • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
	00PA7KEC26A52	AK	N	C	Key top	[H]
	00PA7KEB99C52	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A52	AK	N	C	Key top	[KG]
52	00PA7KEC24A52	AK	N	C	Key top	[KF]
	00PA7KEC32A52	AK	N	C	Key top	[KI]
	00PA7KEC28A52	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A52	AK	N	C	Key top	[KS,KD,KN]
	00PA7KEC33A53	AK	N	C	Key top	[U,Y]
	00PA7KEC26A53	AK	N	C	Key top	[H]
	00PA7KEB99C53	AK	N	C	Key top	[Q,T,E,KE]
53	00PA7KEC25A53	AK	N	C	Key top	[KG]
	00PA7KEC24A53	AK	N	C	Key top	[KF]
	00PA7KEC32A53	AK	N	C	Key top	[KI]
	00PA7KEC28A53	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A53	AK	N	C	Key top	[KS,KD,KN]
	00PA7KEC33A54	AK	N	C	Key top	[U,Y]
	00PA7KEC26A54	AK	N	C	Key top	[H]
	00PA7KEB99C54	AK	N	C	Key top	[Q,T,E,KE]
54	00PA7KEC25A54	AK	N	C	Key top	[KG]
	00PA7KEC24A54	AK	N	C	Key top	[KF]
	00PA7KEC32A54	AK	N	C	Key top	[KI]
	00PA7KEC28A54	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A54	AK	N	C	Key top	[KS,KD,KN]
	00PA7KEC33A55	AK	N	C	Key top	[U,Y]
	00PA7KEC26A55	AK	N	C	Key top	[H]
	00PA7KEB99C55	AK	N	C	Key top	[Q,T,E,KE]
55	00PA7KEC25A55	AK	N	C	Key top	[KG]
	00PA7KEC24A55	AK	N	C	Key top	[KF]
	00PA7KEC32A55	AK	N	C	Key top	[KI]
	00PA7KEC28A55	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A55	AK	N	C	Key top	[KS,KD,KN]
	00PA7KEC33A57	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A57	AQ	N	C	Key top	[H]
	00PA7KEB99C57	AQ	N	C	Key top	[Q,T,E,KE]
57	00PA7KEC25A57	AQ	N	C	Key top	[KG]
	00PA7KEC24A57	AQ	N	C	Key top	[KF]
	00PA7KEC32A57	AQ	N	C	Key top	[KI]
	00PA7KEC28A57	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A57	AQ	N	C	Key top	[KS,KD,KN]
	00PA7KEC33A58	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A58	AQ	N	C	Key top	[H]
	00PA7KEB99C58	AQ	N	C	Key top	[Q,T,E,KE]
58	00PA7KEC25A58	AQ	N	C	Key top	[KG]
	00PA7KEC24A58	AQ	N	C	Key top	[KF]
	00PA7KEC32A58	AQ	N	C	Key top	[KI]
	00PA7KEC28A58	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A58	AQ	N	C	Key top	[KS,KD,KN]
	00PA7KEC33A60	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A60	AQ	N	C	Key top	[H]
	00PA7KEB99C60	AQ	N	C	Key top	[Q,T,E,KE]
60	00PA7KEC25A60	AQ	N	C	Key top	[KG]
	00PA7KEC24A60	AQ	N	C	Key top	[KF]
	00PA7KEC32A60	AQ	N	C	Key top	[KI]
	00PA7KEC28A60	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A60	AQ	N	C	Key top	[KS,KD,KN]
61	00P80L7E43000	AQ	N	C	Key top (Space)(8)	[U,Y]
	00P80L7C52000	AQ		C	Key top (Space)(8)	[Other countries]
	00PA7KEC33A62	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A62	AQ	N	C	Key top	[H]
	00PA7KEB99C62	AQ	N	C	Key top	[Q,T,E,KE]
62	00PA7KEC25A62	AQ	N	C	Key top	[KG]
	00PA7KEC24A62	AQ	N	C	Key top	[KF]
	00PA7KEC32A62	AQ	N	C	Key top	[KI]
	00PA7KEC28A62	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A62	AQ	N	C	Key top	[KS,KD,KN]
	00PA7KEC33A64	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A64	AQ	N	C	Key top	[H]
	00PA7KEB99C64	AQ	N	C	Key top	[Q,T,E,KE]
64	00PA7KEC25A64	AQ	N	C	Key top	[KG]
	00PA7KEC24A64	AQ	N	C	Key top	[KF]
	00PA7KEC32A64	AQ	N	C	Key top	[KI]
	00PA7KEC28A64	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A64	AQ	N	C	Key top	[KS,KD,KN]
	00PA7KEC33A75	AK	N	C	Key top	[U,Y]
	00PA7KEC26A75	AK	N	C	Key top	[H]
	00PA7KEB99C75	AK	N	C	Key top	[Q,T,E,KE]
75	00PD2KE038A75	AQ	N	C	Key top	[KG]
	00PA7KEC24A75	AK	N	C	Key top	[KF]
	00PA7KEC32A75	AK	N	C	Key top	[KI]
	00PA7KEC28A75	AK	N	C	Key top	[KW,KX]

5 Keyboard unit • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
75	00PA7KEC23A75	AK	N	C	Key top	[KS,KD,KN]
76	00PA7KEC33A76	AK	N	C	Key top	[U,Y]
	00PA7KEC26A76	AK	N	C	Key top	[H]
	00PA7KEB99C76	AK	N	C	Key top	[Q,T,E,KE]
	00PD2KE038A76	AQ	N	C	Key top	[KG]
	00PD2KE039A76	AQ	N	C	Key top	[KF]
	00PD2KE044A76	AQ	N	C	Key top	[KI]
	00PA7KEC28A76	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A76	AK	N	C	Key top	[KS,KD,KN]
79	00PA7KEC33A79	AK	N	C	Key top	[U,Y]
	00PA7KEC26A79	AK	N	C	Key top	[H]
	00PA7KEB99C79	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A79	AK	N	C	Key top	[KG]
	00PA7KEC24A79	AK	N	C	Key top	[KF]
	00PA7KEC32A79	AK	N	C	Key top	[KI]
	00PA7KEC28A79	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A79	AK	N	C	Key top	[KS,KD,KN]
80	00PA7KEC33A80	AK	N	C	Key top	[U,Y]
	00PA7KEC26A80	AK	N	C	Key top	[H]
	00PA7KEB99C80	AK	N	C	Key top	[Q,T,E,KE]
	00PD2KE038A80	AQ	N	C	Key top	[KG]
	00PA7KEC24A80	AK	N	C	Key top	[KF]
	00PA7KEC32A80	AK	N	C	Key top	[KI]
	00PA7KEC28A80	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A80	AK	N	C	Key top	[KS,KD,KN]
81	00PA7KEC33A81	AK	N	C	Key top	[U,Y]
	00PA7KEC26A81	AK	N	C	Key top	[H]
	00PA7KEB99C81	AK	N	C	Key top	[Q,T,E,KE]
	00PD2KE038A81	AQ	N	C	Key top	[KG]
	00PD2KE039A81	AQ	N	C	Key top	[KF]
	00PD2KE044A81	AQ	N	C	Key top	[KI]
	00PA7KEC28A81	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A81	AK	N	C	Key top	[KS,KD,KN]
83	00PA7KEC33A83	AK	N	C	Key top	[U,Y]
	00PA7KEC26A83	AK	N	C	Key top	[H]
	00PA7KEB99C83	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A83	AK	N	C	Key top	[KG]
	00PA7KEC24A83	AK	N	C	Key top	[KF]
	00PA7KEC32A83	AK	N	C	Key top	[KI]
	00PA7KEC28A83	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A83	AK	N	C	Key top	[KS,KD,KN]
84	00PA7KEC33A84	AK	N	C	Key top	[U,Y]
	00PA7KEC26A84	AK	N	C	Key top	[H]
	00PA7KEB99C84	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A84	AK	N	C	Key top	[KG]
	00PA7KEC24A84	AK	N	C	Key top	[KF]
	00PA7KEC32A84	AK	N	C	Key top	[KI]
	00PA7KEC28A84	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A84	AK	N	C	Key top	[KS,KD,KN]
85	00PA7KEC33A85	AK	N	C	Key top	[U,Y]
	00PA7KEC26A85	AK	N	C	Key top	[H]
	00PA7KEB99C85	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A85	AK	N	C	Key top	[KG]
	00PA7KEC24A85	AK	N	C	Key top	[KF]
	00PA7KEC32A85	AK	N	C	Key top	[KI]
	00PA7KEC28A85	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A85	AK	N	C	Key top	[KS,KD,KN]
86	00PA7KEC33A86	AK	N	C	Key top	[U,Y]
	00PA7KEC26A86	AK	N	C	Key top	[H]
	00PA7KEB99C86	AK	N	C	Key top	[Q,T,E,KE]
	00PD2KE038A86	AQ	N	C	Key top	[KG]
	00PD2KE039A86	AQ	N	C	Key top	[KF]
	00PD2KE044A86	AQ	N	C	Key top	[KI]
	00PA7KEC28A86	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A86	AK	N	C	Key top	[KS,KD,KN]
89	00PA7KEC33A89	AK	N	C	Key top	[U,Y]
	00PA7KEC26A89	AK	N	C	Key top	[H]
	00PA7KEB99C89	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A89	AK	N	C	Key top	[KG]
	00PA7KEC24A89	AK	N	C	Key top	[KF]
	00PA7KEC32A89	AK	N	C	Key top	[KI]
	00PA7KEC28A89	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A89	AK	N	C	Key top	[KS,KD,KN]
90	00PD2KE045A90	AQ	N	C	Key top	[U,Y]
	00PD2KE043A90	AQ	N	C	Key top	[H]
	00PD2KE037A90	AQ	N	C	Key top	[Q,T,E,KE]
	00PD2KE038A90	AQ	N	C	Key top	[KG]
	00PD2KE039A90	AQ	N	C	Key top	[KF]
	00PD2KE044A90	AQ	N	C	Key top	[KI]
	00PD2KE042A90	AQ	N	C	Key top	[KW,KX]

5 Keyboard unit • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
90	00PD2KE041A90	AQ	N	C	Key top	[KS,KD,KN]
91	00PA7KEC33A91	AK	N	C	Key top	[U,Y]
	00PA7KEC26A91	AK	N	C	Key top	[H]
	00PA7KEB99C91	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A91	AK	N	C	Key top	[KG]
	00PA7KEC24A91	AK	N	C	Key top	[KF]
	00PA7KE032A91	AK	N	C	Key top	[KI]
	00PA7KEC28A91	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A91	AK	N	C	Key top	[KS,KD,KN]
92	00PA7KEC33A92	AK	N	C	Key top	[U,Y]
	00PA7KEC26A92	AK	N	C	Key top	[H]
	00PA7KEB99C92	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A92	AK	N	C	Key top	[KG]
	00PA7KEC24A92	AK	N	C	Key top	[KF]
	00PA7KE032A92	AK	N	C	Key top	[KI]
	00PA7KEC28A92	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A92	AK	N	C	Key top	[KS,KD,KN]
93	00PA7KEC33A93	AK	N	C	Key top	[U,Y]
	00PA7KEC26A93	AK	N	C	Key top	[H]
	00PA7KEB99C93	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A93	AK	N	C	Key top	[KG]
	00PA7KEC24A93	AK	N	C	Key top	[KF]
	00PA7KE032A93	AK	N	C	Key top	[KI]
	00PA7KEC28A93	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A93	AK	N	C	Key top	[KS,KD,KN]
95	00PA7KEC33A95	AK	N	C	Key top	[U,Y]
	00PA7KEC26A95	AK	N	C	Key top	[H]
	00PA7KEB99C95	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A95	AK	N	C	Key top	[KG]
	00PA7KEC24A94	AK	N	C	Key top	[KF]
	00PA7KE032A95	AK	N	C	Key top	[KI]
	00PA7KEC28A95	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A95	AK	N	C	Key top	[KS,KD,KN]
96	00PA7KEC33A96	AK	N	C	Key top	[U,Y]
	00PA7KEC26A96	AK	N	C	Key top	[H]
	00PA7KEB99C96	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A96	AK	N	C	Key top	[KG]
	00PA7KEC24A96	AK	N	C	Key top	[KF]
	00PA7KE032A96	AK	N	C	Key top	[KI]
	00PA7KEC28A96	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A96	AK	N	C	Key top	[KS,KD,KN]
97	00PA7KEC33A97	AK	N	C	Key top	[U,Y]
	00PA7KEC26A97	AK	N	C	Key top	[H]
	00PA7KEB99C97	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A97	AK	N	C	Key top	[KG]
	00PA7KEC24A97	AK	N	C	Key top	[KF]
	00PA7KE032A97	AK	N	C	Key top	[KI]
	00PA7KEC28A97	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A97	AK	N	C	Key top	[KS,KD,KN]
98	00PA7KEC33A98	AK	N	C	Key top	[U,Y]
	00PA7KEC26A98	AK	N	C	Key top	[H]
	00PA7KEB99C98	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A98	AK	N	C	Key top	[KG]
	00PA7KEC24A98	AK	N	C	Key top	[KF]
	00PA7KE032A98	AK	N	C	Key top	[KI]
	00PA7KEC28A98	AK	N	C	Key top	[KW,KX]
	00PA7KEC23A98	AK	N	C	Key top	[KS,KD,KN]
99	00PA7KEC33A99	AQ	N	C	Key top	[U,Y]
	00PA7KEC26A99	AQ	N	C	Key top	[H]
	00PA7KEB99C99	AQ	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25A99	AQ	N	C	Key top	[KG]
	00PA7KEC24A99	AQ	N	C	Key top	[KF]
	00PA7KE032A99	AQ	N	C	Key top	[KI]
	00PA7KEC28A99	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23A99	AQ	N	C	Key top	[KS,KD,KN]
100	00PA7KEC33AA1	AK	N	C	Key top	[U,Y]
	00PA7KEC26AA1	AK	N	C	Key top	[H]
	00PA7KEB99CA1	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AA1	AK	N	C	Key top	[KG]
	00PA7KEC24AA1	AK	N	C	Key top	[KF]
	00PA7KE032AA1	AK	N	C	Key top	[KI]
	00PA7KEC28AA1	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AA1	AK	N	C	Key top	[KS,KD,KN]
101	00PA7KEC33AA2	AK	N	C	Key top	[U,Y]
	00PA7KEC26AA2	AK	N	C	Key top	[H]
	00PA7KEB99CA2	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AA2	AK	N	C	Key top	[KG]
	00PA7KEC24AA2	AK	N	C	Key top	[KF]
	00PA7KE032AA2	AK	N	C	Key top	[KI]
	00PA7KEC28AA2	AK	N	C	Key top	[KW,KX]

5 Keyboard unit • CE720K

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
101	00PA7KEC23AA2	AK	N	C	Key top	[KS,KD,KN]
102	00PA7KEC33AA3	AK	N	C	Key top	[U,Y]
	00PA7KEC26AA3	AK	N	C	Key top	[H]
	00PA7KEB99CA3	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AA3	AK	N	C	Key top	[KG]
	00PA7KEC24AA3	AK	N	C	Key top	[KF]
	00PA7KE032AA3	AK	N	C	Key top	[KI]
	00PA7KEC28AA3	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AA3	AK	N	C	Key top	[KS,KD,KN]
103	00PA7KEC33AA4	AK	N	C	Key top	[U,Y]
	00PA7KEC26AA4	AK	N	C	Key top	[H]
	00PA7KEB99CA4	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AA4	AK	N	C	Key top	[KG]
	00PA7KEC24AA4	AK	N	C	Key top	[KF]
	00PA7KE032AA4	AK	N	C	Key top	[KI]
	00PA7KEC28AA4	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AA4	AK	N	C	Key top	[KS,KD,KN]
104	00PA7KEC33AA5	AK	N	C	Key top	[U,Y]
	00PA7KEC26AA5	AK	N	C	Key top	[H]
	00PA7KEB99CA5	AK	N	C	Key top	[Q,T,E,KE]
	00PD2KE038AA5	AQ	N	C	Key top	[KG]
	00PA7KEC24AA5	AK	N	C	Key top	[KF]
	00PA7KE032AA5	AK	N	C	Key top	[KI]
	00PA7KEC28AA5	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AA5	AK	N	C	Key top	[KS]
	00PD2KE041AD2	AQ	N	C	Key top	[KD,KN]
105	00PA7KEC33AA6	AK	N	C	Key top	[U,Y]
	00PA7KEC26AA6	AK	N	C	Key top	[H]
	00PA7KEB99CA6	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AA6	AK	N	C	Key top	[KG]
	00PA7KEC24AA6	AK	N	C	Key top	[KF]
	00PA7KE032AA6	AK	N	C	Key top	[KI]
	00PA7KEC28AA6	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AA6	AK	N	C	Key top	[KS,KD,KN]
106	00PA7KEC33AA7	AQ	N	C	Key top	[U,Y]
	00PA7KEC26AA7	AQ	N	C	Key top	[H]
	00PA7KEB99CA7	AQ	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AA7	AQ	N	C	Key top	[KG]
	00PA7KEC24AA7	AQ	N	C	Key top	[KF]
	00PA7KE032AA7	AQ	N	C	Key top	[KI]
	00PA7KEC28AA7	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23AA7	AQ	N	C	Key top	[KS,KD,KN]
108	00PA7KEC33AA9	AQ	N	C	Key top	[U,Y]
	00PA7KEC26AA9	AQ	N	C	Key top	[H]
	00PA7KEB99CA9	AQ	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AA9	AQ	N	C	Key top	[KG]
	00PA7KEC24AA9	AQ	N	C	Key top	[KF]
	00PA7KE032AA9	AQ	N	C	Key top	[KI]
	00PA7KEC28AA9	AQ	N	C	Key top	[KW,KX]
	00PA7KEC23AA9	AQ	N	C	Key top	[KS,KD,KN]
110	00PA7KEC33AB2	AK	N	C	Key top	[U,Y]
	00PA7KEC26AB2	AK	N	C	Key top	[H]
	00PA7KEB99CB2	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AB2	AK	N	C	Key top	[KG]
	00PD2KE039AB2	AQ	N	C	Key top	[KF]
	00PA7KE032AB2	AK	N	C	Key top	[KI]
	00PA7KEC28AB2	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AB2	AK	N	C	Key top	[KS,KD,KN]
112	00PA7KEC33AB4	AK	N	C	Key top	[U,Y]
	00PA7KEC26AB4	AK	N	C	Key top	[H]
	00PA7KEB99CB4	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AB4	AK	N	C	Key top	[KG]
	00PA7KEC24AB4	AK	N	C	Key top	[KF]
	00PA7KE032AB4	AK	N	C	Key top	[KI]
	00PA7KEC28AB4	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AB4	AK	N	C	Key top	[KS,KD,KN]
113	00PA7KEC33AB5	AK	N	C	Key top	[U,Y]
	00PA7KEC26AB5	AK	N	C	Key top	[H]
	00PA7KEB99CB5	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AB5	AK	N	C	Key top	[KG]
	00PA7KEC24AB5	AK	N	C	Key top	[KF]
	00PA7KE032AB5	AK	N	C	Key top	[KI]
	00PA7KEC28AB5	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AB5	AK	N	C	Key top	[KS,KD,KN]
114	00PA7KEC33AB6	AK	N	C	Key top	[U,Y]
	00PA7KEC26AB6	AK	N	C	Key top	[H]
	00PA7KEB99CB6	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AB6	AK	N	C	Key top	[KG]
	00PA7KEC24AB6	AK	N	C	Key top	[KF]
	00PA7KE032AB6	AK	N	C	Key top	[KI]

5 Keyboard unit • CE720K

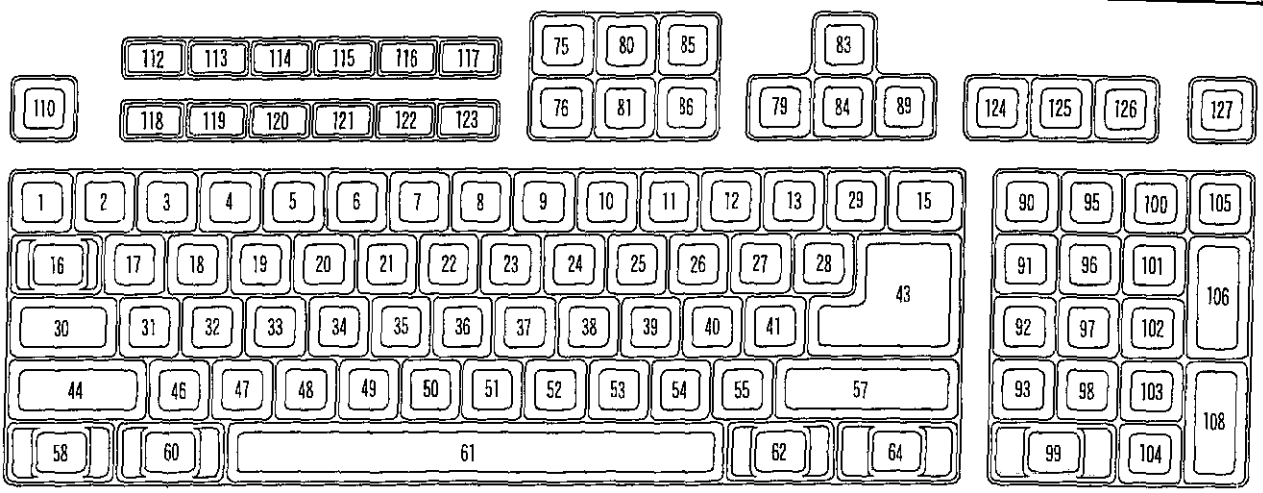
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
114	00PA7KEC28AB6	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AB6	AK	N	C	Key top	[KS,KD,KN]
115	00PA7KEC33AB7	AK	N	C	Key top	[U,Y]
	00PA7KEC26AB7	AK	N	C	Key top	[H]
	00PA7KEB99CB7	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AB7	AK	N	C	Key top	[KG]
	00PA7KEC24AB7	AK	N	C	Key top	[KF]
	00PA7KE032AB7	AK	N	C	Key top	[KI]
	00PA7KEC28AB7	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AB7	AK	N	C	Key top	[KS,KD,KN]
116	00PA7KEC33AB8	AK	N	C	Key top	[U,Y]
	00PA7KEC26AB8	AK	N	C	Key top	[H]
	00PA7KEB99CB8	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AB8	AK	N	C	Key top	[KG]
	00PA7KEC24AB8	AK	N	C	Key top	[KF]
	00PA7KE032AB8	AK	N	C	Key top	[KI]
	00PA7KEC28AB8	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AB8	AK	N	C	Key top	[KS,KD,KN]
117	00PA7KEC33AB9	AK	N	C	Key top	[U,Y]
	00PA7KEC26AB9	AK	N	C	Key top	[H]
	00PA7KEB99CB9	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AB9	AK	N	C	Key top	[KG]
	00PA7KEC24AB9	AK	N	C	Key top	[KF]
	00PA7KE032AB9	AK	N	C	Key top	[KI]
	00PA7KEC28AB9	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AB9	AK	N	C	Key top	[KS,KD,KN]
118	00PA7KEC33AC1	AK	N	C	Key top	[U,Y]
	00PA7KEC26AC1	AK	N	C	Key top	[H]
	00PA7KEB99CC1	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AC1	AK	N	C	Key top	[KG]
	00PA7KEC24AC1	AK	N	C	Key top	[KF]
	00PA7KE032AC1	AK	N	C	Key top	[KI]
	00PA7KEC28AC1	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AC1	AK	N	C	Key top	[KS,KD,KN]
119	00PA7KEC33AC2	AK	N	C	Key top	[U,Y]
	00PA7KEC26AC2	AK	N	C	Key top	[H]
	00PA7KEB99CC2	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AC2	AK	N	C	Key top	[KG]
	00PA7KEC24AC2	AK	N	C	Key top	[KF]
	00PA7KEC32AC2	AK	N	C	Key top	[KI]
	00PA7KEC28AC2	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AC2	AK	N	C	Key top	[KS,KD,KN]
120	00PA7KEC33AC3	AK	N	C	Key top	[U,Y]
	00PA7KEC26AC3	AK	N	C	Key top	[H]
	00PA7KEB99CC3	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AC3	AK	N	C	Key top	[KG]
	00PA7KEC24AC3	AK	N	C	Key top	[KF]
	00PA7KEC32AC3	AK	N	C	Key top	[KI]
	00PA7KEC28AC3	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AC3	AK	N	C	Key top	[KS,KD,KN]
121	00PA7KEC33AC4	AK	N	C	Key top	[U,Y]
	00PA7KEC26AC4	AK	N	C	Key top	[H]
	00PA7KEB99CC4	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AC4	AK	N	C	Key top	[KG]
	00PA7KEC24AC4	AK	N	C	Key top	[KF]
	00PA7KEC32AC4	AK	N	C	Key top	[KI]
	00PA7KEC28AC4	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AC4	AK	N	C	Key top	[KS,KD,KN]
122	00PA7KEC33AC5	AK	N	C	Key top	[U,Y]
	00PA7KEC26AC5	AK	N	C	Key top	[H]
	00PA7KEB99CC5	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AC5	AK	N	C	Key top	[KG]
	00PA7KEC24AC5	AK	N	C	Key top	[KF]
	00PA7KEC32AC5	AK	N	C	Key top	[KI]
	00PA7KEC28AC5	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AC5	AK	N	C	Key top	[KS,KD,KN]
123	00PA7KEC33AC6	AK	N	C	Key top	[U,Y]
	00PA7KEC26AC6	AK	N	C	Key top	[H]
	00PA7KEB99CC6	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AC6	AK	N	C	Key top	[KG]
	00PA7KEC24AC6	AK	N	C	Key top	[KF]
	00PA7KEC32AC6	AK	N	C	Key top	[KI]
	00PA7KEC28AC6	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AC6	AK	N	C	Key top	[KS,KD,KN]
124	00PC5KE213AC7	AQ	N	C	Key top	[U,Y]
	00PC5KE203AC7	AQ	N	C	Key top	[H,Q,T,E,KE]
	00PC5KE206AC7	AQ	N	C	Key top	[KG]
	00PC5KE207AC7	AQ	N	C	Key top	[KF]
	00PC5KE21DAC7	AQ	N	C	Key top	[KI]
	00PC5KE209BC7	AQ	N	C	Key top	[KW,KX]

5 Keyboard unit • CE720K

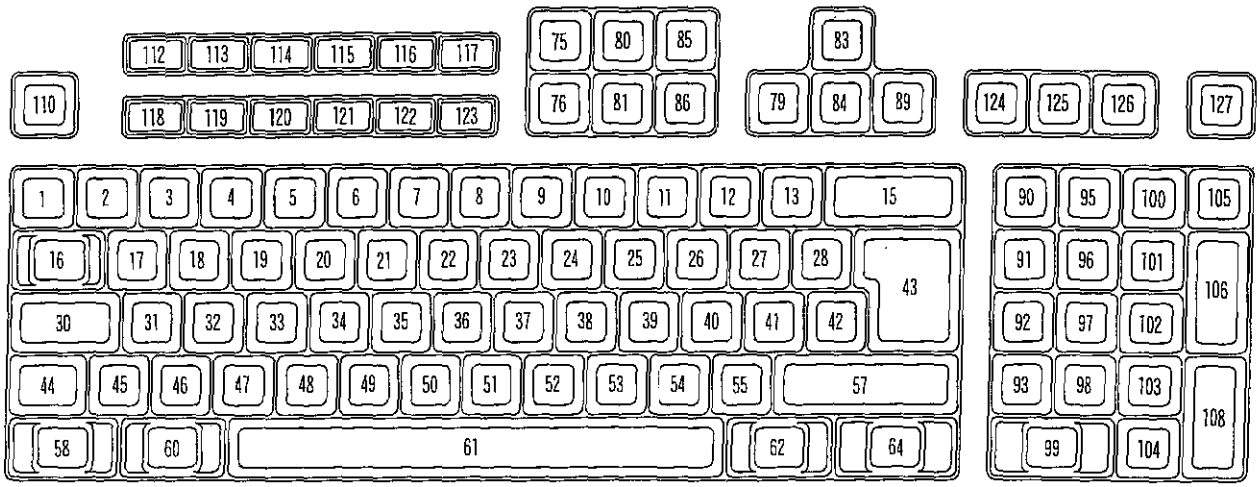
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
124	00PC5KE208AC7	AQ	N	C	Key top	[KS,KD,KN]
125	00PD2KE045AC8	AQ	N	C	Key top	[U,Y]
	00PD2KE043AC8	AQ	N	C	Key top	[H]
	00PD2KE037AC8	AQ	N	C	Key top	[Q,T,E,KE]
	00PD2KE038AC8	AQ	N	C	Key top	[KG]
	00PD2KE039AC8	AQ	N	C	Key top	[KF]
	00PD2KE044AC8	AQ	N	C	Key top	[KI]
	00PD2KE042AC8	AQ	N	C	Key top	[KW,KX]
	00PD2KE041AC8	AQ	N	C	Key top	[KS,KD,KN]
126	00PC5KE213AC9	AQ	N	C	Key top	[U,Y]
	00PC5KE203AC9	AQ	N	C	Key top	[H,Q,T,E,KE]
	00PC5KE206AC9	AQ	N	C	Key top	[KG]
	00PC5KE207AC9	AQ	N	C	Key top	[KF]
	00PC5KE21DAC9	AQ	N	C	Key top	[KI]
	00PC5KE209BC9	AQ	N	C	Key top	[KW,KX]
	00PC5KE208AC9	AQ	N	C	Key top	[KS,KD,KN]
127	00PA7KEC33AD1	AK	N	C	Key top	[U,Y]
	00PA7KEC26AD1	AK	N	C	Key top	[H]
	00PA7KEB99CD1	AK	N	C	Key top	[Q,T,E,KE]
	00PA7KEC25AD1	AK	N	C	Key top	[KG]
	00PA7KEC24AD1	AK	N	C	Key top	[KF]
	00PA7KEC32AD1	AK	N	C	Key top	[KI]
	00PA7KEC28AD1	AK	N	C	Key top	[KW,KX]
	00PA7KEC23AD1	AK	N	C	Key top	[KS,KD,KN]
202	00PSKEUAA000A	AG		B	Push switch	
203	00PSKFLAC000A	AG		B	Push switch	
204	00P19KF005C//	AG		C	Bush	
205	00P16KF005B//	AG		C	Guide	
206	00P19KE007B//	AG	N	C	Pin	[U,Y,Q,T,E,KE]
207	00P25KE056A//	AX	N	C	Insulator	[U,Y,Q,T,E,KE]
	00P25KE058A//	AX	N	C	Insulator	[H,KG,KF,KI,KS,KW,KX]
208	00P25KE057B//	AH	N	C	Insulator	
209	00PSKFLAF000A	AH		B	Switch,soft push	
210	00PSKFLFH000A	AK		B	Push switch	
211	00P19KF009B//	AG	N	C	Pin	[U,Y,H,KS]
	00P19KE009B//	AG	N	C	Pin	[Q,T,E,KE,KG,KF,KI,KW,KX]
212	00P29KE184A//	AV	N	C	Cable	
213	00P23KE044A//	AE	N	C	Couer plate	
214	00P13KF015A//	AB		C	Stopper	
215	00P21KF011A//	AK		C	Lever(1.75)	
216	00P21KF008A//	AD		C	Lever(2)	
217	00P21KF016A//	AE		C	Lever(3)	
218	00P21KF009A//	AF		C	Lever(8)	
219	00P21KF020A//	AG		C	Lever	
220	00P16KF006A//	AG		C	Guide pin	
221	00P27KF021A//	AC		C	Spring	
222	00P21KE023A//	AN		C	Lever	[U,Y,Q,T,E,KE]
223	00P21KE024A//	AN		C	Lever	[U,Y,Q,T,E,KE]
224	00P21KE021A//	AH		C	Lever	[U,Y,Q,T,E,KE]
225	00P21KE022A//	AH		C	Lever	[U,Y,Q,T,E,KE]
226	VHD1S2075K/-1	AB		B	Diode(1S2075K)	
	(Unit)					
901	QSW-K1065ACZZ	BS	N	E	Keyboard unit	[U,Y]
	QSW-K1048ACZZ	BS	N	E	Keyboard unit	[H]
	QSW-K1047ACZZ	BS	N	E	Keyboard unit	[Q,T,E,KE]
	QSW-K1053ACZZ	BS	N	E	Keyboard unit	[KG]
	QSW-K1054ACZZ	BS	N	E	Keyboard unit	[KF]
	QSW-K1055ACZZ	BS	N	E	Keyboard unit	[KI]
	QSW-K1058ACZZ	BS	N	E	Keyboard unit	[KW,KX]
	QSW-K1057ACZZ	BS	N	E	Keyboard unit	[KS,KD,KN]

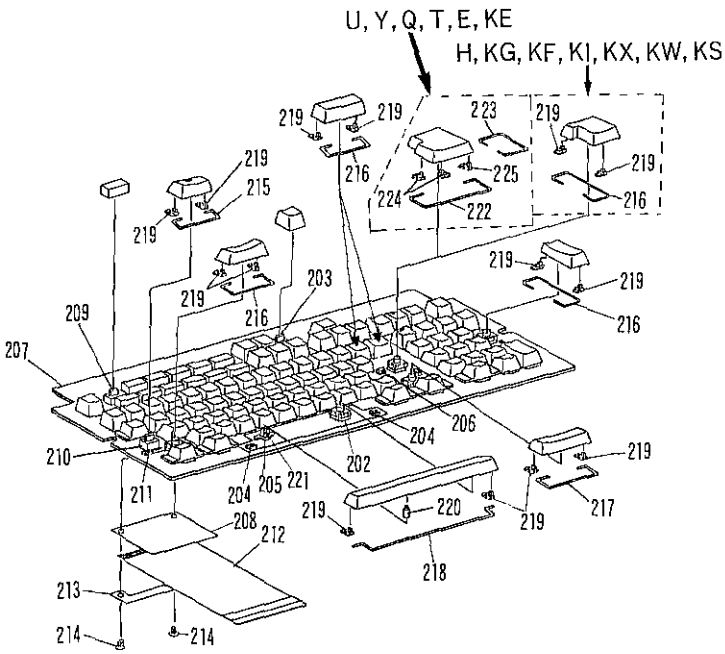
5 Keyboard unit • CE720K

U, Y, Q, T, E, KE



H, KG, KF, KI, KX, KW, KS





6 LED PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM5039SC0E	AB		C	Connector (5pin)
2	VHPGL9HY2//-1	AC		B	LED (GL9HY2)
3	VHPGL9NG2//-1	AB		B	LED (GL9NG2)
4	VRD-RC2EY121J	AA		C	Resistor (1/4W 120Ω ±5%)
5	VRD-RC2EY271J	AA		C	Resistor (1/4W 270Ω ±5%)
	(Unit)				
901	CPWBFI115AC01	AD	N	E	LED PWB unit

7 Key PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW2360SC3J	AE	N	C	Connector (30pin)
2	QCNW-1235ACZZ	AL	N	C	Key control cable + Core (U,Y)
	QCNW-1195ACZZ	AL	N	C	Key control cable (Other countries)
3	RC-EZ336BAC1C	AB	N	C	Capacitor (16WV 33μF)
4	RC-EZ475AAC1E	AB	N	C	Capacitor (25WV 4.7μF)
5	RC-KIE104HCZZ	AB		C	Capacitor (25WV 0.1μF)
6	RCRSZ1031ACZZ	AK	N	B	Crystal
7	RMPTC8472QCKB	AD		B	Block resistor (1/8W 4.7KΩ×8)
8	VCCCPU1HH200J	AB		C	Capacitor (50WV 20pF)
9	VCKYPU1HB681K	AA		C	Capacitor (50WV 680PF)
10	VHDDSS131HV-1	AA		B	Diode (DSS131HV)
11	VHiSN74LS07NS	AF		B	IC (SN74LS07NS)
12	VHiTC74HC138F	AL		B	IC (TC74HC138F)
13	VHiTC74HC244F	AM		B	IC (TC74HC244F)
14	VHiTC74HC373F	AK		B	IC (TC74HC373F)
15	VHi2464/AAA0B	AV	N	B	Key ROM (2464)
16	VHiT80C49AF-1	AV	N	B	IC (T80C49AF)
17	VRD-RC2EY100J	AA		C	Resistor (1/4W 10Ω ±5%)
18	VRD-RC2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
19	VRD-RC2EY104J	AA		C	Resistor (1/4W 100KΩ ±5%)
20	VRD-RC2EY121J	AA		C	Resistor (1/4W 120Ω ±5%)
21	VRD-RC2EY333J	AA		C	Resistor (1/4W 33KΩ ±5%)
22	VRD-RC2EY392J	AA		C	Resistor (1/4W 3.9KΩ ±5%)
	(Unit)				
901	CPWBS1114AC02	BQ	N	E	Key PWB unit (U,Y)
	CPWBS1114AC01	BQ	N	E	Key PWB unit (Other countries)

8 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LANGQ1129ACZB	AT	N	C	Connector angle (U,Y)
	LANGQ1129ACZA	AQ	N	C	Connector angle (G only)
	LANGQ1129ACZZ	AN	N	C	Connector angle (Other countries)
2	LX-BZ2061HCZZ	AB		C	Screw
3	LX-NZ2004HCZZ	AA		C	Nut
4	PCAPH1003ACZZ	AC		C	25P connector protect cap
5	PCAPH1007ACZZ	AD	N	C	25P cap
6	PCAPH1008ACZZ	AC	N	C	9P cap
7	QCNCM0548HC0B	AA		C	Connector (2pin)
8	QCNCM0550HC1J	AB	N	C	Connector (10pin)
9	QCNCM0552HC2E	AP		C	Connector (25pin)
10	QCNCM1091AC3B	AH	N	C	Connector (32pin)
11	QCNCM1094AC9F	AQ	N	C	Connector (96pin)
12	QCNCM1095AC4J	AL	N	C	Connector (40pin)
13	QCNCM2346SC2J	AG		C	Connector (20pin)
14	QCNCM2346SC3D	AL		C	Connector (34pin)
15	QCNCM2346SC4J	AL		C	Connector (40pin)
16	QCNCM6865RC0J	AC		C	Connector (9pin)
17	QCNCW1057ACZZ	AB		C	Connector (Short socket)
18	QCNCM1060AC03	AB		B	Connector (3pin short pin)
19	QCNCW1097AC0J	AL	N	C	Connector (9pin)
20	QCNCW1097AC2E	AL	N	C	Connector (25pin)
21	QCNCW1098AC6B	AM	N	C	Connector (62pin)
22	QCNCW1345CC0E	AC	N	C	Connector (5pin)
23	QCNW-1184ACZZ	AW	N	C	36P-40P harness
24	QSOCZE068HCZZ	AX		C	IC socket (68pin)
25	QSOCZ6420ACZZ	AE		C	IC socket (20pin)
26	QSOCZ6428ACZZ	AE		C	IC socket (28pin)
27	QSOCZ6440ACZZ	AG		C	IC socket (40pin)
28	QSW-D0270FCZZ	AG		B	Dip switch
29	QSW-S1060ACSA	AE	N	B	Slide switch (U only)

8 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
29	QSW-S1060ACZZ	AE	N	B	Slide switch	(Other countries)
30	QSW-S1061ACSA	AE	N	B	Slide switch	(U only)
	QSW-S1061ACZZ	AE	N	B	Slide switch	(Other countries)
31	RC-KZ1018CCZZ	AE		C	Capacitor (250WV 25pF)	
32	RC-KE104HCZZ	AB		C	Capacitor (25WV 0.1μF)	
33	RCiLL1001ACZZ	AC		C	Coil	
34	RCRSP1003CCZZ	AT		B	Crystal (32KHz)	
35	RCRSZ1010HCZZ	AR		B	Crystal (316MHz)	
36	RCRSZ1011HCZZ	AR		B	Crystal (14.7456MHz)	
37	RCRSZ1026ACZZ	AR	N	B	Crystal (14.31818MHz)	
38	RCRSZ1028ACZZ	AR	N	B	Crystal (24.000MHz)	
39	RCRSZ1029ACZZ	AK	N	B	Crystal (16.257MHz)	
40	RCRSZ1030ACZZ	AR	N	B	Crystal (19.2MHz)	
41	RMPTC4102QCKB	AC		B	Block resistor (1KΩ×4 1/8W ±10%)	
42	RMPTC4103QCKB	AC		B	Block resistor (10KΩ×4 1/8W ±10%)	
43	RMPTC4331QCKB	AB		B	Block resistor (330Ω×4 1/8W ±10%)	
44	RMPTC5682QCKB	AB		B	Block resistor (6.8KΩ×5 1/8W ±10%)	
45	RMPTC6472QCJB	AC		B	Block resistor (4.7KΩ×6 1/8W ±5%)	
46	RMPTC8102QCKB	AD		B	Block resistor (1.0KΩ×8 1/8W ±10%)	
47	RMPTC9102QCKB	AD		B	Block resistor (1KΩ×9 1/8W ±10%)	
48	RMPTW6101QCKE	AD		B	Block resistor (100Ω×6)	
49	RVR-Q1005ACSA	AF	N	B	Variable resistor (50KΩ)	(U only)
	RVR-Q1005ACZZ	AF	N	B	Variable resistor (50KΩ)	(Other countries)
50	UBATN1002ACZZ	AT	N	S	Battery (3/5IFT)	
51	VCCCPU1HH101J	AB		C	Capacitor (50WV 100pF)	
52	VCCCPU1HH200J	AB		C	Capacitor (50WV 20pF)	
53	VCCCPU1HH220J	AA		C	Capacitor (50WV 22PF)	
54	VCCCPU1HH470J	AA		C	Capacitor (50WV 47PF)	
55	VCCCPU1HH560J	AA		C	Capacitor (50WV 56pF)	
56	VCEAGU1CW106M	AA		C	Capacitor (16WV 10μF)	
57	VCEAGU1CW107M	AB		C	Capacitor (16WV 100μF)	
58	VCEAGU1CW227M	AB		C	Capacitor (16WV 220μF)	
59	VCEAGU1EW476M	AB		C	Capacitor (25WV 47μF)	
60	VCKYPU1HB103K	AA		C	Capacitor (50WV 0.010μF)	
61	VCKYPU1HB221K	AB		C	Capacitor (50WV 220pF)	
62	VCKYPU1HB222K	AA		C	Capacitor (50WV 2200pF)	
63	VCKYPU1HB331K	AA		C	Capacitor (50WV 330pF)	
64	VCKYPU1HB681K	AA		C	Capacitor (50WV 680PF)	
65	VCQYNU1HM473K	AB		C	Capacitor (50WV 0.047μF)	(U only)
	VCQYNU1HM473M	AA	N	C	Capacitor (50WV 0.047μF)	(Other countries)
66	VCSAVU1CE335M	AB		C	Capacitor (16WV 3.3μF)	
67	VHDDS1588L2-1	AB		B	Diode (DS1588L2)	
68	VHiALS04ANS-1	AD	N	B	IC (ALS04ANS)	
69	VHiALS244ANS1	AL	N	B	IC (ALS244ANS1)	
70	VHiALS245//-1	AW		B	IC (ALS245)	
71	VHiALS253NS-1	AE	N	B	IC (ALS253NS)	
72	VHiALS32NS/-1	AD	N	B	IC (ALS32NS)	
73	VHiALS373NS-1	AL	N	B	IC (ALS373NS)	
74	VHiD41464C-10	AT	N	B	IC (D41464C)	
75	VHiMB4107//-1	BA		B	IC (MB4107)	
76	VHiMN1288//-1	BB	N	B	IC (MN1288)	
77	VHiMN1292//-1	BC	N	B	IC (MN1292)	
78	VHiMN1294//-1	BC	N	B	IC (MN1294)	
79	VHiM41256-Z12	AS	N	B	IC (M41256)	
80	VHiM5M4164-12	AN	N	B	IC (M5M4164)	
81	VHiM5M4464-12	AS	N	B	IC (M5M4464)	
82	VHiN286-10C2H	BY	N	B	IC (N286-10C2H)	
83	VHiSC146818P1	AW		B	IC (SC146818P1)	
84	VHiSC4751//-1	BR	N	B	IC (SC4751)	
85	VHiSC4752//-1	BT	N	B	IC (SC4752)	
86	VHiSN74LS12NS	AD	N	B	IC (SN74LS12NS)	
87	VHiSN74LS14NS	AL	N	B	IC (SN74LS14NS)	
88	VHiSN7406NS-1	AF	N	B	IC (SN7406NS)	
89	VHiSN7407NS-1	AF	N	B	IC (SN7407NS)	
90	VHiTC4066BF-1	AE	N	B	IC (TC4066BF)	
91	VHiTC74HC00FN	AD		B	IC (TC74HC00FN)	
92	VHiTL431CLP-1	AG		B	IC (TL431CLP)	
93	VHiTQS175S/-1	AW	N	B	IC (TQS175S)	
94	VHiUA1488//-1	AH		B	IC (UA1488)	
95	VHiUA1489A/-1	AH		B	IC (UA1489A)	
96	VHiUPD449G/ 1	AQ		B	IC (UPD449G)	
97	VHi27128AAC0B	AS	N	B	CG-ROM (27128)	
98	VHi27256AAF0E	AW	N	B	BIOS-ROM (27256)(Low)	(U,Y,E,T)
	VHi27256AAE0E	AW	N	B	BIOS-ROM (27256)(Low)	(G,H,Q)
	VHi27256AAG0E	AW	N	B	BIOS-ROM (27256)(Low)	(KD,KN)
	VHi27256AAF1E	AW	N	B	BIOS-ROM (27256)(High)	(U,Y,E,T)
	VHi27256AAE1E	AW	N	B	BIOS-ROM (27256)(High)	(G,H,Q)
	VHi27256AAG1E	AW	N	B	BIOS-ROM (27256)(High)	(KD,KN)
99	VHi74F00///-1	AF		B	IC (74F00)	
100	VHi74F04///-1	AE		B	IC (74F04)	

8 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
101	VHi74F373SJ-1	AN	N	B	IC (74F373SJ)
102	VHi74F374SJ-1	AN	N	B	IC (74F374SJ)
103	VHi74LS125ANS	AF	N	B	IC (74LS125ANS)
104	VHi74LS126ANS	AF	N	B	IC (74LS126ANS)
105	VHi74LS244NS1	AH	N	B	IC (74LS244NS1)
106	VHi8742/AAA0B	BG	N	B	IC (8742)
107	VHPPC817D//-1	AD		B	Photo transistor (PC817D)
108	VRD-HT2EY000J	AA		C	Resistor (1/4W 0Ω ±5%)
109	VRD-HT2HY565J	AA	N	C	Resistor (1/2W 5.6MΩ ±5%)
110	VRD-RC2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
111	VRD-RC2EY102J	AA		C	Resistor (1/4W 1.0KΩ ±5%)
112	VRD-RC2EY103J	AA		C	Resistor (1/4W 10KΩ ±5%)
113	VRD-RC2EY122J	AA		C	Resistor (1/4W 1.2KΩ ±5%)
114	VRD-RC2EY152J	AA		C	Resistor (1/4W 1.5KΩ ±5%)
115	VRD-RC2EY153J	AA		C	Resistor (1/4W 15KΩ ±5%)
116	VRD-RC2EY154J	AA		C	Resistor (1/4W 150KΩ ±5%)
117	VRD-RC2EY200J	AA		C	Resistor (1/4W 20Ω ±5%)
118	VRD-RC2EY221J	AA		C	Resistor (1/4W 220Ω ±5%)
119	VRD-RC2EY333J	AA		C	Resistor (1/4W 33KΩ ±5%)
120	VRD-RC2EY433J	AA	N	C	Resistor (1/4W 43KΩ ±5%)
121	VRD-RC2EY472J	AA		C	Resistor (1/4W 4.7KΩ ±5%)
122	VRD-RC2EY682J	AA		C	Resistor (1/4W 6.8KΩ ±5%)
123	VRD-RC2EY822G	AA		C	Resistor (1/4W 8.2KΩ ±2%)
124	VRD-RC2EY822J	AA		C	Resistor (1/4W 8.2KΩ ±5%)
125	VRNRC2EK2201F	AA		C	Resistor (1/4W 200Ω ±1%)
126	VS2SA673-C/-1	AE		B	Transistor (2SA673-C)
127	VS2SC1214-C-1	AE		B	Transistor (2SC1214C)
128	TLABE1290ACZZ	AB	N	C	ROM label
129	RC-K1H105HCZZ	AF		C	Capacitor (1μF)
	(Unit)				
901	DUNTK1796ACZZ	**	N	E	Main PWB unit (U,Y)
	DUNTK1878ACZZ	**	N	E	Main PWB unit (G only)
	DUNTK1700ACZZ	**	N	E	Main PWB unit (Other countries)

9 Valiable resistor PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GCOVH1027ACZZ	AB	N	C	Slide switch cover
2	PSPAY1026ACZZ	AB	N	C	PWB spacer
3	QCNCM0563HC0C	AB	N	B	Connector (3pin)
4	QCNCM1109AC0E	AB	N	C	Connector (5pin)
5	QCNCM5039SC0F	AB	N	C	Connector (6pin)
6	QSW-S1049ACSA	AE	N	B	Slide switch (U only)
	QSW-S1049ACZZ	AE	N	B	Slide switch (Other countries)
7	RCiLZ1003AC03	AA	N	C	Coil (BL01RN1-A62)
8	RVR-Q1003ACSA	AF	N	B	Variable resistor (5KΩ) (U only)
	RVR-Q1003ACZZ	AF	N	B	Variable resistor (5KΩ) (Other countries)
9	RVR-Q1004ACSA	AF	N	B	Variable resistor (50KΩ) (U only)
	RVR-Q1004ACZZ	AF	N	B	Variable resistor (50KΩ) (Other countries)
10	VRD-HT2EY154J	AA		C	Resistor (1/4W 150KΩ ±5%) (Except U)
	(Unit)				
901	CPWBF1116AC02	AE	N	E	Valiable resistor PWB unit (Y only)
	CPWBF1116AC03	AE	N	E	Valiable resistor PWB unit (U only)
	CPWBF1116AC01	AE	N	E	Valiable resistor PWB unit (Other countries)

10 Power supply unit··100V series

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0BRXE104/////	AG		C	Capacitor (250WV 0.1μF) [C1,2,5]
2	0BRDE7100F222	AL		C	Capacitor (250WV 1000pF) [C6,7]
3	0BRDE7120F332	AD	N	C	Capacitor [C8,9]
4	0BRCEUSM1C222	AG		C	Capacitor (16WV 2200pF) [C17]
5	0BRCEUSM1E471	AF		C	Capacitor (25WV 470μF) [C20]
6	0BRCEUSM1E101	AD		C	Capacitor (100μF 25V) [C21,23,25]
7	0BRCEUSM1H101	AE		C	Capacitor (100μF 50V) [C22]
8	0BRCEUSM1V330	AC		C	Capacitor (35WV 33μF) [C28]
9	0BRCEUSM1H100	AC		C	Capacitor (50WV 10μF) [C31,36]
10	0BRCEUSM1C221	AC		C	Capacitor (220μF 16V) [C32A,32B]
11	0BR10PS1-2200	AK	N	C	Capacitor [C19]
12	0BRECQV1H104/	AC	N	C	Capacitor [C13,15,38]
13	0BRECQV1H473/	AB	N	C	Capacitor [C40A,B,30]
14	0BRMDD22J103K	AD		C	Capacitor (630WV 0.01μF) [C37]

10 Power supply unit··100V series

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
15	0BRA1EFS102//	AH	N	C	Capacitor	[C16A,16B]
16	0BRA1AFS222//	AH	N	C	Capacitor	[C18A,B,C]
17	0BRECQV1H474/	AD	N	C	Capacitor	[C45,26]
18	0BRHF12E471M/	AS	N	C	Capacitor	[C10A,B]
19	0BRMDD22G223M	AC	N	C	Capacitor	[C11]
20	0BRECKD3D471L/	AC	N	C	Capacitor	[C12]
21	0BRECKD3D221/	AC	N	C	Capacitor	[C42]
22	0BRCEUSM1H100	AC		C	Capacitor (50WV 10μF)	[C14]
23	0BRCEUSM1E100	AC		C	Capacitor (25WV 10μF)	[C43]
24	0BRCEUSM1E101	AD		C	Capacitor (100μF 25V)	[C27,34]
25	0BRECQV1H104/	AC	N	C	Capacitor	[C41,29,44]
26	0BRECQV1H473/	AB	N	C	Capacitor	[C33,35]
27	0BREU2Z//////	AD		B	Diode	[D2A,B,8,12]
28	0BRFPU-12////	AE	N	B	Diode	[D5,6]
29	0BRRU2//////	AF	N	B	Diode	[D1]
30	0BR1SS82/////	AC		B	Diode	[D3,4,9]
31	0BRERA81-004/	AG	N	B	Diode	[D14]
32	0BRHZ15-2/////	AB	N	B	Zener diode	[ZD1]
33	0BRHZ6A-1/////	AB		B	Diode (HZ6A-1)	[ZD2]
34	0BRHZ3A-1/////	AB		B	Diode (HZ6A-2)	[ZD3]
35	0BRRBV604/////	AH	N	B	Diode stack	[DS1]
36	0BRESAC92M-02	AH	N	B	Diode stack	[DS2]
37	0BRFMB-34M///	AQ	N	B	Diode stack	[DS3]
⚠ 39	0BRGGS5//////	AE	N	A	Fuse	[F1]
40	0BRTS-02-P-SN	AB		C	Clip-fuse	[XF1]
41	0BRUPC78M05//	AH	N	B	IC	[IC1]
42	0BRUPC7912H//	AH	N	B	IC	[IC2]
43	0BRUPC7915H//	AH	N	B	IC	[IC3]
44	0BRTL7705CP-B	AM		B	I.C.	[IC4]
45	0BRUPC317H///	AN		B	IC (UPC317H)	[IC5]
46	0BRTL431CLPB/	AF	N	B	IC	[IC6]
47	0BRSTR9012///	AU	N	B	IC	[IC7]
48	0BR2SC2751-L/	AQ		B	Transistor (2SC2751)	[TR1]
49	0BR2SD1308-K/	AG		B	Transistor (2SD1308)	[TR2]
50	0BR2SC1173-Y/	AG	N	B	Transistor	[TR3]
51	0BR2SC3568-K/	AM		B	Transistor (2SC3568)	[TR4]
52	0BR2SC2655///	AD	N	B	Transistor	[TR5]
53	0BR2SC1815///	AD	N	B	Transistor	[TR6]
54	0BRN13T1//////	AE	N	B	Put	[CR1]
55	0BRPS2401-1//	AG		B	Optical isolator	[PC1,2]
56	0BRTM64KPH500	AE	N	B	Potentiometer	[VR1]
57	0BR5219-03A//	AE		C	Connector	[CN1]
58	0BRB5P-VH/////	AC	N	C	Connector	[CN2]
59	0BR5264-09A//	AP	N	C	Connector	[CN3]
60	0BR5267-04ARD	AB	N	C	Connector	[CN4]
61	0BRB4P-vH/////	AC	N	C	Connector	[CN5]
62	0BR5267-04AWT	AB	N	C	Connector	[CN6]
63	0BR5267-02AWT	AB	N	C	Connector	[CN7]
64	0BR5267-03AWT	AB	N	C	Connector	[CN8]
65	0BR5045-02A//	AB		C	Connector	[CN9]
66	0BR487A-BE471	AG	N	B	Posistor	[PH1]
67	0BR4D-18//////	AL	N	B	Thermistor	[TH1A,B]
68	0BRSC-02-50J/	AP	N	C	Choke coil	[L1]
69	0BRSC-02-20J/	AP	N	C	Choke coil	[L2]
70	0BR4476P03863	AH	N	C	Choke coil	[L4]
71	0BRFL9H471K//	AG		C	Chock coil	[L5]
72	0BRB-20F-38//	AD		B	Core	[L7A,B]
73	0BR4416P06095	BD	N	B	Transformer	[T1]
74	0BR4416P05741	AQ		B	Transformer	[T2]
75	0BRRS2FB10K-J	AB	N	C	Resistor	[R1A,B]
76	0BRRGC5-0.68-	AD	N	C	Resistor	[R4]
77	0BRRS2FB100K-	AC		C	Resistor	[R5]
78	0BRRS2FB22-J/	AC		C	Resistor	[R7]
79	0BRRS2FB33-J/	AB	N	C	Resistor	[R32]
80	0BRRS2FB680-J	AB	N	C	Resistor	[R2AB]
81	0BRNAS114S222	AA	N	C	Resistor	[R3]
82	0BRNAS112S330	AA	N	C	Resistor	[R6]
83	0BRFMR114B391	AC	N	C	Resistor	[R9,10]
84	0BRRMR114B100	AC	N	C	Resistor	[R11,12]
85	0BRFMR112B100	AC	N	C	Resistor	[R30]
86	0BRFC02J-470/	AA	N	C	Resistor	[R18,33]
87	0BRFC02J-821/	AA	N	C	Resistor	[R19]
88	0BRFC02J-471/	AA	N	C	Resistor	[R20]
89	0BRFC02J-221/	AA	N	C	Resistor	[R21]
90	0BRFC02J-102/	AA	N	C	Resistor	[R28,34]
91	0BRFC02J-101/	AA	N	C	Resistor	[R35]
92	0BRNAS114F102	AA	N	C	Resistor	[R41]
93	0BRNAS114F561	AA	N	C	Resistor	[R42]
94	0BRNAS114F103	AA	N	C	Resistor	[R29]
95	0BRNAS112F181	AA	N	C	Resistor	[R14]

10 Power supply unit··100V series

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
96	0BRNAS114S102	AA	N	C	Resistor	[R24]
97	0BRNAS112F681	AA	N	C	Resistor	[R16]
98	0BRNAS112F102	AA	N	C	Resistor	[R17]
99	0BRNAS114S181	AA	N	C	Resistor	[R25]
100	0BRNAS114S182	AA	N	C	Resistor	[R26]
101	0BRNAS114S220	AA	N	C	Resistor	[R27]
102	0BRNAS114F100	AA	N	C	Resistor	[R22]
103	0BRNAS114F681	AA	N	C	Resistor	[R23]
104	0BRNAS114F102	AA	N	C	Resistor	[R36]
105	0BRNAS114F101	AA	N	C	Resistor	[R37]
106	0BRNAS114F103	AA	N	C	Resistor	[R38,39]
107	0BRNAS114F472	AA	N	C	Resistor	[R40]
108	0BRRS2FB100-J	AC		C	Resistor	[R51]
	(Unit)					
901	RDENC1006ACZZ	BX	N	E	Power supply unit (100V series)	

11 Power supply unit··200V series

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	0BRXE104/////	AG		C	Capacitor (250WV 0.1μF)	[C1,2,5]
2	0BRDE7090B102	AD	N	C	Capacitor	[C6,7,8,9]
3	0BRCEUSM1C222	AG		C	Capacitor (16WV 2200μF)	[C17]
4	0BRCEUSM1E471	AF		C	Capacitor (25WV 470μF)	[C20]
5	0BRCEUSM1E101	AD		C	Capacitor (100μF 25V)	[C21,23,25]
6	0BRCEUSM1E101	AD		C	Capacitor (100μF 25V)	[C27,34]
7	0BRCEUSM1H101	AE		C	Capacitor (100μF 50V)	[C22]
8	0BRCEUSM1V330	AC		C	Capacitor (35WV 33μF)	[C28]
9	0BRCEUSM1H100	AC		C	Capacitor (50WV 10μF)	[C31,36]
10	0BRCEUSM1C221	AC		C	Capacitor (220μF 16V)	[C32A,B]
11	0BR10PS102200	AK	N	C	Capacitor	[C19]
12	0BRECQV1H104/	AC	N	C	Capacitor	[C29,41,44]
13	0BRECQV1H104/	AC	N	C	Capacitor	[C23,15,31]
14	0BRECQV1H473/	AB	N	C	Capacitor	[C30,33,35]
15	0BRMDD22J103K	AD		C	Capacitor (630WV 0.01μF)	[C37]
16	0BRA1EFS102//	AH	N	C	Capacitor	[C16A,B]
17	0BRA1AFS222//	AH	N	C	Capacitor	[C18A,B,C]
18	0BRECQV1H474/	AD	N	C	Capacitor	[C45,26]
19	0BRHF12E471M/	AS	N	C	Capacitor	[C10A,B]
20	0BRDE1510E103	AG		C	Capacitor	[C11]
21	0BRECKD3D471/	AC	N	C	Capacitor	[C12]
22	0BRECQV1H473/	AB	N	C	Capacitor	[C40A,B]
23	0BRCEUSM1H100	AC		C	Capacitor (50WV 10μF)	[C14]
24	0BRCEUSM1E100	AC		C	Capacitor (25WV 10μF)	[C43]
25	0BREU2Z//////	AD		B	Diode	[D2A,B,8,12]
26	0BRFPU-12/////	AE	N	B	Diode	[D5,6]
27	0BRRU2B//////	AG		B	Diode	[D1]
28	0BR1SS82/////	AC		B	Diode	[D3,4,9]
29	0BRERA81-004/	AG	N	B	Diode	[D14]
30	0BREU2//////	AD	N	B	Diode	[D10,11]
31	0BRHZ15-2/////	AB	N	B	Zener diode	[ZD1]
32	0BRHZ5B-2/////	AB	N	B	Zener diode	[ZD2]
33	0BRHZ3A-1/////	AB		B	Diode (HZ6A-2)	[ZD3]
34	0BRRBV606/////	AK	N	B	Diode stack	[DS1]
35	0BRESAC92M-02	AH	N	B	Diode stack	[DS2]
36	0BRFMB-34M///	AQ	N	B	Diode stack	[DS3]
⚠ 37	0BRES3-3150//	AE	N	A	Fuse	[F1]
38	0BRTS-02-P-SN	AB		C	Clip-Fuse	[XF1]
39	0BRUPC78M05//	AH	N	B	IC	[IC1]
40	0BRUPC7912H//	AH	N	B	IC	[IC2]
41	0BRUPC7915H//	AH	N	B	IC	[IC3]
42	0BRTL7705CP-B	AM		B	IC	[IC4]
43	0BRUPC317H///	AN		B	IC (UPC317H)	[IC5]
44	0BRTL431CLPB/	AF	N	B	IC	[IC6]
45	0BRSTR9012////	AU	N	B	IC	[IC7]
46	0BR2SC3507////	AU		B	Transistor (2SC3507)	[TR1]
47	0BR2SD1308-K/	AG		B	Transistor (2SD1308)	[TR2]
48	0BR2SC1173-Y/	AG	N	B	Transistor	[TR3]
49	0BR2SC3568-K/	AM		B	Transistor (2SC3568)	[TR4]
50	0BR2SC2655////	AD	N	B	Transistor	[TR5]
51	0BR2SC1815////	AD	N	B	Transistor	[TR6]
52	0BRN13T1//////	AE	N	B	Put	[CR1]
53	0BRTLP-581////	AR	N	B	Photo cupler	[PC1,2]
54	0BRTM64KPH500	AE	N	B	Potentio meter	[VR1]
55	0BR5219-03A//	AE		C	Connector	[CN1]
56	0BRB5P-VH/////	AC	N	C	Connector	[CN2]
57	0BR5264-09A//	AP	N	C	Connector	[CN3]

11 Power supply unit··200V series

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
58	0BR5267-04ARD	AB	N	C	Connector	[CN4]
59	0BRB4P-VH////	AC	N	C	Connector	[CN5]
60	0BR5267-04AWT	AB	N	C	Connector	[CN6]
61	0BR5267-02AWT	AB	N	C	Connector	[CN7]
62	0BR5267-03AWT	AB	N	C	Connector	[CN8]
63	0BR5045-02A//	AB		C	Connector	[CN9]
64	0BR5277-02A//	AG		C	Connector	[CN10]
65	0BR487A-BE471	AG	N	B	Posistor	[PH1]
66	0BR8D-18/////	AQ		B	Thermister	[TH1A,B]
67	0BR4476P04018	AT		C	Choke coil	[L1]
68	0BRSE25H15100	AS	N	C	Choke coil	[L2]
69	0BR4476P03863	AH	N	C	Choke coil	[L4]
70	0BRFL9H471K//	AG		C	Chock coil	[L5]
71	0BRB-20F-38//	AD		B	Core	[L7A,B]
72	0BR4416P06095	BD	N	B	Transfomer	[T1]
73	0BR4416P05741	AQ		B	Transfomer	[T2]
74	0BRRS2FB33K-J	AB	N	C	Resistor	[R1A,B]
75	0BRRGC5-0.82-	AD	N	C	Resistor	[R4]
76	0BRRS2FB68K-J	AB	N	C	Resistor	[R5A,B]
77	0BRRS2FB33-J/	AB	N	C	Resistor	[R7]
78	0BRRS2FB680-J	AB	N	C	Resistor	[R2A,B]
79	0BRNAS114S222	AA	N	C	Resistor	[R3]
80	0BRNAS112S330	AA	N	C	Resistor	[R6]
81	0BRNAS112S101	AA	N	C	Resistor	[R32]
82	0BRFMR114B271	AC	N	C	Resistor	[R9]
83	0BRFMR114B821	AC	N	C	Resistor	[R10]
84	0BRFMR114B100	AC	N	C	Resistor	[R11,12]
85	0BRFMR112B150	AC	N	C	Resistor	[R30]
86	0BRNAS114F103	AA	N	C	Resistor	[R29]
87	0BRNAS114F102	AA	N	C	Resistor	[R41]
88	0BRNAS114F561	AA	N	C	Resistor	[R42]
89	0BRNAS114S154	AA	N	C	Resistor	[R43]
90	0BRFC02J-470/	AA	N	C	Resistor	[R18,33]
91	0BRFC02J-821/	AA	N	C	Resistor	[R19]
92	0BRFC02J-471/	AA	N	C	Resistor	[R20]
93	0BRFC02J-221/	AA	N	C	Resistor	[R21]
94	0BRFC02J-102/	AA	N	C	Resistor	[R28,34]
95	0BRFC02J-101/	AA	N	C	Resistor	[R35]
96	0BRNAS112F181	AA	N	C	Resistor	[R14]
97	0BRNAS112F681	AA	N	C	Resistor	[R16]
98	0BRNAS112F102	AA	N	C	Resistor	[R17]
99	0BRNAS114S102	AA	N	C	Resistor	[R15]
100	0BRNAS114S122	AA	N	C	Resistor	[R24]
101	0BRNAS114S181	AA	N	C	Resistor	[R25]
102	0BRNAS114S182	AA	N	C	Resistor	[R26]
103	0BRNAS114S220	AA	N	C	Resistor	[R27]
104	0BRNAS114F100	AA	N	C	Resistor	[R22]
105	0BRNAS114F681	AA	N	C	Resistor	[R25]
106	0BRNAS114F102	AA	N	C	Resistor	[R36]
107	0BRNAS114F101	AA	N	C	Resistor	[R37]
108	0BRNAS114F103	AA	N	C	Resistor	[R38,39]
109	0BRNAS114F472	AA	N	C	Resistor	[R40]
110	0BRRS2FB100-J	AC		C	Resistor	[R31]
	(Unit)					
901	RDENC1007ACZZ	BY	N	E	Power supply unit (200V series)	

12 Hard disk interface PWB unit···PC-7221 only

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0CT900800028//	BD	N	B	IC (27128-25)
2	0CT900800002//	BQ	N	B	IC (NDC 864)
3	0CT900800003//	BS	N	B	IC (NDC 870)
4	0CT900800004//	BE	N	B	IC (NCL 2000)
5	0CT900800005//	BG	N	B	IC (NCL 2002)
6	0CT900800006//	BB	N	B	MPU (μPD70008AG-6)
7	0CT900800007//	AP	N	B	IC (74F00NS)
8	0CT900800008//	AP	N	B	IC (74F02NS)
9	0CT900800009//	AT	N	B	IC (74F74NS)
10	0CT900800010//	AX	N	B	IC (74HCT240NS)
11	0CT900800011//	AG	N	B	IC (74LS00NS)
12	0CT900800012//	AG	N	B	IC (74LS04NS)
13	0CT900800013//	AN	N	B	IC (74LS14NS)
14	0CT900800014//	AH	N	B	IC (74LS32NS)
15	0CT900800015//	AM	N	B	IC (74LS123NS)
16	0CT900800016//	AM	N	B	IC (74LS125ANS)
17	0CT900800017//	AP	N	B	IC (74LS174NS)
18	0CT900800018//	AK	N	B	IC (74LS74NS)
19	0CT900800019//	AX	N	B	IC (MC3487P)
20	0CT900800020//	BB	N	B	IC (NDC 871-01)
21	0CT900800021//	AF	N	C	Resistor (C09×2.2KΩJ)
22	0CT900800022//	AF	N	C	Resistor (C09×6.8KΩJ)
23	0CT900800023//	AF	N	C	Resistor (C09×47KΩJ)
24	0CT900800024//	AA	N	C	Resistor (CRG 1/8 331J)(330Ω)
25	0CT900800025//	AA	N	C	Resistor (CRG 1/8 431J)(430Ω)
26	0CT900800026//	AA	N	C	Resistor (CRG 1/8 102J)(1KΩ)
27	0CT900800027//	AA	N	C	Resistor (CRG 1/8 682J)(6.8KΩ)
29	0CT900800029//	AC	N	C	Capacitor (GR40F104Z25)(0.1μF)
30	0CT900800030//	AC	N	C	Capacitor (GR40CH680J50)(68pF)
31	0CT900800031//	AG	N	C	Capacitor (KMA25VB-47)(47μF 25WB)
32	0CT900800032//	AL	N	C	Inductor coil (NL453232-101K)(100μH)
33	0CT900800033//	AP	N	C	Inductor coil (EL0405SKI-1R8J)(1.8μH)
34	0CT900800034//	AM	N	C	Inductor coil (SN-3-200)
35	0CT900800035//	BL	N	C	Coil (500C62ES)
36	0CT900800036//	BA	N	C	Coil (DCS-03-20)
37	0CT900800037//	AZ	N	B	Crystal (DOC-49)(15MHz)
38	0CT900800038//	AZ	N	B	Crystal (DOC-49)(5MHz)
39	0CT900800039//	AP	N	C	Sensor (PST518A)(4.2V ±0.2V)
40	0CT900800040//	AK	N	C	IC socket (641267-3)(28pin)
41	0CT900800041//	BE	N	C	Connector (00-9072-240-901883)(40P)
42	0CT900800042//	AX	N	C	Connector (PS-26PE-D4T1-B1)(24P)
43	0CT900800043//	AV	N	C	Connector (350211-1)(4P)
44	0CT900800044//	AC	N	C	Connector (00-9067-022-000-801)(2P2)
45	0CT900800045//	AD	N	C	Connector (00-9067-042-000-801)(4P2)
46	0CT900800046//	AE	N	C	Connector (00-9067-062-000-801)(6P2)
47	0CT900800047//	AC	N	C	Receptacle (00-9067-020-000-805)
48	0CT900800048//	AS	N	C	Resistor (6MOL 10KΩ)
49	0CT900800049//	AE	N	B	Terminal (TP8G)
50	0CT900800050//	AC	N	C	Capacitor (GR40B102K50)(1000pF)
	(Unit)				
901	DUNTK1693ACZZ	CK	N	E	HD interface PWB unit (PC-7221)

■ Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
[C]				
CBDRP1020AC0E	3- 17	BM	N	E
//	3- 110	BM	N	E
CBDRP1020AC0H	3- 17	BP	N	E
CBDRP1020AC0U	3- 17	BP	N	E
CBDRP1020AC0Y	3- 17	BP	N	E
CBDRP1021AC0G	3- 110	BP	N	E
CBDRP1022AC0F	3- 110	BP	N	E
CBDRP1023AC0I	3- 110	BP	N	E
CCABA1047AC02	1- 1	BZ	N	E
CCABA1047AC03	1- 1	BZ	N	E
CCABA1047AC11	1- 1	BZ	N	E
CCABA1047AC12	1- 1	BZ	N	E
CCABB1041AC40	1- 41	BG	N	E
CCABB1041AC41	1- 41	BE	N	E
CCABB1041AC42	1- 41	BE	N	E
CCABB1041AC50	1- 41	BE	N	E
CCABF2116HC01	4- 3	AX		D
CCABF2116HC03	4- 3	AW	N	D
CCNW-2814SC01	3- 11	AX		B
CFRM-1004AC01	2- 56	AZ	N	E
CFRM-1004AC02	2- 56	BA	N	E
CFRM-1005AC01	1- 33	AW	N	E
CFRM-1005AC02	1- 33	AV	N	E
CPLTP2060HC02	1- 7	AH		C
CPLTP2060HC04	1- 7	AM	N	C
CPWBF1115AC01	1- 74	AD	N	E
//	6- 901	AD	N	E
CPWBF1116AC01	1- 77	AE	N	E
//	9- 901	AE	N	E
CPWBF1116AC02	1- 77	AE	N	E
//	9- 901	AE	N	E
CPWBF1116AC03	1- 77	AE	N	E
//	9- 901	AE	N	E
CPWBS1114AC01	4- 7	BQ	N	E
//	7- 901	BQ	N	E
CPWBS1114AC02	4- 7	BQ	N	E
//	7- 901	BQ	N	E
CSOCA1017CCZZ	2- 35	BE		D
[D]				
DFLP-1085ACZZ	3- 14	AZ	N	D
//	3- 104	AZ	N	D
DFLP-1086ACZZ	3- 14	AZ	N	D
DFLP-1087ACZZ	3- 15	AZ	N	D
//	3- 116	AZ	N	D
DFLP-1088ACZZ	3- 15	AZ	N	D
DUNT-1694ACZZ	2- 12	**	N	E
DUNT-1695ACSA	2- 6	CG	N	E
DUNT-1695ACZZ	2- 6	CG	N	E
DUNT-1697ACZZ	4- 901	CM	N	E
DUNT-1715ACZZ	4- 901	CM	N	E
DUNT-1786ACZZ	1- 51	CV	N	E
DUNT-1790ACZZ	1- 51	CV	N	E
DUNT-1791ACZZ	4- 901	CM	N	E
DUNTK1693ACZZ	2- 17	CK	N	E
//	12- 901	CK	N	E
DUNTK1700ACZZ	2- 28	**	N	E
//	8- 901	**	N	E
DUNTK1796ACZZ	2- 28	**	N	E
//	8- 901	**	N	E
DUNTK1878ACZZ	2- 28	**	N	E
//	8- 901	**	N	E
[G]				
GCABE1042ACSA	4- 10	AN	N	D
GCABE1042ACZZ	4- 10	AN	N	D
GCASP1007ACSA	1- 22	AC	N	C
GCASP1007ACZZ	1- 22	AC	N	C
GCASP2023HCZZ	3- 61	AP		D
//	3- 201	AP		D
GCOVH1022ACZZ	4- 11	AC	N	D
GCOVH1024ACS1	2- 1	AG	N	D
GCOVH1024ACZ1	2- 1	AG	N	D
GCOVH1025ACZZ	2- 31	AK	N	C
GCOVH1026ACZZ	1- 35	AG	N	C
GCOVH1027ACZZ	9- 1	AB	N	C
GCOVH1032ACZZ	1- 38	AD	N	D
GFTAU1040ACSA	1- 25	AY	N	C
GFTAU1040ACZZ	1- 25	AY	N	C
GFTAZ1034ACZZ	1- 42	AL	N	C
GFTAZ1039ACZZ	2- 29	AL	N	C
GFTAZ2030HCZZ	1- 34	AF		C
GLEGG1009HCSA	1- 27	AB	N	C
GLEGG1009HCZZ	1- 27	AC		C
GLEGG1024CCZZ	1- 4	AA		C
GLEGG2008HCSA	4- 1	AC		C
GLEGG2008HCSC	4- 1	AC	N	C
GLEGP1009ACZZ	1- 27	AC	N	C
[H]				
HPNLC1026ACSA	2- 11	AF	N	D
HPNLC1026ACZZ	2- 11	AF	N	D
HPNLC2140HCSA	1- 3	AV	N	D
HPNLC2140HCZZ	1- 3	AP		D
HPNLC2141HCSA	2- 43	AE	N	D
HPNLC2141HCZZ	2- 43	AE		D
[J]				
JBTN-2048HCSB	1- 19	AC	N	D
JBTN-2048HCSC	1- 19	AE	N	D
JHNDP2004HCSA	1- 32	AY	N	C
JHNDP2004HCZZ	1- 32	AY		C
JKNBZ1876CCSA	1- 8	AB	N	C
JKNBZ1876CC01	1- 8	AB		C
[L]				
LANGF1530CCZZ	1- 13	AC		C
LANGG2301HCZZ	1- 71	AD		C
LANGQ1129ACZA	8- 1	AQ	N	C
LANGQ1129ACZB	8- 1	AT	N	C
LANGQ1129ACZZ	8- 1	AN	N	C
LANGQ2303HCZB	2- 37	AK	N	D
LANGQ2349HCZZ	1- 67	AD		C
LANGT1123ACZZ	2- 13	AH	N	C
LANGT1124ACZZ	1- 37	AC	N	C
LANGT1127ACZZ	2- 5	AF	N	C
LANGT1147ACZZ	2- 39	AF	N	C
LANGT2302HCZC	1- 65	AQ		C
LANGT2309HCZA	1- 80	AC	N	C
LBSHC5020BCZZ	1- 36	AB		C
LBSHZ2037SCZZ	2- 53	AD		C
LHLDW2045SCZZ	2- 58	AC		C
LPINS2030HCZZ	1- 30	AH		C
LPINS2031HCZZ	1- 24	AD		C
LPINS2032HCZZ	1- 5	AC		C
LPLTP1013ACZZ	3- 13	AC	N	D
//	3- 102	AC	N	D
LPLTP1015ACZZ	2- 4	AH	N	C
LSTPP2004HCZZ	1- 18	AC		C
LX-BZ1020ACZZ	4- 9	AA	N	C
LX-BZ1022ACZZ	2- 52	AB		C
LX-BZ1159CCZZ	1- 10	AA		C
LX-BZ2055HCZZ	1- 62	AB		C
LX-BZ2058HCZZ	1- 46	AA		C
LX-BZ2061HCZZ	8- 2	AB		C
LX-NZ2004HCZZ	8- 3	AA		C
[M]				
MLEVP1044CCSA	1- 11	AB	N	C
MLEVP1044CC01	1- 11	AB		C
MLEVP2023HCS1	1- 29	AF	N	C
MLEVP2023HCZ1	1- 29	AF	N	C
MLEVP2024HCS1	1- 31	AF	N	C
MLEVP2024HCZ1	1- 31	AF	N	C
MLOK-1004ACZZ	1- 61	AD	N	C
MSPRC2024HCZZ	1- 21	AA		C
MSPRC2025HCZZ	1- 6	AA		C
MSPRC2027HCZZ	1- 63	AA		C
MSPRC2029HCZZ	1- 12	AC		C
MSPRC2030HCZZ	1- 15	AC		C
MSPRD2028HCZZ	1- 64	AA		C
[N]				
NFANP1011ACZZ	2- 41	BA	N	B
[P]				
PBAR-1001ACZZ	1- 20	AC	N	C
PBAR-2011HCZZ	1- 17	AL		C
PCAPH1003ACZZ	8- 4	AC		C
PCAPH1007ACZZ	8- 5	AD	N	C
PCAPH1008ACZZ	8- 6	AC	N	C
PCUSG1006ACZZ	2- 38	AB		C
PDMPO1001ACZZ	1- 72	AE		C
PFILW1003ACSA	1- 2	AL	N	C
PFILW1003ACSB	1- 2	AL	N	C
PFILW1003ACZZ	1- 2	AL	N	C
PGUMM1004ACZZ	2- 54	AE		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
PSHEZ1009ACZZ	2- 57	AD	N	C
PSHEZ1010ACZZ	2- 51	AC	N	C
PSPAY1026ACZZ	9- 2	AB	N	C
PSPAZ1018ACZZ	2- 55	AB	N	C
PSPAZ2037HCZZ	1- 39	AE		C
PTME-2001HCZZ	1- 16	AC		C
PZETY1020ACZZ	2- 21	AK	N	C
PZETZ1024ACZZ	1- 47	AD	N	C
PZETZ1026ACZZ	1- 40	AC	N	C
〔Q〕				
QACCB0002PAZZ	3- 11	AY		B
QACCD7611QCN2	3- 11	AQ	N	B
QACCD7611QCZZ	3- 11	AT		B
QACCF7320QCZZ	3- 11	AX	N	B
QACCL7620QCZZ	3- 11	AW		B
QACCV6620QCZZ	3- 11	AV		B
QCNCM0548HC0B	8- 7	AA		C
QCNCM0550HC1J	8- 8	AB	N	C
QCNCM0552HC2E	8- 9	AP		C
QCNCM0563HC0C	9- 3	AB	N	B
QCNCM1060AC03	8- 18	AB		B
QCNCM1091AC3B	8- 10	AH	N	C
QCNCM1094AC9F	8- 11	AQ	N	C
QCNCM1095AC4J	8- 12	AL	N	C
QCNCM1109AC0E	9- 4	AB	N	C
QCNCM2346SC2J	8- 13	AG		C
QCNCM2346SC3D	8- 14	AL		C
QCNCM2346SC4J	8- 15	AL		C
QCNCM5039SC0E	6- 1	AB		C
QCNCM5039SC0F	9- 5	AB	N	C
QCNCM6865RC0I	8- 16	AC		C
QCNCW1057ACZZ	8- 17	AB		C
QCNCW1097AC0I	8- 19	AL	N	C
QCNCW1097AC2E	8- 20	AL	N	C
QCNCW1098AC6B	8- 21	AM	N	C
QCNCW1345CC0E	8- 22	AC	N	C
QCNCW2360SC3J	7- 1	AE	N	C
QCNW-1184ACZZ	8- 23	AW	N	C
QCNW-1186ACZZ	2- 15	AU	N	C
QCNW-1187ACZZ	2- 9	AH	N	C
QCNW-1188ACZZ	2- 8	AC	N	C
QCNW-1189ACZZ	2- 25	AH	N	C
QCNW-1191ACZZ	1- 75	AH	N	C
QCNW-1193ACZZ	2- 45	AF	N	C
QCNW-1194ACZZ	2- 45	AE	N	C
QCNW-1195ACZZ	4- 6	AL	N	C
〃	7- 2	AL	N	C
QCNW-1196ACZZ	1- 78	AE	N	C
QCNW-1197ACZZ	1- 79	AL		C
QCNW-1199ACZZ	2- 14	AP	N	C
QCNW-1200ACZZ	2- 26	AQ	N	C
QCNW-1215ACZZ	2- 27	AC	N	B
QCNW-1216ACZZ	2- 48	AC	N	C
〃	2- 49	AC	N	C
QCNW-1217ACZZ	2- 7	AX	N	C
QCNW-1218ACZZ	2- 10	AK	N	C
QCNW-1219ACZZ	1- 69	AC	N	C
QCNW-1222ACZZ	2- 45	AE	N	C
QCNW-1223ACZZ	2- 45	AG	N	C
QCNW-1235ACZZ	4- 6	AL	N	C
〃	7- 2	AL	N	C
QCNW-1236ACSA	1- 79	AL	N	C
QCNW-2330HCSA	3- 12	AT	N	C
QCNW-2330HCZZ	3- 12	AT		C
〃	3- 101	AT		C
QPLGA0010UCZZ	3- 11	AM		C
QPLGA1001ACZZ	3- 11	AH		B
QPLGA2005HCZZ	2- 33	AP		C
QPLGZ1003ACZZ	2- 35	AX	N	C
QSOCZE068HCZZ	8- 24	AX		C
QSOCZ6420ACZZ	8- 25	AE		C
QSOCZ6428ACZZ	8- 26	AE		C
QSOCZ6440ACZZ	8- 27	AG		C
QSW-C9221QCZZ	2- 44	AK		B
QSW-D0270FCZZ	8- 28	AG		B
QSW-K1047ACZZ	4- 4	BS	N	E
〃	5- 901	BS	N	E
QSW-K1048ACZZ	4- 4	BS	N	E
〃	5- 901	BS	N	E
QSW-K1053ACZZ	4- 4	BS	N	E

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
QSW-K1053ACZZ	5- 901	BS	N	E
QSW-K1054ACZZ	4- 4	BS	N	E
〃	5- 901	BS	N	E
QSW-K1055ACZZ	4- 4	BS	N	E
〃	5- 901	BS	N	E
QSW-K1057ACZZ	4- 4	BS	N	E
〃	5- 901	BS	N	E
QSW-K1058ACZZ	4- 4	BS	N	E
〃	5- 901	BS	N	E
QSW-K1065ACZZ	4- 4	BS	N	E
〃	5- 901	BS	N	E
QSW-M2043HCZZ	1- 68	AL		B
QSW-S1049ACSA	9- 6	AE	N	B
QSW-S1049ACZZ	9- 6	AE	N	B
QSW-S1060ACSA	8- 29	AE	N	B
QSW-S1060ACZZ	8- 29	AE	N	B
QSW-S1061ACSA	8- 30	AE	N	B
QSW-S1061ACZZ	8- 30	AE	N	B
〔R〕				
RALMB1007HCZZ	2- 40	AK		B
RC-EZ336BAC1C	7- 3	AB	N	C
RC-EZ475AAC1E	7- 4	AB	N	C
RC-KZ1018CCZZ	8- 31	AE		C
RC-KIE104HCZZ	7- 5	AB		C
〃	8- 32	AB		C
RC-KIH105HCZZ	8- 129	AF		C
RCiLL1001ACZZ	8- 33	AC		C
RCiLZ1003AC03	9- 7	AA	N	C
RCRSP1003CCZZ	8- 34	AT		B
RCRSZ1010HCZZ	8- 35	AR		B
RCRSZ1011HCZZ	8- 36	AR		B
RCRSZ1026ACZZ	8- 37	AR	N	B
RCRSZ1028ACZZ	8- 38	AR	N	B
RCRSZ1029ACZZ	8- 39	AK	N	B
RCRSZ1030ACZZ	8- 40	AR	N	B
RCRSZ1031ACZZ	7- 6	AK	N	B
RDENC1006ACZZ	2- 22	BX	N	E
〃	10- 901	BX	N	E
RDENC1007ACZZ	2- 22	BY	N	E
〃	11- 901	BY	N	E
RMPTC4102QCKB	8- 41	AC		B
RMPTC4103QCKB	8- 42	AC		B
RMPTC4331QCKB	8- 43	AB		B
RMPTC5682QCKB	8- 44	AB		B
RMPTC6472QCJB	8- 45	AC		B
RMPTC8102QCKB	8- 46	AD		B
RMPTC8472QCKB	7- 7	AD		B
RMPTC9102QCKB	8- 47	AD		B
RMPTW6101QCKE	8- 48	AD		B
RVR-Q1003ACSA	9- 8	AF	N	B
RVR-Q1003ACZZ	9- 8	AF	N	B
RVR-Q1004ACSA	9- 9	AF	N	B
RVR-Q1004ACZZ	9- 9	AF	N	B
RVR-Q1005ACSA	8- 49	AF	N	B
RVR-Q1005ACZZ	8- 49	AF	N	B
〔S〕				
SPAKA1834ACZZ	3- 3	AX	N	D
SPAKA1835ACZZ	3- 2	BC	N	D
SPAKA1836ACZZ	3- 4	AK	N	D
SPAKA1838ACZZ	3- 62	AK	N	D
SPAKA1891ACZZ	3- 107	AC	N	D
SPAKA1897ACZZ	3- 18	AE	N	D
SPAKA1899ACZZ	3- 6	AH	N	D
SPAKA2430HCZZ	3- 108	AL		D
SPAKA2433HCZZ	3- 103	AE		D
SPAKA2529HCZZ	3- 62	AF		D
〃	3- 202	AF		D
SPAKA2530HCZZ	3- 8	AB		D
SPAKA2531HCZZ	3- 19	AD		D
SPAKA2604HCZZ	3- 111	AU		D
SPAKC1837ACZZ	3- 5	AS	N	D
SPAKC1845ACZZ	3- 112	AL	N	D
SPAKC1851ACZZ	3- 5	AS	N	D
SPAKC1853ACZZ	3- 5	AT	N	D
SPAKC1855ACZZ	3- 5	AS	N	D
SPAKC1856ACZZ	3- 5	AT	N	D
SPAKC1857ACZZ	3- 5	AS	N	D
SPAKC2612HCZZ	3- 16	AH		D
〃	3- 105	AH		D
SPAKP2370HCZZ	3- 7	AF		D

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
SPAKP2397SCZZ	3- 1	AC		D
//	3- 109	AC		D
SSAKA0005WCZZ	3- 9	AA		D
SSAKA0231QCZZ	3- 114	AA		D
[T]				
TCADZ1056ACZZ	3- 106	AG	N	D
TINSE1390ACZZ	3- 63	BD	N	D
TINSE1391ACZZ	3- 63	BD	N	D
TINSE1393ACZZ	3- 63	BD	N	D
//	3- 203	BD	N	D
TINSE1394ACZZ	3- 64	AX	N	D
TINSE1395ACZZ	3- 64	AX	N	D
//	3- 204	AX	N	D
TINSE1396ACZZ	3- 10	AY	N	D
TINSE1401ACZZ	3- 10	BG	N	D
//	3- 113	BG	N	D
TINSE1420ACZZ	3- 115	BD	N	D
TINSF1398ACZZ	3- 203	BD	N	D
TINSG1399ACZZ	3- 203	BD	N	D
TINSI1400ACZZ	3- 203	BD	N	D
TLABE1290ACZZ	8- 128	AB	N	C
TLABM1245ACZZ	4- 12	AC	N	C
TLABM1248ACZZ	4- 12	AC	N	C
TLABM1249ACZZ	4- 12	AC	N	C
TLABM1250ACZZ	4- 12	AC	N	C
TLABM1251ACZZ	4- 12	AC	N	C
TLABM1252ACZZ	4- 12	AC	N	C
TLABM1253ACZZ	4- 12	AC	N	C
TLABM1254ACZZ	4- 12	AC	N	C
TLABM1280ACZZ	4- 12	AC	N	C
TLABZ1275ACSA	1- 43	AB	N	C
[U]				
UBATN1002ACZZ	8- 50	AT	N	S
UBDRP1020ACZZ	3- 65	AW	N	D
//	3- 205	AW	N	D
UBDRP1021ACZZ	3- 205	AW	N	D
UBDRP1022ACZZ	3- 205	AW	N	D
UBDRP1023ACZZ	3- 205	AW	N	D
UBNDA1008CCZZ	3- 20	AA		C
[V]				
VCCCPU1HH101J	8- 51	AB		C
VCCCPU1HH200J	7- 8	AB		C
//	8- 52	AB		C
VCCCPU1HH220J	8- 53	AA		C
VCCCPU1HH470J	8- 54	AA		C
VCCCPU1HH560J	8- 55	AA		C
VCEAGU1CW106M	8- 56	AA		C
VCEAGU1CW107M	8- 57	AB		C
VCEAGU1CW227M	8- 58	AB		C
VCEAGU1EW476M	8- 59	AB		C
VCKYPU1HB103K	8- 60	AA		C
VCKYPU1HB221K	8- 61	AB		C
VCKYPU1HB222K	8- 62	AA		C
VCKYPU1HB331K	8- 63	AA		C
VCKYPU1HB681K	7- 9	AA		C
//	8- 64	AA		C
VCQYNU1HM473K	8- 65	AB		C
VCQYNU1HM473M	8- 65	AA	N	C
VCSAVU1CE335M	8- 66	AB		C
VHDDSS131HV-1	7- 10	AA		B
VHDDS1588L2-1	8- 67	AB		B
VHDIS2075K/-1	5- 226	AB		B
VHIALS04ANS-1	8- 68	AD	N	B
VHIALS244ANS1	8- 69	AL	N	B
VHIALS245//-1	8- 70	AW		B
VHIALS253NS-1	8- 71	AE	N	B
VHIALS32NS/-1	8- 72	AD	N	B
VHIALS373NS-1	8- 73	AL	N	B
VHID41464C-10	8- 74	AT	N	B
VHIMB4107//-1	8- 75	BA		B
VHIMN1288//-1	8- 76	BB	N	B
VHIMN1292//-1	8- 77	BC	N	B
VHIMN1294//-1	8- 78	BC	N	B
VHIM41256-Z12	8- 79	AS	N	B
VHIM5M4164-12	8- 80	AN	N	B
VHIM5M4464-12	8- 81	AS	N	B
VHIN286-10C2H	8- 82	BY	N	B
VHISC146818P1	8- 83	AW		B
VHISC4751//-1	8- 84	BR	N	B
VHISC4752//-1	8- 85	BT	N	B

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
VHISN74LS07NS	7- 11	AF		B
VHISN74LS12NS	8- 86	AD	N	B
VHISN74LS14NS	8- 87	AL	N	B
VHISN7406NS-1	8- 88	AF	N	B
VHISN7407NS-1	8- 89	AF	N	B
VHITC4066BF-1	8- 90	AE	N	B
VHITC74HC00FN	8- 91	AD		B
VHITC74HC138F	7- 12	AL		B
VHITC74HC244F	7- 13	AM		B
VHITC74HC373F	7- 14	AK		B
VHITL431CLP-1	8- 92	AG		B
VHITQS175S/-1	8- 93	AW	N	B
VHIT80C49AF-1	7- 16	AV	N	B
VHIUA1488//-1	8- 94	AH		B
VHIUA1489A/-1	8- 95	AH		B
VHIUPD449G/-1	8- 96	AQ		B
VHI2464/AAA0B	7- 15	AV	N	B
VHI27128AAC0B	8- 97	AS	N	B
VHI27256AAE0E	8- 98	AW	N	B
VHI27256AAE1E	8- 98	AW	N	B
VHI27256AAF0E	8- 98	AW	N	B
VHI27256AAF1E	8- 98	AW	N	B
VHI27256AAG0E	8- 98	AW	N	B
VHI27256AAG1E	8- 98	AW	N	B
VHI74F00///-1	8- 99	AF		B
VHI74F04///-1	8- 100	AE		B
VHI74F373SJ-1	8- 101	AN	N	B
VHI74F374SJ-1	8- 102	AN	N	B
VHI74LS125ANS	8- 103	AF	N	B
VHI74LS126ANS	8- 104	AF	N	B
VHI74LS244NS1	8- 105	AH	N	B
VHI8742/AAA0B	8- 106	BG	N	B
VHPGL9HY2//-1	6- 2	AC		B
VHPGL9NG2//-1	6- 3	AB		B
VHPPC817D//-1	8- 107	AD		B
VRD-HT2EY000J	8- 108	AA		C
VRD-HT2EY154J	9- 10	AA		C
VRD-HT2HY565J	8- 109	AA	N	C
VRD-RC2EY100J	7- 17	AA		C
VRD-RC2EY101J	7- 18	AA		C
//	8- 110	AA		C
VRD-RC2EY102J	8- 111	AA		C
VRD-RC2EY103J	8- 112	AA		C
VRD-RC2EY104J	7- 19	AA		C
VRD-RC2EY121J	6- 4	AA		C
//	7- 20	AA		C
VRD-RC2EY122J	8- 113	AA		C
VRD-RC2EY152J	8- 114	AA		C
VRD-RC2EY153J	8- 115	AA		C
VRD-RC2EY154J	8- 116	AA		C
VRD-RC2EY200J	8- 117	AA		C
VRD-RC2EY221J	8- 118	AA		C
VRD-RC2EY271J	6- 5	AA		C
VRD-RC2EY333J	7- 21	AA		C
//	8- 119	AA		C
VRD-RC2EY392J	7- 22	AA		C
VRD-RC2EY433J	8- 120	AA	N	C
VRD-RC2EY472J	8- 121	AA		C
VRD-RC2EY682J	8- 122	AA		C
VRD-RC2EY822G	8- 123	AA		C
VRD-RC2EY822J	8- 124	AA		C
VRNRC2EK2201F	8- 125	AA		C
VS2SA673-C/-1	8- 126	AE		B
VS2SC1214-C-1	8- 127	AE		B
[X]				
XBBSC30P06000	1- 9	AA		C
XBBSC30P08000	2- 36	AA		C
XBBSD30P05000	1- 26	AA	N	C
//	2- 2	AA	N	C
XBBSD30P06000	1- 23	AA		C
//	2- 16	AA		C
//	2- 30	AA		C
XBPBZ40P06K00	2- 46	AA		C
//	2- 47	AA		C
XBPSD20P04000	1- 73	AA		C
XBPSD20P08000	1- 70	AA		C
XBPSD30P04000	4- 8	AA		C
XBPSD30P06K00	2- 3	AA		C
XBPSD30P06000	2- 32	AA		C
XBPSD40P06K00	2- 50	AA		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
XBPSD40P08KS0	1- 28	AA		C
XBPSD40P28KS0	2- 42	AA		C
XBSSD30P08000	2- 32	AA		C
〃	2- 34	AA		C
XBSSD40P06000	1- 66	AA		C
XBTSC40P06000	1- 44	AA		C
XCPSD26P06000	1- 14	AA		C
XUBSC30P10000	4- 2	AA	N	C
XUBSD30P08000	1- 76	AA		C
XUBSF30P10000	4- 2	AA		C
XUPSD30P08000	4- 5	AA		C
〔0〕				
0BRA1AFS222//	10- 16	AH	N	C
〃	11- 17	AH	N	C
0BRA1EFS102//	10- 15	AH	N	C
〃	11- 16	AH	N	C
0BRB-20F-38//	10- 72	AD		B
〃	11- 71	AD		B
0BRB4P-VH////	10- 61	AC	N	C
〃	11- 59	AC	N	C
0BRB5P-VH////	10- 58	AC	N	C
〃	11- 56	AC	N	C
0BRCEUSM1C221	10- 10	AC		C
〃	11- 10	AC		C
0BRCEUSM1C222	10- 4	AG		C
〃	11- 3	AG		C
0BRCEUSM1E100	10- 23	AC		C
〃	11- 24	AC		C
0BRCEUSM1E101	10- 6	AD		C
〃	10- 24	AD		C
〃	11- 5	AD		C
〃	11- 6	AD		C
0BRCEUSM1E471	10- 5	AF		C
〃	11- 4	AF		C
0BRCEUSM1H100	10- 9	AC		C
〃	10- 22	AC		C
〃	11- 9	AC		C
〃	11- 23	AC		C
0BRCEUSM1H101	10- 7	AE		C
〃	11- 7	AE		C
0BRCEUSM1V330	10- 8	AC		C
〃	11- 8	AC		C
0BRDE1510E103	11- 20	AG		C
0BRDE7090B102	11- 2	AD	N	C
0BRDE7100F222	10- 2	AL		C
0BRDE7120F332	10- 3	AD	N	C
0BRECKD3D221/	10- 21	AC	N	C
0BRECKD3D471/	10- 20	AC	N	C
〃	11- 21	AC	N	C
0BRECQV1H104/	10- 12	AC	N	C
〃	10- 25	AC	N	C
〃	11- 12	AC	N	C
〃	11- 13	AC	N	C
0BRECQV1H473/	10- 13	AB	N	C
〃	10- 26	AB	N	C
〃	11- 14	AB	N	C
〃	11- 22	AB	N	C
0BRECQV1H474/	10- 17	AD	N	C
〃	11- 18	AD	N	C
0BRERA81-004/	10- 31	AG	N	B
〃	11- 29	AG	N	B
0BRESAC92M-02	10- 36	AH	N	B
〃	11- 35	AH	N	B
0BRES3-3150//	11- 37	AE	N	A
0BREU2//////	11- 30	AD	N	B
0BREU2Z//////	10- 27	AD		B
〃	11- 25	AD		B
0BRFC02J-101/	10- 91	AA	N	C
〃	11- 95	AA	N	C
0BRFC02J-102/	10- 90	AA	N	C
〃	11- 94	AA	N	C
0BRFC02J-221/	10- 89	AA	N	C
〃	11- 93	AA	N	C
0BRFC02J-470/	10- 86	AA	N	C
〃	11- 90	AA	N	C
0BRFC02J-471/	10- 88	AA	N	C
〃	11- 92	AA	N	C
0BRFC02J-821/	10- 87	AA	N	C
〃	11- 91	AA	N	C
0BRFL9H471K//	10- 71	AG		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
0BRFL9H471K//	11- 70	AG		C
0BRFMB-34M///	10- 37	AQ	N	B
〃	11- 36	AQ	N	B
0BRFMR112B100	10- 85	AC	N	C
0BRFMR112B150	11- 85	AC	N	C
0BRFMR114B100	11- 84	AC	N	C
0BRFMR114B271	11- 82	AC	N	C
0BRFMR114B391	10- 83	AC	N	C
0BRFMR114B821	11- 83	AC	N	C
0BRFPU-12////	10- 28	AE	N	B
〃	11- 26	AE	N	B
0BRGGS5//////	10- 39	AE	N	A
0BRHF12E471M/	10- 18	AS	N	C
〃	11- 19	AS	N	C
0BRHZ15-2////	10- 32	AB	N	B
〃	11- 31	AB	N	B
0BRHZ3A-1////	10- 34	AB		B
〃	11- 33	AB		B
0BRHZ5B-2////	11- 32	AB	N	B
0BRHZ6A-1////	10- 33	AB		B
0BRMDD22G223M	10- 19	AC	N	C
0BRMDD22J103K	10- 14	AD		C
〃	11- 15	AD		C
0BRNAS112F102	10- 98	AA	N	C
〃	11- 98	AA	N	C
0BRNAS112F181	10- 95	AA	N	C
〃	11- 96	AA	N	C
0BRNAS112F681	10- 97	AA	N	C
〃	11- 97	AA	N	C
0BRNAS112S101	11- 81	AA	N	C
0BRNAS112S330	10- 82	AA	N	C
〃	11- 80	AA	N	C
0BRNAS114F100	10- 102	AA	N	C
〃	11- 104	AA	N	C
0BRNAS114F101	10- 105	AA	N	C
〃	11- 107	AA	N	C
0BRNAS114F102	10- 92	AA	N	C
〃	10- 104	AA	N	C
〃	11- 87	AA	N	C
〃	11- 106	AA	N	C
0BRNAS114F103	10- 94	AA	N	C
〃	10- 106	AA	N	C
〃	11- 86	AA	N	C
〃	11- 108	AA	N	C
0BRNAS114F472	10- 107	AA	N	C
〃	11- 109	AA	N	C
0BRNAS114F561	10- 93	AA	N	C
〃	11- 88	AA	N	C
0BRNAS114F681	10- 103	AA	N	C
〃	11- 105	AA	N	C
0BRNAS114S102	10- 96	AA	N	C
〃	11- 99	AA	N	C
0BRNAS114S122	11- 100	AA	N	C
0BRNAS114S154	11- 89	AA	N	C
0BRNAS114S181	10- 99	AA	N	C
〃	11- 101	AA	N	C
0BRNAS114S182	10- 100	AA	N	C
〃	11- 102	AA	N	C
0BRNAS114S220	10- 101	AA	N	C
〃	11- 103	AA	N	C
0BRNAS114S222	10- 81	AA	N	C
〃	11- 79	AA	N	C
0BRN13T1//////	10- 54	AE	N	B
〃	11- 52	AE	N	B
0BRPS2401-1//	10- 55	AG		B
0BRRBV604////	10- 35	AH	N	B
0BRRBV606////	11- 34	AK	N	B
0BRRGC5-0.68-	10- 76	AD	N	C
0BRRGC5-0.82-	11- 75	AD	N	C
0BRRMR114B100	10- 84	AC	N	C
0BRRS2FB10K-J	10- 75	AB	N	C
0BRRS2FB100-J	10- 108	AC		C
〃	11- 110	AC		C
0BRRS2FB100K-	10- 77	AC		C
0BRRS2FB22-J/	10- 78	AC		C
0BRRS2FB33-J/	10- 79	AB	N	C
〃	11- 77	AB	N	C
0BRRS2FB33K-J	11- 74	AB	N	C
0BRRS2FB68K-J	11- 76	AB	N	C
0BRRS2FB680-J	10- 80	AB	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
0BRRS2FB680-J	11- 78	AB	N	C
0BRRU2///////	10- 29	AF	N	B
0BRRU2B//////	11- 27	AG		B
0BRSC-02-20J/	10- 69	AP	N	C
0BRSC-02-50J/	10- 68	AP	N	C
0BRSE25H15100	11- 68	AS	N	C
0BRSTR9012///	10- 47	AU	N	B
//	11- 45	AU	N	B
0BRTLP-581///	11- 53	AR	N	B
0BRTL431CLPB/	10- 46	AF	N	B
//	11- 44	AF	N	B
0BRTL7705CP-B	10- 44	AM		B
//	11- 42	AM		B
0BRTM64KPH500	10- 56	AE	N	B
//	11- 54	AE	N	B
0BRTS-02-P-SN	10- 40	AB		C
//	11- 38	AB		C
0BRUPC317H///	10- 45	AN		B
//	11- 43	AN		B
0BRUPC78M05//	10- 41	AH	N	B
//	11- 39	AH	N	B
0BRUPC7912H//	10- 42	AH	N	B
//	11- 40	AH	N	B
0BRUPC7915H//	10- 43	AH	N	B
//	11- 41	AH	N	B
0BRXE104/////	10- 1	AG		C
//	11- 1	AG		C
0BR1SS82/////	10- 30	AC		B
//	11- 28	AC		B
0BR10PS1-2200	10- 11	AK	N	C
0BR10PS102200	11- 11	AK	N	C
0BR2SC1173-Y/	10- 50	AG	N	B
//	11- 48	AG	N	B
0BR2SC1815///	10- 53	AD	N	B
//	11- 51	AD	N	B
0BR2SC2655///	10- 52	AD	N	B
//	11- 50	AD	N	B
0BR2SC2751-L/	10- 48	AQ		B
0BR2SC3507///	11- 46	AU		B
0BR2SC3568-K/	10- 51	AM		B
//	11- 49	AM		B
0BR2SD1308-K/	10- 49	AG		B
//	11- 47	AG		B
0BR4D-18/////	10- 67	AL	N	B
0BR4416P05741	10- 74	AQ		B
//	11- 73	AQ		B
0BR4416P06095	10- 73	BD	N	B
//	11- 72	BD	N	B
0BR4476P03863	10- 70	AH	N	C
//	11- 69	AH	N	C
0BR4476P04018	11- 67	AT		C
0BR487A-BE471	10- 66	AG	N	B
//	11- 65	AG	N	B
0BR5045-02A//	10- 65	AB		C
//	11- 63	AB		C
0BR5219-03A//	10- 57	AE		C
//	11- 55	AE		C
0BR5264-09A//	10- 59	AP	N	C
//	11- 57	AP	N	C
0BR5267-02AWT	10- 63	AB	N	C
//	11- 61	AB	N	C
0BR5267-03AWT	10- 64	AB	N	C
//	11- 62	AB	N	C
0BR5267-04ARD	10- 60	AB	N	C
//	11- 58	AB	N	C
0BR5267-04AWT	10- 62	AB	N	C
//	11- 60	AB	N	C
0BR5277-02A//	11- 64	AG		C
0BR8D-18/////	11- 66	AQ		B
0CT90080002//	12- 2	BQ	N	B
0CT90080003//	12- 3	BS	N	B
0CT90080004//	12- 4	BE	N	B
0CT90080005//	12- 5	BG	N	B
0CT90080006//	12- 6	BB	N	B
0CT90080007//	12- 7	AP	N	B
0CT90080008//	12- 8	AP	N	B
0CT90080009//	12- 9	AT	N	B
0CT90080010//	12- 10	AX	N	B
0CT90080011//	12- 11	AG	N	B
0CT90080012//	12- 12	AG	N	B

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
0CT90080013//	12- 13	AN	N	B
0CT90080014//	12- 14	AH	N	B
0CT90080015//	12- 15	AM	N	B
0CT90080016//	12- 16	AM	N	B
0CT90080017//	12- 17	AP	N	B
0CT90080018//	12- 18	AK	N	B
0CT90080019//	12- 19	AX	N	B
0CT90080020//	12- 20	BB	N	B
0CT90080021//	12- 21	AF	N	C
0CT90080022//	12- 22	AF	N	C
0CT90080023//	12- 23	AF	N	C
0CT90080024//	12- 24	AA	N	C
0CT90080025//	12- 25	AA	N	C
0CT90080026//	12- 26	AA	N	C
0CT90080027//	12- 27	AA	N	C
0CT90080028//	12- 1	BD	N	B
0CT90080029//	12- 29	AC	N	C
0CT90080030//	12- 30	AC	N	C
0CT90080031//	12- 31	AG	N	C
0CT90080032//	12- 32	AL	N	C
0CT90080033//	12- 33	AP	N	C
0CT90080034//	12- 34	AM	N	C
0CT90080035//	12- 35	BL	N	C
0CT90080036//	12- 36	BA	N	C
0CT90080037//	12- 37	AZ	N	B
0CT90080038//	12- 38	AZ	N	B
0CT90080039//	12- 39	AP	N	C
0CT90080040//	12- 40	AK	N	C
0CT90080041//	12- 41	BE	N	C
0CT90080042//	12- 42	AX	N	C
0CT90080043//	12- 43	AV	N	C
0CT90080044//	12- 44	AC	N	C
0CT90080045//	12- 45	AD	N	C
0CT90080046//	12- 46	AE	N	C
0CT90080047//	12- 47	AC	N	C
0CT90080048//	12- 48	AS	N	C
0CT90080049//	12- 49	AE	N	B
0CT90080050//	12- 50	AC	N	C
00PA7KEB99CA1	5- 100	AK	N	C
00PA7KEB99CA2	5- 101	AK	N	C
00PA7KEB99CA3	5- 102	AK	N	C
00PA7KEB99CA4	5- 103	AK	N	C
00PA7KEB99CA5	5- 104	AK	N	C
00PA7KEB99CA6	5- 105	AK	N	C
00PA7KEB99CA7	5- 106	AQ	N	C
00PA7KEB99CA9	5- 108	AQ	N	C
00PA7KEB99CB2	5- 110	AK	N	C
00PA7KEB99CB4	5- 112	AK	N	C
00PA7KEB99CB5	5- 113	AK	N	C
00PA7KEB99CB6	5- 114	AK	N	C
00PA7KEB99CB7	5- 115	AK	N	C
00PA7KEB99CB8	5- 116	AK	N	C
00PA7KEB99CB9	5- 117	AK	N	C
00PA7KEB99CC1	5- 118	AK	N	C
00PA7KEB99CC2	5- 119	AK	N	C
00PA7KEB99CC3	5- 120	AK	N	C
00PA7KEB99CC4	5- 121	AK	N	C
00PA7KEB99CC5	5- 122	AK	N	C
00PA7KEB99CC6	5- 123	AK	N	C
00PA7KEB99CD1	5- 127	AK	N	C
00PA7KEB99C01	5- 1	AK	N	C
00PA7KEB99C02	5- 2	AK	N	C
00PA7KEB99C03	5- 3	AK	N	C
00PA7KEB99C04	5- 4	AK	N	C
00PA7KEB99C05	5- 5	AK	N	C
00PA7KEB99C06	5- 6	AK	N	C
00PA7KEB99C07	5- 7	AK	N	C
00PA7KEB99C08	5- 8	AK	N	C
00PA7KEB99C09	5- 9	AK	N	C
00PA7KEB99C10	5- 10	AK	N	C
00PA7KEB99C11	5- 11	AK	N	C
00PA7KEB99C12	5- 12	AK	N	C
00PA7KEB99C13	5- 13	AK	N	C
00PA7KEB99C15	5- 15	AQ	N	C
00PA7KEB99C16	5- 16	AQ	N	C
00PA7KEB99C17	5- 17	AK	N	C
00PA7KEB99C18	5- 18	AK	N	C
00PA7KEB99C19	5- 19	AK	N	C
00PA7KEB99C20	5- 20	AK	N	C
00PA7KEB99C21	5- 21	AK	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
00PA7KEB99C22	5- 22	AK	N	C
00PA7KEB99C23	5- 23	AK	N	C
00PA7KEB99C24	5- 24	AK	N	C
00PA7KEB99C25	5- 25	AK	N	C
00PA7KEB99C26	5- 26	AK	N	C
00PA7KEB99C27	5- 27	AK	N	C
00PA7KEB99C28	5- 28	AK	N	C
00PA7KEB99C29	5- 29	AK	N	C
00PA7KEB99C31	5- 31	AK	N	C
00PA7KEB99C32	5- 32	AK	N	C
00PA7KEB99C33	5- 33	AK	N	C
00PA7KEB99C34	5- 34	AK	N	C
00PA7KEB99C35	5- 35	AK	N	C
00PA7KEB99C36	5- 36	AK	N	C
00PA7KEB99C37	5- 37	AK	N	C
00PA7KEB99C38	5- 38	AK	N	C
00PA7KEB99C39	5- 39	AK	N	C
00PA7KEB99C40	5- 40	AK	N	C
00PA7KEB99C41	5- 41	AK	N	C
00PA7KEB99C43	5- 43	AQ	N	C
00PA7KEB99C44	5- 44	AQ	N	C
00PA7KEB99C46	5- 46	AK	N	C
00PA7KEB99C47	5- 47	AK	N	C
00PA7KEB99C48	5- 48	AK	N	C
00PA7KEB99C49	5- 49	AK	N	C
00PA7KEB99C50	5- 50	AK	N	C
00PA7KEB99C51	5- 51	AK	N	C
00PA7KEB99C52	5- 52	AK	N	C
00PA7KEB99C53	5- 53	AK	N	C
00PA7KEB99C54	5- 54	AK	N	C
00PA7KEB99C55	5- 55	AK	N	C
00PA7KEB99C57	5- 57	AQ	N	C
00PA7KEB99C58	5- 58	AQ	N	C
00PA7KEB99C60	5- 60	AQ	N	C
00PA7KEB99C62	5- 62	AQ	N	C
00PA7KEB99C64	5- 64	AQ	N	C
00PA7KEB99C75	5- 75	AK	N	C
00PA7KEB99C76	5- 76	AK	N	C
00PA7KEB99C79	5- 79	AK	N	C
00PA7KEB99C80	5- 80	AK	N	C
00PA7KEB99C81	5- 81	AK	N	C
00PA7KEB99C83	5- 83	AK	N	C
00PA7KEB99C84	5- 84	AK	N	C
00PA7KEB99C85	5- 85	AK	N	C
00PA7KEB99C86	5- 86	AK	N	C
00PA7KEB99C89	5- 89	AK	N	C
00PA7KEB99C91	5- 91	AK	N	C
00PA7KEB99C92	5- 92	AK	N	C
00PA7KEB99C93	5- 93	AK	N	C
00PA7KEB99C95	5- 95	AK	N	C
00PA7KEB99C96	5- 96	AK	N	C
00PA7KEB99C97	5- 97	AK	N	C
00PA7KEB99C98	5- 98	AK	N	C
00PA7KEB99C99	5- 99	AQ	N	C
00PA7KEC23AA1	5- 100	AK	N	C
00PA7KEC23AA2	5- 101	AK	N	C
00PA7KEC23AA3	5- 102	AK	N	C
00PA7KEC23AA4	5- 103	AK	N	C
00PA7KEC23AA5	5- 104	AK	N	C
00PA7KEC23AA6	5- 105	AK	N	C
00PA7KEC23AA7	5- 106	AQ	N	C
00PA7KEC23AA9	5- 108	AQ	N	C
00PA7KEC23AB2	5- 110	AK	N	C
00PA7KEC23AB4	5- 112	AK	N	C
00PA7KEC23AB5	5- 113	AK	N	C
00PA7KEC23AB6	5- 114	AK	N	C
00PA7KEC23AB7	5- 115	AK	N	C
00PA7KEC23AB8	5- 116	AK	N	C
00PA7KEC23AB9	5- 117	AK	N	C
00PA7KEC23AC1	5- 118	AK	N	C
00PA7KEC23AC2	5- 119	AK	N	C
00PA7KEC23AC3	5- 120	AK	N	C
00PA7KEC23AC4	5- 121	AK	N	C
00PA7KEC23AC5	5- 122	AK	N	C
00PA7KEC23AC6	5- 123	AK	N	C
00PA7KEC23AD1	5- 127	AK	N	C
00PA7KEC23AD4	5- 45	AK	N	C
00PA7KEC23AD5	5- 41	AK	N	C
00PA7KEC23AD6	5- 40	AK	N	C
00PA7KEC23AD9	5- 12	AK	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
00PA7KEC23A02	5- 2	AK	N	C
00PA7KEC23A06	5- 6	AK	N	C
00PA7KEC23A07	5- 7	AK	N	C
00PA7KEC23A13	5- 13	AK	N	C
00PA7KEC23A15	5- 15	AQ	N	C
00PA7KEC23A16	5- 16	AQ	N	C
00PA7KEC23A17	5- 17	AK	N	C
00PA7KEC23A18	5- 18	AK	N	C
00PA7KEC23A19	5- 19	AK	N	C
00PA7KEC23A20	5- 20	AK	N	C
00PA7KEC23A21	5- 21	AK	N	C
00PA7KEC23A22	5- 22	AK	N	C
00PA7KEC23A23	5- 23	AK	N	C
00PA7KEC23A24	5- 24	AK	N	C
00PA7KEC23A25	5- 25	AK	N	C
00PA7KEC23A26	5- 26	AK	N	C
00PA7KEC23A27	5- 27	AK	N	C
00PA7KEC23A31	5- 31	AK	N	C
00PA7KEC23A32	5- 32	AK	N	C
00PA7KEC23A33	5- 33	AK	N	C
00PA7KEC23A34	5- 34	AK	N	C
00PA7KEC23A35	5- 35	AK	N	C
00PA7KEC23A36	5- 36	AK	N	C
00PA7KEC23A37	5- 37	AK	N	C
00PA7KEC23A38	5- 38	AK	N	C
00PA7KEC23A39	5- 39	AK	N	C
00PA7KEC23A40	5- 40	AK	N	C
00PA7KEC23A41	5- 41	AK	N	C
00PA7KEC23A43	5- 43	AQ	N	C
00PA7KEC23A44	5- 44	AQ	N	C
00PA7KEC23A46	5- 46	AK	N	C
00PA7KEC23A47	5- 47	AK	N	C
00PA7KEC23A48	5- 48	AK	N	C
00PA7KEC23A49	5- 49	AK	N	C
00PA7KEC23A50	5- 50	AK	N	C
00PA7KEC23A51	5- 51	AK	N	C
00PA7KEC23A52	5- 52	AK	N	C
00PA7KEC23A53	5- 53	AK	N	C
00PA7KEC23A54	5- 54	AK	N	C
00PA7KEC23A55	5- 55	AK	N	C
00PA7KEC23A57	5- 57	AQ	N	C
00PA7KEC23A58	5- 58	AQ	N	C
00PA7KEC23A60	5- 60	AQ	N	C
00PA7KEC23A62	5- 62	AQ	N	C
00PA7KEC23A64	5- 64	AQ	N	C
00PA7KEC23A75	5- 75	AK	N	C
00PA7KEC23A76	5- 76	AK	N	C
00PA7KEC23A79	5- 79	AK	N	C
00PA7KEC23A80	5- 80	AK	N	C
00PA7KEC23A81	5- 81	AK	N	C
00PA7KEC23A83	5- 83	AK	N	C
00PA7KEC23A84	5- 84	AK	N	C
00PA7KEC23A85	5- 85	AK	N	C
00PA7KEC23A86	5- 86	AK	N	C
00PA7KEC23A89	5- 89	AK	N	C
00PA7KEC23A91	5- 91	AK	N	C
00PA7KEC23A92	5- 92	AK	N	C
00PA7KEC23A93	5- 93	AK	N	C
00PA7KEC23A95	5- 95	AK	N	C
00PA7KEC23A96	5- 96	AK	N	C
00PA7KEC23A97	5- 97	AK	N	C
00PA7KEC23A98	5- 98	AK	N	C
00PA7KEC23A99	5- 99	AQ	N	C
00PA7KEC24AA1	5- 100	AK	N	C
00PA7KEC24AA2	5- 101	AK	N	C
00PA7KEC24AA3	5- 102	AK	N	C
00PA7KEC24AA4	5- 103	AK	N	C
00PA7KEC24AA5	5- 104	AK	N	C
00PA7KEC24AA6	5- 105	AK	N	C
00PA7KEC24AA7	5- 106	AQ	N	C
00PA7KEC24AA9	5- 108	AQ	N	C
00PA7KEC24AB4	5- 112	AK	N	C
00PA7KEC24AB5	5- 113	AK	N	C
00PA7KEC24AB6	5- 114	AK	N	C
00PA7KEC24AB7	5- 115	AK	N	C
00PA7KEC24AB8	5- 116	AK	N	C
00PA7KEC24AB9	5- 117	AK	N	C
00PA7KEC24AC1	5- 118	AK	N	C
00PA7KEC24AC2	5- 119	AK	N	C
00PA7KEC24AC3	5- 120	AK	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
00PA7KEC24AC4	5- 121	AK	N	C	
00PA7KEC24AC5	5- 122	AK	N	C	
00PA7KEC24AC6	5- 123	AK	N	C	
00PA7KEC24AD1	5- 127	AK	N	C	
00PA7KEC24A01	5- 1	AK	N	C	
00PA7KEC24A02	5- 2	AK	N	C	
00PA7KEC24A15	5- 15	AQ	N	C	
00PA7KEC24A16	5- 16	AQ	N	C	
00PA7KEC24A17	5- 17	AK	N	C	
00PA7KEC24A18	5- 18	AK	N	C	
00PA7KEC24A19	5- 19	AK	N	C	
00PA7KEC24A20	5- 20	AK	N	C	
00PA7KEC24A21	5- 21	AK	N	C	
00PA7KEC24A22	5- 22	AK	N	C	
00PA7KEC24A23	5- 23	AK	N	C	
00PA7KEC24A24	5- 24	AK	N	C	
00PA7KEC24A25	5- 25	AK	N	C	
00PA7KEC24A26	5- 26	AK	N	C	
00PA7KEC24A27	5- 27	AK	N	C	
00PA7KEC24A31	5- 31	AK	N	C	
00PA7KEC24A32	5- 32	AK	N	C	
00PA7KEC24A33	5- 33	AK	N	C	
00PA7KEC24A34	5- 34	AK	N	C	
00PA7KEC24A35	5- 35	AK	N	C	
00PA7KEC24A36	5- 36	AK	N	C	
00PA7KEC24A37	5- 37	AK	N	C	
00PA7KEC24A38	5- 38	AK	N	C	
00PA7KEC24A39	5- 39	AK	N	C	
00PA7KEC24A40	5- 40	AK	N	C	
00PA7KEC24A41	5- 41	AK	N	C	
00PA7KEC24A42	5- 42	AK	N	C	
00PA7KEC24A43	5- 43	AQ	N	C	
00PA7KEC24A44	5- 44	AQ	N	C	
00PA7KEC24A45	5- 45	AK	N	C	
00PA7KEC24A46	5- 46	AK	N	C	
00PA7KEC24A47	5- 47	AK	N	C	
00PA7KEC24A48	5- 48	AK	N	C	
00PA7KEC24A49	5- 49	AK	N	C	
00PA7KEC24A50	5- 50	AK	N	C	
00PA7KEC24A51	5- 51	AK	N	C	
00PA7KEC24A52	5- 52	AK	N	C	
00PA7KEC24A53	5- 53	AK	N	C	
00PA7KEC24A54	5- 54	AK	N	C	
00PA7KEC24A55	5- 55	AK	N	C	
00PA7KEC24A57	5- 57	AQ	N	C	
00PA7KEC24A58	5- 58	AQ	N	C	
00PA7KEC24A60	5- 60	AQ	N	C	
00PA7KEC24A62	5- 62	AQ	N	C	
00PA7KEC24A64	5- 64	AQ	N	C	
00PA7KEC24A75	5- 75	AK	N	C	
00PA7KEC24A79	5- 79	AK	N	C	
00PA7KEC24A80	5- 80	AK	N	C	
00PA7KEC24A83	5- 83	AK	N	C	
00PA7KEC24A84	5- 84	AK	N	C	
00PA7KEC24A85	5- 85	AK	N	C	
00PA7KEC24A89	5- 89	AK	N	C	
00PA7KEC24A91	5- 91	AK	N	C	
00PA7KEC24A92	5- 92	AK	N	C	
00PA7KEC24A93	5- 93	AK	N	C	
00PA7KEC24A94	5- 95	AK	N	C	
00PA7KEC24A96	5- 96	AK	N	C	
00PA7KEC24A97	5- 97	AK	N	C	
00PA7KEC24A98	5- 98	AK	N	C	
00PA7KEC24A99	5- 99	AQ	N	C	
00PA7KEC25AA1	5- 100	AK	N	C	
00PA7KEC25AA2	5- 101	AK	N	C	
00PA7KEC25AA3	5- 102	AK	N	C	
00PA7KEC25AA4	5- 103	AK	N	C	
00PA7KEC25AA6	5- 105	AK	N	C	
00PA7KEC25AA7	5- 106	AQ	N	C	
00PA7KEC25AA9	5- 108	AQ	N	C	
00PA7KEC25AB2	5- 110	AK	N	C	
00PA7KEC25AB4	5- 112	AK	N	C	
00PA7KEC25AB5	5- 113	AK	N	C	
00PA7KEC25AB6	5- 114	AK	N	C	
00PA7KEC25AB7	5- 115	AK	N	C	
00PA7KEC25AB8	5- 116	AK	N	C	
00PA7KEC25AB9	5- 117	AK	N	C	
00PA7KEC25AC1	5- 118	AK	N	C	
00PA7KEC25AC2	5- 119	AK	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
00PA7KEC25AC3	5- 120	AK	N	C	
00PA7KEC25AC4	5- 121	AK	N	C	
00PA7KEC25AC5	5- 122	AK	N	C	
00PA7KEC25AC6	5- 123	AK	N	C	
00PA7KEC25AD1	5- 127	AK	N	C	
00PA7KEC25A01	5- 1	AK	N	C	
00PA7KEC25A02	5- 2	AK	N	C	
00PA7KEC25A03	5- 3	AK	N	C	
00PA7KEC25A04	5- 4	AK	N	C	
00PA7KEC25A05	5- 5	AK	N	C	
00PA7KEC25A06	5- 6	AK	N	C	
00PA7KEC25A07	5- 7	AK	N	C	
00PA7KEC25A08	5- 8	AK	N	C	
00PA7KEC25A09	5- 9	AK	N	C	
00PA7KEC25A10	5- 10	AK	N	C	
00PA7KEC25A11	5- 11	AK	N	C	
00PA7KEC25A12	5- 12	AK	N	C	
00PA7KEC25A13	5- 13	AK	N	C	
00PA7KEC25A15	5- 15	AQ	N	C	
00PA7KEC25A16	5- 16	AQ	N	C	
00PA7KEC25A17	5- 17	AK	N	C	
00PA7KEC25A18	5- 18	AK	N	C	
00PA7KEC25A19	5- 19	AK	N	C	
00PA7KEC25A20	5- 20	AK	N	C	
00PA7KEC25A21	5- 21	AK	N	C	
00PA7KEC25A22	5- 22	AK	N	C	
00PA7KEC25A23	5- 23	AK	N	C	
00PA7KEC25A24	5- 24	AK	N	C	
00PA7KEC25A25	5- 25	AK	N	C	
00PA7KEC25A26	5- 26	AK	N	C	
00PA7KEC25A27	5- 27	AK	N	C	
00PA7KEC25A28	5- 28	AK	N	C	
00PA7KEC25A31	5- 31	AK	N	C	
00PA7KEC25A32	5- 32	AK	N	C	
00PA7KEC25A33	5- 33	AK	N	C	
00PA7KEC25A34	5- 34	AK	N	C	
00PA7KEC25A35	5- 35	AK	N	C	
00PA7KEC25A36	5- 36	AK	N	C	
00PA7KEC25A37	5- 37	AK	N	C	
00PA7KEC25A38	5- 38	AK	N	C	
00PA7KEC25A39	5- 39	AK	N	C	
00PA7KEC25A40	5- 40	AK	N	C	
00PA7KEC25A41	5- 41	AK	N	C	
00PA7KEC25A42	5- 42	AK	N	C	
00PA7KEC25A43	5- 43	AQ	N	C	
00PA7KEC25A44	5- 44	AQ	N	C	
00PA7KEC25A45	5- 45	AK	N	C	
00PA7KEC25A46	5- 46	AK	N	C	
00PA7KEC25A47	5- 47	AK	N	C	
00PA7KEC25A48	5- 48	AK	N	C	
00PA7KEC25A49	5- 49	AK	N	C	
00PA7KEC25A50	5- 50	AK	N	C	
00PA7KEC25A51	5- 51	AK	N	C	
00PA7KEC25A52	5- 52	AK	N	C	
00PA7KEC25A53	5- 53	AK	N	C	
00PA7KEC25A54	5- 54	AK	N	C	
00PA7KEC25A55	5- 55	AK	N	C	
00PA7KEC25A57	5- 57	AQ	N	C	
00PA7KEC25A58	5- 58	AQ	N	C	
00PA7KEC25A60	5- 60	AQ	N	C	
00PA7KEC25A62	5- 62	AQ	N	C	
00PA7KEC25A64	5- 64	AQ	N	C	
00PA7KEC25A79	5- 79	AK	N	C	
00PA7KEC25A83	5- 83	AK	N	C	
00PA7KEC25A84	5- 84	AK	N	C	
00PA7KEC25A85	5- 85	AK	N	C	
00PA7KEC25A89	5- 89	AK	N	C	
00PA7KEC25A91	5- 91	AK	N	C	
00PA7KEC25A92	5- 92	AK	N	C	
00PA7KEC25A93	5- 93	AK	N	C	
00PA7KEC25A95	5- 95	AK	N	C	
00PA7KEC25A96	5- 96	AK	N	C	
00PA7KEC25A97	5- 97	AK	N	C	
00PA7KEC25A98	5- 98	AK	N	C	
00PA7KEC25A99	5- 99	AQ	N	C	
00PA7KEC26AA1	5- 100	AK	N	C	
00PA7KEC26AA2	5- 101	AK	N	C	
00PA7KEC26AA3	5- 102	AK	N	C	
00PA7KEC26AA4	5- 103	AK	N	C	
00PA7KEC26AA5	5- 104	AK	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART. RANK
00PA7KEC26AA6	5- 105	AK	N	C
00PA7KEC26AA7	5- 106	AQ	N	C
00PA7KEC26AA9	5- 108	AQ	N	C
00PA7KEC26AB2	5- 110	AK	N	C
00PA7KEC26AB4	5- 112	AK	N	C
00PA7KEC26AB5	5- 113	AK	N	C
00PA7KEC26AB6	5- 114	AK	N	C
00PA7KEC26AB7	5- 115	AK	N	C
00PA7KEC26AB8	5- 116	AK	N	C
00PA7KEC26AB9	5- 117	AK	N	C
00PA7KEC26AC1	5- 118	AK	N	C
00PA7KEC26AC2	5- 119	AK	N	C
00PA7KEC26AC3	5- 120	AK	N	C
00PA7KEC26AC4	5- 121	AK	N	C
00PA7KEC26AC5	5- 122	AK	N	C
00PA7KEC26AC6	5- 123	AK	N	C
00PA7KEC26AD1	5- 127	AK	N	C
00PA7KEC26A01	5- 1	AK	N	C
00PA7KEC26A02	5- 2	AK	N	C
00PA7KEC26A03	5- 3	AK	N	C
00PA7KEC26A04	5- 4	AK	N	C
00PA7KEC26A05	5- 5	AK	N	C
00PA7KEC26A06	5- 6	AK	N	C
00PA7KEC26A07	5- 7	AK	N	C
00PA7KEC26A08	5- 8	AK	N	C
00PA7KEC26A09	5- 9	AK	N	C
00PA7KEC26A10	5- 10	AK	N	C
00PA7KEC26A11	5- 11	AK	N	C
00PA7KEC26A12	5- 12	AK	N	C
00PA7KEC26A13	5- 13	AK	N	C
00PA7KEC26A15	5- 15	AQ	N	C
00PA7KEC26A16	5- 16	AQ	N	C
00PA7KEC26A17	5- 17	AK	N	C
00PA7KEC26A18	5- 18	AK	N	C
00PA7KEC26A19	5- 19	AK	N	C
00PA7KEC26A20	5- 20	AK	N	C
00PA7KEC26A21	5- 21	AK	N	C
00PA7KEC26A22	5- 22	AK	N	C
00PA7KEC26A23	5- 23	AK	N	C
00PA7KEC26A24	5- 24	AK	N	C
00PA7KEC26A25	5- 25	AK	N	C
00PA7KEC26A26	5- 26	AK	N	C
00PA7KEC26A27	5- 27	AK	N	C
00PA7KEC26A28	5- 28	AK	N	C
00PA7KEC26A31	5- 31	AK	N	C
00PA7KEC26A32	5- 32	AK	N	C
00PA7KEC26A33	5- 33	AK	N	C
00PA7KEC26A34	5- 34	AK	N	C
00PA7KEC26A35	5- 35	AK	N	C
00PA7KEC26A36	5- 36	AK	N	C
00PA7KEC26A37	5- 37	AK	N	C
00PA7KEC26A38	5- 38	AK	N	C
00PA7KEC26A39	5- 39	AK	N	C
00PA7KEC26A40	5- 40	AK	N	C
00PA7KEC26A42	5- 42	AK	N	C
00PA7KEC26A43	5- 43	AQ	N	C
00PA7KEC26A44	5- 44	AQ	N	C
00PA7KEC26A45	5- 45	AK	N	C
00PA7KEC26A46	5- 46	AK	N	C
00PA7KEC26A47	5- 47	AK	N	C
00PA7KEC26A48	5- 48	AK	N	C
00PA7KEC26A49	5- 49	AK	N	C
00PA7KEC26A50	5- 50	AK	N	C
00PA7KEC26A51	5- 51	AK	N	C
00PA7KEC26A52	5- 52	AK	N	C
00PA7KEC26A53	5- 53	AK	N	C
00PA7KEC26A54	5- 54	AK	N	C
00PA7KEC26A55	5- 55	AK	N	C
00PA7KEC26A57	5- 57	AQ	N	C
00PA7KEC26A58	5- 58	AQ	N	C
00PA7KEC26A60	5- 60	AQ	N	C
00PA7KEC26A62	5- 62	AQ	N	C
00PA7KEC26A64	5- 64	AQ	N	C
00PA7KEC26A75	5- 75	AK	N	C
00PA7KEC26A76	5- 76	AK	N	C
00PA7KEC26A79	5- 79	AK	N	C
00PA7KEC26A80	5- 80	AK	N	C
00PA7KEC26A81	5- 81	AK	N	C
00PA7KEC26A83	5- 83	AK	N	C
00PA7KEC26A84	5- 84	AK	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART. RANK
00PA7KEC26A85	5- 85	AK	N	C
00PA7KEC26A86	5- 86	AK	N	C
00PA7KEC26A89	5- 89	AK	N	C
00PA7KEC26A91	5- 91	AK	N	C
00PA7KEC26A92	5- 92	AK	N	C
00PA7KEC26A93	5- 93	AK	N	C
00PA7KEC26A95	5- 95	AK	N	C
00PA7KEC26A96	5- 96	AK	N	C
00PA7KEC26A97	5- 97	AK	N	C
00PA7KEC26A98	5- 98	AK	N	C
00PA7KEC26A99	5- 99	AQ	N	C
00PA7KEC28AA1	5- 100	AK	N	C
00PA7KEC28AA2	5- 101	AK	N	C
00PA7KEC28AA3	5- 102	AK	N	C
00PA7KEC28AA4	5- 103	AK	N	C
00PA7KEC28AA5	5- 104	AK	N	C
00PA7KEC28AA6	5- 105	AK	N	C
00PA7KEC28AA7	5- 106	AQ	N	C
00PA7KEC28AA9	5- 108	AQ	N	C
00PA7KEC28AB2	5- 110	AK	N	C
00PA7KEC28AB4	5- 112	AK	N	C
00PA7KEC28AB5	5- 113	AK	N	C
00PA7KEC28AB6	5- 114	AK	N	C
00PA7KEC28AB7	5- 115	AK	N	C
00PA7KEC28AB8	5- 116	AK	N	C
00PA7KEC28AB9	5- 117	AK	N	C
00PA7KEC28AC1	5- 118	AK	N	C
00PA7KEC28AC2	5- 119	AK	N	C
00PA7KEC28AC3	5- 120	AK	N	C
00PA7KEC28AC4	5- 121	AK	N	C
00PA7KEC28AC5	5- 122	AK	N	C
00PA7KEC28AC6	5- 123	AK	N	C
00PA7KEC28AD1	5- 127	AK	N	C
00PA7KEC28A05	5- 5	AK	N	C
00PA7KEC28A06	5- 6	AK	N	C
00PA7KEC28A10	5- 10	AK	N	C
00PA7KEC28A11	5- 11	AK	N	C
00PA7KEC28A15	5- 15	AQ	N	C
00PA7KEC28A16	5- 16	AQ	N	C
00PA7KEC28A17	5- 17	AK	N	C
00PA7KEC28A18	5- 18	AK	N	C
00PA7KEC28A19	5- 19	AK	N	C
00PA7KEC28A20	5- 20	AK	N	C
00PA7KEC28A21	5- 21	AK	N	C
00PA7KEC28A22	5- 22	AK	N	C
00PA7KEC28A23	5- 23	AK	N	C
00PA7KEC28A24	5- 24	AK	N	C
00PA7KEC28A25	5- 25	AK	N	C
00PA7KEC28A26	5- 26	AK	N	C
00PA7KEC28A31	5- 31	AK	N	C
00PA7KEC28A32	5- 32	AK	N	C
00PA7KEC28A33	5- 33	AK	N	C
00PA7KEC28A34	5- 34	AK	N	C
00PA7KEC28A35	5- 35	AK	N	C
00PA7KEC28A36	5- 36	AK	N	C
00PA7KEC28A37	5- 37	AK	N	C
00PA7KEC28A38	5- 38	AK	N	C
00PA7KEC28A39	5- 39	AK	N	C
00PA7KEC28A40	5- 40	AK	N	C
00PA7KEC28A43	5- 43	AQ	N	C
00PA7KEC28A44	5- 44	AQ	N	C
00PA7KEC28A46	5- 46	AK	N	C
00PA7KEC28A47	5- 47	AK	N	C
00PA7KEC28A48	5- 48	AK	N	C
00PA7KEC28A49	5- 49	AK	N	C
00PA7KEC28A50	5- 50	AK	N	C
00PA7KEC28A51	5- 51	AK	N	C
00PA7KEC28A52	5- 52	AK	N	C
00PA7KEC28A53	5- 53	AK	N	C
00PA7KEC28A54	5- 54	AK	N	C
00PA7KEC28A55	5- 55	AK	N	C
00PA7KEC28A57	5- 57	AQ	N	C
00PA7KEC28A58	5- 58	AQ	N	C
00PA7KEC28A60	5- 60	AQ	N	C
00PA7KEC28A62	5- 62	AQ	N	C
00PA7KEC28A64	5- 64	AQ	N	C
00PA7KEC28A75	5- 75	AK	N	C
00PA7KEC28A76	5- 76	AK	N	C
00PA7KEC28A79	5- 79	AK	N	C
00PA7KEC28A80	5- 80	AK	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
00PA7KEC28A81	5- 81	AK	N	C
00PA7KEC28A83	5- 83	AK	N	C
00PA7KEC28A84	5- 84	AK	N	C
00PA7KEC28A85	5- 85	AK	N	C
00PA7KEC28A86	5- 86	AK	N	C
00PA7KEC28A89	5- 89	AK	N	C
00PA7KEC28A91	5- 91	AK	N	C
00PA7KEC28A92	5- 92	AK	N	C
00PA7KEC28A93	5- 93	AK	N	C
00PA7KEC28A95	5- 95	AK	N	C
00PA7KEC28A96	5- 96	AK	N	C
00PA7KEC28A97	5- 97	AK	N	C
00PA7KEC28A98	5- 98	AK	N	C
00PA7KEC28A99	5- 99	AQ	N	C
00PA7KEC32AC2	5- 119	AK	N	C
00PA7KEC32AC3	5- 120	AK	N	C
00PA7KEC32AC4	5- 121	AK	N	C
00PA7KEC32AC5	5- 122	AK	N	C
00PA7KEC32AC6	5- 123	AK	N	C
00PA7KEC32AD1	5- 127	AK	N	C
00PA7KEC32A01	5- 1	AK	N	C
00PA7KEC32A02	5- 2	AK	N	C
00PA7KEC32A03	5- 3	AK	N	C
00PA7KEC32A04	5- 4	AK	N	C
00PA7KEC32A05	5- 5	AK	N	C
00PA7KEC32A06	5- 6	AK	N	C
00PA7KEC32A07	5- 7	AK	N	C
00PA7KEC32A08	5- 8	AK	N	C
00PA7KEC32A09	5- 9	AK	N	C
00PA7KEC32A10	5- 10	AK	N	C
00PA7KEC32A11	5- 11	AK	N	C
00PA7KEC32A12	5- 12	AK	N	C
00PA7KEC32A13	5- 13	AK	N	C
00PA7KEC32A15	5- 15	AQ	N	C
00PA7KEC32A16	5- 16	AQ	N	C
00PA7KEC32A17	5- 17	AK	N	C
00PA7KEC32A18	5- 18	AK	N	C
00PA7KEC32A19	5- 19	AK	N	C
00PA7KEC32A20	5- 20	AK	N	C
00PA7KEC32A21	5- 21	AK	N	C
00PA7KEC32A22	5- 22	AK	N	C
00PA7KEC32A23	5- 23	AK	N	C
00PA7KEC32A24	5- 24	AK	N	C
00PA7KEC32A25	5- 25	AK	N	C
00PA7KEC32A44	5- 44	AQ	N	C
00PA7KEC32A45	5- 45	AK	N	C
00PA7KEC32A46	5- 46	AK	N	C
00PA7KEC32A47	5- 47	AK	N	C
00PA7KEC32A48	5- 48	AK	N	C
00PA7KEC32A49	5- 49	AK	N	C
00PA7KEC32A50	5- 50	AK	N	C
00PA7KEC32A51	5- 51	AK	N	C
00PA7KEC32A52	5- 52	AK	N	C
00PA7KEC32A53	5- 53	AK	N	C
00PA7KEC32A54	5- 54	AK	N	C
00PA7KEC32A55	5- 55	AK	N	C
00PA7KEC32A57	5- 57	AQ	N	C
00PA7KEC32A58	5- 58	AQ	N	C
00PA7KEC32A60	5- 60	AQ	N	C
00PA7KEC32A62	5- 62	AQ	N	C
00PA7KEC32A64	5- 64	AQ	N	C
00PA7KEC32A75	5- 75	AK	N	C
00PA7KEC32A79	5- 79	AK	N	C
00PA7KEC32A80	5- 80	AK	N	C
00PA7KEC32A83	5- 83	AK	N	C
00PA7KEC32A84	5- 84	AK	N	C
00PA7KEC32A85	5- 85	AK	N	C
00PA7KEC32A89	5- 89	AK	N	C
00PA7KEC33AA1	5- 100	AK	N	C
00PA7KEC33AA2	5- 101	AK	N	C
00PA7KEC33AA3	5- 102	AK	N	C
00PA7KEC33AA4	5- 103	AK	N	C
00PA7KEC33AA5	5- 104	AK	N	C
00PA7KEC33AA6	5- 105	AK	N	C
00PA7KEC33AA7	5- 106	AQ	N	C
00PA7KEC33AA9	5- 108	AQ	N	C
00PA7KEC33AB2	5- 110	AK	N	C
00PA7KEC33AB4	5- 112	AK	N	C
00PA7KEC33AB5	5- 113	AK	N	C
00PA7KEC33AB6	5- 114	AK	N	C

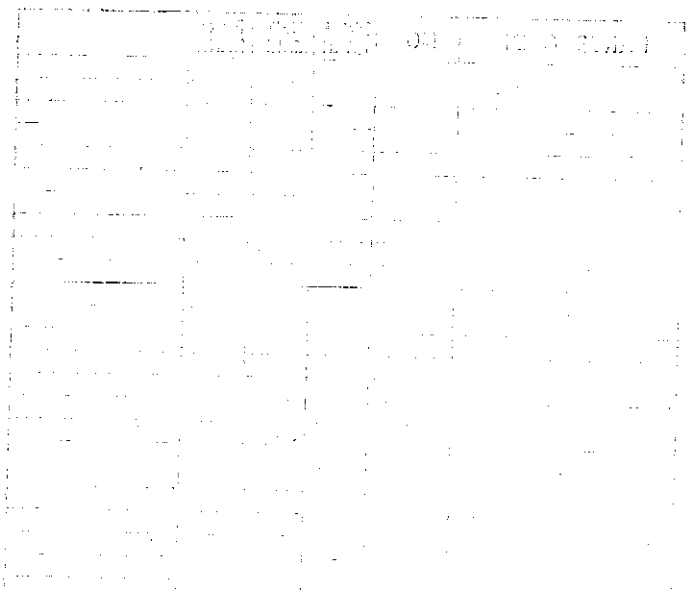
PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
00PA7KEC33AB7	5- 115	AK	N	C
00PA7KEC33AB8	5- 116	AK	N	C
00PA7KEC33AB9	5- 117	AK	N	C
00PA7KEC33AC1	5- 118	AK	N	C
00PA7KEC33AC2	5- 119	AK	N	C
00PA7KEC33AC3	5- 120	AK	N	C
00PA7KEC33AC4	5- 121	AK	N	C
00PA7KEC33AC5	5- 122	AK	N	C
00PA7KEC33AC6	5- 123	AK	N	C
00PA7KEC33AD1	5- 127	AK	N	C
00PA7KEC33A01	5- 1	AK	N	C
00PA7KEC33A02	5- 2	AK	N	C
00PA7KEC33A03	5- 3	AK	N	C
00PA7KEC33A04	5- 4	AK	N	C
00PA7KEC33A05	5- 5	AK	N	C
00PA7KEC33A06	5- 6	AK	N	C
00PA7KEC33A07	5- 7	AK	N	C
00PA7KEC33A08	5- 8	AK	N	C
00PA7KEC33A09	5- 9	AK	N	C
00PA7KEC33A10	5- 10	AK	N	C
00PA7KEC33A11	5- 11	AK	N	C
00PA7KEC33A12	5- 12	AK	N	C
00PA7KEC33A13	5- 13	AK	N	C
00PA7KEC33A15	5- 15	AQ	N	C
00PA7KEC33A16	5- 16	AQ	N	C
00PA7KEC33A17	5- 17	AK	N	C
00PA7KEC33A18	5- 18	AK	N	C
00PA7KEC33A19	5- 19	AK	N	C
00PA7KEC33A20	5- 20	AK	N	C
00PA7KEC33A21	5- 21	AK	N	C
00PA7KEC33A22	5- 22	AK	N	C
00PA7KEC33A23	5- 23	AK	N	C
00PA7KEC33A24	5- 24	AK	N	C
00PA7KEC33A25	5- 25	AK	N	C
00PA7KEC33A26	5- 26	AK	N	C
00PA7KEC33A27	5- 27	AK	N	C
00PA7KEC33A28	5- 28	AK	N	C
00PA7KEC33A29	5- 29	AK	N	C
00PA7KEC33A31	5- 31	AK	N	C
00PA7KEC33A32	5- 32	AK	N	C
00PA7KEC33A33	5- 33	AK	N	C
00PA7KEC33A34	5- 34	AK	N	C
00PA7KEC33A35	5- 35	AK	N	C
00PA7KEC33A36	5- 36	AK	N	C
00PA7KEC33A37	5- 37	AK	N	C
00PA7KEC33A38	5- 38	AK	N	C
00PA7KEC33A39	5- 39	AK	N	C
00PA7KEC33A40	5- 40	AK	N	C
00PA7KEC33A41	5- 41	AK	N	C
00PA7KEC33A43	5- 43	AQ	N	C
00PA7KEC33A44	5- 44	AQ	N	C
00PA7KEC33A46	5- 46	AK	N	C
00PA7KEC33A47	5- 47	AK	N	C
00PA7KEC33A48	5- 48	AK	N	C
00PA7KEC33A49	5- 49	AK	N	C
00PA7KEC33A50	5- 50	AK	N	C
00PA7KEC33A51	5- 51	AK	N	C
00PA7KEC33A52	5- 52	AK	N	C
00PA7KEC33A53	5- 53	AK	N	C
00PA7KEC33A54	5- 54	AK	N	C
00PA7KEC33A55	5- 55	AK	N	C
00PA7KEC33A57	5- 57	AQ	N	C
00PA7KEC33A58	5- 58	AQ	N	C
00PA7KEC33A60	5- 60	AQ	N	C
00PA7KEC33A62	5- 62	AQ	N	C
00PA7KEC33A64	5- 64	AQ	N	C
00PA7KEC33A75	5- 75	AK	N	C
00PA7KEC33A76	5- 76	AK	N	C
00PA7KEC33A79	5- 79	AK	N	C
00PA7KEC33A80	5- 80	AK	N	C
00PA7KEC33A81	5- 81	AK	N	C
00PA7KEC33A83	5- 83	AK	N	C
00PA7KEC33A84	5- 84	AK	N	C
00PA7KEC33A85	5- 85	AK	N	C
00PA7KEC33A86	5- 86	AK	N	C
00PA7KEC33A89	5- 89	AK	N	C
00PA7KEC33A91	5- 91	AK	N	C
00PA7KEC33A92	5- 92	AK	N	C
00PA7KEC33A93	5- 93	AK	N	C
00PA7KEC33A95	5- 95	AK	N	C

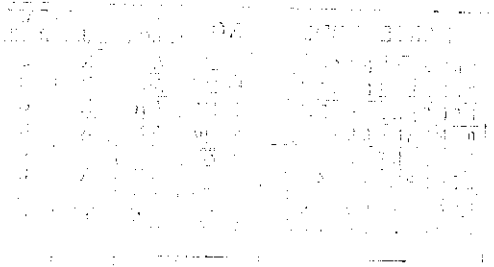
PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
00PA7KEC33A96	5- 96	AK	N	C
00PA7KEC33A97	5- 97	AK	N	C
00PA7KEC33A98	5- 98	AK	N	C
00PA7KEC33A99	5- 99	AQ	N	C
00PA7KE032AA1	5- 100	AK	N	C
00PA7KE032AA2	5- 101	AK	N	C
00PA7KE032AA3	5- 102	AK	N	C
00PA7KE032AA4	5- 103	AK	N	C
00PA7KE032AA5	5- 104	AK	N	C
00PA7KE032AA6	5- 105	AK	N	C
00PA7KE032AA7	5- 106	AQ	N	C
00PA7KE032AA9	5- 108	AQ	N	C
00PA7KE032AB2	5- 110	AK	N	C
00PA7KE032AB4	5- 112	AK	N	C
00PA7KE032AB5	5- 113	AK	N	C
00PA7KE032AB6	5- 114	AK	N	C
00PA7KE032AB7	5- 115	AK	N	C
00PA7KE032AB8	5- 116	AK	N	C
00PA7KE032AB9	5- 117	AK	N	C
00PA7KE032AC1	5- 118	AK	N	C
00PA7KE032A26	5- 26	AK	N	C
00PA7KE032A31	5- 31	AK	N	C
00PA7KE032A32	5- 32	AK	N	C
00PA7KE032A33	5- 33	AK	N	C
00PA7KE032A34	5- 34	AK	N	C
00PA7KE032A35	5- 35	AK	N	C
00PA7KE032A36	5- 36	AK	N	C
00PA7KE032A37	5- 37	AK	N	C
00PA7KE032A38	5- 38	AK	N	C
00PA7KE032A39	5- 39	AK	N	C
00PA7KE032A42	5- 42	AK	N	C
00PA7KE032A43	5- 43	AQ	N	C
00PA7KE032A91	5- 91	AK	N	C
00PA7KE032A92	5- 92	AK	N	C
00PA7KE032A93	5- 93	AK	N	C
00PA7KE032A95	5- 95	AK	N	C
00PA7KE032A96	5- 96	AK	N	C
00PA7KE032A97	5- 97	AK	N	C
00PA7KE032A98	5- 98	AK	N	C
00PA7KE032A99	5- 99	AQ	N	C
00PC5KE203AC7	5- 124	AQ	N	C
00PC5KE203AC9	5- 126	AQ	N	C
00PC5KE206AC7	5- 124	AQ	N	C
00PC5KE206AC9	5- 126	AQ	N	C
00PC5KE207AC7	5- 124	AQ	N	C
00PC5KE207AC9	5- 126	AQ	N	C
00PC5KE207A03	5- 3	AQ	N	C
00PC5KE207A04	5- 4	AQ	N	C
00PC5KE207A05	5- 5	AQ	N	C
00PC5KE207A06	5- 6	AQ	N	C
00PC5KE207A07	5- 7	AQ	N	C
00PC5KE207A08	5- 8	AQ	N	C
00PC5KE207A09	5- 9	AQ	N	C
00PC5KE207A10	5- 10	AQ	N	C
00PC5KE207A11	5- 11	AQ	N	C
00PC5KE207A12	5- 12	AQ	N	C
00PC5KE207A13	5- 13	AQ	N	C
00PC5KE208AC7	5- 124	AQ	N	C
00PC5KE208AC9	5- 126	AQ	N	C
00PC5KE208AD3	5- 45	AQ	N	C
00PC5KE208AD8	5- 13	AQ	N	C
00PC5KE208A03	5- 3	AQ	N	C
00PC5KE208A04	5- 4	AQ	N	C
00PC5KE208A08	5- 8	AQ	N	C
00PC5KE208A09	5- 9	AQ	N	C
00PC5KE208A10	5- 10	AQ	N	C
00PC5KE208A11	5- 11	AQ	N	C
00PC5KE208A12	5- 12	AQ	N	C
00PC5KE208A28	5- 28	AQ	N	C
00PC5KE208A45	5- 45	AQ	N	C
00PC5KE209BC7	5- 124	AQ	N	C
00PC5KE209BC9	5- 126	AQ	N	C
00PC5KE209B02	5- 2	AQ	N	C
00PC5KE209B03	5- 3	AQ	N	C
00PC5KE209B04	5- 4	AQ	N	C
00PC5KE209B07	5- 7	AQ	N	C
00PC5KE209B08	5- 8	AQ	N	C
00PC5KE209B09	5- 9	AQ	N	C
00PC5KE209B12	5- 12	AQ	N	C
00PC5KE209B13	5- 13	AQ	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
00PC5KE209B27	5- 27	AQ	N	C
00PC5KE209B28	5- 28	AQ	N	C
00PC5KE209B41	5- 41	AQ	N	C
00PC5KE209B45	5- 45	AQ	N	C
00PC5KE21DAC7	5- 124	AQ	N	C
00PC5KE21DAC9	5- 126	AQ	N	C
00PC5KE210A27	5- 27	AQ	N	C
00PC5KE213AC7	5- 124	AQ	N	C
00PC5KE213AC9	5- 126	AQ	N	C
00PD2KE037AC8	5- 125	AQ	N	C
00PD2KE037A30	5- 30	AT	N	C
00PD2KE037A90	5- 90	AQ	N	C
00PD2KE038AA5	5- 104	AQ	N	C
00PD2KE038AC8	5- 125	AQ	N	C
00PD2KE038A30	5- 30	AT	N	C
00PD2KE038A75	5- 75	AQ	N	C
00PD2KE038A76	5- 76	AQ	N	C
00PD2KE038A80	5- 80	AQ	N	C
00PD2KE038A81	5- 81	AQ	N	C
00PD2KE038A86	5- 86	AQ	N	C
00PD2KE038A90	5- 90	AQ	N	C
00PD2KE039AB2	5- 110	AQ	N	C
00PD2KE039AC8	5- 125	AQ	N	C
00PD2KE039A28	5- 28	AT	N	C
00PD2KE039A30	5- 30	AT	N	C
00PD2KE039A76	5- 76	AQ	N	C
00PD2KE039A81	5- 81	AQ	N	C
00PD2KE039A86	5- 86	AQ	N	C
00PD2KE039A90	5- 90	AQ	N	C
00PD2KE041AC8	5- 125	AQ	N	C
00PD2KE041AD2	5- 104	AQ	N	C
00PD2KE041AD7	5- 1	AQ	N	C
00PD2KE041AE1	5- 1	AQ	N	C
00PD2KE041AE2	5- 13	AT	N	C
00PD2KE041A01	5- 1	AQ	N	C
00PD2KE041A05	5- 5	AQ	N	C
00PD2KE041A30	5- 30	AT	N	C
00PD2KE041A42	5- 42	AQ	N	C
00PD2KE041A90	5- 90	AQ	N	C
00PD2KE042AC8	5- 125	AQ	N	C
00PD2KE042A01	5- 1	AQ	N	C
00PD2KE042A30	5- 30	AT	N	C
00PD2KE042A42	5- 42	AT	N	C
00PD2KE042A90	5- 90	AQ	N	C
00PD2KE043AC8	5- 125	AQ	N	C
00PD2KE043A30	5- 30	AT	N	C
00PD2KE043A41	5- 41	AQ	N	C
00PD2KE043A90	5- 90	AQ	N	C
00PD2KE044AC8	5- 125	AQ	N	C
00PD2KE044A28	5- 28	AT	N	C
00PD2KE044A30	5- 30	AT	N	C
00PD2KE044A40	5- 40	AT	N	C
00PD2KE044A41	5- 41	AT	N	C
00PD2KE044A76	5- 76	AQ	N	C
00PD2KE044A81	5- 81	AQ	N	C
00PD2KE044A86	5- 86	AQ	N	C
00PD2KE044A90	5- 90	AQ	N	C
00PD2KE045AC8	5- 125	AQ	N	C
00PD2KE045A30	5- 30	AT	N	C
00PD2KE045A90	5- 90	AQ	N	C
00PSKEUAA000A	5- 202	AG		B
00PSKFLAC000A	5- 203	AG		B
00PSKFLAF000A	5- 209	AH		B
00PSKFLFH000A	5- 210	AK		B
00P13KF015A//	5- 214	AB		C
00P16KF005B//	5- 205	AG		C
00P16KF006A//	5- 220	AG		C
00P19KE007B//	5- 206	AG	N	C
00P19KE009B//	5- 211	AG	N	C
00P19KF005C//	5- 204	AG		C
00P19KF009B//	5- 211	AG	N	C
00P21KE021A//	5- 224	AH		C
00P21KE022A//	5- 225	AH		C
00P21KE023A//	5- 222	AN		C
00P21KE024A//	5- 223	AN		C
00P21KF008A//	5- 216	AD		C
00P21KF009A//	5- 218	AF		C
00P21KF011A//	5- 215	AK		C
00P21KF016A//	5- 217	AE		C
00P21KF020A//	5- 219	AG		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
00P23KE044A//	5- 213	AE	N	C
00P25KE056A//	5- 207	AX	N	C
00P25KE057B//	5- 208	AH	N	C
00P25KE058A//	5- 207	AX	N	C
00P27KF021A//	5- 221	AC		C
00P29KE184A//	5- 212	AV	N	C
00P80L7C52000	5- 61	AQ		C
00P80L7E43000	5- 61	AQ	N	C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK





SHARP

SHARP CORPORATION
Information Systems Group
Quality & Reliability Control Center
Yamatokoriyama, Nara 639-11, Japan
1987 June Printed in Japan Ⓢ