SAMSUNG SEMICONDUCTOR, INC.

JANUARY 1985

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KM4128 946766

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131,072-BIT NMOS DYNAMIC RAM 6711

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GENERAL DESCRIPTION

The KM4128 is a fully decoded NMOS dynamic random access memory organized as 131,072 one-bit words. It consists of two KM4164A 64Kx1 DRAMS interconnected in a stacked DIP arrangement.

Two $\overline{RAS}$ inputs are provided for separetely selecting either the top or bottom 64K section of the KM4128A. The other pins are connected in parallel.

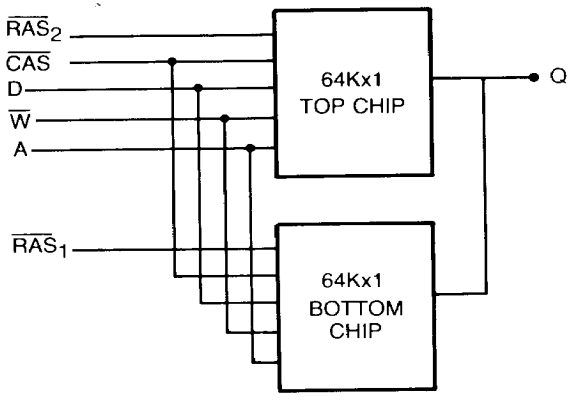
The design is optimized for high speed, high performance applications such as computer memory, buffer memory, and peripheral storage where low power dissipation and compact board layout are required.

Multiplexed row and column address inputs permit the KM4128 to be housed in a plastic 16-pin stacked DIP. The KM4128 is fabricated using Tristar's silicon gate NMOS Double-layer Polysilicon process.

FEATURES

- 128Kx1 in 16-pin stacked DIP
- Row Access Time/Cycle Time
  - KM4128-15 150/260ns
  - KM4128-20 200/345ns
- Low power: 44mW standby, 220mW active
- Common I/O using Early Write
- Dout held indefinitely by CAS
- Schmitt triggers on activating inputs
- Single +5V ± 10% power supply
- 4msec/256 cycle refresh
- Two $\overline{RAS}$ inputs for selecting top or bottom 64K memory chips

FUNCTIONAL BLOCK DIAGRAM



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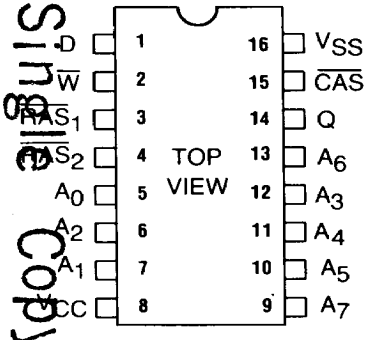
PIN CONFIGURATION



RAS1 Bottom Chip
RAS2 Top Chip

NOTE: IEEE STD. 662-1980 symbols are used in this data sheet. D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

ABSOLUTE MAXIMUM RATINGS (See Note)

RATING		SYMBOL	VALUE	UNITS
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	− 1 to + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	− 1 to + 7.0	V
Storage Temperature	Plastic	T_{stg}	− 40 to + 125	°C
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

PARAMETER	SYMBOL	VALUE			UNIT	OPERATING TEMPERATURE
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to + 70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all Inputs	V_{IH}	2.4	—	V_{CC+1}	V	
Input Low Voltage, all Inputs	V_{IL}	− 1.0	—	0.8	V	

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

PARAMETER	SYMBOL	Min	Max	UNITS
OPERATING CURRENT* Average Power Supply Current (RAS, CAS cycling; t_{RC} = min.; see notes 10, 11)	I_{CC1}	—	40	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}/\overline{CAS}$ = V_{IH}; see note 10)	I_{CC2}	—	8	mA
REFRESH CURRENT* Average Power Supply Current (CAS = V_{IH}; $\overline{RAS}1$ & $\overline{RAS}2$ Cycling t_{RC} = min ;see note 11)	I_{CC3}	—	60	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min ; see notes 10, 11)	I_{CC4}	—	35	mA
INPUT LEAKAGE CURRENT any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V	I_{IL}	− 20	20	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OL}	− 20	20	μA
OUTPUT LEVEL Output High Voltage (I_{OH} = 5.0 mA)	V_{OH}	2.4	—	V
OUTPUT LEVEL Output Low Voltage (I_{OL} = mA)	V_{OL}	—	0.4	V

CAPACITANCE (T_A = 25 °C)

PARAMETER	SYMBOL	VALUE			UNITS
		Min	Typ	Max	
Input Capacitance A_0 — A_7, D	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{CAS}$, $\overline{W}$	C_{IN2}	—	—	5	pF
Input Capacitance $\overline{RAS}1$, $\overline{RAS}2$	C_{IN3}	—	—	4	pF
Output Capacitance Q	C_{OUT}	—	—	14	pF

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted. See notes 1, 2, & 3)

PARAMETER	NOTES	SYMBOL		KM4128-15		KM4128-20		UNITS
		ALTERNATE	*STANDARD	Min	Max	Min	Max	
Time between Refresh		t_{REF}	TRVRV		4		4	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	260		345		ns
Read-Write/Read-Modify-Write Cycle Time		t_{RWC}	TRELREL	295		370		ns
Page Mode Cycle Time		t_{PC}	TCELCEL	175		225		ns
Access Time from $\overline{RAS}$	(4), (6)	t_{RAC}	TRELQV		150		200	ns
Access Time from $\overline{CAS}$	(5), (6)	t_{CAC}	TCELQV		85		120	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	35	0	40	ns
Transition Time		t_T	TT	3	100	3	100	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	100		135		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	150	10,000	200	10,000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	75		100		ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	TCEHCEL	35		40		ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)	(9)	t_{CPN}	TCEHCEL	30		35		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	85	∞	120	∞	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	150		200		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	(4)	t_{RCD}	TRELCEL	25	65	30	80	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	TCEHREL	0		0		ns
Row Address Set Up Time		t_{ASR}	TAVREL	0		0		ns
Row Address Hold Time		t_{RAH}	TRELAX	20		25		ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0		0		ns
Column Address Hold Time		t_{CAH}	TCELAX	40		50		ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	(8)	t_{RCH}	TCEHWX	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	(8)	t_{RRH}	TREHWX	0		0		ns
Write Command Set Up Time	(7)	t_{WCS}	TWLCEL	0		0		ns
Write Command Hold Time		t_{WCH}	TCELWH	50		60		ns
Write Command Pulse Width		t_{WP}	TWLWH	45		55		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	45		55		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	45		55		ns
Data In Set Up Time		t_{DS}	TDVCEL	0		0		ns
Data In Hold Time		t_{DH}	TCELDX	45		55		ns
$\overline{CAS}$ to $\overline{W}$ Delay	(7)	t_{CWD}	TCELWL	75		100		ns
$\overline{RAS}$ to $\overline{W}$ Delay	(7)	t_{RWD}	TRELWL	140		180		ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	TRELAX	100		130		ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	TRELWH	110		140		ns
Data-In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	TRELDX	105		135		ns

See notes on following page.

*These symbols are described in IEEE Std. 662-1980: IEEE Standard Terminology for Semiconductor memory.

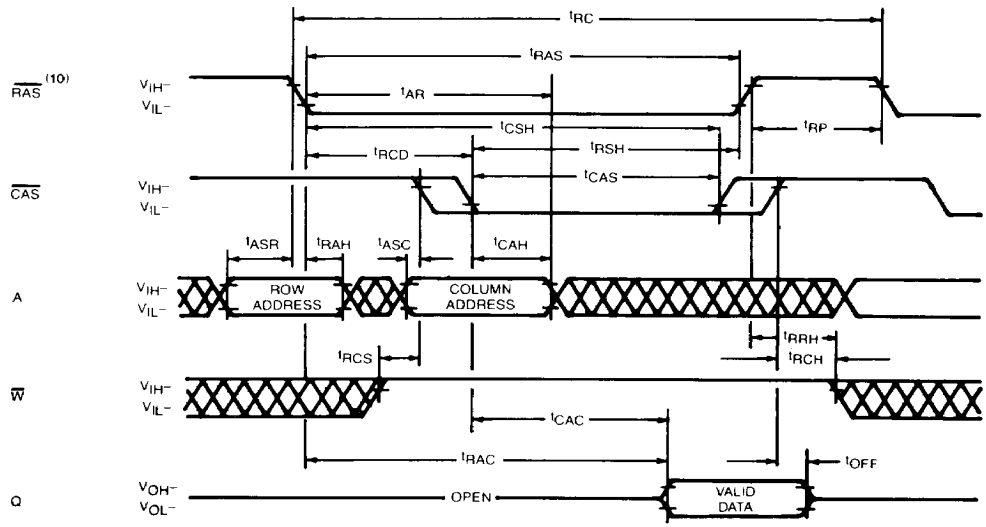
NOTES

1. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. This requirement applies to $\overline{RAS1}$ and $\overline{RAS2}$ separately.
2. AC characteristics assume T_T = 5ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min.) V_{IL} (max.).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} \geq t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle, and the data out pin will remain open circuit (high impedance) throughout the entire cycle.

   If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, D_{out} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer $\overline{CAS}$ must be pulsed high for t_{CPN}. Note 8 applies to determine valid data out.
10. $\overline{RAS}$ indicates either $\overline{RAS1}$ or $\overline{RAS2}$ but not both simultaneously.
11. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

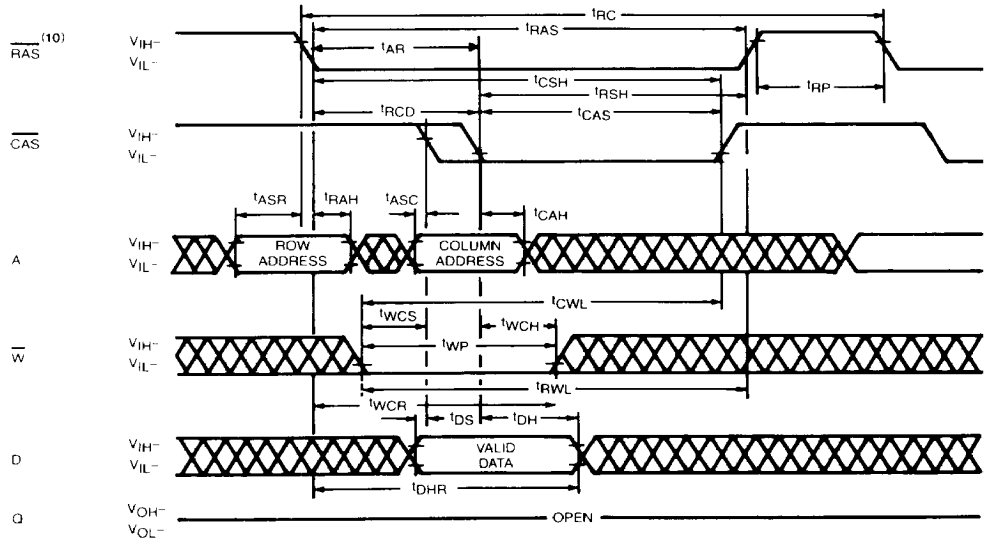
TIMING DIAGRAMS

READ CYCLE

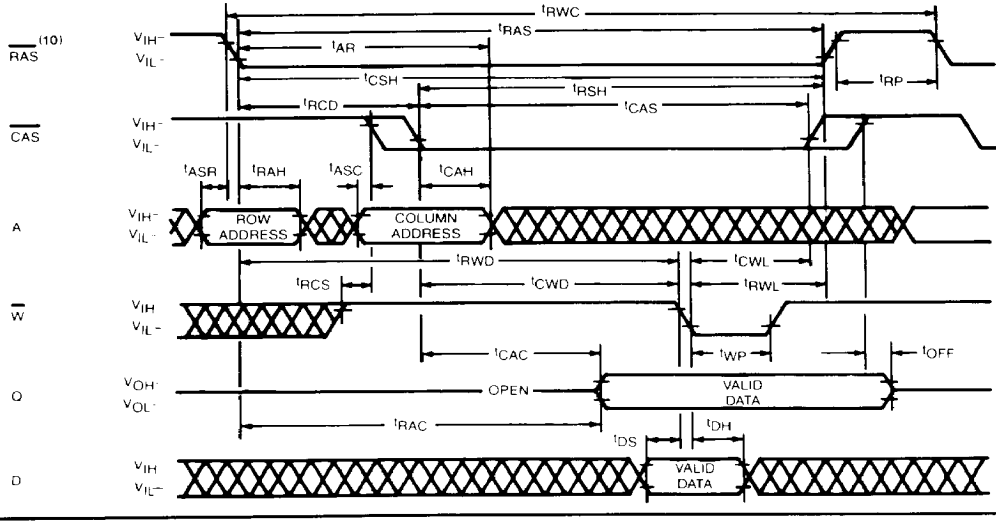


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



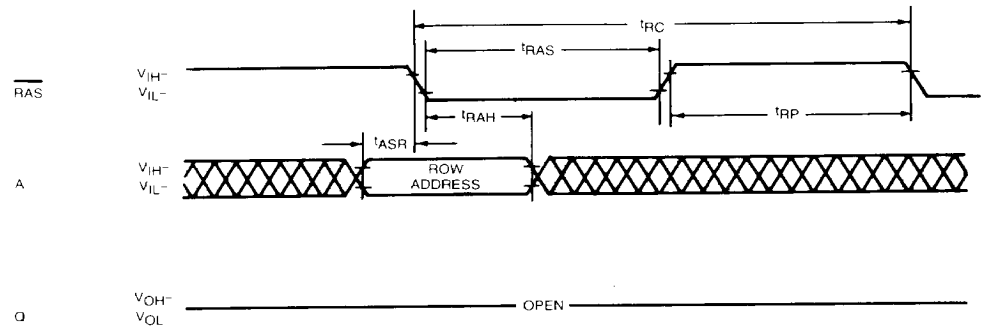
READ-WRITE/READ-MODIFY-WRITE CYCLE



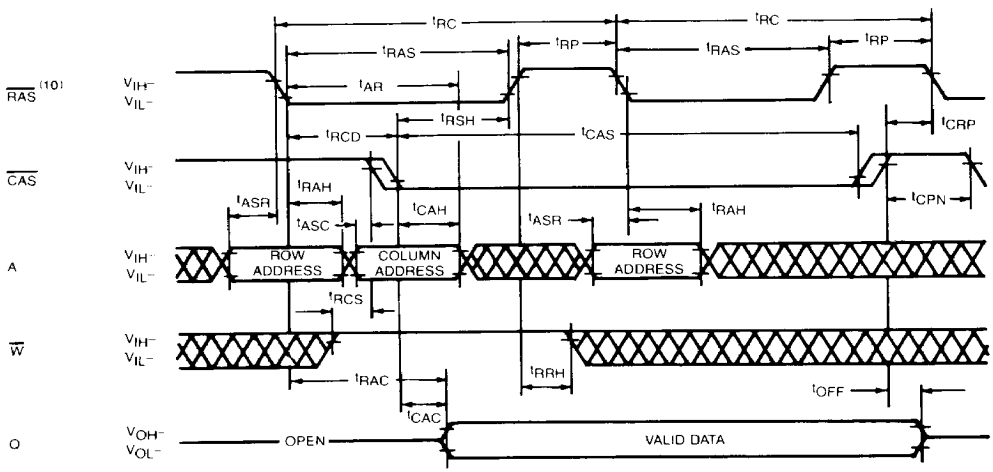
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = Don't Care

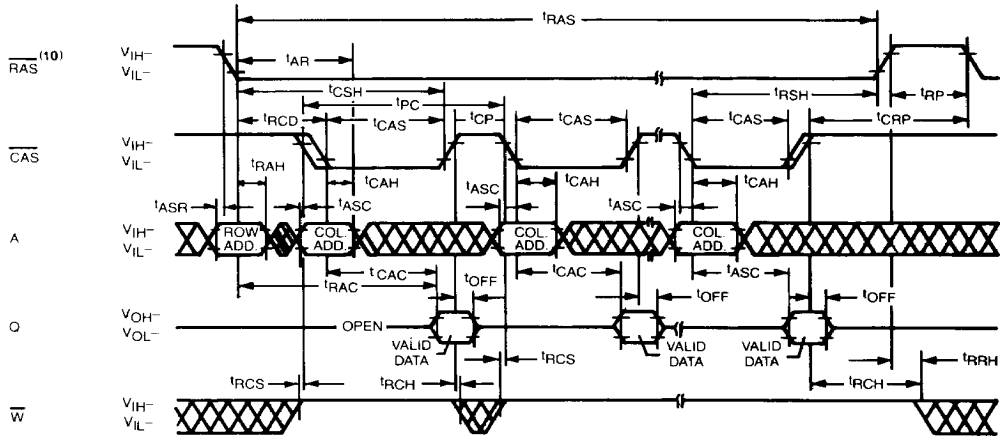


HIDDEN $\overline{RAS}$-ONLY REFRESH CYCLE

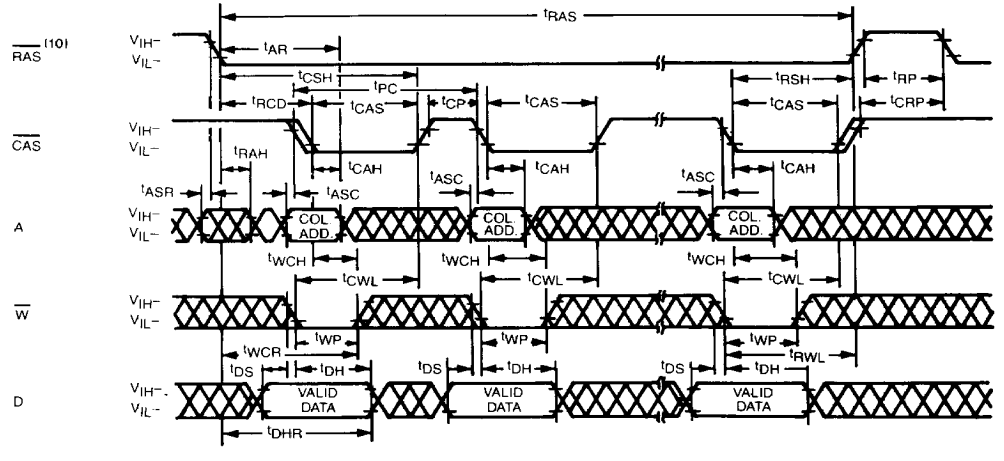


TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE

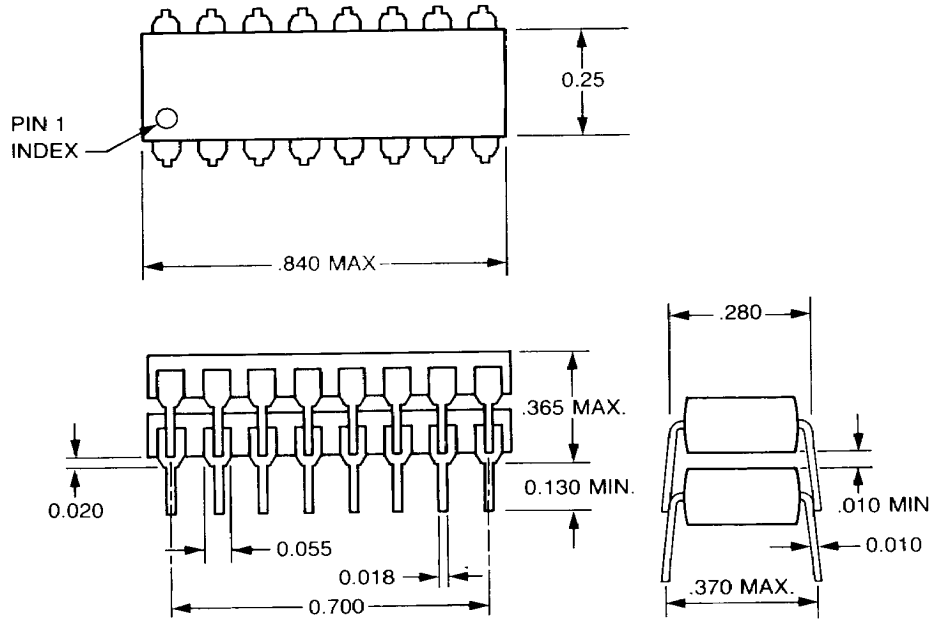


PAGE MODE WRITE CYCLE



PACKAGE DIMENSIONS

16-LEAD PLASTIC STACKED DIP



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