F4116
16,384 x 1 Dynamic RAM

MOS Memory Products

Description

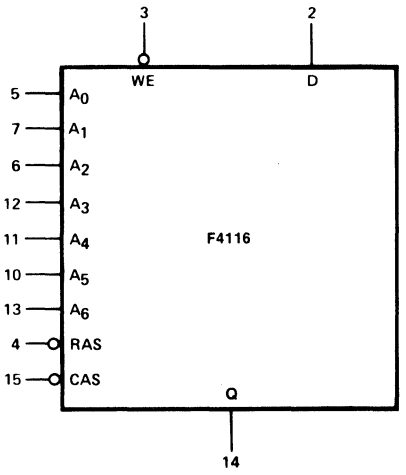
The F4116 is a 16,384-bit MOS dynamic Random Access Memory (RAM) configured as 16,384 one-bit words. It is manufactured using Fairchild's n-channel silicon gate, double-poly Isoplanar process. The use of the single-transistor memory cell along with address multiplexing techniques permits the packaging of the F4116 in a standard 16-pin dual in-line package. This package allows construction of highly dense memory systems utilizing widely available automated testing and insertion equipment.

- **INDUSTRY STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **LOW CAPACITANCE, TTL-COMPATIBLE INPUTS (INCLUDING CLOCKS)**
- **ON-CHIP ADDRESS AND INPUT DATA LATCHES**
- **3-STATE TTL-COMPATIBLE OUTPUT WITH DATA VALID TIME CONTROLLED BY $\overline{CAS}$**
- **COMMON I/O CAPABILITY**
- **TWO DIMENSIONAL SELECTION BY DECODING BOTH $\overline{RAS}$ AND $\overline{CAS}$**
- **STANDARD 10% SUPPLIES (+12 V, +5 V, AND −5 V)**
- **FLEXIBLE TIMING WITH PAGE-MODE AND EXTENDED PAGE BOUNDARIES**
- **128-CYCLE $\overline{RAS}$-ONLY REFRESH**

Pin Names

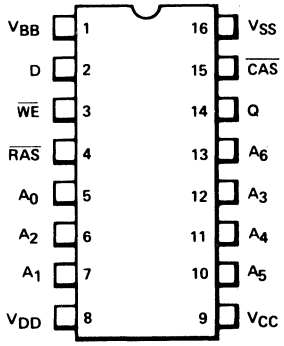
A_0-A_6	Address Inputs
D	Data Input
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{RAS}$	Row Address Strobe Input (Active LOW Clock)
$\overline{CAS}$	Column Address Strobe Input (Active LOW Clock)
Q	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	0 V Power Supply
V_{BB}	−5 V Power Supply
V_{DD}	+12 V Power Supply

Logic Symbol



V_{SS} = Pin 16
V_{CC} = Pin 9
V_{DD} = Pin 8
V_{BB} = Pin 1

Connection Diagram 16-Pin DIP



(Top View)

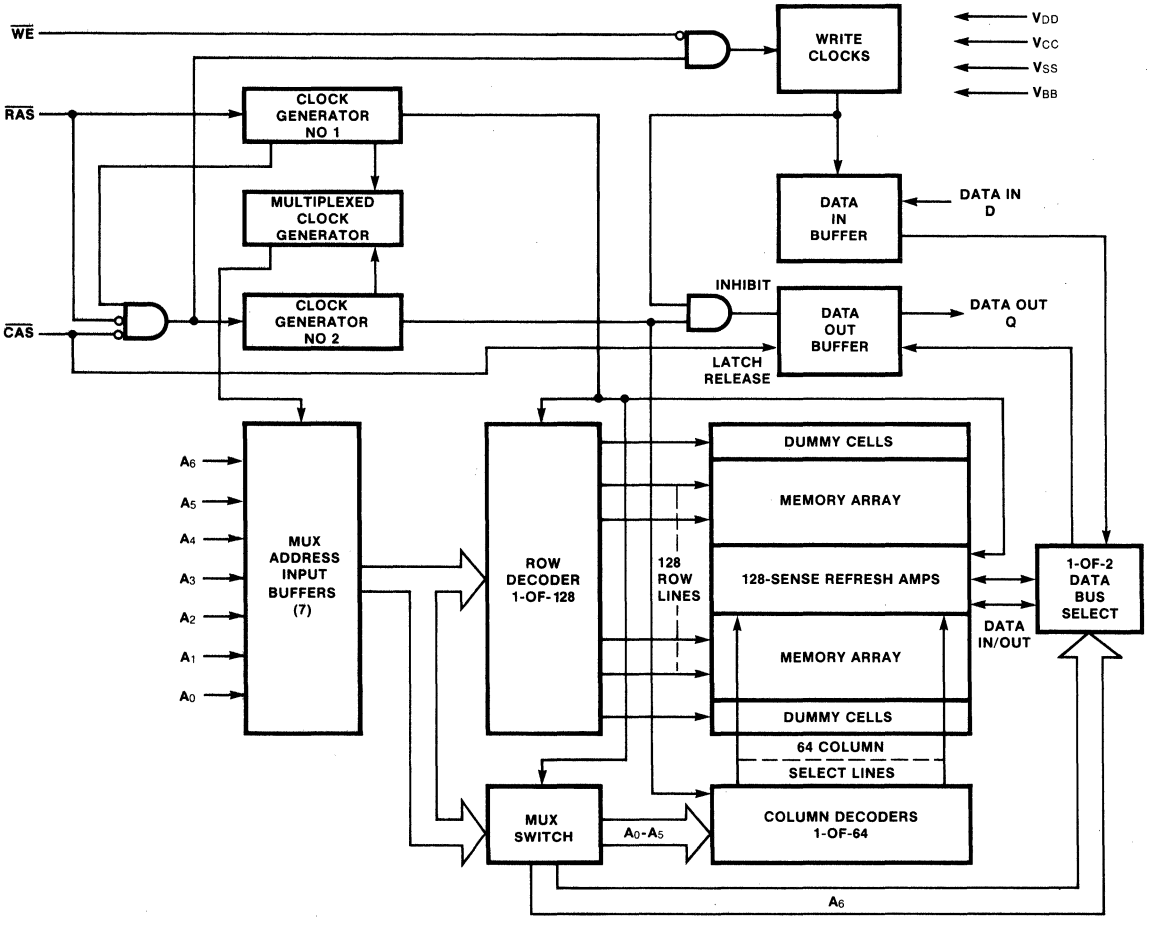
Package	Outline	Order Code
Ceramic DIP	2C	D
Plastic DIP	UB	P

Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$ V)	−0.5 V to +20 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	−65°C to +150°C
Power Dissipation	1 W
Voltage on V_{DD}, V_{CC} Supplies Relative to V_{SS}	−1.0 V to +15 V
Short-circuit Output Current	50 mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Functional Description

Addressing

The 14 address bits required to decode one-of-16,384 cell locations in the F4116 are entered using a 2-phase multiplexing operation; first, the 7-bit row address is entered followed by the 7-bit column address. First the 7-bit row address is applied to the seven address inputs of the F4116 and latched into the chip by Row Address Strobe ($\overline{RAS}$) which is the first of two externally applied TTL-level clocks. The second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the seven column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, trigger on-chip clock generators which control the internal sequencing of events on the chip. Advanced techniques used in handling the row and column address information allow the address multiplexing operation to be performed without lengthening the critical timing path governing the access time. The activation of $\overline{CAS}$ strobes the column address latch but this event as well as other internal events governed by the $\overline{CAS}$ clock generator may be inhibited until certain prerequisite events controlled by the $\overline{RAS}$ clock generator have occurred.

More specifically, a window of time exists, extending from $t_{RCD(min)}$ to $t_{RCD(max)}$ during which $\overline{CAS}$ may become active without impacting the access time. Stated another way, as long as $\overline{CAS}$ occurs during this window, the access time will be specified by t_{RAC}. If $\overline{CAS}$ occurs a certain delay after this window of time, the $\overline{RAS}$ clock generator no longer inhibits the $\overline{CAS}$ clock generator and the magnitude of this delay will add directly to the overall access time. This lengthened access time is now referenced to $\overline{CAS}$ rather than $\overline{RAS}$ and is lengthened by the amount of time that t_{RCD} exceeds the $t_{RCD(max)}$ limit. This gated-$\overline{CAS}$ feature allows greater flexibility since the $\overline{CAS}$ clock may be externally activated as soon as the hold time for the row address has been met and the address inputs have been changed from row address to column address information.

Page Mode Operation

The page-mode feature of the F4116 allows successive memory cycles accessing the same row in the memory matrix to be concatenated together in such a way that the common row address need be supplied only once. The result is faster access times with no corresponding increase in power. The page-mode option may be used in conjunction with any of the defined memory operations, and is accomplished by supplying the row address to the chip and holding $\overline{RAS}$ LOW throughout all subsequent memory cycles for which the row address is common.

Since $\overline{RAS}$ makes its initial negative transition only once, no additional dynamic power is dissipated due to $\overline{RAS}$ on any subsequent cycles performed within that row. The access and cycle times are also shortened since the time required to supply a row address is eliminated.

Data Input

In a write operation, the data to be input into memory is strobed into an on-chip register during $\overline{RAS}$ by a combination of $\overline{CAS}$ and Write Enable ($\overline{WE}$). The strobe is formed by the last of these two signals to make its negative transition. This presents several possibilities in how a write cycle may be performed. In an "early-write" cycle ($\overline{WE}$ active LOW before $\overline{CAS}$ goes LOW), Data In (D) is strobed by $\overline{CAS}$ and thus the set-up and hold times are referenced to this signal edge. If D is not yet valid at the time $\overline{CAS}$ becomes active (or if the cycle is a read-write or read-modify-write) then $\overline{WE}$ must be delayed. In this delayed-write mode, the D set-up and hold times are referenced to $\overline{WE}$ rather than $\overline{CAS}$. (See the timing diagrams.)

Data Output

The Data Out (Q) latch and buffer unconditionally assume the high-impedance state whenever $\overline{CAS}$ is HIGH, i.e., inactive. If the cycle being performed is a read, read-modify-write, or a delayed write cycle, then the Q latch and buffer will remain high impedance until the access time, after which Q will assume the value of the data read from the selected cell. This output data is of the same polarity (not inverted) as the input data and will remain valid as long as $\overline{CAS}$ is kept active, i.e., LOW. However, if the cycle is an "early-write" cycle or if the chip fails to receive both $\overline{RAS}$ and $\overline{CAS}$, then Q will remain high impedance throughout the cycle. This feature allows systems which write exclusively in the early-write mode to connect D and Q directly together.

Another advantage of this "unlatched output" feature is that OR-tied outputs in a memory matrix require no special action to be turned off. Unlike other types of RAMs which require a negative transition of $\overline{CAS}$ to become high impedance, the F4116's output is already high impedance whenever $\overline{CAS}$ is HIGH, i.e., inactive. This means that $\overline{CAS}$ need not be supplied to unused devices and therefore may be used for device selection. Thus a reduction in external decoding logic is possible by using both $\overline{RAS}$ and $\overline{CAS}$ in a 2-dimensional decoding/selection scheme.

$\overline{RAS}$ and $\overline{CAS}$ Clock Conditions

$\overline{RAS}$ and $\overline{CAS}$ cycle	Device active
$\overline{RAS}$ only cycle	Device deselected, refresh
$\overline{CAS}$ only cycle	Device deselected
Neither $\overline{RAS}$ nor $\overline{CAS}$	Device deselected, standby

Extended Page Boundary

A further implication of using both $\overline{RAS}$ and $\overline{CAS}$ for device decoding/selection is in extending page boundaries for page-mode operation. If only $\overline{RAS}$ is decoded, then any given page is limited to only 128 different column addresses within that page (i.e., seven column address bits correspond to $2^7 = 128$ column addresses). Therefore, for memory systems using more than 16K words of data, page boundaries may be extended from 128 addresses per page up to any multiple of 128 addresses merely by decoding which 16K memory bank also gets a $\overline{CAS}$ (subject to $t_{RAS(max)}$ limitation). This is accomplished by supplying $\overline{RAS}$ to all devices in order to latch in the row address information and then decoding which bank of 16K words also gets $\overline{CAS}$. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ will respond with a valid memory cycle.

Input/Output Levels

All inputs, including the two address strobes, interface directly with TTL. The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Termination resistors are normally required in a system to prevent ringing due to line inductance and reflections. In high-speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series termination may by employed at some degradation of system speed. The 3-state output buffer is a low impedance to V_{CC} for logic "1" and low impedance to V_{SS} for logic "0". The effective resistance to V_{CC} is 420 Ω maximum and 135 Ω typically. The effective resistance to V_{SS} is 95 Ω maximum and 35 Ω typically.

Refresh

The matrix of 128 x 128 memory cells in the F4116 is refreshed by executing a memory cycle at each of the 128 row addresses within each interval of 2 ms or less. Although any cycle in which $\overline{RAS}$ occurs accomplishes a refresh operation, the refresh is most easily accomplished in the $\overline{RAS}$-only-refresh mode. This type of refresh operation results in decreased power dissipation, since $\overline{CAS}$ remains inactive.

Power Dissipation/Standby

Since the F4116 uses dynamic memory cells, this means that most of the dissipated power is a result of an address strobe edge. There is, however, a small dc component of dissipated power that is associated with the precharging of the sense amplifiers. Thus, the total power dissipated is a function of both operating frequency and duty cycle. Typically, the power is 350 mW at 1 μs cycle time with a worst case power of less than 462 mW at 375 ns cycle time. To reduce overall system power during standby, $\overline{RAS}$-only-refresh cycles should be performed with $\overline{CAS}$ held HIGH.

The V_{CC} supply is not used in the internal memory operations of the F4116, but rather is used only at the output buffer and thus, for some applications, may be powered from the supply voltage of the logic to which the chip's output is interfaced. This means that I_{CC}, the current drawn from the V_{CC} supply, is a function of output loading. During battery standby operation, the V_{CC} pin may be unpowered, if desired, without affecting the refresh operation. This allows all system logic, except the $\overline{RAS}$ timing circuitry and the refresh address logic, to be turned off during battery standby to conserve power.

Memory Power Up

The F4116 requires no particular power supply sequencing as long as the absolute maximum rating conditions are observed. However, in order to insure compliance with the absolute maximum ratings, by providing larger voltage margins, it is recommended that power supplies be sequenced at power-up such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits, significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state.

After power is applied to the device, the F4116 requires several cycles before proper device operation is achieved. Any eight cycles which perform refresh are adequate for this purpose.

DC Requirements T_A = 0°C to +70°C (See Notes 1 and 2)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{DD}	Supply Voltage	10.8	12	13.2	V	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	Note 5
V_{SS}	Supply Voltage	0	0	0	V	
V_{BB}	Supply Voltage	−5.7	−5.0	−4.5	V	
V_{IHC}	Input HIGH Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.4		7.0	V	
V_{IH}	Input HIGH Voltage, All Inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.2		7.0	V	
V_{IL}	Input LOW Voltage, All Inputs	−1.0		0.8	V	

DC Characteristics Over full range of voltage and temperature

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage		2.4			V	I_{OUT} = −5.0 mA, Note 5
V_{OL}	Output LOW Voltage				0.4	V	I_{OUT} = 4.2 mA, Note 5
I_{DD}	Average V_{DD} Current	Normal Operation			35	mA	For F4116-4 Refresh I_{DD} = 27 mA Max. Note 3
		Standby			1.5	mA	
		Refresh			25	mA	
		Page Mode			27	mA	
I_{CC}	Average V_{CC} Current	Normal Operation/ Page Mode					Note 4
		Standby/Refresh	−10		10	μA	
I_{BB}	Average V_{BB} Current	Normal Operation/ Refresh/Page Mode			200	μA	
		Standby			100	μA	
I_{IN}	Input Leakage Current (Any Input)		−10		10	μA	
I_{OUT}	Output Leakage Current		−10		10	μA	
C_{IN1}	Input Capacitance, A_0-A_6, D			4.0	5.0	pF	Note 6
C_{IN2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$			8.0	10	pF	Note 6
C_{OUT}	Output Capacitance, Q			5.0	7.0	pF	$\overline{CAS}$ = V_{IHC}

Notes on following pages.

Recommended ac Operating Conditions Over full range of voltage and temperature

Symbol	Characteristic	F4116-2		F4116-3		F4116-4		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	320		375		410		ns	7
t_{RWC}	Read-Write Cycle Time	320		375		425		ns	7
t_{RMW}	Read Modify Write Cycle Time	320		405		500		ns	7
t_{PC}	Page Mode Cycle Time	170		225		275		ns	7
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165	ns	9, 10
t_{OFF}	Output Buffer Turn-off Delay	0	40	0	50	0	60	ns	11
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10,000	200	10,000	250	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	12
t_{ASR}	Row Address Set-up Time	0		0		0			
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-up Time	−10		−10		−10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_T	Transition Time (Rise and Fall)	3.0	35	3.0	50	3.0	50	ns	13
t_{RCS}	Read Command Set-up Time (RMW)	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{WCS}	Write Command Set-up Time	−20		−20		−20		ns	14
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	50		70		85		ns	15
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		ns	15
t_{DS}	Data In Set-up Time	0		0		0		ns	16
t_{DH}	Data In Hold Time	45		55		75		ns	16
t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		ns	

Notes on following page.

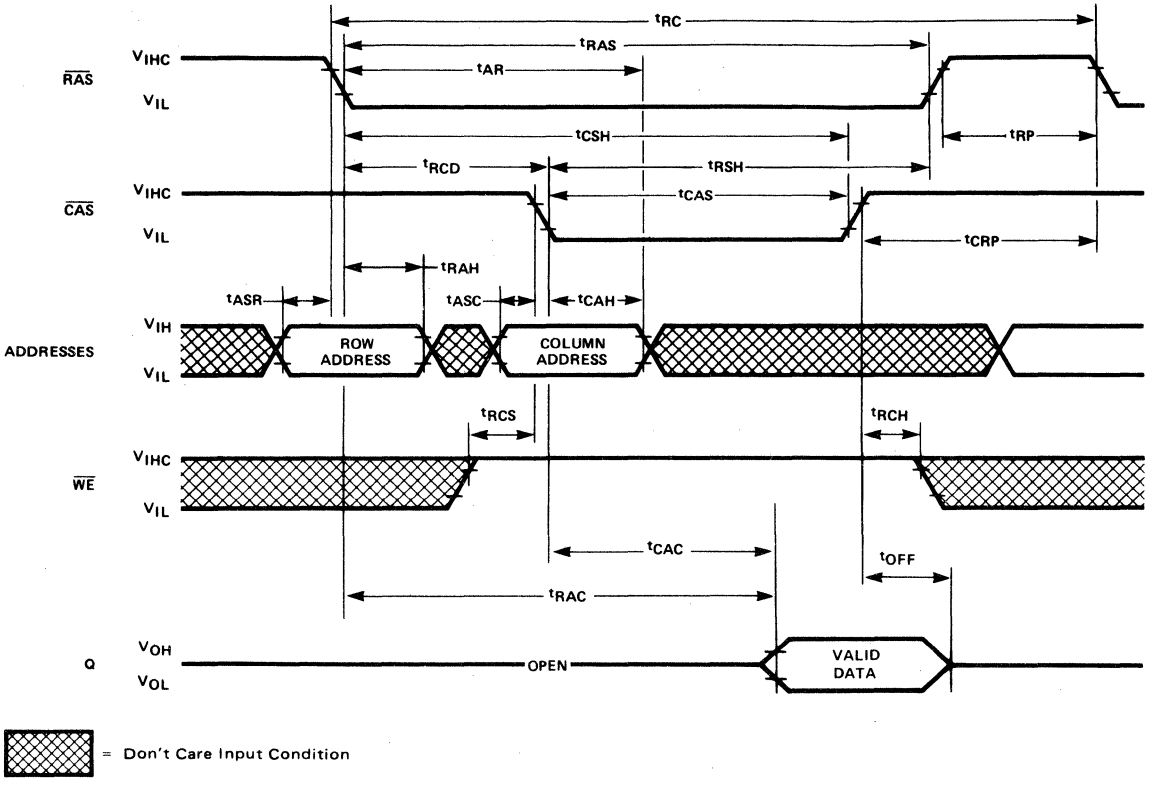
Recommended ac Operating Conditions (Cont'd)

Symbol	Characteristic	F4116-2		F4116-3		F4116-4		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CP}	$\overline{CAS}$ Precharge Time (Page-Mode)	60		80		100		ns	
t_{RF}	Refresh Period		2.0		2.0		2.0	ms	
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	60		80		90		ns	17
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	110		145		175		ns	17

Notes

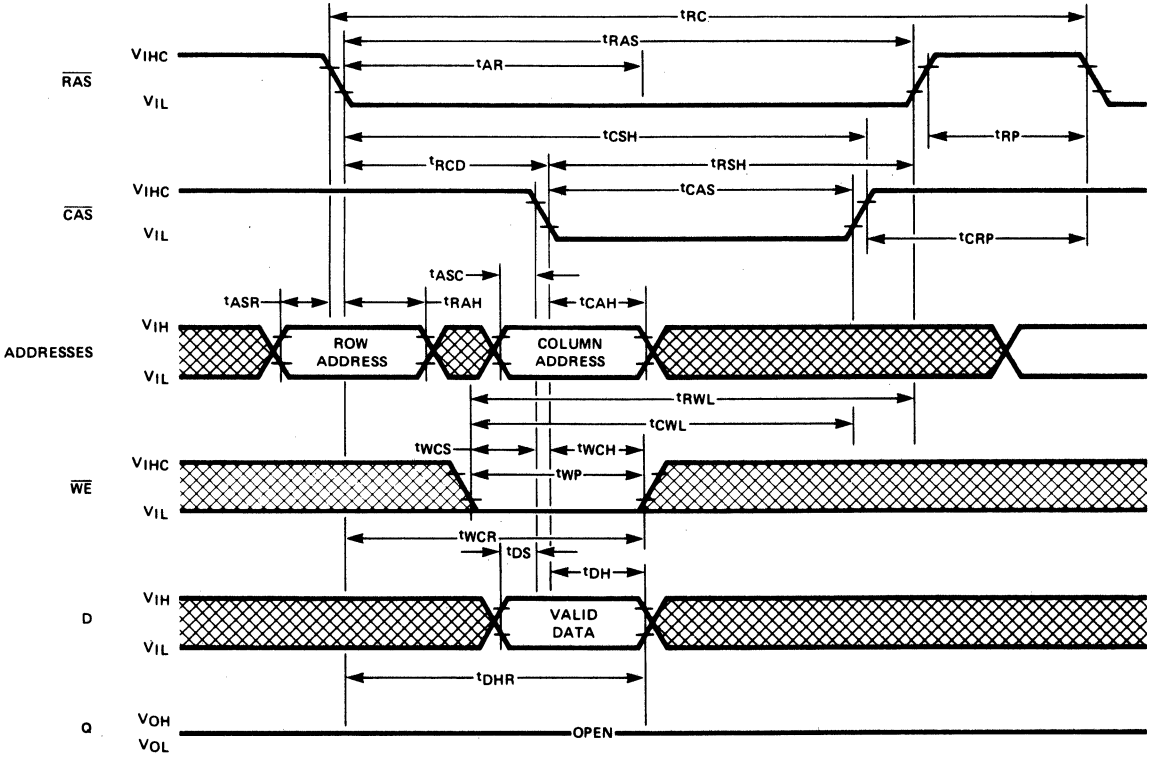
1. The ambient temperature (T_A) is specified here for operation at frequencies up to that frequency determined by the minimum cycle time. Operation at high cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided ac operating parameters are met.
2. All voltages are referenced to V_{SS} = 0 V.
3. I_{DD} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.
4. I_{CC} depends upon output loading. The V_{CC} is connected to the output buffer only. During readout of HIGH level data, V_{CC} is connected through a low impedance (135 Ω typ) to Data Out. At other times I_{CC} consists of leakage currents only.
5. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of reducing power in the standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH(min)}$ specification is not guaranteed in this mode.
6. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with ΔV = 3 V and power supplies at normal levels.
7. The specifications for $t_{RC(min)}$, $t_{RWC(min)}$, $t_{RMW(min)}$ and $t_{PC(min)}$ are used only to indicate cycle time at which proper operation over full temperature range (0°C ≤ T_A ≤ 70°C) is assured. All transition times, t_T, are assumed to be 5 ns.
8. Assumes that $t_{RCD} \leq t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
10. Measured with a load equivalent to two TTL loads and 100 pF.
11. $t_{OFF(max)}$ defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
12. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
13. $V_{IHC(min)}$ or $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Composite timing parameters (such as cycle times) assume 5 ns transition times.
14. t_{WCS} is a restrictive operating parameter. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the Data Out pin will remain open circuit (high impedance) throughout the entire cycle, otherwise the cycle is a delayed write cycle.
15. The parameters t_{RWL} and t_{CWL} reference $\overline{WE}$ (for a read-modify-write cycle) to either $\overline{RAS}$ or $\overline{CAS}$ respectively, whichever is the first to go HIGH.
16. t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.
17. t_{RWD} and t_{CWD} are restrictive operating parameters due to the following characteristics:
    If $t_{CWD} < t_{CWD(min)}$, the Data Out will be indeterminate.
    If $t_{CWD} \geq t_{CWD(min)}$, the Data Out will contain the data read from the selected cell.

Timing Diagrams
Read Cycle

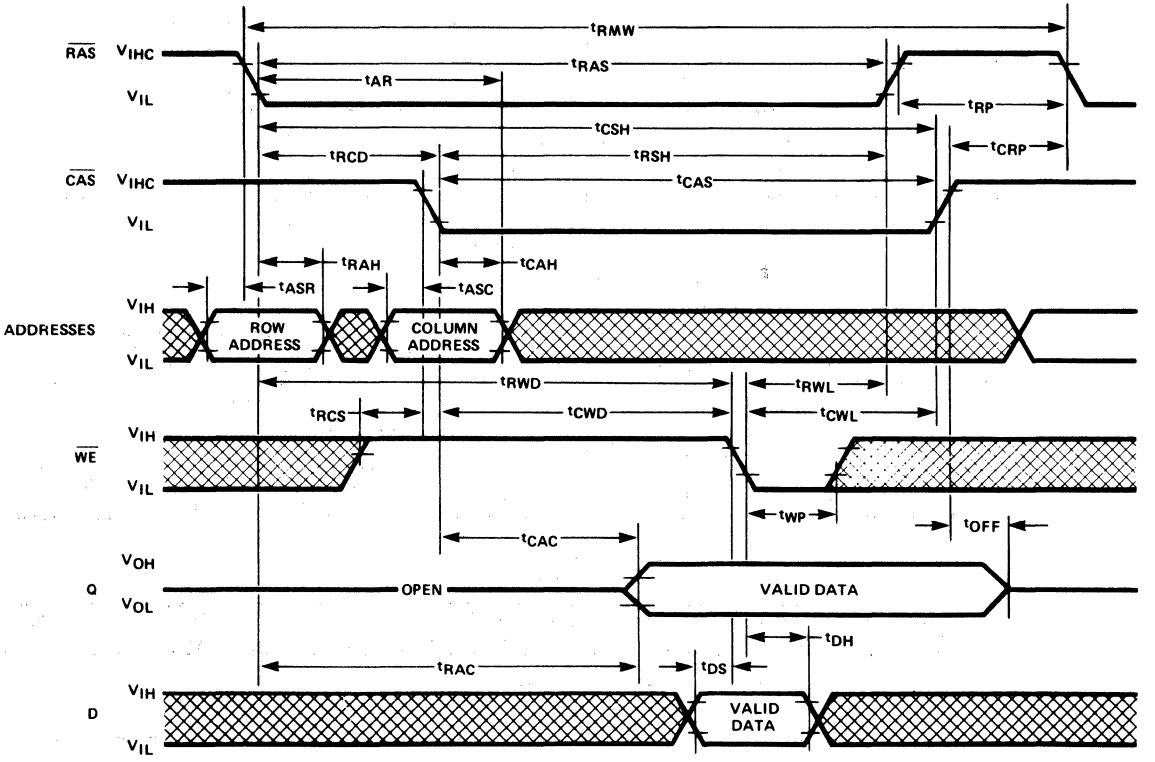


= Don't Care Input Condition

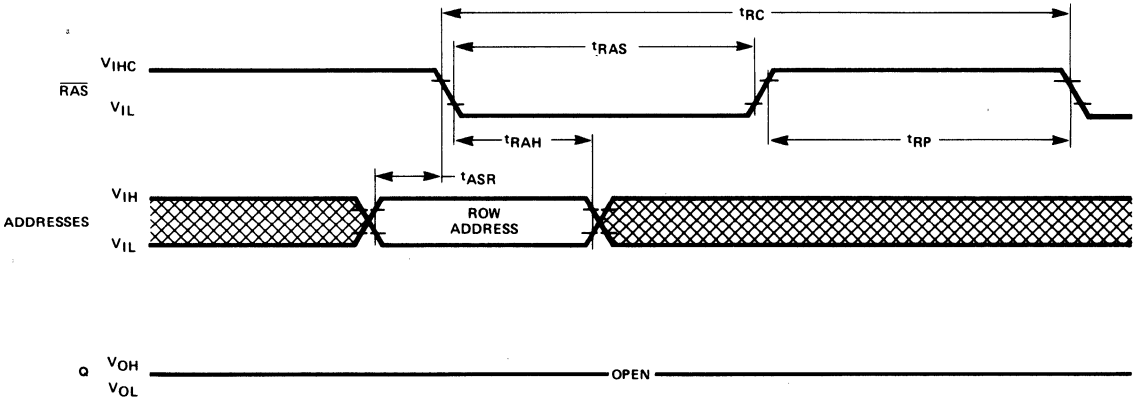
Write Cycle (Early Write)



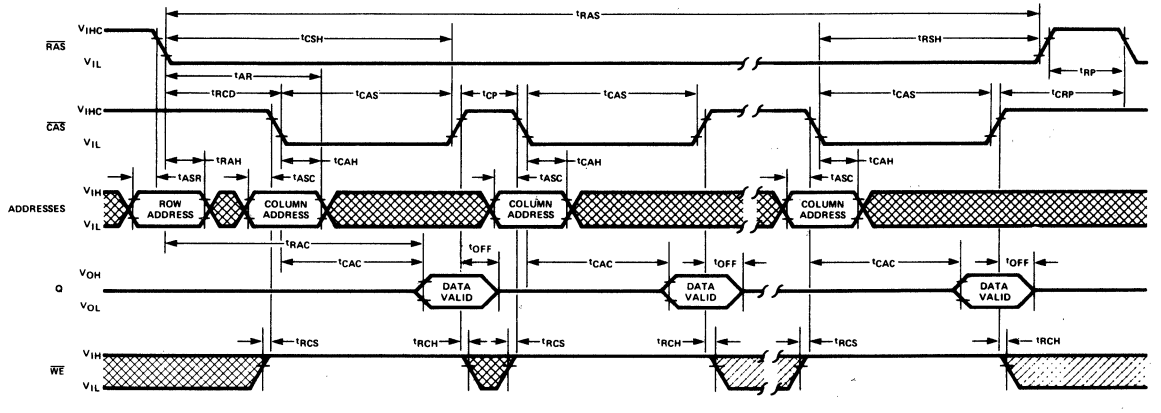
Read-Write/Read-Modify-Write Cycle



"$\overline{RAS}$ ONLY" Refresh Cycle

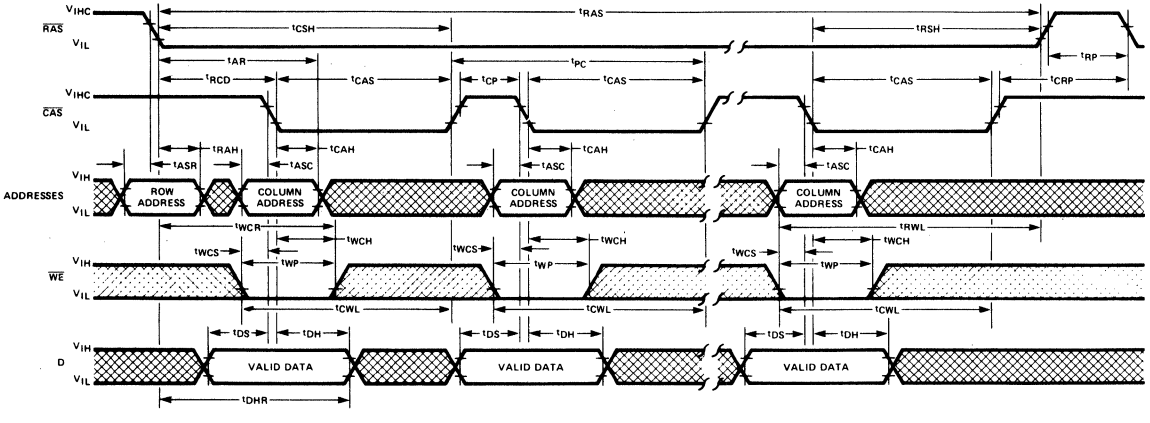


Page Mode Read Cycle

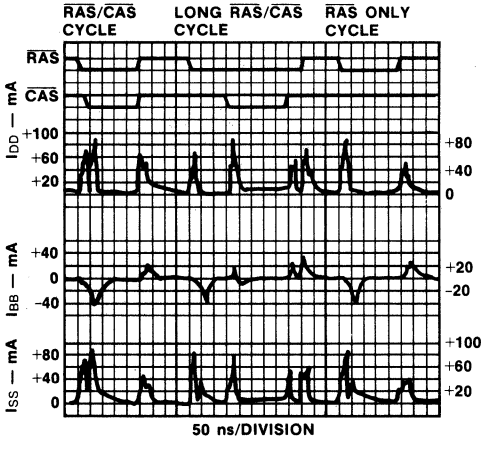


= Don't Care Input Condition

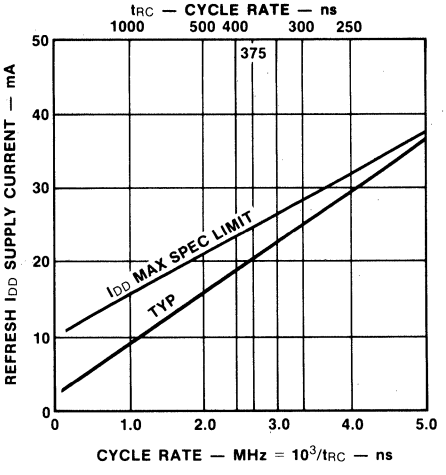
Page Mode Write Cycle (Early Write)



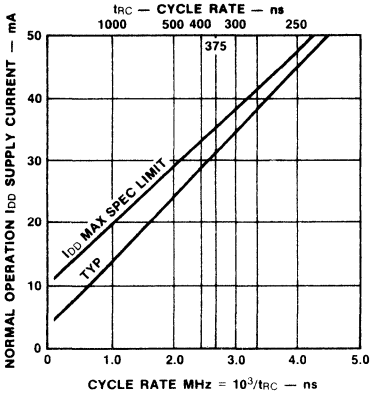
Typical Current Waveforms



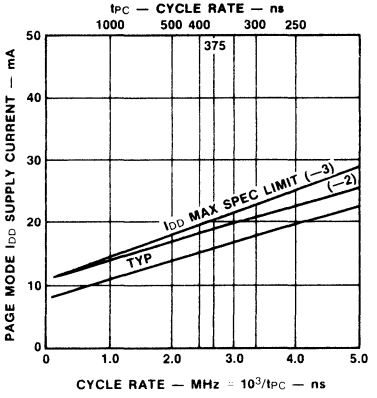
Refresh I_{DD} vs Cycle Rate



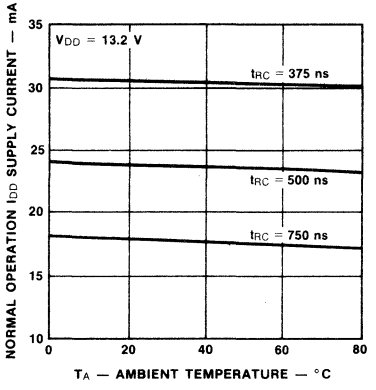
Normal Operation I_{DD} vs Cycle Rate



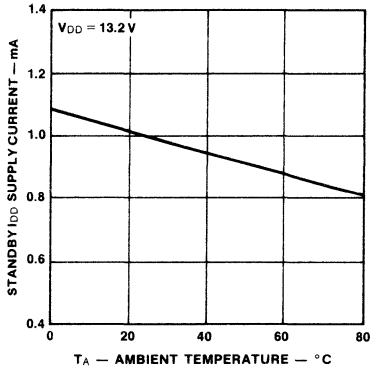
Page Mode I_{DD} vs Cycle Rate



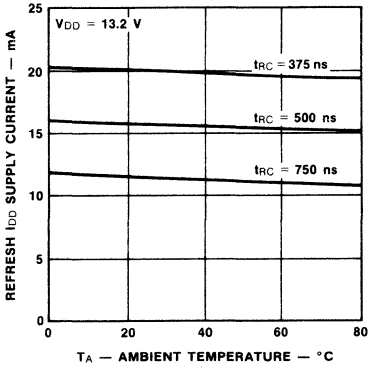
Normal Operation I_{DD} vs Ambient Temperature



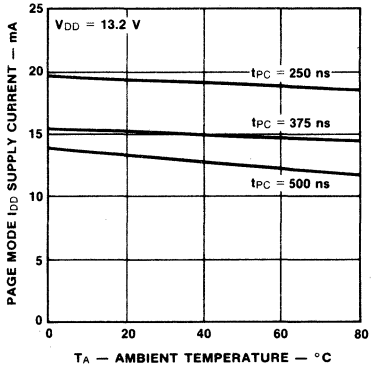
Standby I_{DD} vs Ambient Temperature



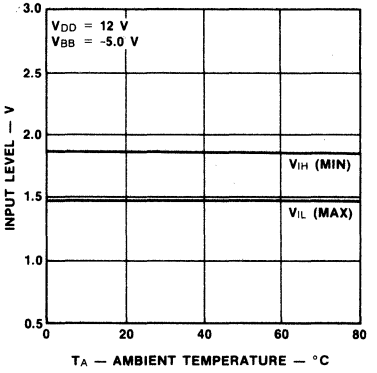
Refresh I_{DD} vs Ambient Temperature



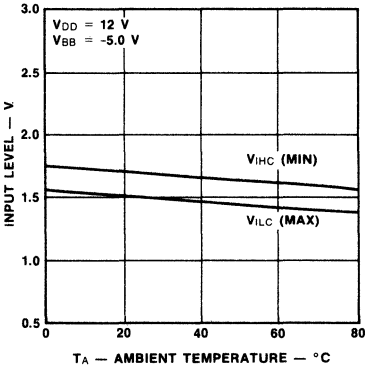
Page Mode I_{DD} vs Ambient Temperature



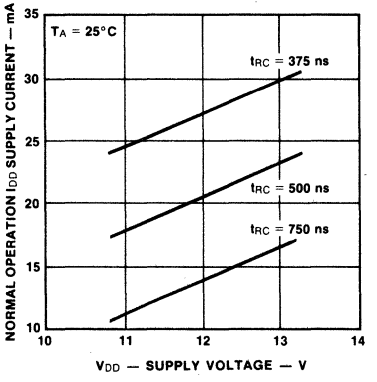
Address Data Input Levels vs T_A



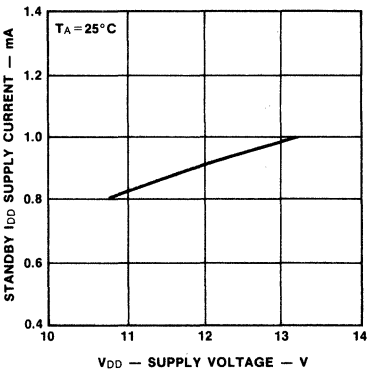
Clock Input Levels vs T_A



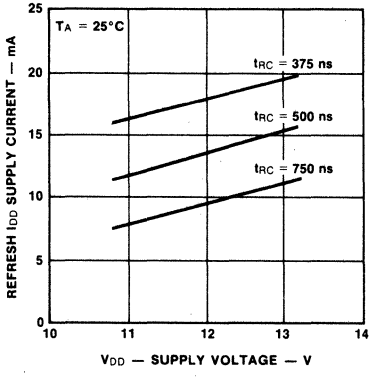
Normal Operation I_{DD} vs V_{DD}



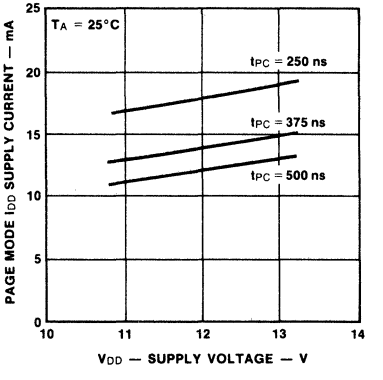
Standby I_{DD} vs V_{DD}



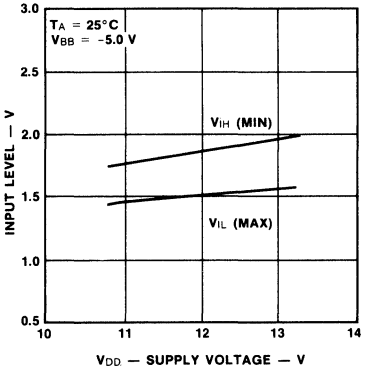
Refresh I_{DD} vs V_{DD}



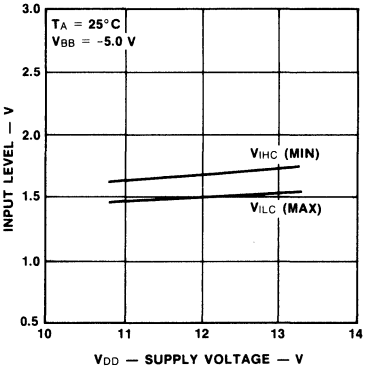
Page Mode I_{DD} vs V_{DD}



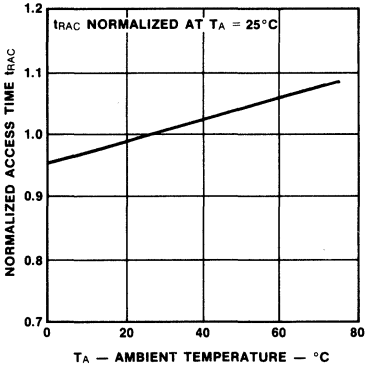
Address Data Input Levels vs V_{DD}



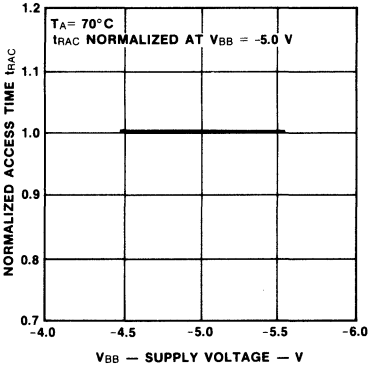
Clock Input Level vs V_{DD}



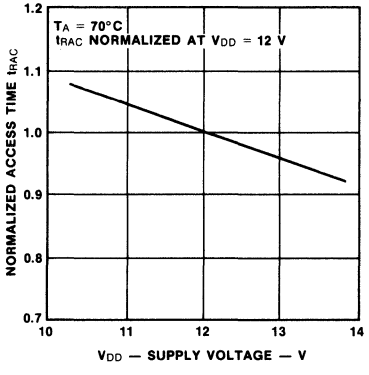
Access Time (Normalized) vs T_A



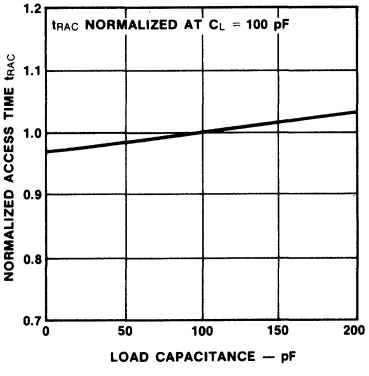
Access Time (Normalized) vs V_{BB}



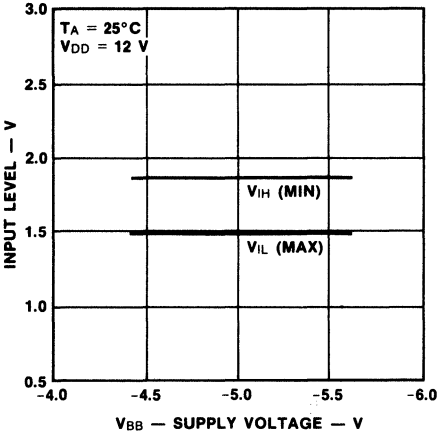
Access Time (Normalized) vs V_{DD}



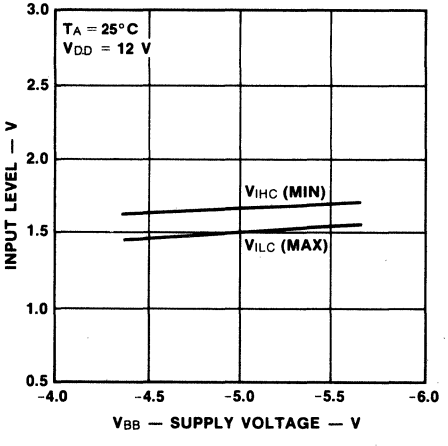
Normalized Access Time vs Load Capacitance



Address and Data Input Levels vs V_{BB}



Clock Input Level vs V_{BB}



Applications and Testing

F4116 Data Scramble

In order to assist engineers in testing the F4116 16,384 x 1-bit dynamic Random Access Memory, information concerning the internal polarity and location of the stored data is provided as follows. *Figure 1* shows a block diagram of the various figures and how they relate to each other.

Address Scrambling

The relationship of the external (data sheet) address to the actual internal row or column address is shown in *Figure 2*. This information may be required to locate a specific location on the chip, when only its external pin address is known. The actual chip addresses (converted to decimal) are shown in *Figure 3*.

Figure 4 shows the external logic necessary to descramble the F4116 internal logic shown in *Figure 2*. For example, addressing column "0", via the system address inputs (A_0-A_6 = LOW), selects the actual chip column 0 shown in *Figure 3*. Setting a "1" on the system column address inputs (0000001), selects the adjacent actual column "1" on the chip. This correspondence holds for all rows and columns when using the transformation supplied in *Figure 4*.

The tables provided in *Figures 5* and *6* show the relationship of the system address (decimal) to the external (data sheet) address converted to octal. In other words, *Figures 5* and *6* are simply truth tables for the logic shown in *Figure 4*.

Data Inversion

Since the F4116 employs balanced sense amps, it is necessary to store some of the data in inverted form. This is decoded internally so it does not appear to the user, and need only be considered when testing. The input and output EXOR gates shown in *Figure 1* provide the proper inversions necessary to have all data written in the same polarity. It should be noted that A_6, shown in *Figure 1*, is referenced to the most significant bit of the system row address. This is because the inversion is only related to the row address and must be independent of the multiplexing operation.

Fig. 1 Relationship of various scrambling and inversion networks

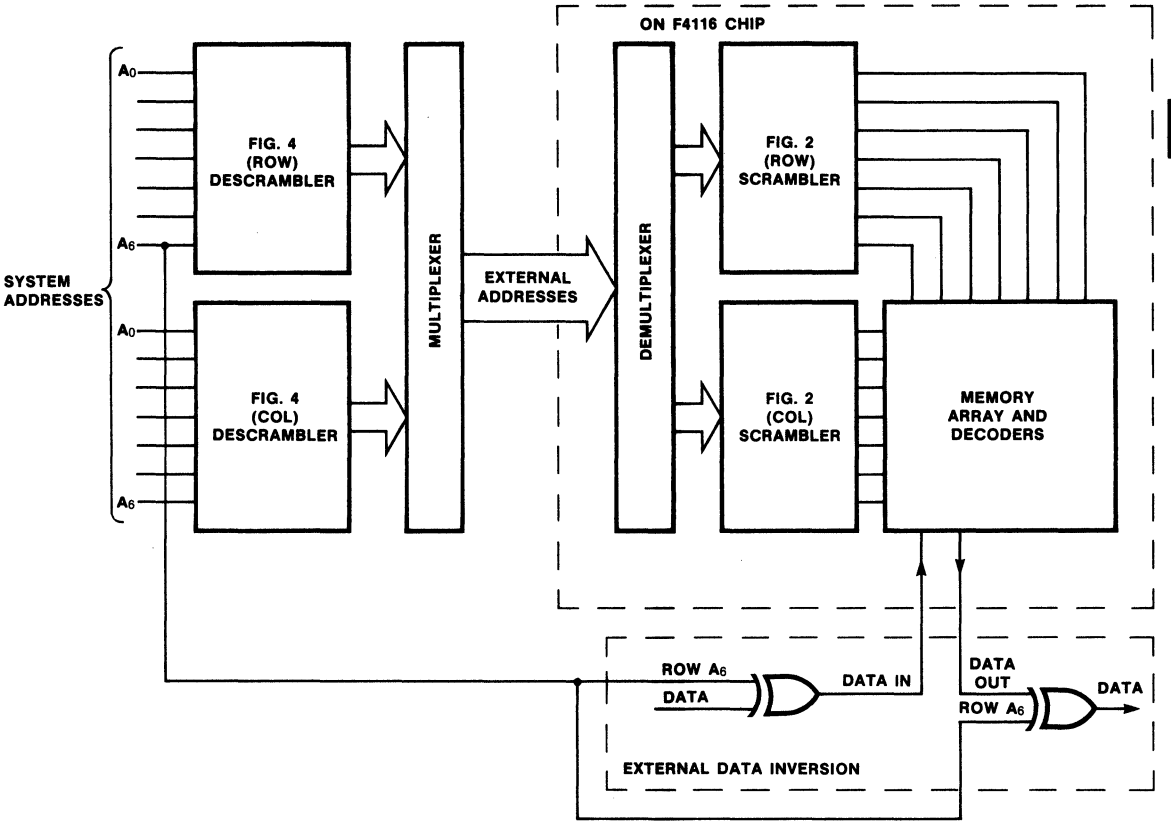


Fig. 2 Relationship of external addresses to actual row and column positions (multiplexer not shown). Refer to *Figure 3* for actual positions converted to decimal.

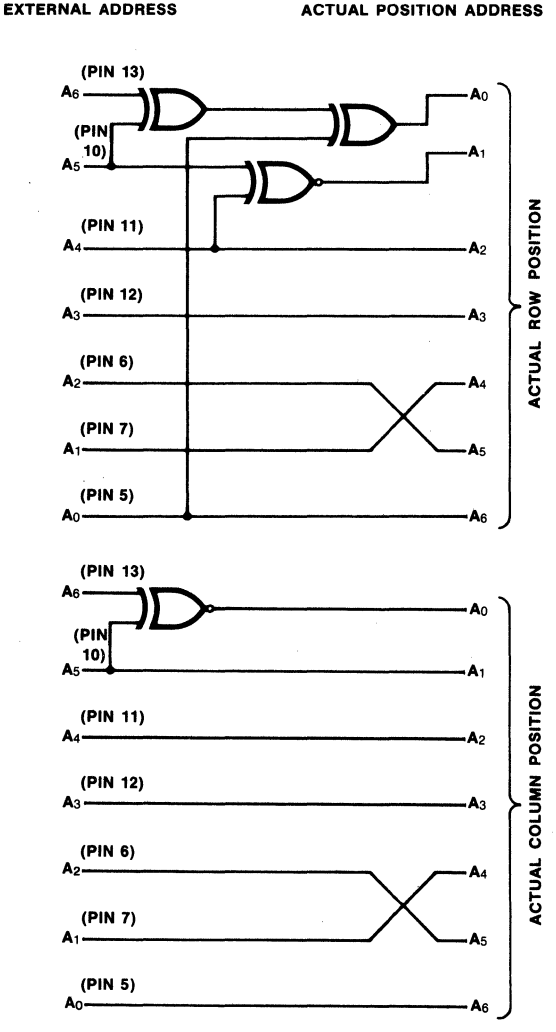
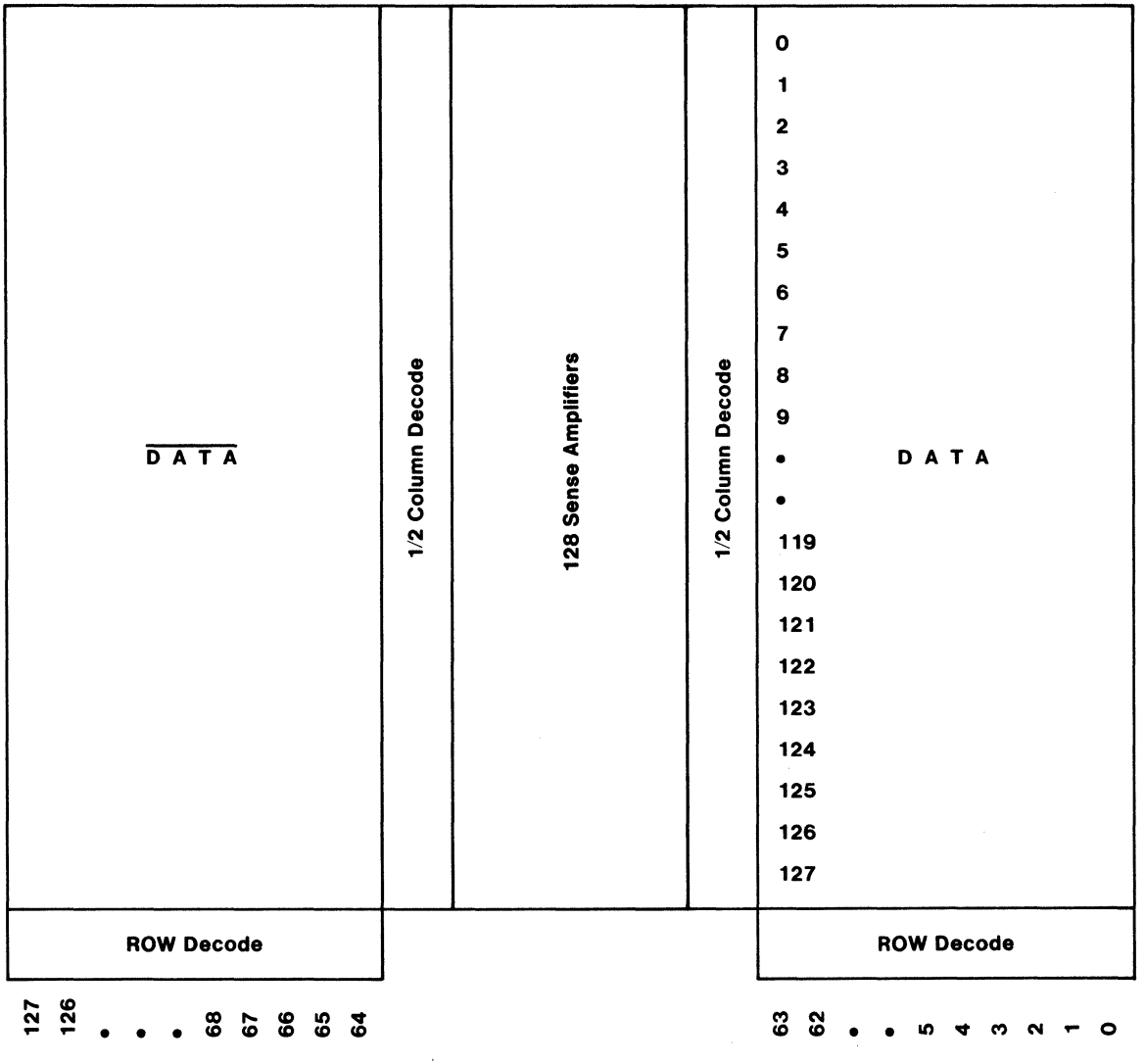
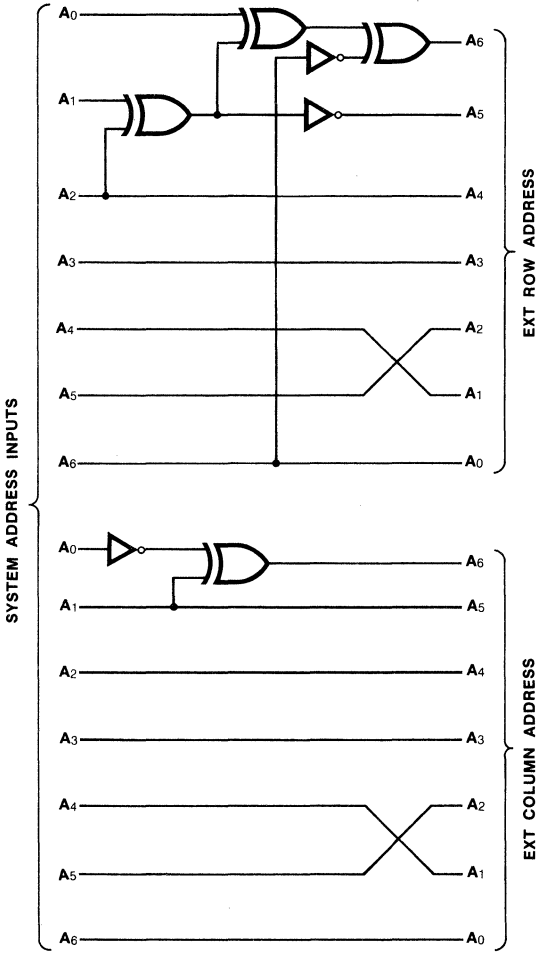


Fig. 3 F4116 Bit Map



Actual column and row position addresses converted to decimal. Conversion to the external address is explained in the text.

Fig. 4 External address transformation required to descramble F4116 internal decoder shown in *Figure 1* (multiplexer not shown).



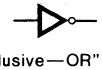
Note
The logic symbols  and  are used solely to indicate the logic function "Exclusive—OR" and "NOT", respectively. The above figure is not a suggested implementation of logic.

Fig. 5 System Row Address (Decimal) To External Address (Octal) Conversion Table

System Row Address	External Address	System Row Address	External Address	System Row Address	External Address	System Row Address	External Address
0	1 4 0	32	1 4 4	64	0 4 1	96	0 4 5
1	0 4 0	33	0 4 4	65	1 4 1	97	1 4 5
2	0 0 0	34	0 0 4	66	1 0 1	98	1 0 5
3	1 0 0	35	1 0 4	67	0 0 1	99	0 0 5
4	0 2 0	36	0 2 4	68	1 2 1	100	1 2 5
5	1 2 0	37	1 2 4	69	0 2 1	101	0 2 5
6	1 6 0	38	1 6 4	70	0 6 1	102	0 6 5
7	0 6 0	39	0 6 4	71	1 6 1	103	1 6 5
8	1 5 0	40	1 5 4	72	0 5 1	104	0 5 5
9	0 5 0	41	0 5 4	73	1 5 1	105	1 5 5
10	0 1 0	42	0 1 4	74	1 1 1	106	1 1 5
11	1 1 0	43	1 1 4	75	0 1 1	107	0 1 5
12	0 3 0	44	0 3 4	76	1 3 1	108	1 3 5
13	1 3 0	45	1 3 4	77	0 3 1	109	0 3 5
14	1 7 0	46	1 7 4	78	0 7 1	110	0 7 5
15	0 7 0	47	0 7 4	79	1 7 1	111	1 7 5
16	1 4 2	48	1 4 6	80	0 4 3	112	0 4 7
17	0 4 2	49	0 4 6	81	1 4 3	113	1 4 7
18	0 0 2	50	0 0 6	82	1 0 3	114	1 0 7
19	1 0 2	51	1 0 0	83	0 0 3	115	0 0 7
20	0 2 2	52	0 2 6	84	1 2 3	116	1 2 7
21	1 2 2	53	1 2 6	85	0 2 3	117	0 2 7
22	1 6 2	54	1 6 6	86	0 6 3	118	0 6 7
23	0 6 2	55	0 6 6	87	1 6 3	119	1 6 7
24	1 5 2	56	1 5 6	88	0 5 3	120	0 5 7
25	0 5 2	57	0 5 6	89	1 5 3	121	1 5 7
26	0 1 2	58	0 1 6	90	1 1 3	122	1 1 7
27	1 1 2	59	1 1 6	91	0 1 3	123	0 1 7
28	0 3 2	60	0 3 6	92	1 3 3	124	1 3 7
29	1 3 2	61	1 3 6	93	0 3 3	125	0 3 7
30	1 7 2	62	1 7 6	94	0 7 3	126	0 7 7
31	0 7 2	63	0 7 6	95	1 7 3	127	1 7 7

Fig. 6 System Column Address (Decimal) To External Address (Octal) Conversion Table

System Column Address	External Address	System Column Address	External Address	System Column Address	External Address	System Column Address	External Address
0	1 0 0	32	1 0 4	64	1 0 1	96	1 0 5
1	0 0 0	33	0 0 4	65	0 0 1	97	0 0 5
2	0 4 0	34	0 4 4	66	0 4 1	98	0 4 5
3	1 4 0	35	1 4 4	67	1 4 1	99	1 4 5
4	1 2 0	36	1 2 4	68	1 2 1	100	1 2 5
5	0 2 0	37	0 2 4	69	0 2 1	101	0 2 5
6	0 6 0	38	0 6 4	70	0 6 1	102	0 6 5
7	1 6 0	39	1 6 4	71	1 6 1	103	1 6 5
8	1 1 0	40	1 1 4	72	1 1 1	104	1 1 5
9	0 1 0	41	0 1 4	73	0 1 1	105	0 1 5
10	0 5 0	42	0 5 4	74	0 5 1	106	0 5 5
11	1 5 0	43	1 5 4	75	1 5 1	107	1 5 5
12	1 3 0	44	1 3 4	76	1 3 1	108	1 3 5
13	0 3 0	45	0 3 4	77	0 3 1	109	0 3 5
14	0 7 0	46	0 7 4	78	0 7 1	110	0 7 5
15	1 7 0	47	1 7 4	79	1 7 1	111	1 7 5
16	1 0 2	48	1 0 6	80	1 0 3	112	1 0 7
17	0 0 2	49	0 0 6	81	0 0 3	113	0 0 7
18	0 4 2	50	0 4 6	82	0 4 3	114	0 4 7
19	1 4 2	51	1 4 6	83	1 4 3	115	1 4 7
20	1 2 2	52	1 2 6	84	1 2 3	116	1 2 7
21	0 2 2	53	0 2 6	85	0 2 3	117	0 2 7
22	0 6 2	54	0 6 6	86	0 6 3	118	0 6 7
23	1 6 2	55	1 6 6	87	1 6 3	119	1 6 7
24	1 1 2	56	1 1 6	88	1 1 3	120	1 1 7
25	0 1 2	57	0 1 6	89	0 1 3	121	0 1 7
26	0 5 2	58	0 5 6	90	0 5 3	122	0 5 7
27	1 5 2	59	1 5 6	91	1 5 3	123	1 5 7
28	1 3 2	60	1 3 6	92	1 3 3	124	1 3 7
29	0 3 2	61	0 3 6	93	0 3 3	125	0 3 7
30	0 7 2	62	0 7 6	94	0 7 3	126	0 7 7
31	1 7 2	63	1 7 6	95	1 7 3	127	1 7 7