HY53C256 Series

256K x 1-bit CMOS DRAM

DESCRIPTION

The HY53C256 is fast dynamic RAM organized 262,144 x 1-bit. The HY53C256 utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY53C256 to be packaged in a standard 300mil 16pin PDIP, 330mil 18pin PLCC.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V± 10% tolerence and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. CMOS standbY 5.5mW (L-part)
  11.0mW
  Max. TTL standby 11.0mW (L-part)
  16.5mW
  Max. operating

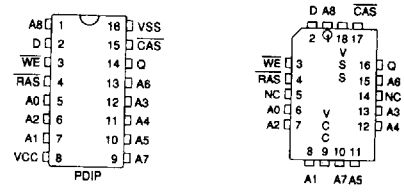
Speed	Power
70	385mW
80	330mW
10	275mW

- **Single power supply of 5V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tPC
70	70ns	15ns	50ns
80	80ns	20ns	55ns
10	100ns	25ns	60ns

- **Fast page mode operation**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh**
- **256 refresh cycles / 4ms**

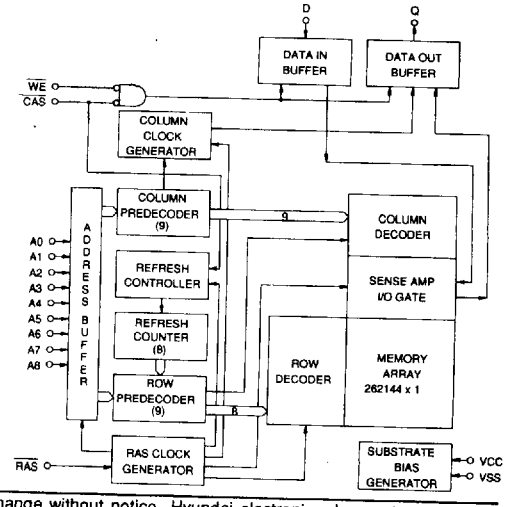
PIN CONNECTION



PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0-A8	Address Input
D	Data Input
Q	Data Output
Vcc	Power (+ 5V)
Vss	Ground

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature• Time	260• 10	°C• sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+ 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le V_{CC}$, All other pins not under test= V_{SS}		-10	10	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC}= t_{RC} (min.)	70 80 100	- - -	70 60 50	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs≥ V_{SS}	 L-part	- -	3 2	mA	4
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	70 80 100	- - -	70 60 50	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	t_{PC}= t_{PC} (min.)	70 80 100	- - -	45 40 35	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≤ V_{CC}–0.2V	 L-part	- -	2 1	mA	 4
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	70 80 100	- - -	70 60 50	mA	1,3
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while $\overline{RAS}$= V_{IL} and $\overline{CAS}$= V_{IH}.
4. I_{CC2}(max.)= 2mA and I_{CC5}(max.)= 1mA are only applied to L-part only (HY53C256LS and HY53C256LF).

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HY53C256S/F/LS/LF						UNIT	NOTE
			-70		-80		-10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	130	-	145	-	175	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	175	-	210	-	ns	
3	tPC	Fast Page Mode Cycle Time	50	-	55	-	60	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	75	-	85	-	95	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	-	45	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	45	-	50	-	55	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	20	0	25	ns	5
11	tT	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	50	-	55	-	65	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	70	75K	80	75K	100	75K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	75K	80	75K	100	75K	ns	
15	tRSH(W)	$\overline{RAS}$ Hold Time in Write Cycle	25	-	25	-	30	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
17	tCAS(W)	$\overline{CAS}$ Pulse Width in Write Cycle	20	-	25	-	30	-	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	55	25	60	25	75	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	20	35	20	40	20	55	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	-	15	-	15	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	15	-	15	-	15	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	20	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	55	-	60	-	70	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	45	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	5	-	5	-	5	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	5	-	5	-	5	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	20	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	55	-	60	-	70	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	20	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	20	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	55	-	60	-	70	-	ns	
39	tREF	Refresh Period (256 cycles)	-	4	-	4	-	4	ms	
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY53C256S/F/LS/LF						UNIT	NOTE
			-70		-80		-10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	-	20	-	25	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	70	-	80	-	100	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	35	-	40	-	45	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	20	-	25	-	30	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	15	-	15	-	20	-	ns	
48	tRSH(R)	$\overline{RAS}$ Hold Time in Read Cycle	15	-	20	-	25	-	ns	
49	tCAS(R)	$\overline{CAS}$ Pulse Width in Read Cycle	15	75K	20	75K	25	75K	ns	
50	tRRW	$\overline{RAS}$ Pulse Width (RMW)	95	-	110	-	135	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T= 5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

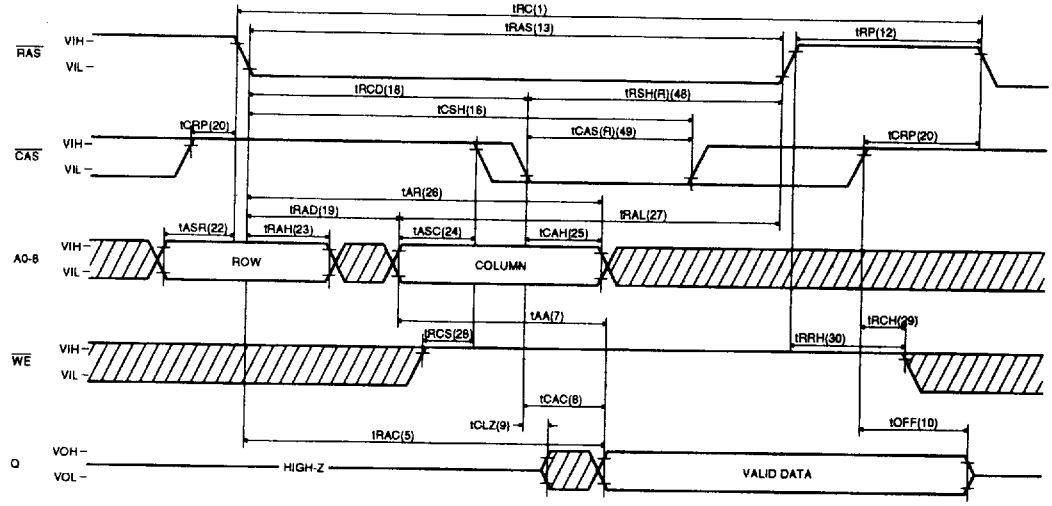
CAPACITANCE

(T_A= 25°C, V_{CC}= 5V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

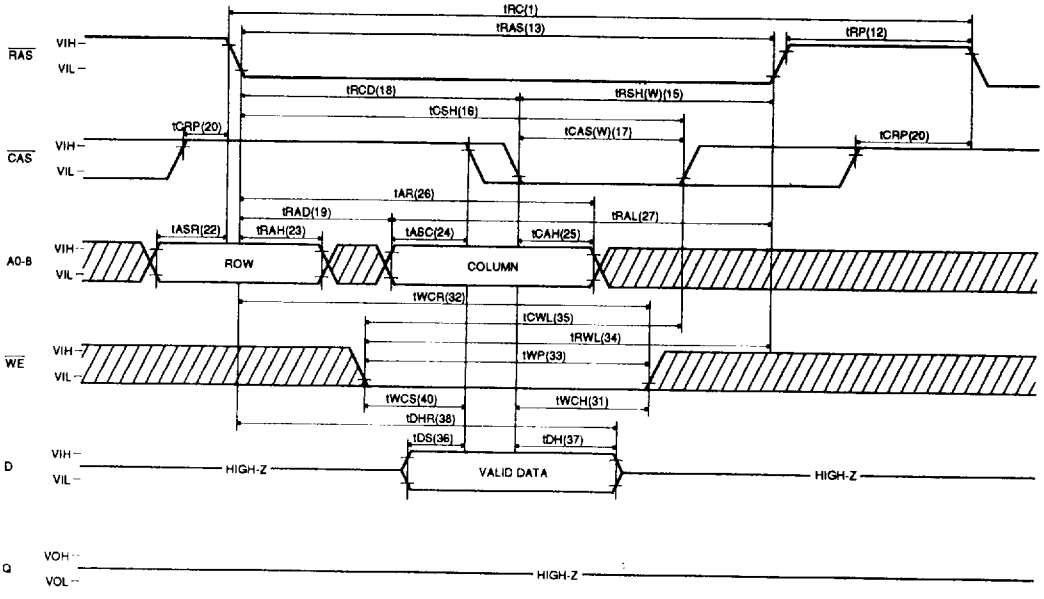
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A8, D)	-	6	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	-	8	pF
C_{OUT}	Output Capacitance (Q)	-	8	pF

TIMING DIAGRAM

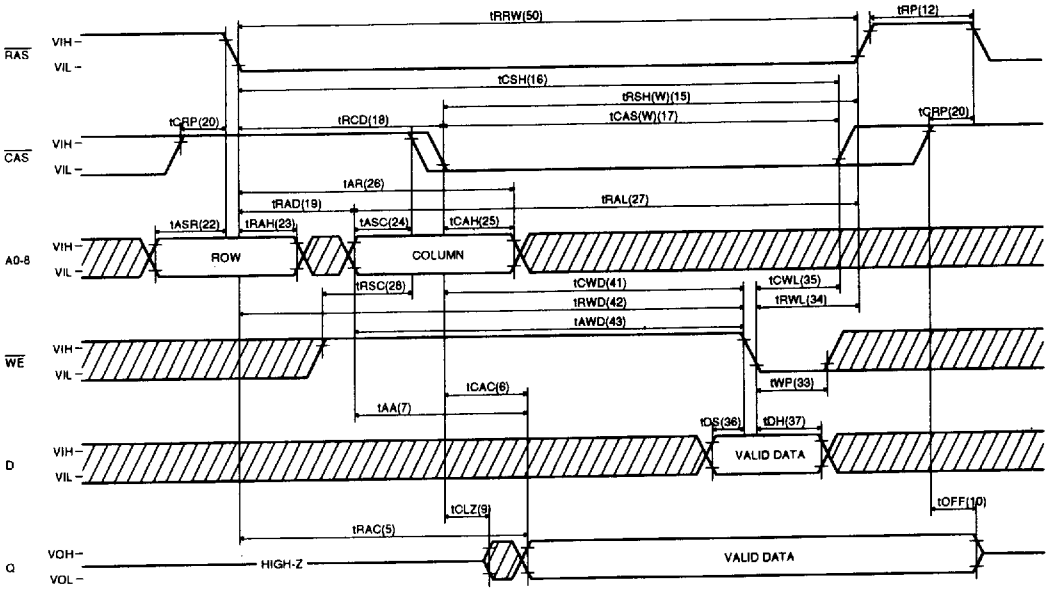
READ CYCLE



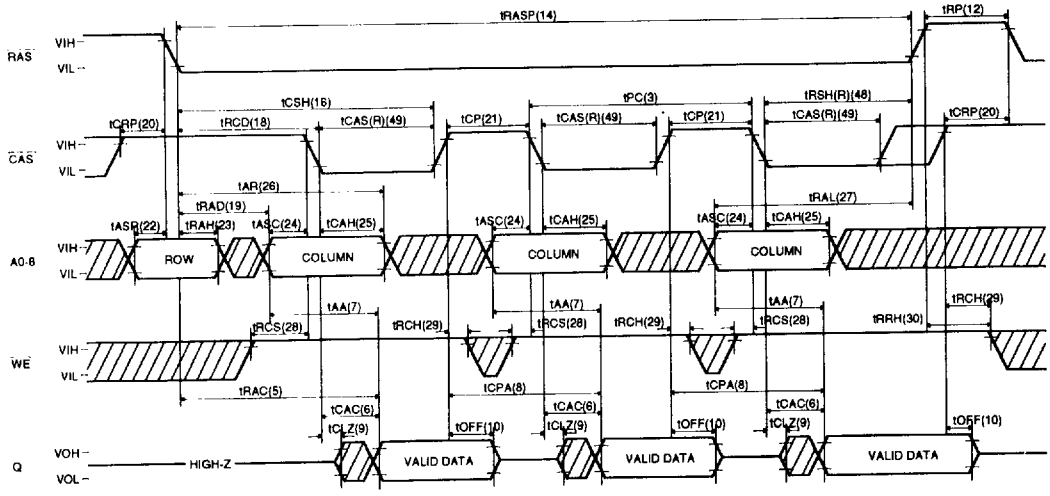
EARLY WRITE CYCLE



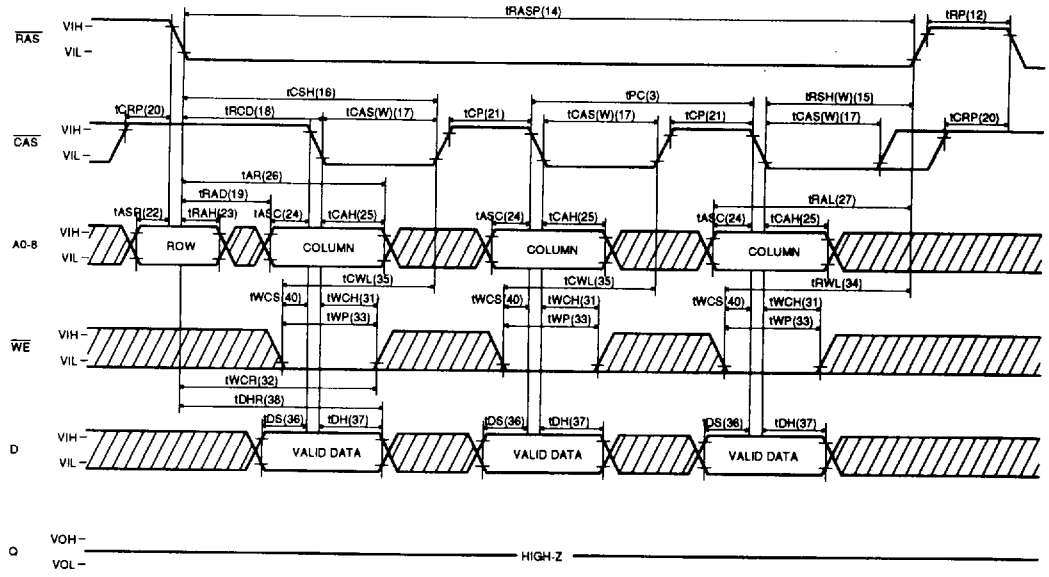
READ-MODIFY-WRITE CYCLE



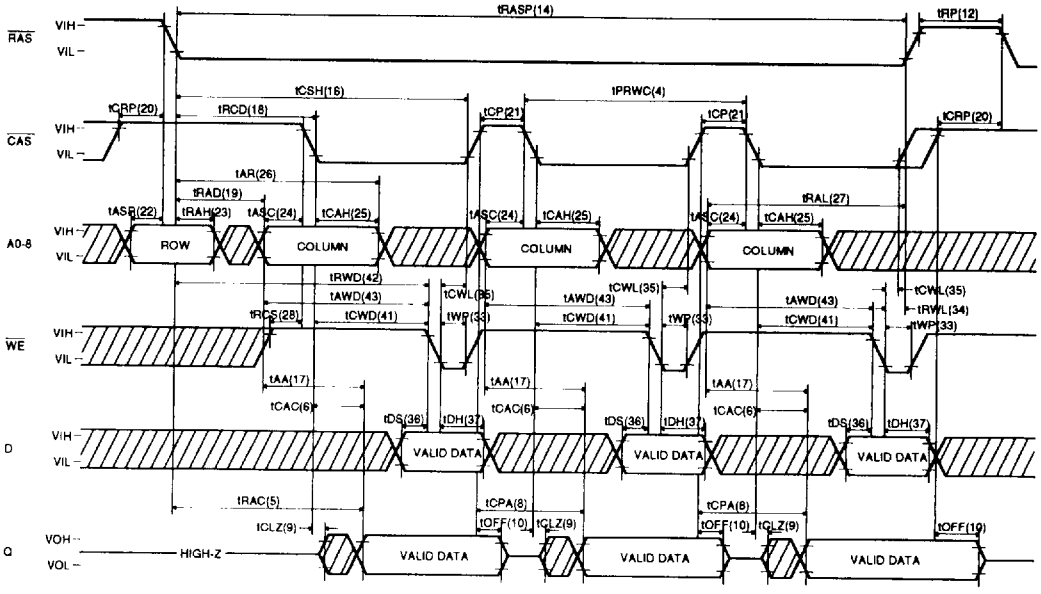
FAST PAGE MODE READ CYCLE



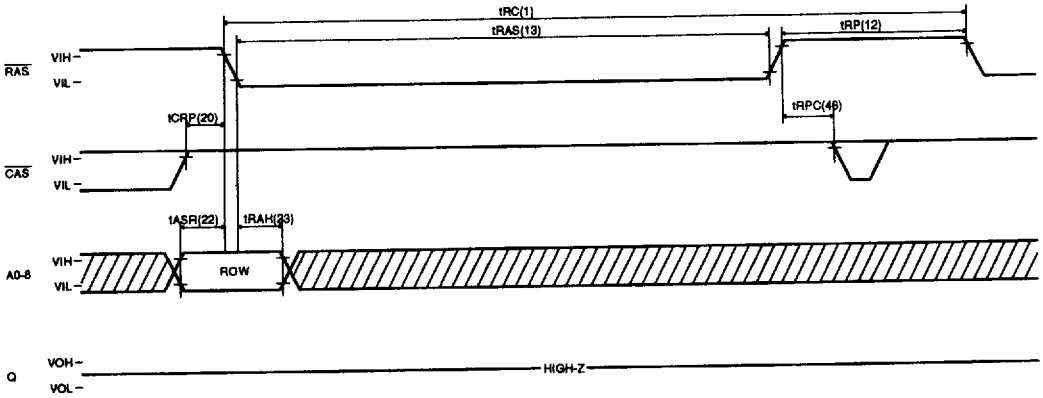
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

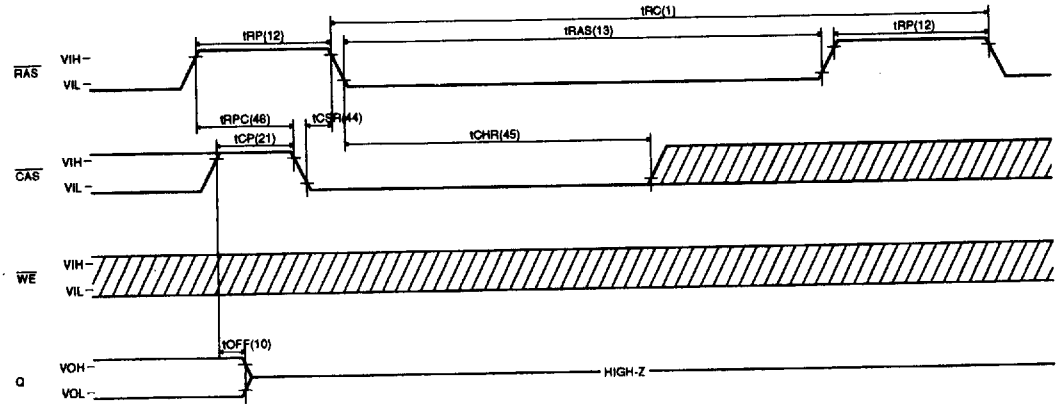


RAS-ONLY REFRESH CYCLE



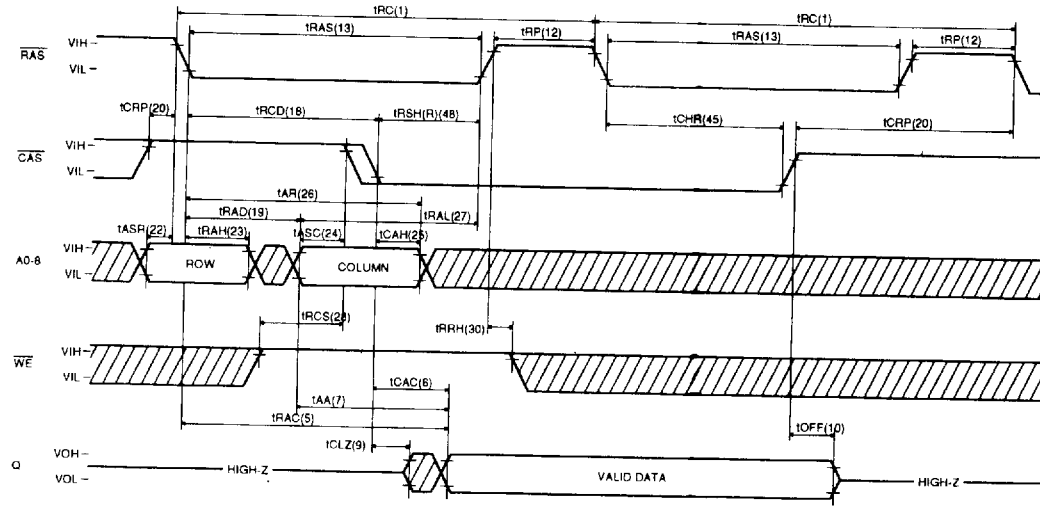
NOTE : $\overline{WE}$="H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

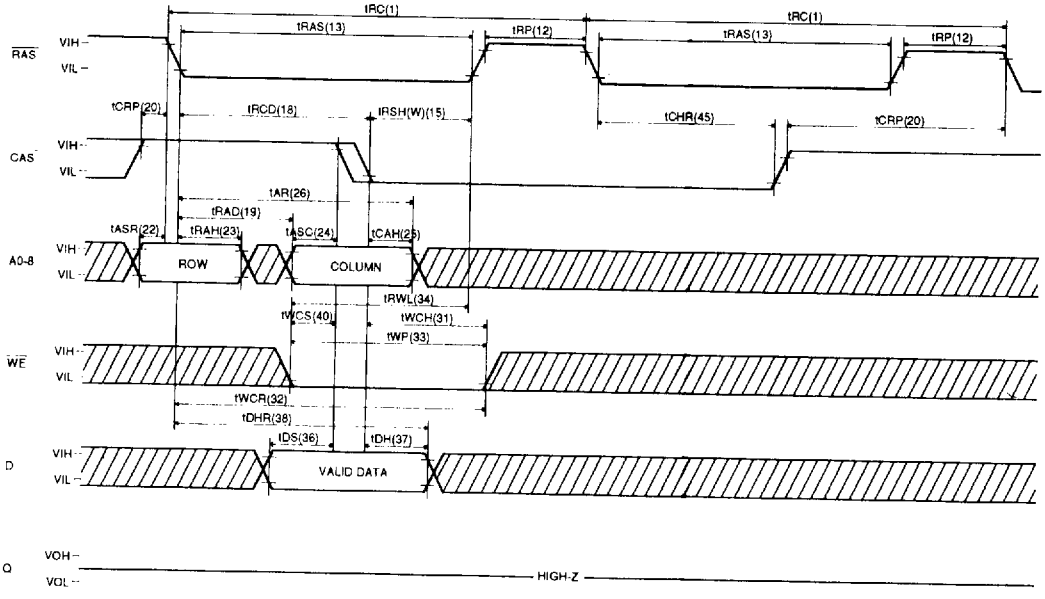


NOTE : A0-8="H" or "L"

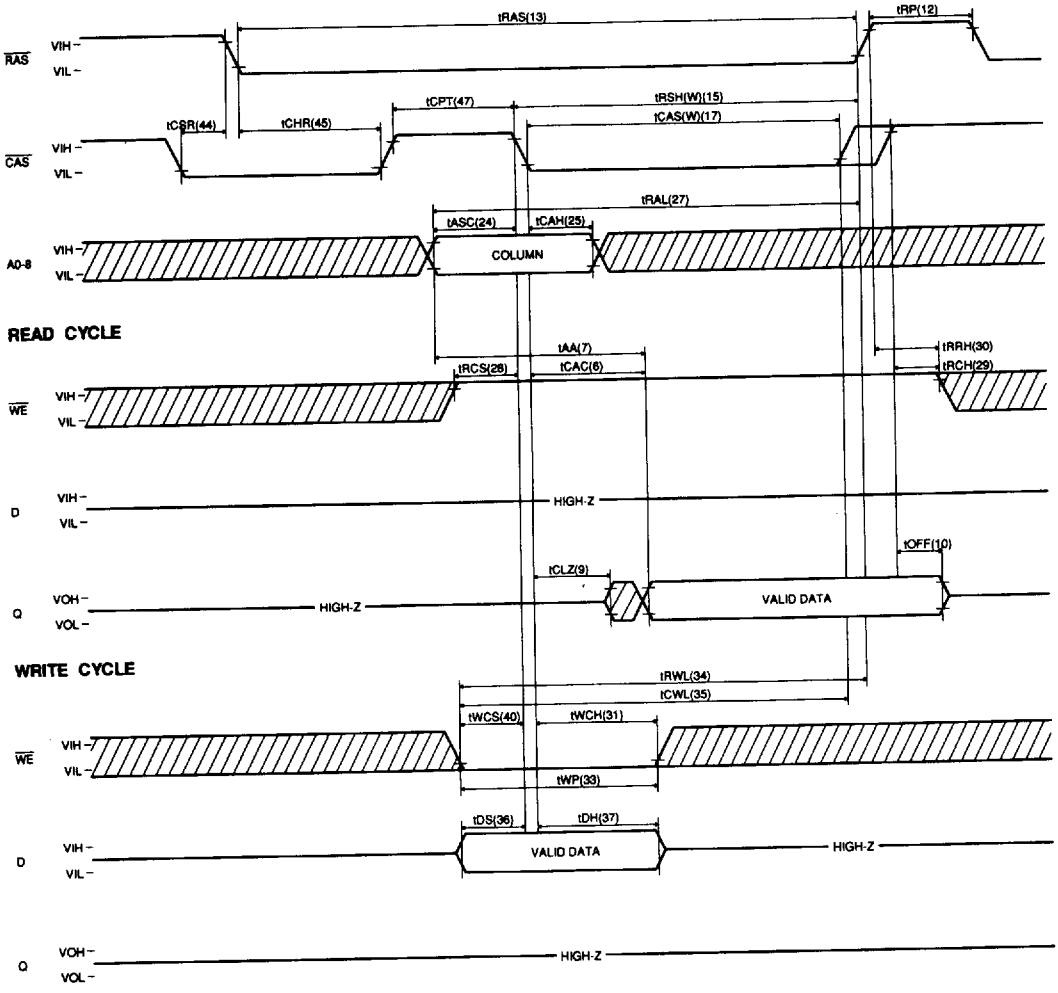
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

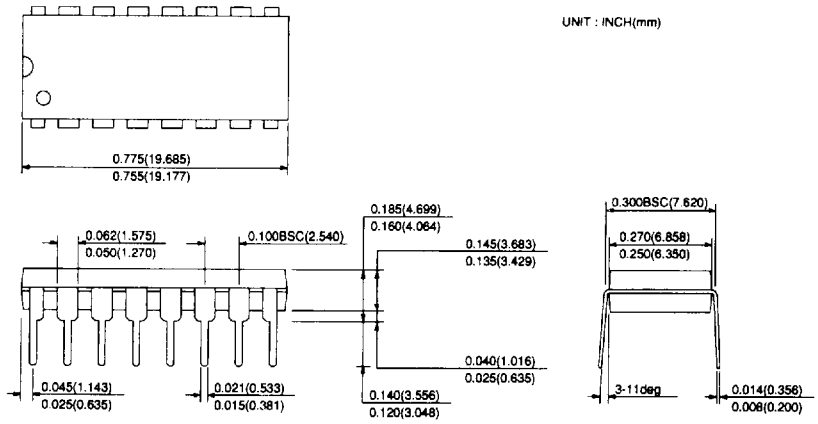


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

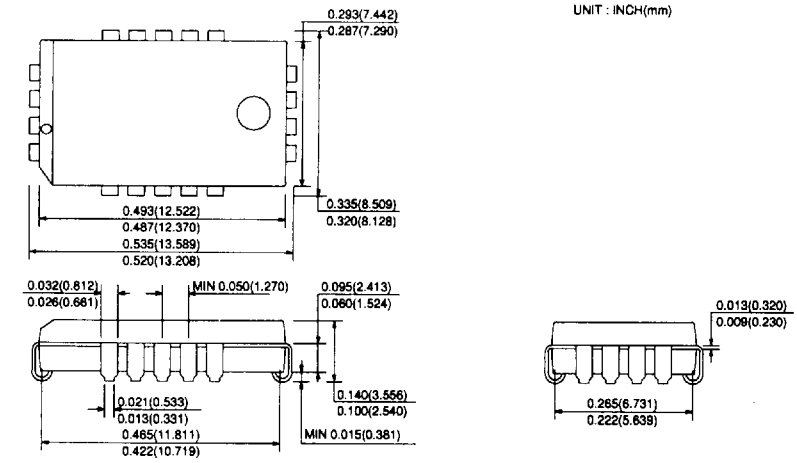


PACKAGE INFORMATION

300 mil 16 pin Plastic Dual In Line Package (S)



330 mil 18 pin Plastic Leaded Chip Carrier (F)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY53C256S	70/80/10		PDIP
HY53C256LS	70/80/10	L-part	PDIP
HY53C256F	70/80/10		PLCC
HY53C256LF	70/80/10	L-part	PLCC