DRAM

256K x 1 DRAM

PAGE MODE

FEATURES

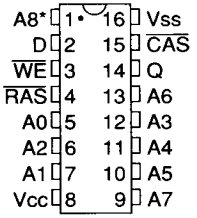
- Industry standard pinout, timing and functions
- All inputs, outputs, and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby; 150mW active, typical
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256-cycle refresh in 4ms
- Optional PAGE MODE access cycle

OPTIONS

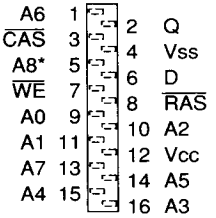
	MARKING
• Timing	
100ns access	-10
120ns access	-12
150ns access	-15
• Packages	
Plastic DIP	None
Ceramic DIP	C
Plastic ZIP	Z
PLCC	EJ

PIN ASSIGNMENT (Top View)

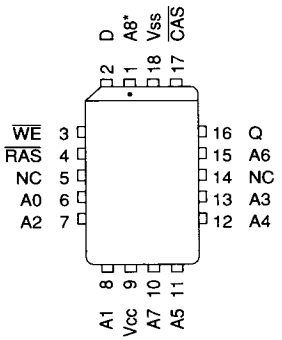
16-Pin DIP
(A-1, B-1)



16-Pin ZIP
(C-1)



18-Pin PLCC
(D-1)



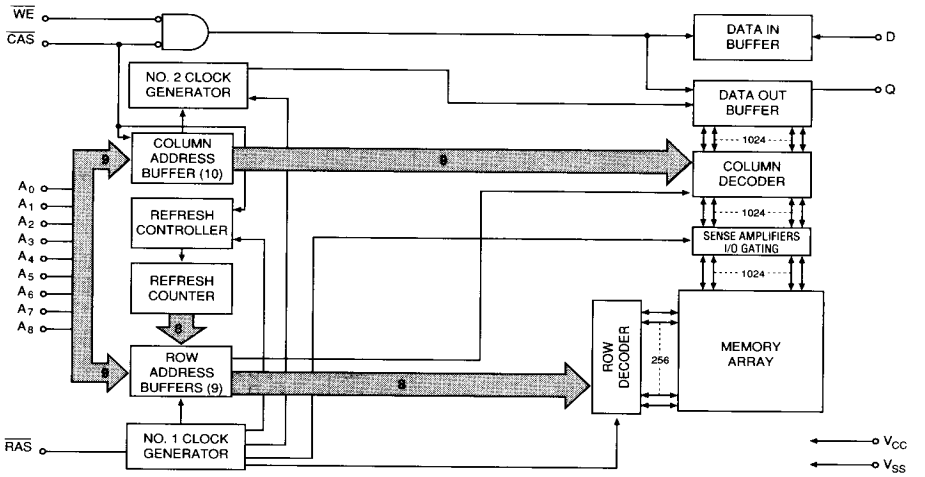
*Address not used for $\overline{RAS}$-ONLY refresh

GENERAL DESCRIPTION

The MT1259 is a randomly accessed solid-state memory containing 262,144 bits organized in a x1 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data-in (D) is latched when $\overline{WE}$ strobes LOW.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, LATE-WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (refresh) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence). Micron recommends evenly spaced refresh cycles for maximum data integrity.

FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

Function	RAS	CAS	WE	Addresses		
				tR	tC	
Standby	H	X	X	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS-ONLY REFRESH	L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A(Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 4, 6) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0V	I_I	-10	10	µA	
OUTPUT LEAKAGE Output leakage current (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low (Logic 0) Voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-10	-12	-15	UNITS	NOTES
STANDBY CURRENT: TTL input levels ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles)	I_{CC1}	5	5	5	mA	
OPERATING CURRENT: Random READ/WRITE ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC2}	55	55	45	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling: ^tPC = ^tPC (MIN))	I_{CC3}	55	55	45	mA	2
REFRESH CURRENT: $\overline{RAS}$-ONLY ($\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; ^tRC = ^tRC (MIN))	I_{CC4}	40	40	35	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling; ^tRC = ^tRC (MIN))	I_{CC5}	55	55	45	mA	2, 20

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8, D	C_{I1}		5	pF	18
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		8	pF	18
Output Capacitance: Q	C_O		7	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

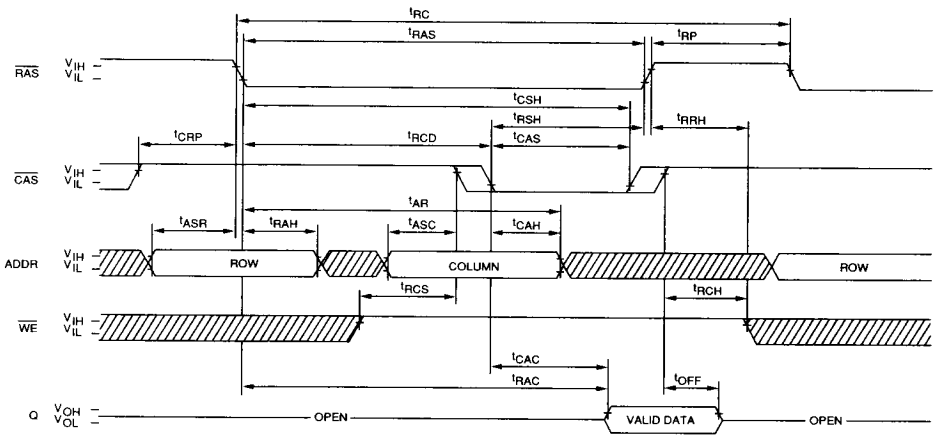
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	tRC	190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	tRWC	220		255		295		ns	
PAGE-MODE cycle time	tPC	90		100		120		ns	6, 7
Access time from $\overline{RAS}$	tRAC		100		120		150	ns	7, 8
Access time from $\overline{CAS}$	tCAC		50		60		75	ns	7, 9
$\overline{RAS}$ pulse width	tRAS	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	tRSH	50		60		75		ns	
$\overline{RAS}$ precharge time	tRP	80		90		100		ns	
$\overline{CAS}$ pulse width	tCAS	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	tCSH	100		120		150		ns	
$\overline{CAS}$ precharge time	tCPN	25		25		30		ns	19
$\overline{CAS}$ precharge time (PAGE MODE)	tCP	30		30		35		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	25	50	25	60	25	75	ns	13
$\overline{CAS}$ to $\overline{RAS}$ setup time	tCRP	15		20		20		ns	
Row address setup time	tASR	0		0		0		ns	
Row address hold time	tRAH	15		15		15		ns	
Column address setup time	tASC	0		0		0		ns	
Column address hold time	tCAH	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	70		80		100		ns	
READ command setup time	tRCS	0		0		0		ns	
READ command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	14
READ command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	
Output buffer turn-off delay	tOFF	0	30	0	30	0	35	ns	12
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	1
WRITE command hold time	tWCH	35		40		45		ns	
WRITE command hold time referenced to $\overline{RAS}$	tWCR	85		100		120		ns	
WRITE command pulse width	tWP	35		40		45		ns	
WRITE command to $\overline{RAS}$ lead time	tRWL	35		40		45		ns	
WRITE command to $\overline{CAS}$ lead time	tCWL	35		40		45		ns	
Data-in setup time	tDS	0		0		0		ns	15
Data-in hold time	tDH	35		40		45		ns	15
Data-in hold time referenced to $\overline{RAS}$	tDHR	85		100		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	tCWD	40		50		60		ns	16
$\overline{RAS}$ to $\overline{WE}$ delay	tRWD	90		110		135		ns	16
Transition time (rise or fall)	tT	3	100	3	100	3	100	ns	5, 17
Refresh period (256 cycles)	tREF		4		4		4	ms	21
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	20		25		30		ns	20
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$) refresh	tCSR	15		20		20		ns	20
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	20

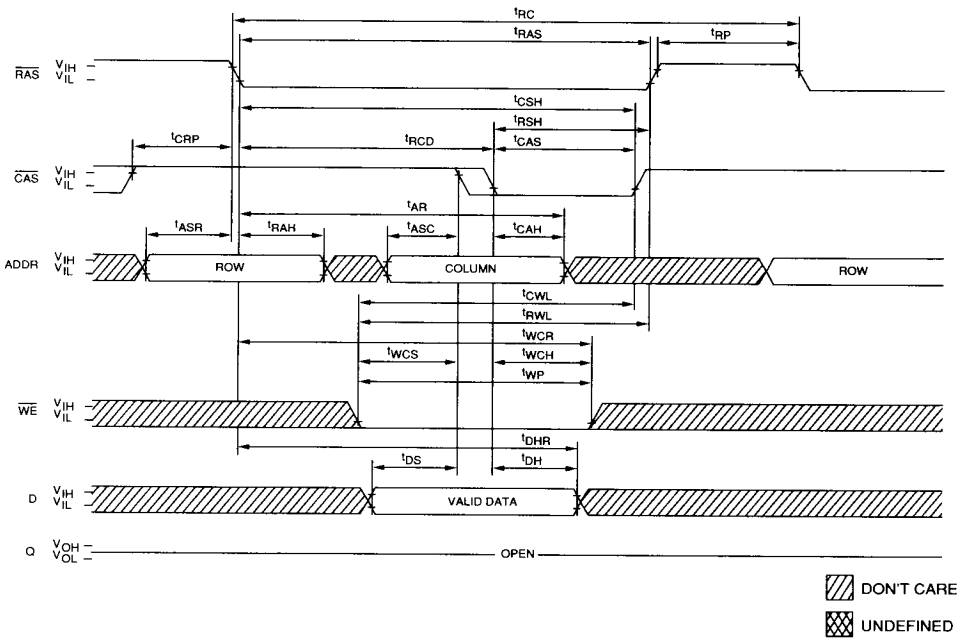
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^tT = 5ns.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
9. Assumes that $^tRCD \ge ^tRCD$ (MAX).
10. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
11. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
14. ^tRCH is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
16. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \ge ^tCWD$ (MIN) and $^tRWD \ge ^tRWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. This parameter is sampled. Capacitance is calculated from the equation $C = I\,^{dt}/_{dv}$ with dv = 3V and V_{CC} = 5V.
19. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.

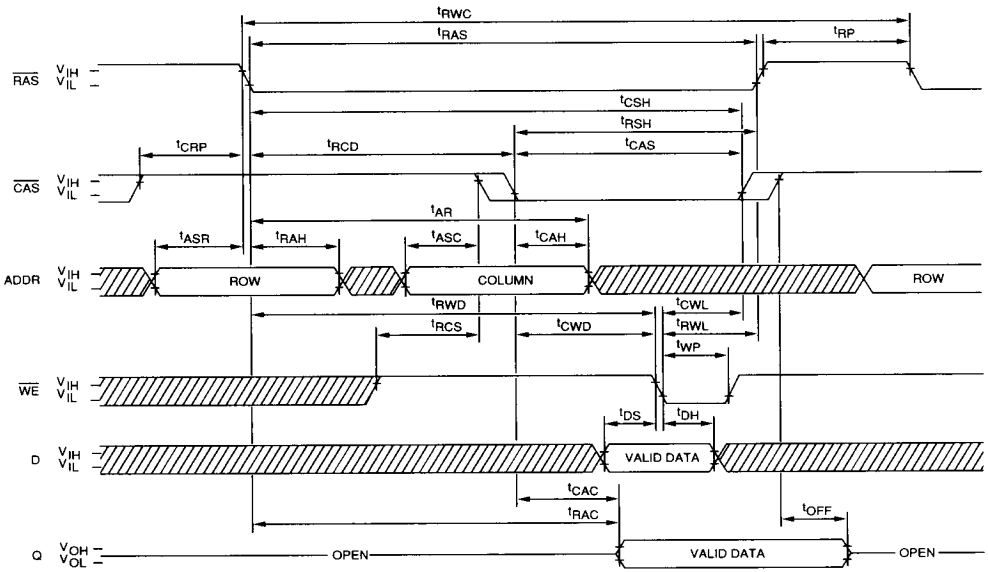
READ CYCLE



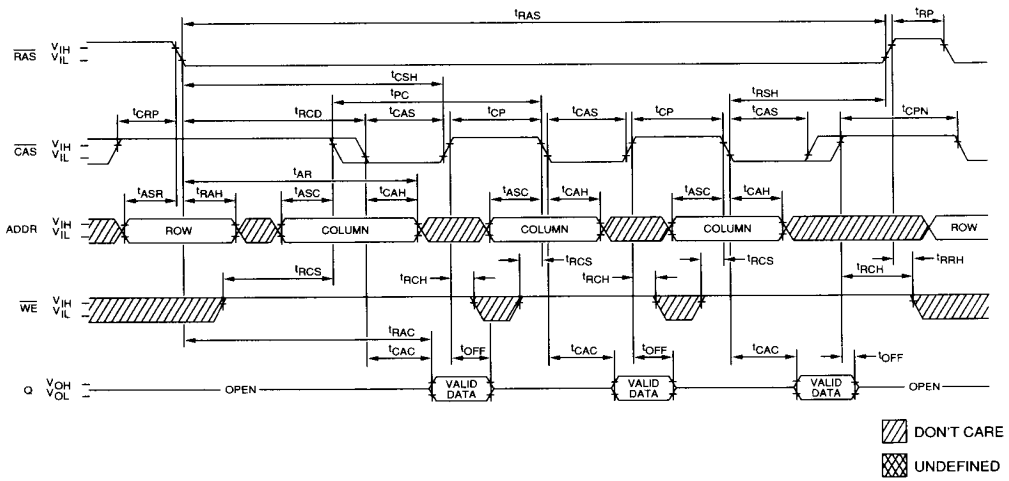
EARLY-WRITE CYCLE



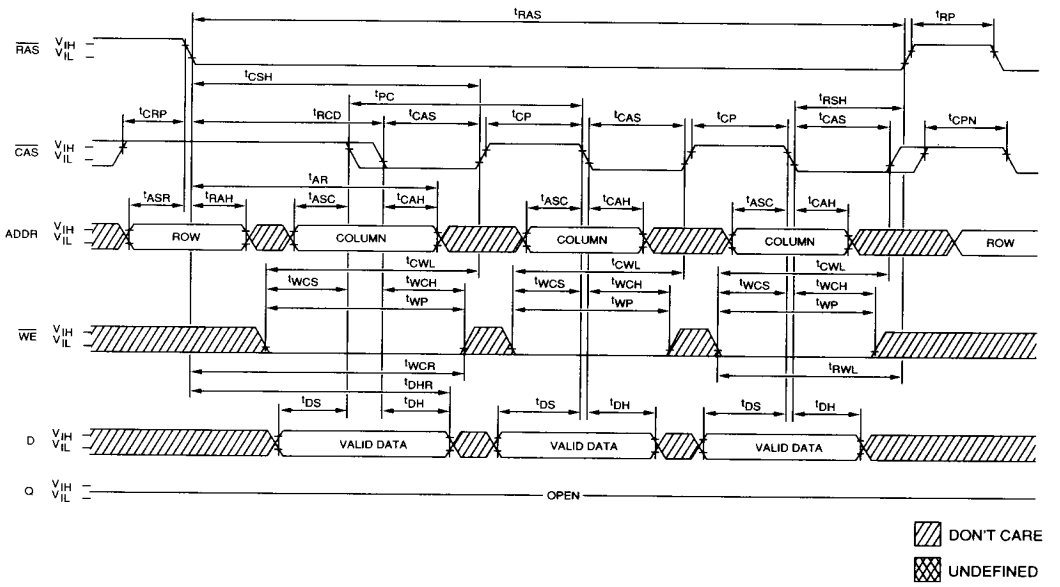
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



PAGE-MODE READ CYCLE

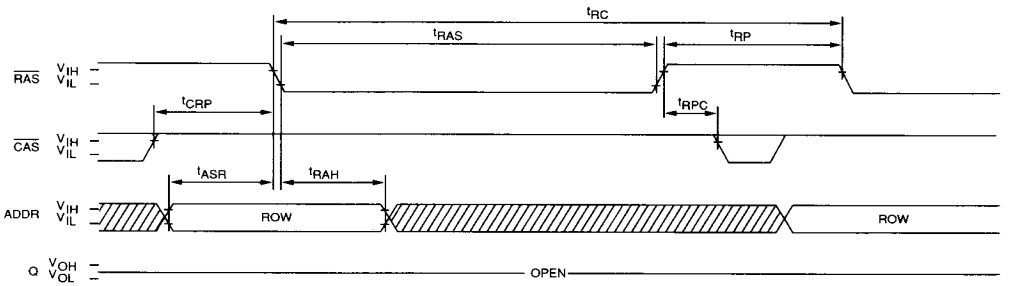


PAGE-MODE EARLY-WRITE CYCLE



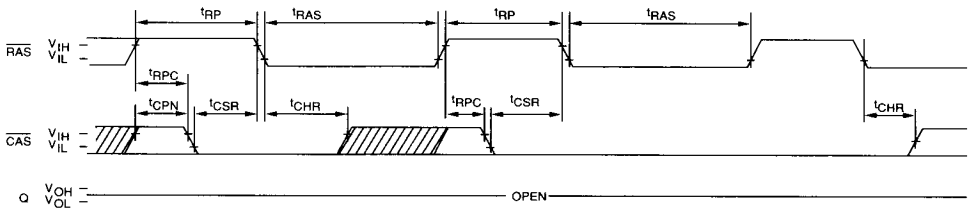
RAS-ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and WE = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE

(A_0 - A_8 and WE = DON'T CARE)



HIDDEN REFRESH CYCLE

(WE = HIGH) [21]