2164B
65,536 x 1-BIT DYNAMIC RAM WITH PAGE MODE

- **Performance Range**

	t_{RAC}	t_{CAC}	t_{RC}
2164B-12	120 ns	60 ns	220 ns
2164B-15	150 ns	75 ns	260 ns

- **Page Mode Capability**
- **Single +5V ±10% Power Supply**
- **Common I/O Using Early Write**
- **TTL Compatible Inputs and Output**
- **Schmitt Triggers on all Input Control Lines**
- **$\overline{RAS}$-Only and Hidden Refresh Capability**
- **128 Cycle/2 ms Refresh**
- **JEDEC Standard Pinout in 16-Pin DIP**

The 2164B is a fully decoded NMOS dynamic random access memory organized as 65,536 one-bit words. The design is optimized for high speed, high performance applications such as computer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The 2164B features page mode which allows high speed random access of up to 256-bits within the same row. Multiplexed row and column address inputs permit the 2164B to be housed in a standard 16-pin DIP.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

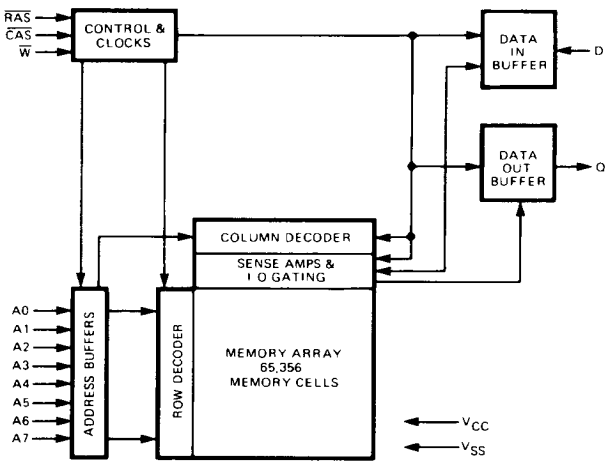


Figure 1. Functional Block Diagram

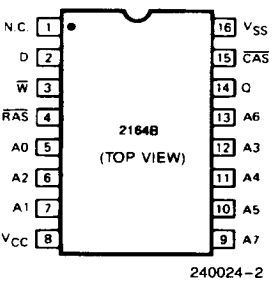


Figure 2. Pin Configuration

PIN NAMES

A_0–A_7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

45 Res Only
004971
4971 TTL

August 1987
Order Number: 240024-001

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin
Relative to V_{SS} ..... −2.0V to +7.0V
Voltage on V_{CC} Supply
Relative to V_{SS} ..... −1V to +7.5V
Storage Temperature ..... −65°C to +150°C
Power Dissipation 1.0W
Short Circuit Output Current ..... 50 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS Voltages referenced to V_{SS}, T_A = 0 to 70°C

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4		V_{CC} + 1	V
V_{IL}	Input Low Voltage	−2.0		0.8	V

D.C. AND OPERATING CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

Symbol	Parameter		Min	Max	Units	Test Conditions
I_{CC1}	Operating Current*	2164B-12 2164B-15		50 45	mA mA	$\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = Min.
I_{CC2}	Standby Current			4	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ Cycles Min.
I_{CC3}	$\overline{RAS}$-Only Refresh Current*	2164B-12 2164B-15		40 35	mA mA	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC} = Min.
I_{CC4}	Page Mode Current*	2164B-12 2164B-15		35 30	mA mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = Min.
I_{IL}	Input Leakage Current		−10	10	μA	Any Input 0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, All Other Pins Not under Test
I_{OL}	Output Leakage Current		−10	10	μA	Data Out is Disabled, 0 ≤ V_{OUT} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V
V_{OH}	Output High Voltage Level		2.4		V	I_{OH} = 5 mA
V_{OL}	Output Low Voltage Level			0.4	V	I_{OL} = 4.2 mA

***NOTE:**
I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE T_A = 25°C

Symbol	Parameter	Min	Max	Units
C_{IN1}	Input Capacitance (A_0–A_7, D)		5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)		7	pF
C_{OUT}	Output Capacitance (Q)		6	pF

A.C. CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See Notes 1, 2.

Symbol	Parameter	2164B-12		2164B-15		Units
		Min	Max	Min	Max	
t_{RC}	Random Read or Write Cycle Time			260		ns
t_{RWC}	Read-Modify-Write Cycle Time	255		300		ns
t_{RAC}(3, 4)	Access Time from $\overline{RAS}$		120		150	ns
t_{CAC}(3, 5)	Access Time from $\overline{CAS}$		60		75	ns
t_{OFF}(6)	Output Buffer Turn-Off Delay	0	30	0	35	ns
t_T	Transition Time (Rise and Fall)	3	100	3	100	ns
t_{RP}	$\overline{RAS}$ Precharge Time	90		100		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	ns
t_{RSH}	$\overline{RAS}$ Hold Time	60		75		ns
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	ns
t_{CSH}	$\overline{CAS}$ Hold Time	120		150		ns
t_{RCD}(4)	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		ns
t_{ASR}	Row Address Set-Up Time	0		0		ns
t_{RAH}	Row Address Hold Time	18		20		ns
t_{ASC}	Column Address Set-Up Time	0		0		ns
t_{CAH}	Column Address Hold Time	30		35		ns
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	90		110		ns
t_{RCS}	Read Command Set-Up Time	0		0		ns
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		ns
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		ns
$_S$(7)	Write Command Set-Up Time	0		0		ns
t_{WCH}	Write Command Hold Time	35		45		ns
t_{WP}	Write Command Pulse Width	35		45		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35		45		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35		45		ns
t_{DS}	Data-In Set-Up Time	0		0		ns
t_{DH}	Data-In Hold Time	35		40		ns
t_{CWD}(7)	$\overline{CAS}$ to Write Enable Delay	55		65		ns
t_{RWD}(7)	$\overline{RAS}$ to Write Enable Delay	115		140		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		115		ns
t_{PC}	Page Mode Cycle Time	120		145		ns
t_{CP}	$\overline{CAS}$ Precharge Time (Page Mode Only)	45		60		ns

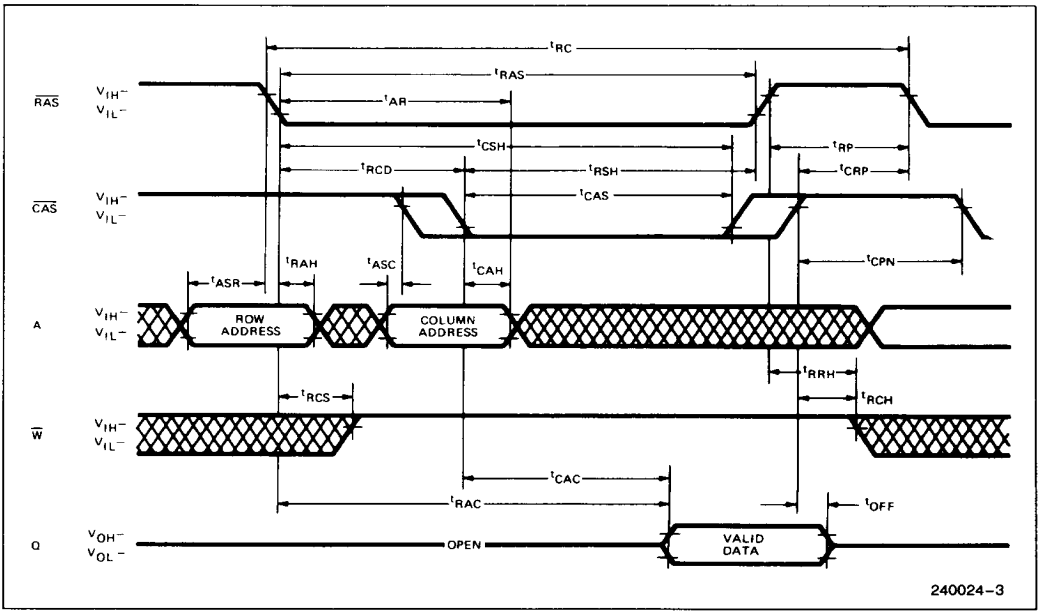
A.C. CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See Notes 1, 2. (Continued)

Symbol	Parameter	2164B-12		2164B-15		Units
		Min	Max	Min	Max	
t_{CPN}	$\overline{CAS}$ Precharge Time (All Cycles Except Page Mode)	25		30		ns
t_{REF}	Refresh Period		2		2	ms

NOTES:
1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5 ns for all inputs.
3. Measured with a load equivalent to a 2 TTL loads and 100 pF.
4. Operation within the T_{RCD}(max) limit insures that T_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by T_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{CWD} and t_{RWD} are restrictive operating parameters for the read-modify-write cycle only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a late write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

TIMING DIAGRAMS

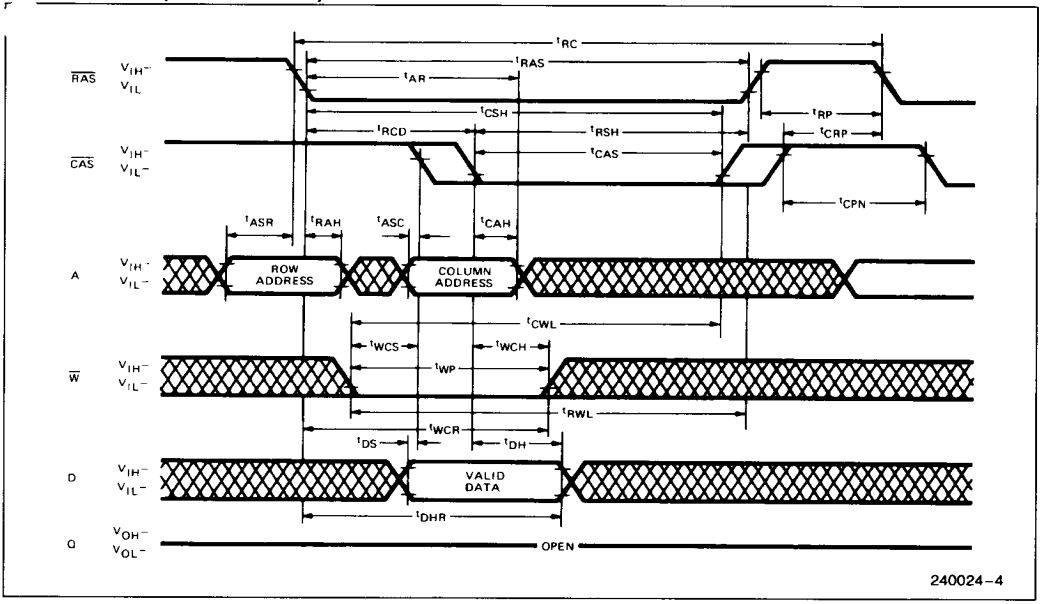
READ CYCLE



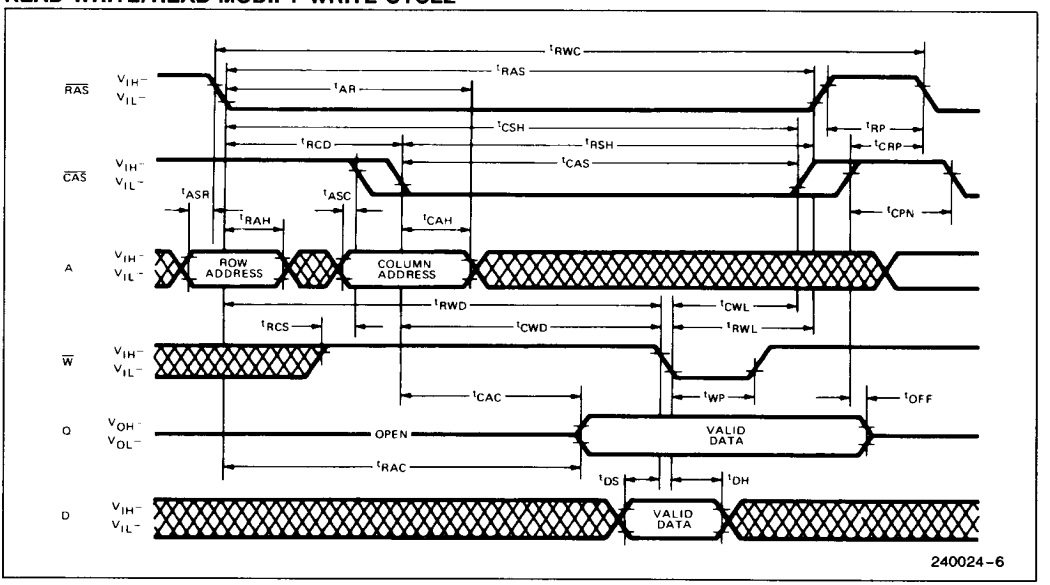
DON'T CARE

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



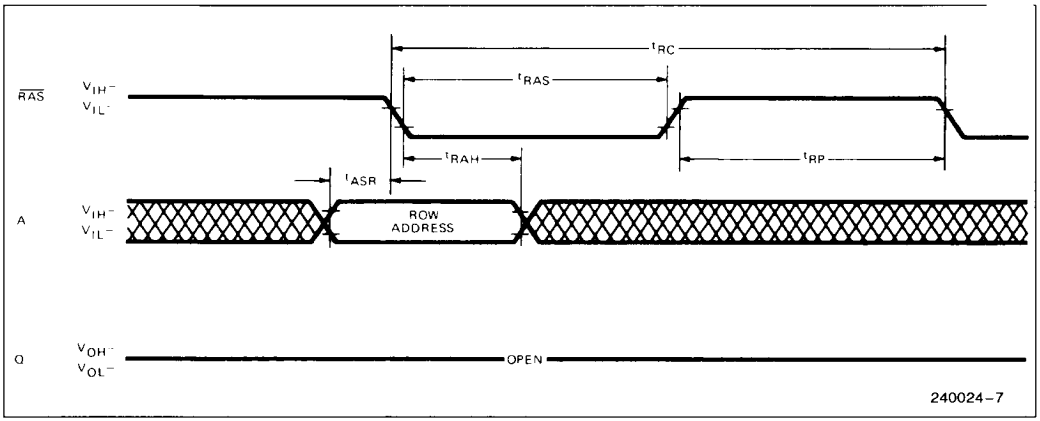
READ-WRITE/READ-MODIFY-WRITE CYCLE



DON'T CARE

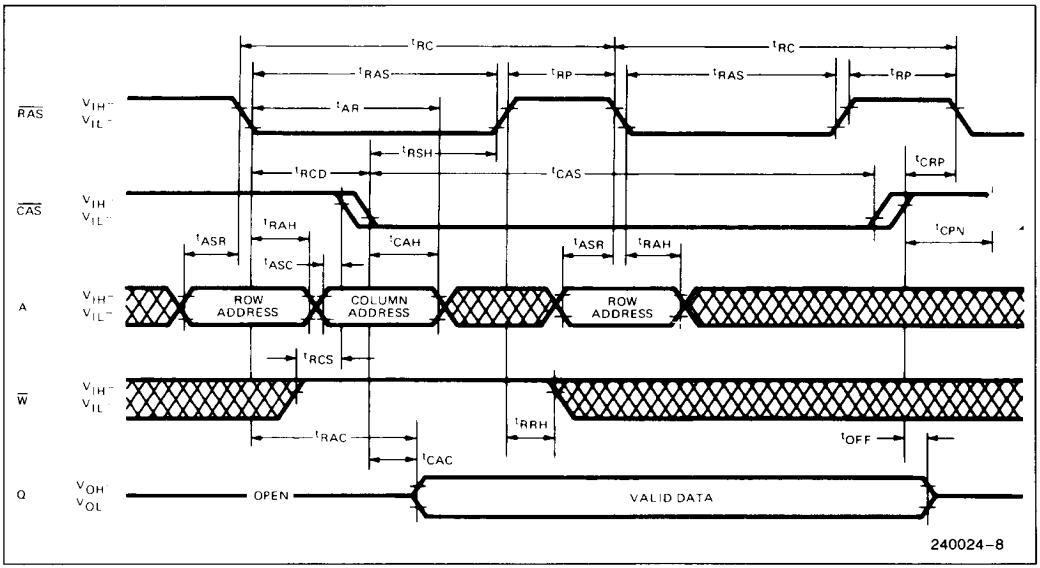
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE



NOTE:
$\overline{CAS}$ = V_{IH}, $\overline{W}$, D = Don't care

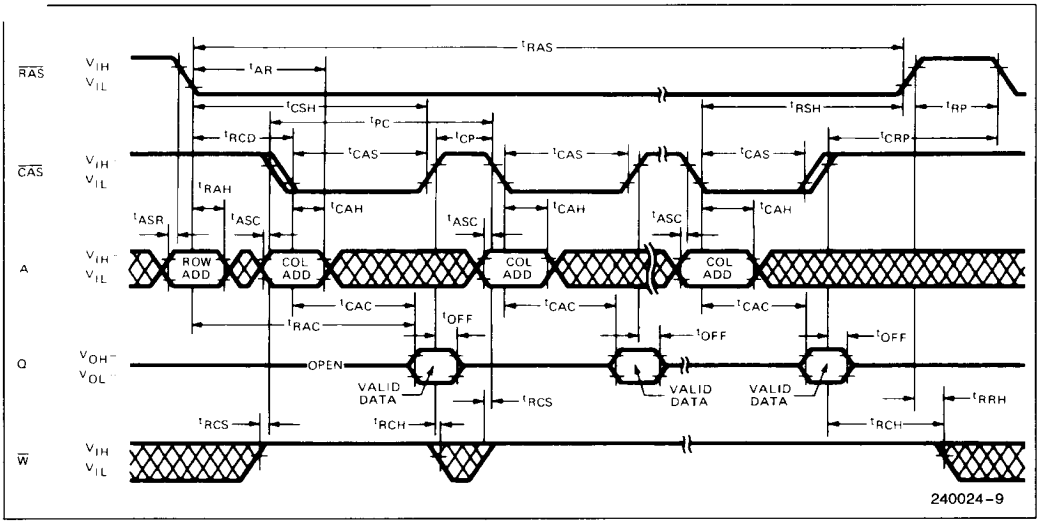
HIDDEN REFRESH CYCLE



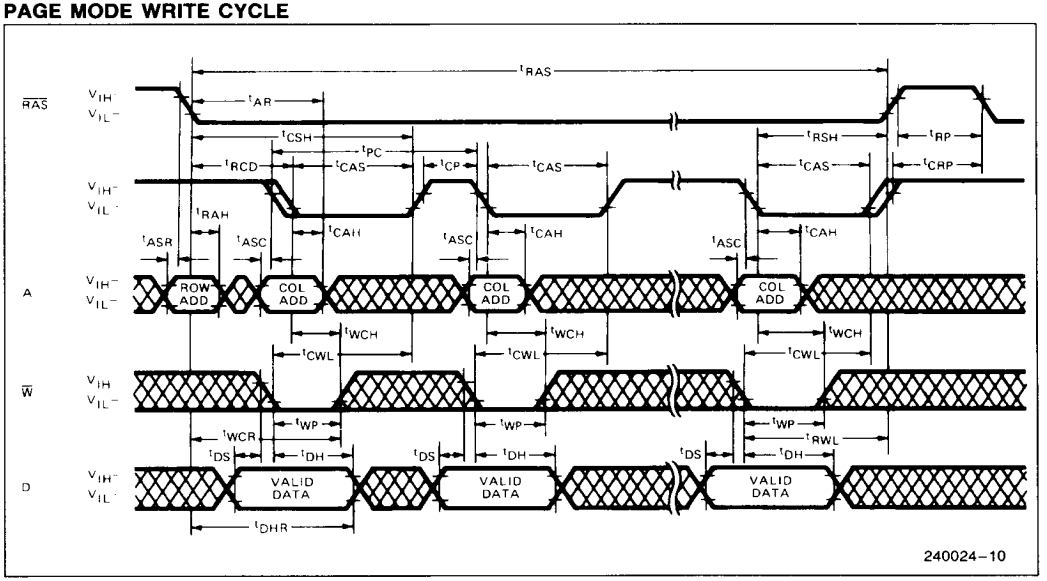
DON'T CARE

TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DON'T CARE

DEVICE OPERATION

The 2164B contains 65,536 memory locations. Sixteen address bits are required to address a particular memory location. Since the 2164B has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the 2164B begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any 2164B cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the 2164B begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The output of the 2164B remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The 2164B can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The 2164B has a tri-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write).

Whenever $\overline{CAS}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the 2164B operating cycles are listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode write, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the 2164B is stored on a tiny capacitor in each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 2 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and strobing in a refresh row address with $\overline{RAS}$.

Other Refresh Methods: It is also possible to refresh the 2164B by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only refresh is the preferred method.

Page Mode

Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS}$ = V_{SS} during power-up the 2164B might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100 μs is required after power-up followed by 8 initialized cycles before proper device operation is assured. Eight initialization cycles are also required after any 2 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the 2164B inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the 2164B input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20Ω to 40Ω.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMs. The impedance is minimized if all the power supply traces to all the DRAMs run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

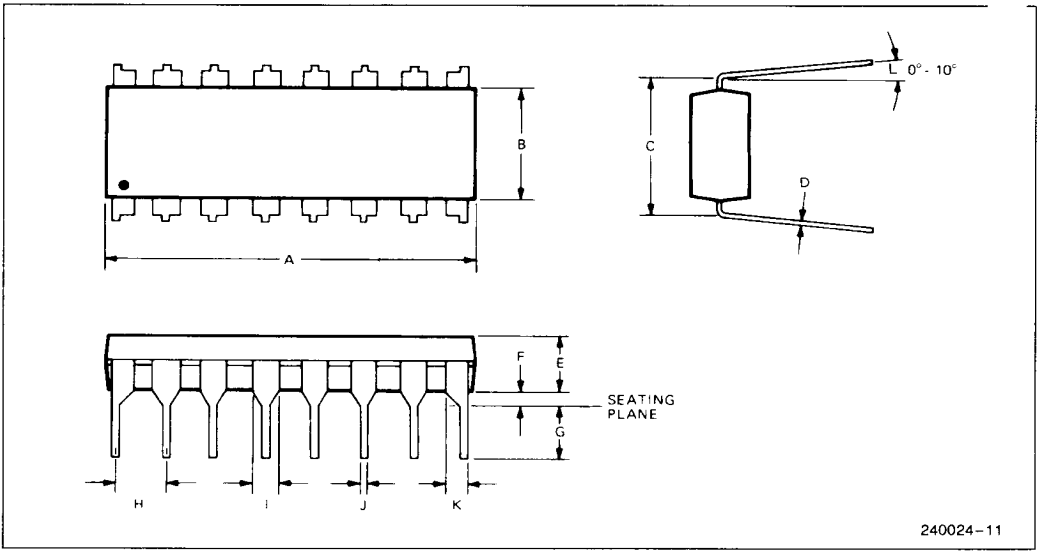
The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500 mv.

A high frequency 0.1 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each 2164B using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the 2164B and they supply much of the current used by the 2164B during cycling.

In addition, a large tantalum capacitor with a value of 47 μF to 100 μF should be used for bulk decoupling to recharge the 0.1 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE



Item	Millimeters	Inches
A	19.43 ±0.25	0.765 ±0.01
B	6.86 ±0.25	0.270 ±0.01
C	7.62 ±0.25	0.300 ±0.01
D	0.28 ±0.05	0.011 ±0.002
E	3.56 ±0.12	0.140 ±0.005
F	0.506 ±0.10	0.020 ±0.004
G	3.43 ±0.38	0.135 ±0.015
H	2.54 ±0.25	0.100 ±0.010
I	1.52 ±0.25	0.060 ±0.010
J	0.457 ±0.05	0.018 ± 0.002
K	0.94 ±0.25	0.037 ±0.010
L	5° ±5°	5° ±5°