51C64L
LOW POWER 64K X 1
CHMOS DYNAMIC RAM

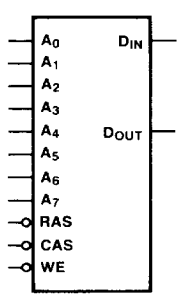
	51C64L-10	51C64L-12
Maximum Access Time (ns)	100	120
Maximum CHMOS Standby Current (mA)	0.05	0.05

- **Low Power Data Retention**
  - **Standby current, CHMOS — 50μA (max.)**
  - **Refresh period, $\overline{RAS}$-Only — 64 ms (max.)**
  - **Data retention current — 80μA (max.)**
- **Low Operating Current — 35mA (max.)**
- **Fully TTL Compatible Inputs and Outputs**
- **Low Input/Output Capacitance**
- **High Reliability Plastic — 16 Pin DIP**

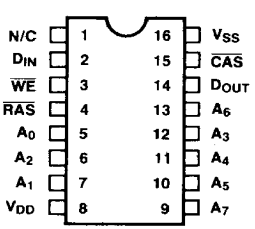
The Intel® 51C64L is a low power 65,536 x 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C64L offers features not provided by an NMOS dynamic RAM: CHMOS standby current and extended $\overline{RAS}$-Only refresh for low data retention power. All inputs and outputs are fully TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

The 51C64L offers a maximum standby current of 50 μA when $\overline{RAS} \geq V_{DD}$-0.5V. During standby (i.e. refresh only cycles) the refresh period can be extended to 64 ms to reduce the total current required for data retention to less than 80 μA (max). The 51C64L combines low power with high density for portable and battery backup applications.

LOGIC SYMBOL



PIN CONFIGURATION



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_7	ADDRESS INPUTS
D_{IN}	DATA IN
D_{OUT}	DATA OUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

June 1984
Order Number: 280025-001

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . Plastic -55°C to +125°C
Voltage on Any Pin except V_{DD} and D_{OUT} Relative to V_{SS} . . . . . -2.0V to 7.5V
Voltage on V_{DD} Relative to V_{SS} . . . . . -1.0V to 7.5V
Voltage on D_{OUT} Relative to V_{SS} . . . . . -2.0V to V_{DD} + 1V
Data Out Current . . . . . 50 mA
Power Dissipation 1.0W

†COMMENT:
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	51C64L			Unit	Test Conditions	Notes
		Min.	Typ.[2]	Max.			
I_{DD1}	V_{DD} Supply Current, Operating		27	37	mA	$t_{RC} = t_{RC}$ (min), for −10 specification	3,4
			23	35	mA	$t_{RC} = t_{RC}$ (min), for −12 specification	
I_{DD2}	V_{DD} Supply Current, TTL Standby		0.7	2	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, all other inputs and output ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh		24	37	mA	$t_{RC} = t_{RC}$ (min), for −10 specification	4
			20	35	mA	$t_{RC} = t_{RC}$ (min), for −12 specification	
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		3	4	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IL}, all other inputs and output ≥ V_{SS}	3
I_{DD6}	V_{DD} Supply Current, CHMOS Standby		0.008	0.05	mA	$\overline{RAS} \geq V_{DD} - 0.5V$ and $\overline{CAS}$ at V_{IH}, all other inputs and output ≥ V_{SS}	
$\|I_{LI}\|$	Input Load Current (any pin)			1	μA	$V_{IN} = V_{SS}$ to V_{DD}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			1	μA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, $D_{OUT} = V_{SS}$ to V_{DD}	
V_{IL}	Input Low Voltage (all inputs)	−1.0		0.8	V		5
V_{IH}	Input High Voltage (all inputs)	2.4		V_{DD} + 1	V		5
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 4.2$ mA	6
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -5$ mA	6

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are at $T_A = 25°C$ and $V_{DD} = +5V$.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Address, D_{IN}	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	4	5	pF
C_{OUT}	D_{OUT}	4	6	pF

†NOTE:
Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

A.C. CHARACTERISTICS[1, 2, 3]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

#	JEDEC Symbol	Symbol	Parameter	51C64L-10		51C64L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	160		190		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	100		120		ns	
5	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		ns	
6	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		ns	
7	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		15		ns	
8	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		ns	
9	t_{RL1CL2}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	30	80	35	95	ns	4
10	t_{AVCL2}	t_{ASC}	Column Address Set-up Time	0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10		15		ns	
12	t_{RL1AX}	t_{AR}	Column Address Hold Time From $\overline{RAS}$	40		50		ns	
	t_{RVRV}	$t_{REF\,1}$	Time Between Refresh		4		4	ms	5
	t_{RVRV}	$t_{REF\,2}$	Time Between Refresh ($\overline{RAS}$-Only)		64		64	ms	5
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	6
13	t_{CL1QX}	t_{ON}	Output Buffer Turn On Delay	0	20	0	25	ns	
14	t_{CH2QZ}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	25	ns	

NOTES:

1. All voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).
3. A.C. Characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, V_{IL} (min) $\geq V_{SS}$ and V_{IH} (max) $\leq V_{DD}$.
4. t_{RCD} (max) is specified for reference only.
5. The 51C64L extends the refresh period to 64 ms during $\overline{RAS}$-Only refresh operation.
6. t_T is measured between V_{IH} (min) and V_{IL} (max).

A.C. CHARACTERISTICS (Con't.)

Read Cycle

#	JEDEC Symbol	Symbol	Parameter	51C64L-10		51C64L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
15	t_{RL1QV}	t_{RAC}	Access Time From $\overline{RAS}$		100		120	ns	7
16	t_{CL1QV}	t_{CAC}	Access Time From $\overline{CAS}$		20		25	ns	8,9
17	t_{AVQV}	t_{CAA}	Access Time From Column Address		55		65	ns	9
18	$t_{CL1CH1(R)}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width (Read Cycle)	20	75000	25	75000	ns	
19	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		ns	
20	t_{WH2CL2}	t_{RCS}	Read Command Set-up Time	0		0		ns	
21	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	55		65		ns	
22	t_{CH2WX}	t_{RCH}	Read Com. Hold Time Ref. to $\overline{CAS}$	0		0		ns	10
23	t_{RH2WX}	t_{RRH}	Read Com. Hold Time Ref. to $\overline{RAS}$	10		10		ns	10

Write Cycle

#	JEDEC Symbol	Symbol	Parameter	51C64L-10		51C64L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
24	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	35		40		ns	
25	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width (Write Cycle)	30	75000	35	75000	ns	
26	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		ns	
27	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35		ns	
28	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	20		25		ns	
29	t_{WL1CL2}	t_{WCS}	Write Command Set-up Time	0		0		ns	11
30	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	30		35		ns	
31	t_{DVCL2}	t_{DS}	Data-In Set-up Time	0		0		ns	
32	t_{CL1DX}	t_{DH}	Data-In Hold Time	20		25		ns	

NOTES:

7. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If $t_{RCD} > t_{RCD}$ (max) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).
8. Assumes $t_{RCD} \geq t_{RCD}$ (max).
9. If $t_{ASC} < (t_{CAA}$ (max) - t_{CAC} (max) - $t_T)$, then access time is defined by t_{CAA} rather than by t_{CAC}.
10. Either t_{RCH} or t_{RRH} must be satisfied.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the date out pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

A.C. CHARACTERISTICS (Con't.)

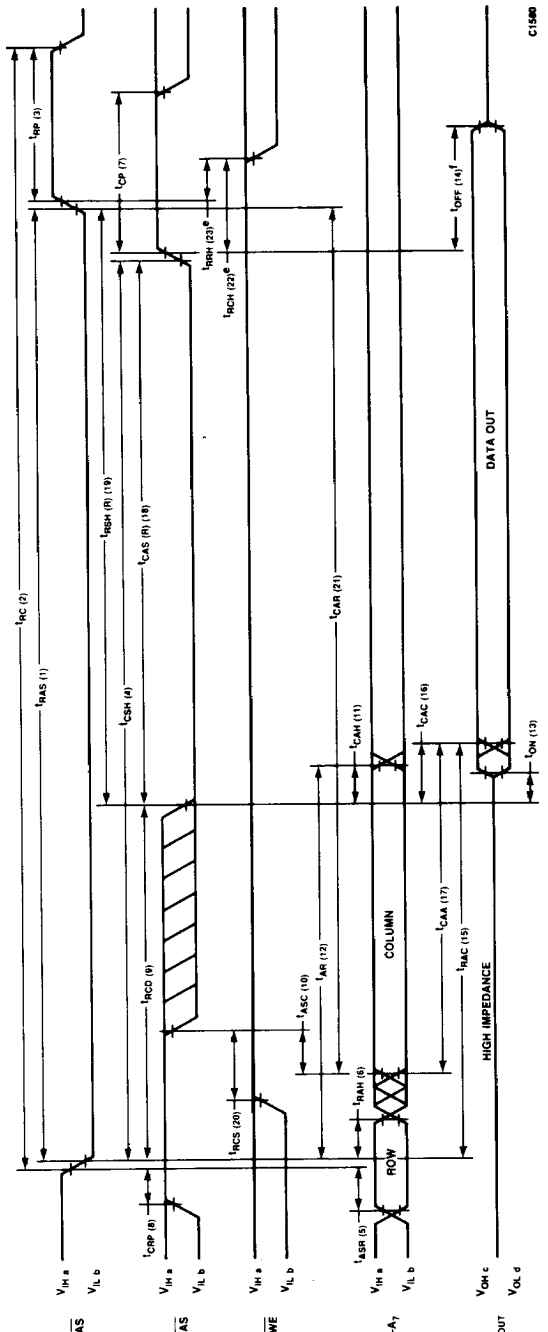
Read-Modify-Write Cycle 12

#	JEDEC Symbol	Symbol	Parameter	51C64L-10		51C64L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
33	$t_{RL2RL2(RMW)}$	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	195		230		ns	
34	$t_{RL1RH1(RMW)}$	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	135	75000	160	75000	ns	
35	$t_{CL1CH1(RMW)}$	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	55	75000	65	75000	ns	
36	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		ns	13
37	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20		25		ns	13
38	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	55		65		ns	13

NOTES:

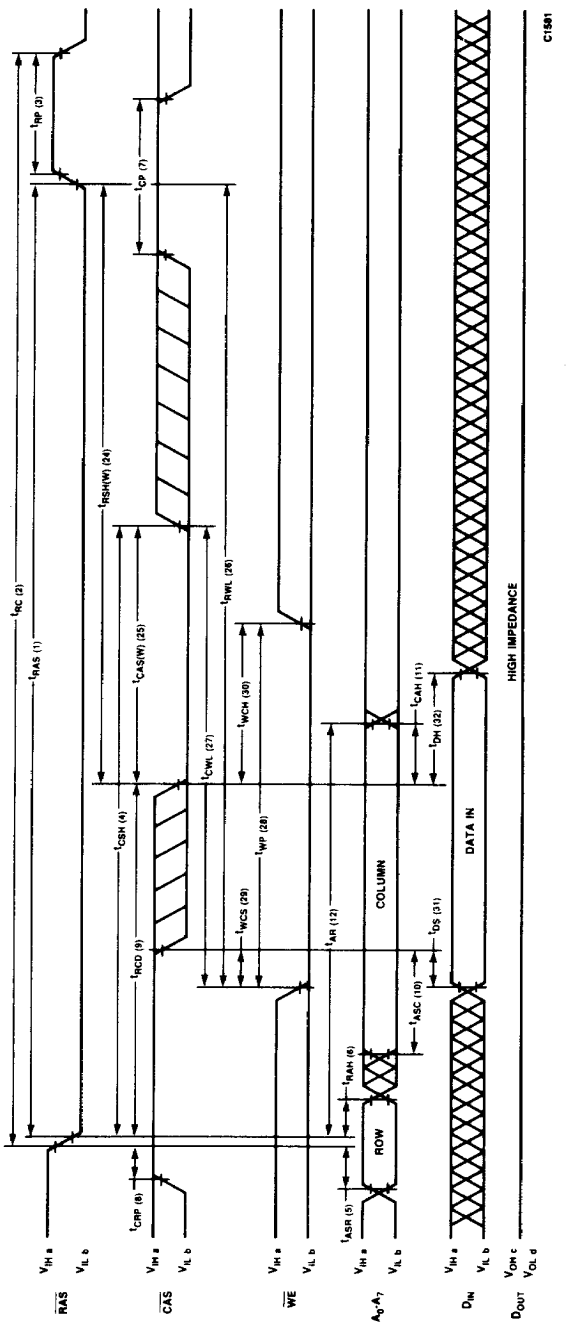
12. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data out pin will remain in high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.

WAVEFORMS
Read Cycle



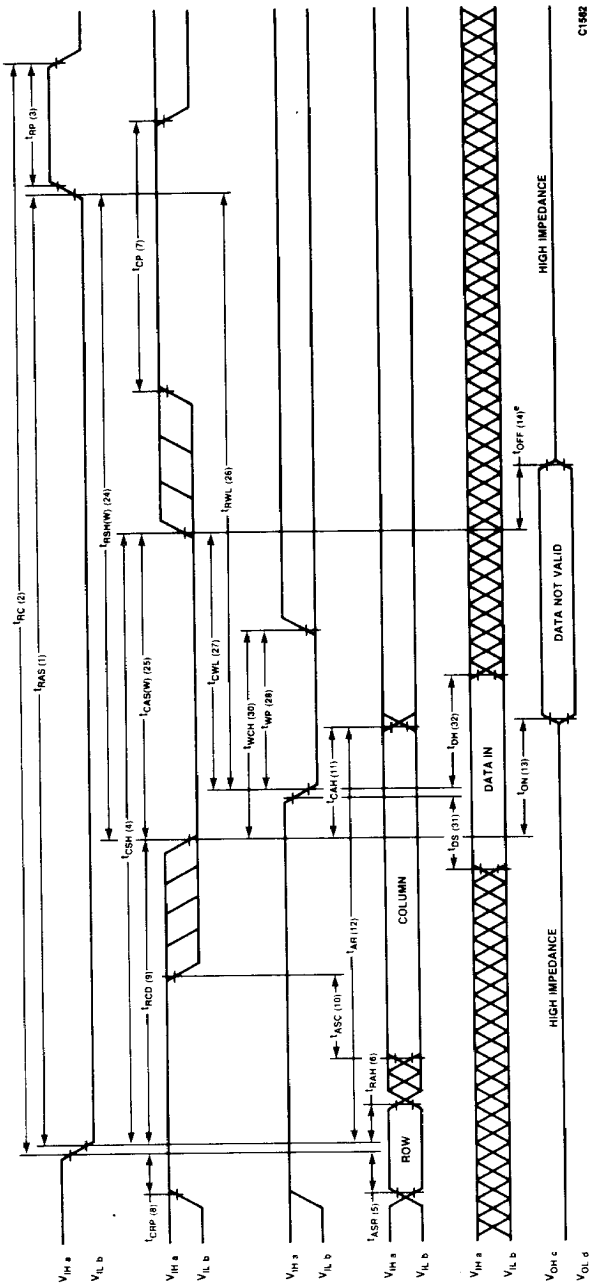
NOTES:
a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. Either t_{RCH} or t_{RRH} must be satisfied.
f. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

WAVEFORMS (Cont.)
Write Cycle ($\overline{CAS}$ Controlled)[e]



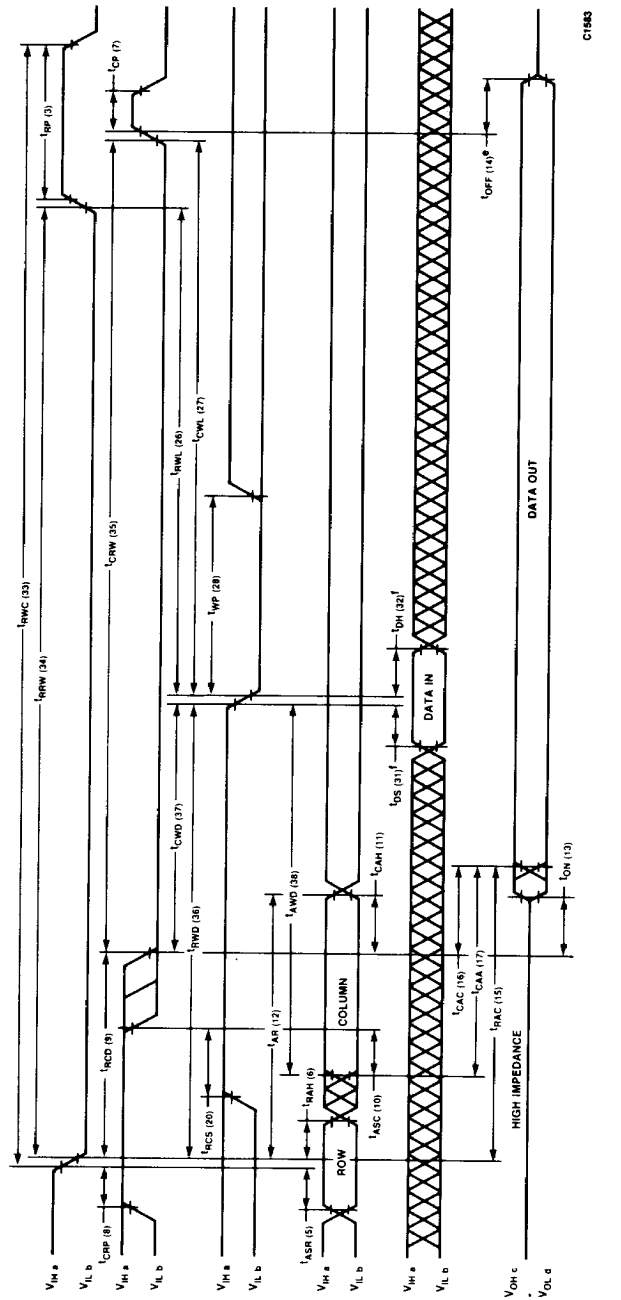
NOTES:
a., **b.** V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c., **d.** V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ latches column address and data-in.

WAVEFORMS (Cont.)
Write Cycle ($\overline{WE}$ Controlled)[f]



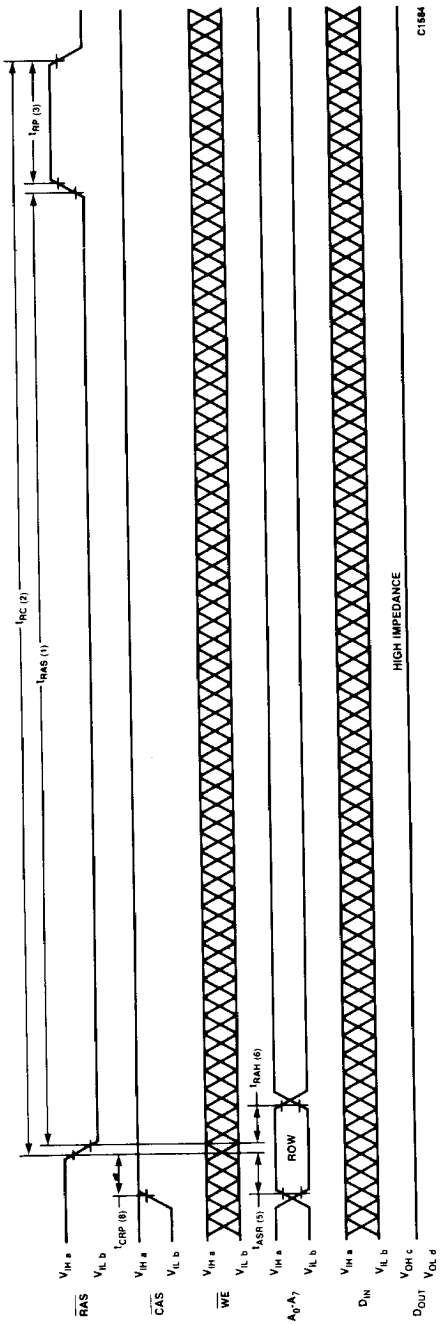
NOTES:
a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition. $\overline{CAS}$ latches the column address while $\overline{WE}$ latches the data-in.

WAVEFORMS (Cont.)
Read/Modify/Write Cycle



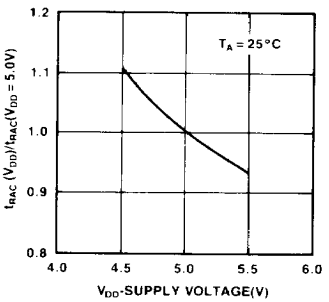
NOTES:
a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.
f. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

WAVEFORMS (Cont.)
RAS-Only Refresh Cycle

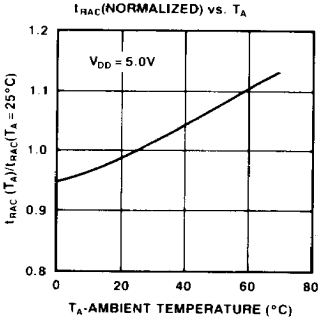


NOTES:
a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

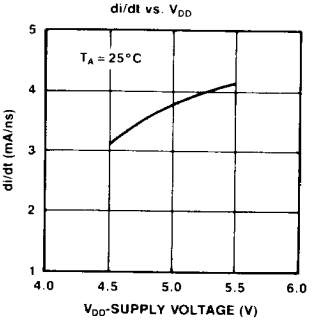
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) vs. V_{DD}



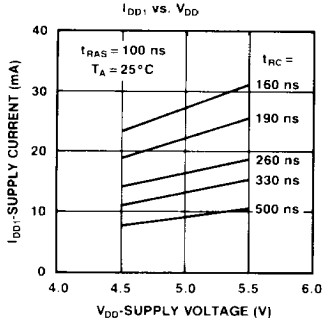
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC}(NORMALIZED) vs. T_A



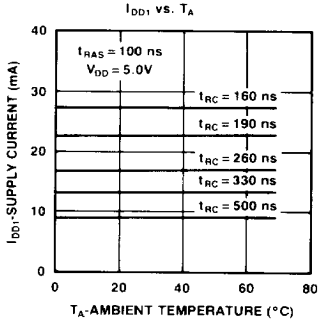
GRAPH 3
TYPICAL CURRENT TRANSIENTS
di/dt vs. V_{DD}



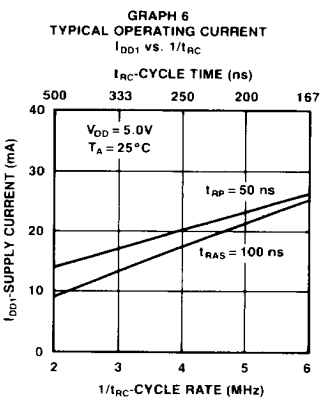
GRAPH 4
TYPICAL OPERATING CURRENT
I_{DD1} vs. V_{DD}



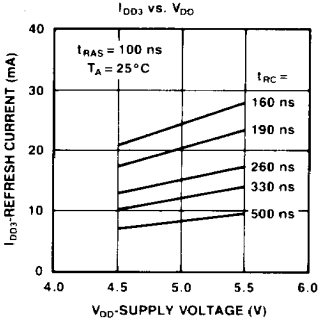
GRAPH 5
TYPICAL OPERATING CURRENT
I_{DD1} vs. T_A



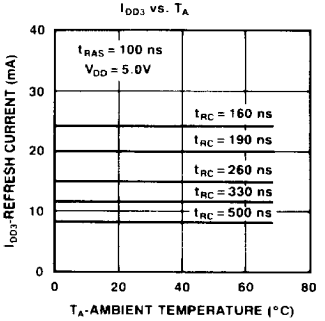
GRAPH 6
TYPICAL OPERATING CURRENT
I_{DD1} vs. $1/t_{RC}$



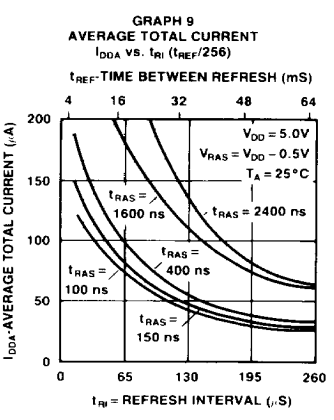
GRAPH 7
TYPICAL REFRESH CURRENT
I_{DD3} vs. V_{DD}



GRAPH 8
TYPICAL REFRESH CURRENT
I_{DD3} vs. T_A



GRAPH 9
AVERAGE TOTAL CURRENT
I_{DDA} vs. t_{RI} (t_{REF}/256)



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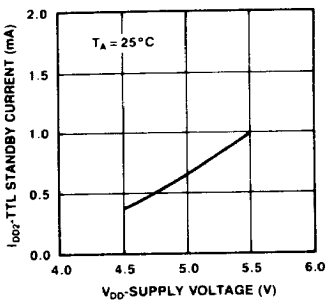
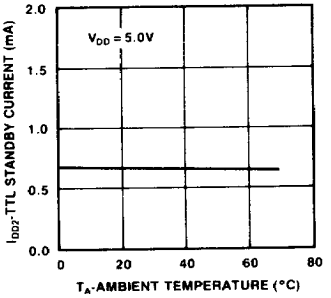
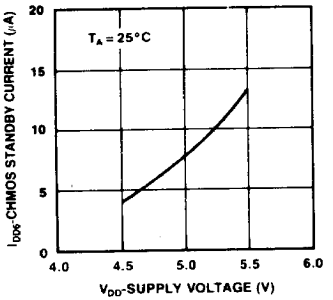
GRAPH 10
TYPICAL TTL STANDBY CURRENT
I_{DD2} vs. V_{DD}



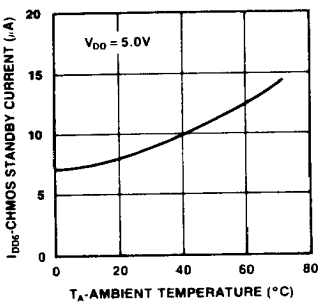
GRAPH 11
TYPICAL TTL STANDBY CURRENT
I_{DD2} vs. T_A



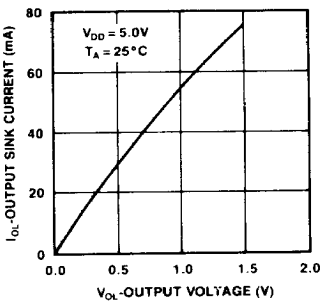
GRAPH 12
TYPICAL CHMOS STANDBY CURRENT
I_{DD6} vs. V_{DD}



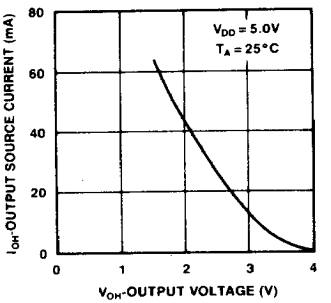
GRAPH 13
TYPICAL CHMOS STANDBY CURRENT
I_{DD6} vs. T_A



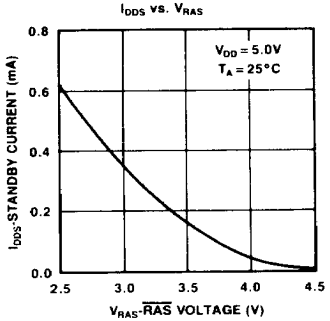
GRAPH 14
TYPICAL OUTPUT SINK CURRENT
I_{OL} vs. V_{OL}



GRAPH 15
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} vs. V_{OH}



GRAPH 16
AVERAGE STANDBY CURRENT
RELATIVE TO $\overline{RAS}$ VOLTAGE
I_{DDS} vs. V_{RAS}



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FUNCTIONAL DESCRIPTIONS

The 51C64L is a CHMOS dynamic RAM optimized for low power applications. The functionality is similar to a traditional dynamic RAM. The 51C64L reads and writes data by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent upon a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

Memory Cycle

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} and t_{CP}, has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out becomes valid only when t_{RAC}, t_{CAA}, and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

Write Cycle

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched in by $\overline{CAS}$. The write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the later of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the output (D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ will maintain the output in the high impedance state; terminating with $\overline{WE}$ allows the output to go active.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only cycle will perform refresh.

Extended Refresh Cycle

The 51C64L extends the refresh cycle period to 64 milliseconds for $\overline{RAS}$-Only refresh cycles. This feature reduces the total current consumption to a maximum of 80 micro Amperes, and typically 15 micro Amperes, for data retention ($\overline{RAS}$-Only refresh operation for the 51C64L-12). The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC}\, I_{ACTIVE}) + (t_{RI} - t_{RC})\,(I_{STANDBY})}{t_{RI}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time or $t_{REF}/256$

Before entering or leaving an extended refresh period, the entire array must be refreshed at the normal interval of four milliseconds. This can be accomplished by either a burst or distributed refresh.

Data Out Operation

The 51C64L Data Output (D_{OUT}, which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}), the output is in the high impedance state. Table 1 summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles

Table 1. Intel 51C64L Data Output Operation for Various Types of Cycles

Type of Cycle	Data Out State
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Only Cycle	High Impedance

containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).

The V_{DD} current (I_{DD}) requirement of the 51C64L during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ = V_{ss} during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

Soft Error Rate

Soft errors are random, non-recurring changes in memory logic states caused by the impact of an ionizing particle, such as an alpha particle. For example, a logic "0" may change to a logic "1". The average soft error rate (SER) of the 51C64L is less than 10 FITs. This is determined by accelerated testing using an alpha particle source and is subsequently confirmed by system testing. Ther SER is a function of the operating voltage, cycle time, package, and the alpha particle source. Intel measures the SER at $V_{DD} = 4.75V$, and $t_{cycle} = 1\mu s$. A thorium source of 1.6×10^5 $\alpha/cm^2/hr$. is used because it best matches the package energy spectra.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS,* and A.P. #172, *CHMOS DRAMS in Graphics Applications.*