Personal Computer Hardware Reference Library

IBM Asynchronous Communications Adapter

6361501

IBM Asynchronous Communications Adapter

Contents

Description

The Asynchronous Communications Adapter's system control signals and voltage requirements are provided through a 2- by 31-position card-edge connector. Two jumper modules are provided on the adapter. One jumper module selects either RS-232C or current-loop operation. The other jumper module selects one of two addresses for the adapter, so two adapters may be used in one system. An additional jumper is required on connector J13 if the adapter is to be installed in expansion slot 8 of an IBM Personal Computer XT or IBM Portable Personal Computer (see "Selecting the Interface Format and Adapter Address" in this section).

The adapter is fully programmable and supports asynchronous communications only. It will add and remove start bits, stop bits, and parity bits. A programmable baud-rate generator allows operation from 50 baud to 9600 baud. Five-, six-, seven-, or eight-bit characters with 1, 1-1/2, or 2 stop bits are supported. A fully prioritized interrupt system controls transmit, receive, error, line status, and data set interrupts. Diagnostic capabilities provide loopback functions of transmit/receive and input/output signals.

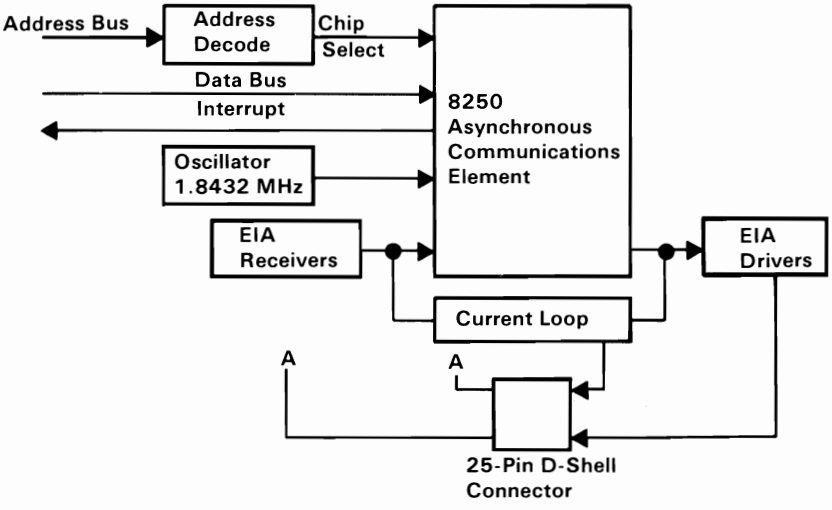
The major component of the adapter is an INS8250 LSI chip or functional equivalent. Features in addition to those listed above are:

- Full double buffering eliminating the need for precise synchronization
- Independent receiver clock input
- False-start bit detection
- Line-break generation and detection

- Modem control functions:

  Clear to send (CTS)
  Request to send (RTS)
  Data set ready (DSR)
  Data terminal ready (DTR)
  Ring indicator (RI)
  Carrier detect (CD)

All communication protocol is a function of the system microcode and must be loaded before the adapter is operational. All pacing of the interface and control signal status must be handled by the system software. The following figure is a block diagram of the IBM Asynchronous Communications Adapter.



Asynchronous Communications Adapter Block Diagram

Programming Considerations

Modes Of Operation

The different modes of operation are selected by programming the 8250 Asynchronous Communications Element. This is done by selecting the I/O address (hex 3F8 to 3FF primary, and hex 2F8 to 2FF secondary) and writing data out to the adapter. Address bits A0, A1, and A2, select the different registers that define the modes of operation. Also, bit 7—the divisor latch access bit (DLAB)—of the line-control register is used to select certain registers.

I/O Decode (in Hex)			
Primary Adapter	Alternate Adapter	Register Selected	DLAB State
3F8	2F8	TX Buffer	DLAB = 0 (Write)
3F8	2F8	RX Buffer	DLAB = 0 (Read)
3F8	2F8	Divisor Latch LSB	DLAB = 1
3F9	2F9	Divisor Latch MSB	DLAB = 1
3F9	2F9	Interrupt Enable Register	
3FA	2FA	Interrupt Identification Registers	
3FB	2FB	Line Control Register	
3FC	2FC	Modem Control Register	
3FD	2FD	Line Status Register	
3FE	2FE	Modem Status Register	

I/O Decodes

Hex Addresses 3F8 to 3FF AND 2F8 TO 2FF											
A9	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**DLAB**	**Register**
1	1/0	1	1	1	1	1	x	x	x		
							0	0	0	0	Receive Buffer (read). Transmit Holding Reg. (write)
							0	0	1	0	Interrupt Enable
							0	1	0	x	Interrupt Identification
							0	1	1	x	Line Control
							1	0	0	x	Modem Control
							1	0	1	x	Line Status
							1	1	0	x	Modem Status
							1	1	1	x	None
							0	0	0	1	Divisor Latch (LSB)
							0	0	1	1	Divisor Latch (MSB)

Note: Bit 8 will be logical 1 for the adapter designated as primary or a logical 0 for the adapter designated as alternate (as defined by the address jumper module on the adapter).

A2, A1 and A0 bits are "don't cares" and are used to select the different register of the communications chip.

Address Bits

INS8250

The INS8250 has a number of accessible registers. The system programmer may access or control any of the INS8250 registers through the system unit's microprocessor. These registers are used to control INS8250 operations and to transmit and receive data. The following figure provides a listing and description of the accessible registers.

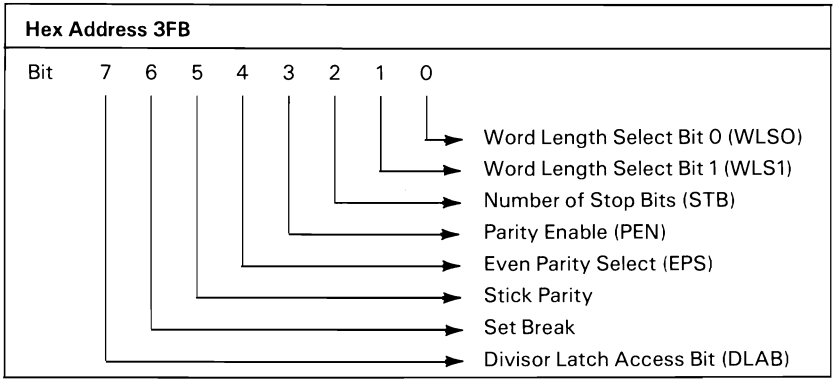
Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All bits Low (0-3 Forced and 4-7 Permanent).
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	Except Bits 5 and 6 are High
Modem Status Register	Master Reset	Bits 0-3 Low Bits 4-7 - Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errors)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (RCVR Data Ready)	Read IIR/ Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
OUT 2	Master Reset	High
RTS	Master Reset	High
DTR	Master Reset	High
OUT 1	Master Reset	High

Asynchronous Communications Reset Functions

Line-Control Register

The system programmer specifies the format of the asynchronous data communications exchange through the line-control register. In addition to controlling the format, the programmer may retrieve the contents of the line-control register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

The contents of the line-control register are as follows:



Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logical 0, one stop bit is generated or checked in the transmitted or received data, respectively. If bit 2 is logical 1 when a 5-bit word length is selected through bits 0 and 1, 1-1/2 stop bits are generated or checked. If bit 2 is logical 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated or checked.

Bit 3: This bit is the parity enable bit. When bit 3 is a logical 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed.)

Bit 4: This bit is the even parity select bit. When bit 3 is a logical 1 and bit 4 is a logical 0, an odd number of logical 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logical 1 and bit 4 is a logical 1, an even number of bits is transmitted or checked.

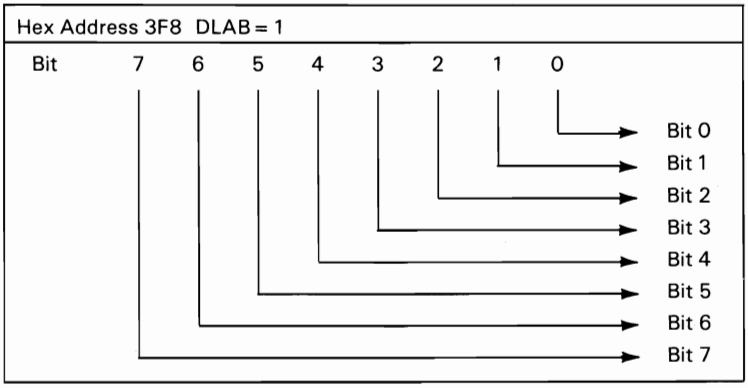
Bit 5: This bit is the stick parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is transmitted and then detected by the receiver as a logical 0 if bit 4 is a logical 1, or as a logical 1 if bit 4 is a logical 0.

Bit 6: This bit is the set break control bit. When bit 6 is a logical 1, the serial output (SOUT) is forced to the spacing (logical 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logical 0. This feature enables the system unit's microprocessor to alert a terminal in a computer communications system.

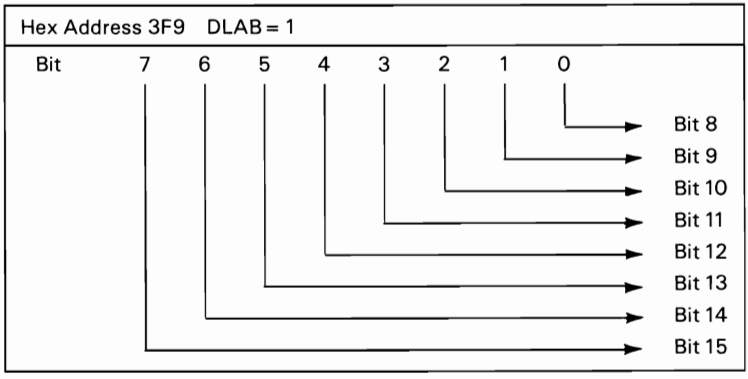
Bit 7: This bit is the divisor latch access bit (DLAB). It must be set high (logical 1) to access the divisor latches of the baud-rate generator during a read or write operation. It must be set low (logical 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

Programmable Baud-Rate Generator

The INS8250 contains a programmable baud-rate generator that is capable of taking the clock input (1.8432 MHz) and dividing it by any divisor from 1 to (2^{16}-1). The output frequency of the baud generator is 16 x the baud rate (divisor # =(frequency input)/(baud rate x 16)). Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization in order to ensure desired operation of the baud-rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.



Divisor Latch Least Significant Bit (DLL)



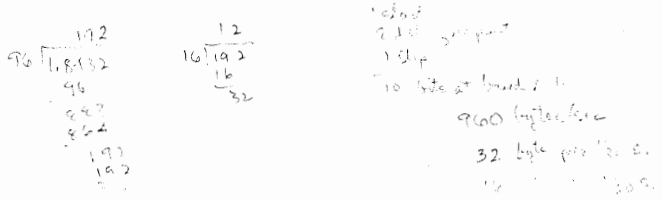
Divisor Latch Most Significant Bit (DLM)

The following figure illustrates the use of the baud-rate generator with a frequency of 1.8432 MHz. For baud rates of 9600 and below, the error obtained is minimal.

Note: The maximum operating frequency of the baud-rate generator is 3.1 MHz. In no case should the data speed be greater than 9600 baud.

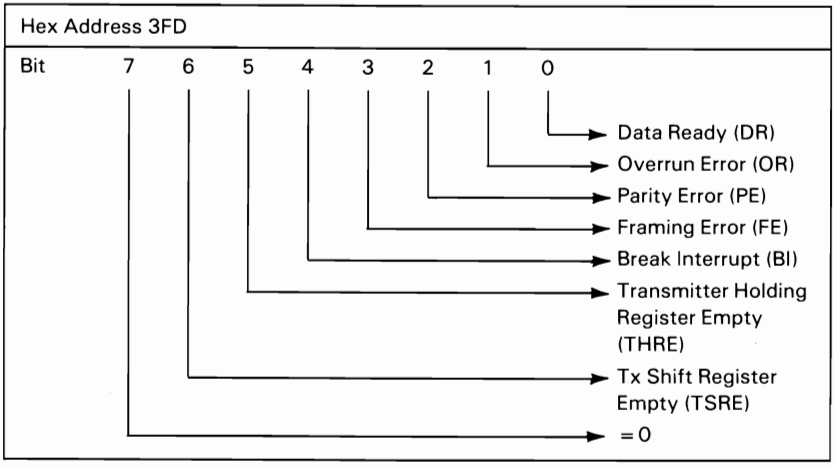
Desired Baud Rate	Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent Error Difference Between Desired and Actual
50	2304	900	—
75	1536	600	—
110	1047	417	0.026
134.5	857	359	0.058
150	768	300	—
300	384	180	—
600	192	0C0	—
1200	96	060	—
1800	64	040	—
2000	58	03A	0.69
2400	48	030	—
3600	32	020	—
4800	24	018	—
7200	16	010	—
9600	12	00C	—

Baud Rate at 1.843 MHz



Line Status Register (LSR)

This 8-bit register provides status information to the system unit's microprocessor concerning the data transfer. The contents of the line status register are indicated and described in the following figure.



Line Status Register (LSR)

Bit 0: This bit is the receiver data ready (DR) indicator. Bit 0 is set to logical 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 may be reset to a logical 0 either by the system unit's microprocessor reading the data in the receiver buffer register or by writing logical 0 into it from the system unit's microprocessor.

Bit 1: This bit is the overrun error (OE) indicator. Bit 1 indicates that data in the receiver buffer register was not read by the system unit's microprocessor before the next character was transferred into the receiver buffer register, thereby destroying the previous character. The OE indicator is reset whenever the system unit's microprocessor reads the contents of the line status register.

Bit 2: This bit is the parity error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity select bit. The PE bit is

set to logical 1 upon detection of a parity error and is reset to logical 0 whenever the system unit's microprocessor reads the contents of the line status register.

Bit 3: This bit is the framing error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to logical 1 whenever the stop bit following the last data bit or parity is detected as a zero bit (spacing level).

Bit 4: This bit is the break interrupt (BI) indicator. Bit 4 is set to logical 1 whenever the received data input is held in the spacing (logical 0) state for longer than a full-word transmission time (that is, the total time of start bit + data bits + parity + stop bits).

> **Note:** Bits 1 through 4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the transmitter-holding-register-empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the system unit's microprocessor when the transmit-holding-register-empty interrupt enable is set high. The THRE bit is set to logical 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logical 0 concurrently with the loading of the transmitter holding register by the system unit's microprocessor.

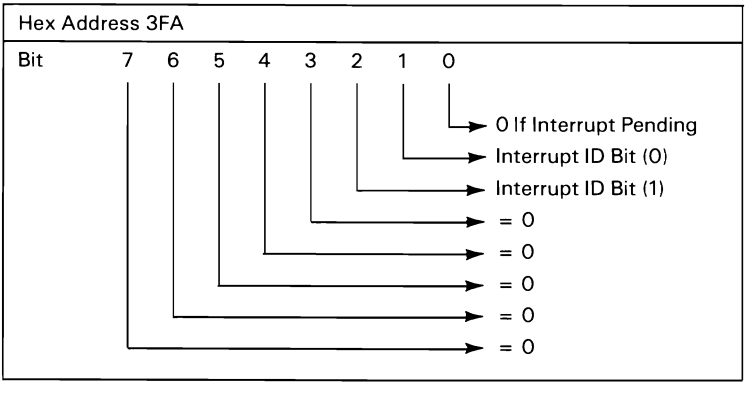
Bit 6: This bit is the transmitter-shift-register-empty (TSRE) indicator. Bit 6 is set to logical 1 whenever the transmitter shift register is idle. It is reset to logical 0 upon a data transfer from the transmitter holding register to the transmitter shift register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logical 0.

Interrupt Identification Register (IIR)

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels: receiver line status (priority 1), received data ready (priority 2), transmitter holding register empty (priority 3), and modem status (priority 4).

Information indicating that a prioritized interrupt is pending, and the type of prioritized interrupt, is stored in the interrupt identification register. Refer to the "Interrupt Control Functions" table. The interrupt identification register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending, and no other interrupts are acknowledged until that particular interrupt is serviced by the system unit's microprocessor. The contents of the IIR are indicated and described in the following figure.



Interrupt Identification Register (IIR)

Bit 0: This bit can be used in either a hard-wired prioritized or polled environment to indicate whether an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is logical 1, no interrupt is pending, and polling (if used) is continued.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending, as indicated in the "Interrupt Control Functions" table.

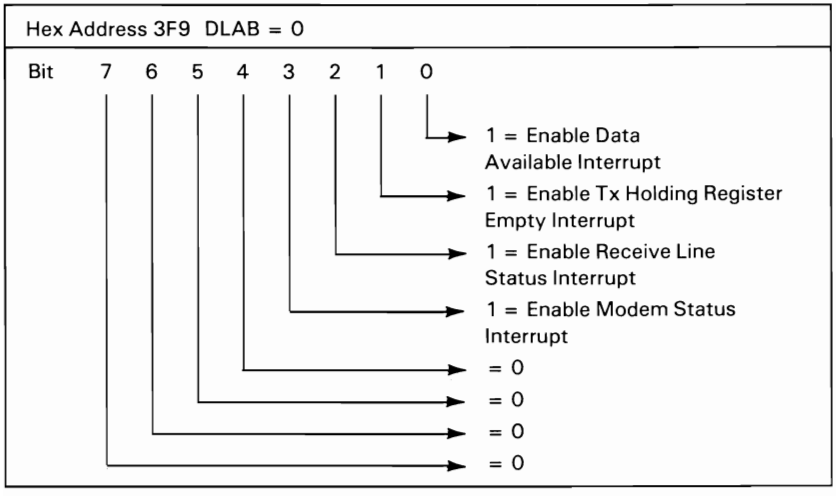
Bits 3 through 7: These five bits of the IIR are always logical 0.

Interrupt ID Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Direct	Reading the Modem Status Register

Interrupt Control Functions

Interrupt Enable Register

This 8-bit register enables the four types of interrupt of the INS8250 to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt enable register. Similarly, by setting the appropriate bits of this register to logical 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the interrupt identification register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the line status and modem status registers. The contents of the interrupt enable register are indicated and described in the following figure.



Interrupt Enable Register (IER)

Bit 0: This bit enables the received-data-available interrupt when set to logical 1.

Bit 1: This bit enables the transmitter-holding-register-empty interrupt when set to logical 1.

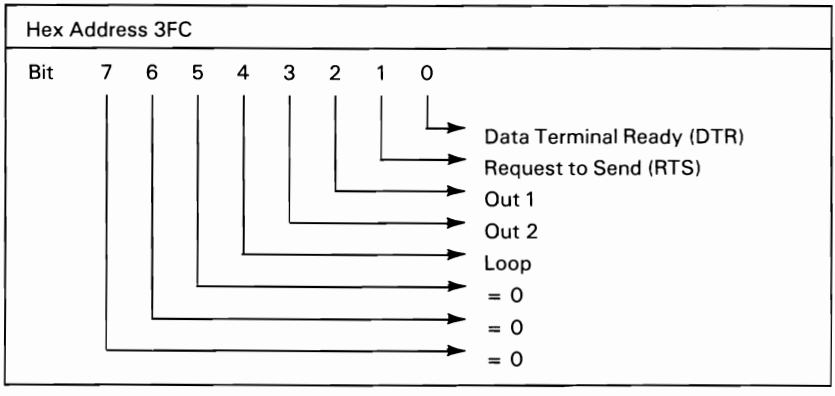
Bit 2: This bit enables the receiver-line-status interrupt when set to logical 1.

Bit 3: This bit enables the modem-status interrupt when set to logical 1.

Bits 4 through 7: These four bits are always logical 0.

Modem Control Register

This 8-bit register controls the interface with the modem or data set (or a peripheral device emulating a modem). The contents of the modem control register are indicated and described as follows:



Modem Control Register (MCR)

Bit 0: This bit controls the data terminal ready (-DTR) output. When bit 0 is set to a high level, the -DTR output is forced to an active low. When bit 0 is reset to low level, the -DTR output is forced high.

> **Note:** The -DTR output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding modem or data set.

Bit 1: This bit controls the request to send (-RTS) output. Bit 1 affects the -RTS output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the output 1 (-OUT 1) signal, which is an auxiliary user-designated output. Bit 2 affects the -OUT 1 output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the output 2 (-OUT 2) signal, which is an auxiliary user-designated output. Bit 3 affects the -OUT 2 output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logical 1, the following occurs: the transmitter serial output (SOUT) is set to the marking (logical 1) state; the receiver serial input (SIN) is disconnected; the output of the transmitter shift register is "looped back" into the receiver shift register input; the four modem control inputs (-CTS, -DSR, -RLSD, and -RI) are disconnected; and the four modem control outputs (-DTR, -RTS, -OUT 1, and -OUT 2) are internally connected to the four modem control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the system unit's microprocessor to verify the transmit-data and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts also are operational, but the interrupts' sources are now the lower four bits of the modem control register instead of the four modem control inputs. The interrupts are still controlled by the interrupt enable register.

The INS8250 interrupt system can be tested by writing into the lower four bits of the modem status register. Setting any of these bits to a logical 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to normal operation, the registers must be reprogrammed for normal operation, then bit 4 of the modem control register must be reset to logical 0.

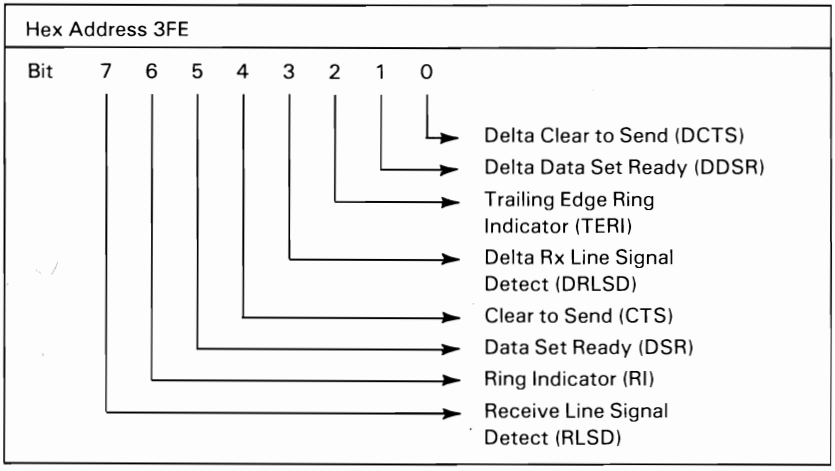
Bits 5 through 7: These bits are permanently set to logical 0.

Modem Status Register

This 8-bit register provides the current state of the control lines from the modem (or peripheral device) to the system unit's microprocessor. In addition to this current-state information, four bits of the modem status register provide change information. These bits are set to logical 1 whenever a control

input from the modem changes state. They are reset to logical 0 whenever the system unit's microprocessor reads the modem status register.

The content of the modem status register is indicated and described in the following figure.



Modem Status Register (MSR)

Bit 0: This bit is the delta clear to send (DCTS) indicator. Bit 0 indicates that the -CTS input to the chip has changed state since the last time it was read by the system unit's microprocessor.

Bit 1: This bit is the delta data set ready (DDSR) indicator. Bit 1 indicates that the -DSR input to the chip has changed state since the last time it was read by the system unit's microprocessor.

Bit 2: This bit is the trailing edge of the ring indicator (TERI) detector. Bit 2 indicates that the -RI input to the chip has changed from an on (logical 1) to an off (logical 0) condition.

Bit 3: This bit is the delta received line signal detector (DRLSD) indicator. Bit 3 indicates that the -RLSD input to the chip has changed state.

> **Note:** Whenever bit 0, 1, 2, or 3 is set to logical 1, a modem status interrupt is generated.

Bit 4: This bit is the complement of the clear to send (-CTS) input. If bit 4 (LOOP) of the modem control register (MCR) is set to logical 1, the bit is equivalent to RTS in the MCR.

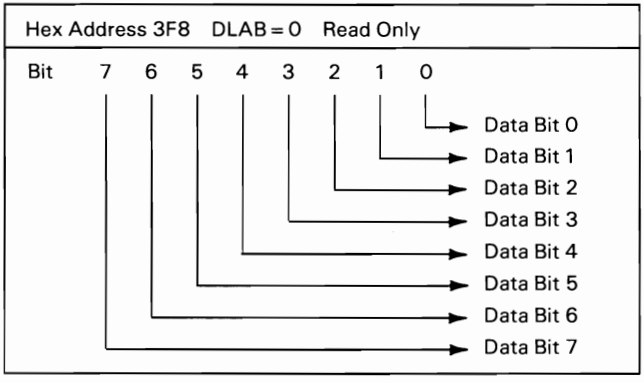
Bit 5: This bit is the complement of the data set ready (-DSR) input. If bit 4 of the MCR is set to logical 1, the bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the ring indicator (-RI) input. If bit 4 of the MCR is set to logical 1, the bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the received line signal detect (-RLSD) input. If bit 4 of the MCR is set to logical 1, the bit is equivalent to OUT 2 of the MCR.

Receiver Buffer Register

The receiver buffer register contains the received character, which is defined in the following figure.

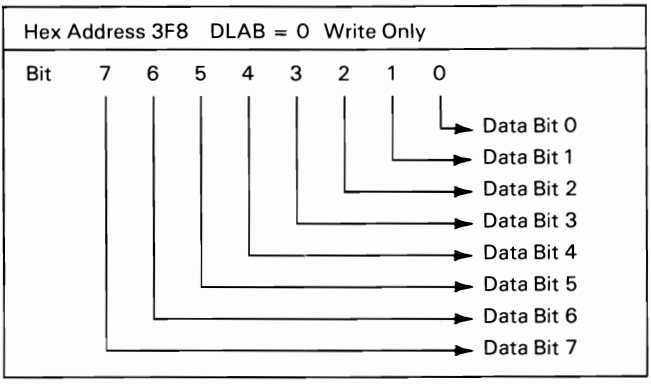


Receiver Buffer Register (RBR)

Bit 0 is the least-significant bit and is the first bit serially received.

Transmitter Holding Register

The transmitter holding register contains the character to be serially transmitted and is defined as follows:

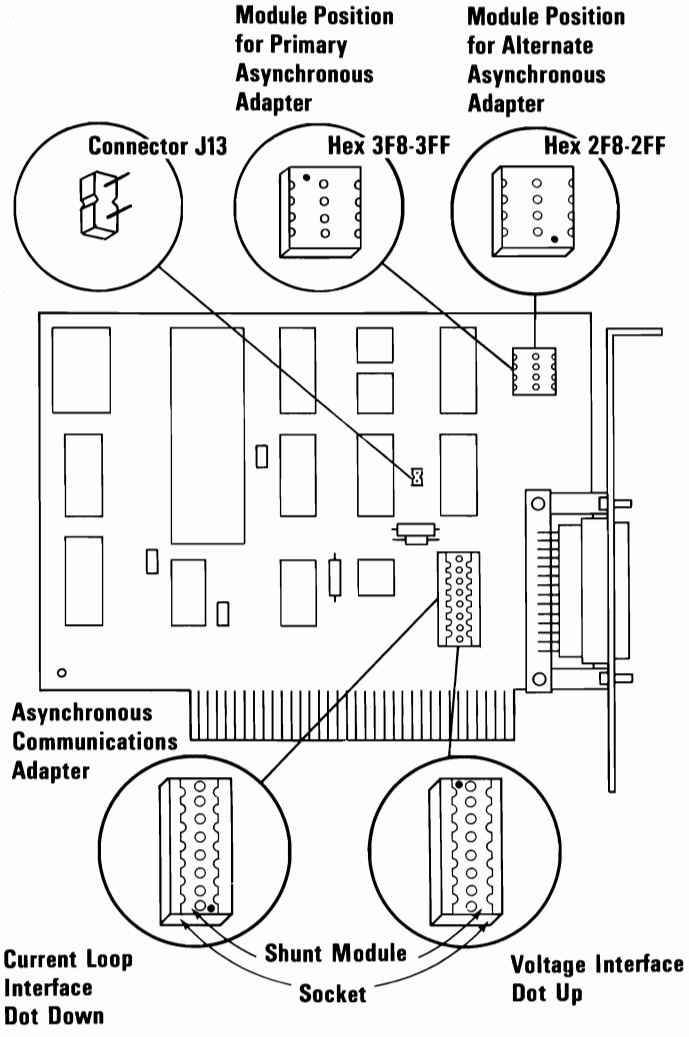


Transmitter Holding Register (THR)

Bit 0 is the least-significant bit and is the first bit serially transmitted.

Selecting the Interface Format and Adapter Address

The voltage or current-loop interface and adapter address are selected by plugging in programmed shunt modules with the locator dots up or down. See the following figure for the configurations.

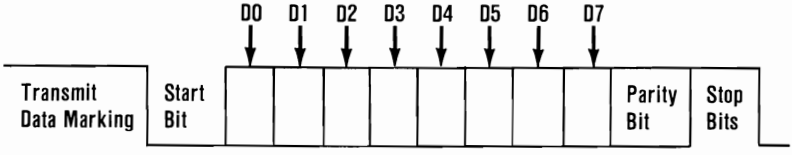


If the adapter is to be installed in expansion slot 8 of an IBM Personal Computer XT or IBM Portable Personal Computer, a jumper is required on connector J13.

Interrupts

One interrupt line is provided to the system. This interrupt is IRQ4 for a primary adapter, or IRQ3 for an alternate adapter, and is positive active. To allow the communications adapter to send interrupts to the system, bit 3 of the modem control register must be set to 1 (high). At this point, any interrupts allowed by the interrupt enable register will cause an interrupt.

The data format will be as follows:



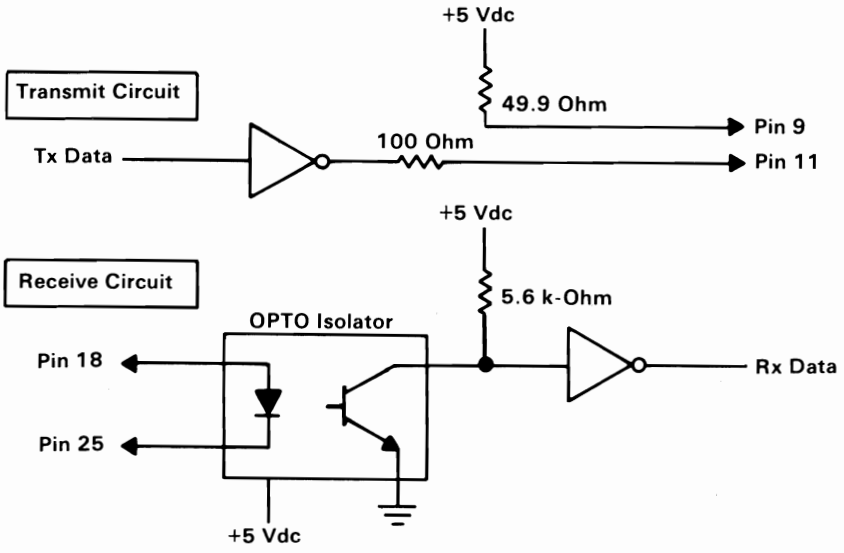
Data bit 0 is the first bit to be transmitted or received. The adapter automatically inserts the start bit, the correct parity bit if programmed to do so, and the stop bit (1, 1-1/2, or 2 depending on the command in the line-control register).

Interface

The communications adapter provides an EIA RS-232C-like interface. One 25-pin, D-shell, male connector is provided to attach various peripheral devices. In addition, a current-loop interface is also located in this same connector. A jumper block is provided to manually select either the voltage interface or the current-loop interface.

The current-loop interface is provided to attach certain printers provided by IBM that use this particular type of interface. IBM recommends that the current loop not be used beyond a distance of 15.3 meters (50 feet) as measured by the length of cable between the two interconnected points.

Pin 18	+ receive current loop data
Pin 25	- receive current loop return
Pin 11	- transmit current loop data
Pin 9	+ transmit current loop return



Current Loop Interface

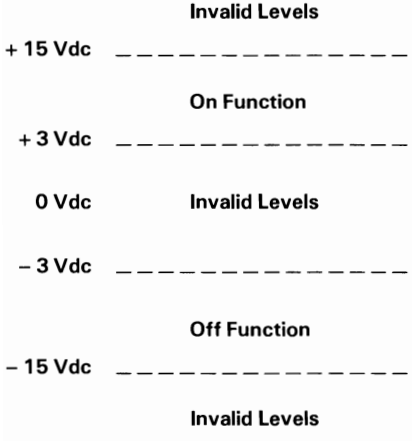
The voltage interface is a serial interface. It supports certain data and control signals, as follows:

Pin 2	Transmitted Data
Pin 3	Received Data
Pin 4	Request to Send
Pin 5	Clear to Send
Pin 6	Data Set Ready
Pin 7	Signal Ground
Pin 8	Carrier Detect
Pin 20	Data Terminal Ready
Pin 22	Ring Indicator

The adapter converts these signals to or from TTL levels from or to EIA voltage levels. These signals are sampled or generated by the communications control chip. These signals can then be sensed by the system software to determine the state of the interface or peripheral device.

Voltage Interchange Information

Interchange Voltage	Binary State	Signal Condition	Interface Control Function
Positive Voltage =	Binary (0)	= Spacing	= On
Negative Voltage =	Binary (1)	= Marking	= Off



The signal will be considered in the *marking* condition when the voltage on the interchange circuit, measured at the interface

point, is more negative than -3 Vdc with respect to signal ground. The signal will be considered in the *spacing* condition when the voltage is more positive than +3 Vdc with respect to signal ground. The region between +3 Vdc and -3 Vdc is defined as the transition region, and considered an invalid level. The voltage that is more negative than -15 Vdc or more positive than +15 Vdc will also be considered an invalid level.

During the transmission of data, the marking condition will be used to denote the binary state 1, and the spacing condition will be used to denote the binary state 0.

For interface control circuits, the function is on when the voltage is more positive than +3 Vdc with respect to signal ground and is off when the voltage is more negative than -3 Vdc with respect to signal ground.

INS8250 Functional Pin Description

The following describes the function of all INS8250 input/output pins. Some of these descriptions refer to internal circuits.

> **Note:** In the following descriptions, a low represents a logical 0 (0 Vdc nominal) and a high represents a logical 1 (+2.4. Vdc nominal).

Input Signals

Chip Select (CS0, CS1, -CS2), Pins 12-14: When CS0 and CS1 are high and -CS2 is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) address strobe (-ADS) input. This enables communications between the INS8250 and the system unit's microprocessor.

Data Input Strobe (DISTR, -DISTR), Pins 22 and 21: When DISTR is high or -DISTR is low while the chip is selected, it allows the system unit's microprocessor to read status information or data from a selected register of the INS8250.

> **Note:** Only an active DISTR or -DISTR input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the -DISTR line input permanently high, if not used.

Data Output Strobe (DOSTR, -DOSTR), Pins 19 and 18: When DOSTR is high or -DOSTR is low while the chip is selected, it allows the system unit's microprocessor to write data or control words into a selected register of the INS8250.

> **Note:** Only an active DOSTR or -DOSTR input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the -DOSTR input permanently high, if not used.

Address Strobe (-ADS), Pin 25: When low, provides latching for the register select (A0, A1, A2) and chip select (CS0, CS1, -CS2) signals.

> **Note:** An active -ADS input is required when the register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the ADS input permanently low.

Register Select (A0, A1, A2), Pins 26-28: These three inputs are used during a read or write operation to select an INS8250 register to read or write to as indicated in the following table. Note that the state of the divisor latch access bit (DLAB), which is the most significant bit of the line-control register, affects the selection of certain INS8250 registers. The DLAB must be set high by the system software to access the baud-rate generator divisor latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (Read), Transmitter Holding Register (Write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (Read Only)
X	0	1	1	Line Control
X	1	0	0	Modem Control
X	1	0	1	Line Status
X	1	1	0	Modem Control Status
X	1	1	1	None
1	0	0	0	Divisor Latch (Least Significant Bit)
1	0	0	1	Divisor Latch (Most Significant Bit)

Master Reset (MR), Pin 35: When high, clears all registers (except the receiver buffer, transmitter holding, and divisor latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, -OUT 1, -OUT 2, -RTS, -DTR) are affected by an active MR input. Refer to the "Asynchronous Communications Reset Functions" table.

Receiver Clock (RCLK), Pin 9: This input is the 16 x baud-rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, modem, or data set).

Clear to Send (-CTS), Pin 36: The -CTS signal is a modem control function input whose condition can be tested by the system unit's microprocessor by reading bit 4 (CTS) of the modem status register. Bit 0 (DCTS) of the modem status register indicates whether the CTS input has changed state since the previous reading of the modem status register.

> **Note:** Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

Data Set Ready (-DSR), Pin 37: When low, indicates that the modem or data set is ready to establish the communications link and transfer data with the INS8250. The -DSR signal is a modem-control function input whose condition can be tested by

the system unit's microprocessor by reading bit 5 (DSR) of the modem status register. Bit 1 (DDSR) of the modem status register indicates whether the -DSR input has changed since the previous reading of the modem status register.

> **Note:** Whenever the DSR bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

Received Line Signal Detect (-RLSD), Pin 38: When low, indicates that the data carrier had been detected by the modem or data set. The -RLSD signal is a modem-control function input whose condition can be tested by the system unit's microprocessor by reading bit 7 (RLSD) of the modem status register. Bit 3 (DRLSD) of the modem status register indicates whether the RLSD input has changed state since the previous reading of the modem status register.

> **Note:** Whenever the RLSD bit of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled.

Ring Indicator (-RI), Pin 39: When low, indicates that a telephone ringing signal has been received by the modem or data set. The -RI signal is a modem-control function input whose condition can be tested by the system unit's microprocessor by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates whether the -RI input has changed from a low to high state since the previous reading of the modem status register.

> **Note:** Whenever the RI bit of the modem status register changes from a high to a low state, an interrupt is generated if the modem status interrupt is enabled.

VCC, Pin 40: +5 Vdc supply.

VSS, Pin 20: Ground (0 Vdc) reference.

Output Signals

Data Terminal Ready (-DTR), Pin 33: When low, informs the modem or data set that the INS8250 is ready to communicate. The -DTR output signal can be set to an active low by programming bit 0 (DTR) of the modem control register to a high level. The -DTR signal is set high upon a master reset operation.

Request to Send (-RTS), Pin 32: When low, informs the modem or data set that the INS8250 is ready to transmit data. The -RTS output signal can be set to an active low by programming bit 1 (RTS) of the modem control register to a high level. The -RTS signal is set high upon a master reset operation.

Output 1 (-OUT 1), Pin 34: User-designated output that can be set to an active low by programming bit 2 (-OUT 1) of the modem control register to a high level. The -OUT 1 signal is set high upon a master reset operation.

Output 2 (-OUT 2), Pin 31: User-designated output that can be set to an active low by programming bit 3 (-OUT 2) of the modem control register to a high level. The -OUT 2 signal is set high upon a master reset operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active CS0, CS1, and -CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logical 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the system unit's microprocessor is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the system unit's microprocessor and the INS8250 on the D7–D0 data bus) at all times, except when the system unit's microprocessor is reading data.

Baud Out (-BAUDOUT), Pin 15: 16 x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud-rate generator divisor latches. The -BAUDOUT may also be used for the receiver section by typing this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled through the interrupt enable register: receiver error flag, received data available, transmitter holding register empty, or modem status. The INTRPT signal is reset low upon the appropriate interrupt service or a master reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral device, modem, or data set). The SOUT signal is set to the marking (logical 1) state upon a master reset operation.

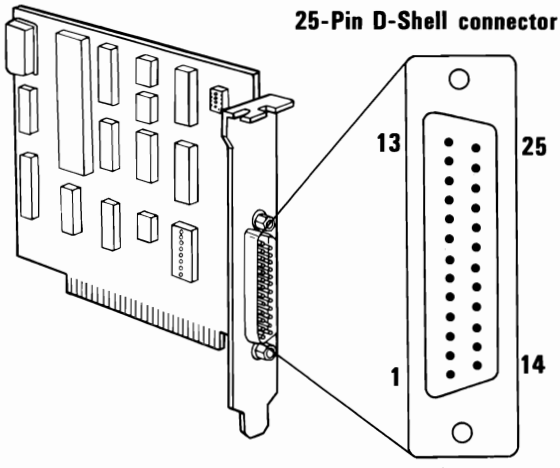
Input/Output Signals

Data Bus (D7–D0), Pins 1–8: This bus comprises eight tri-state input/output lines. The bus provides bidirectional communications between the INS8250 and the system unit's microprocessor. Data, control words, and status information are transferred through the D7-D0 data bus.

External Clock Input/Output (XTAL1, XTAL2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Specifications

The following page shows the connecter pin assignments and specifications for the Asynchronous Communications Adapter.

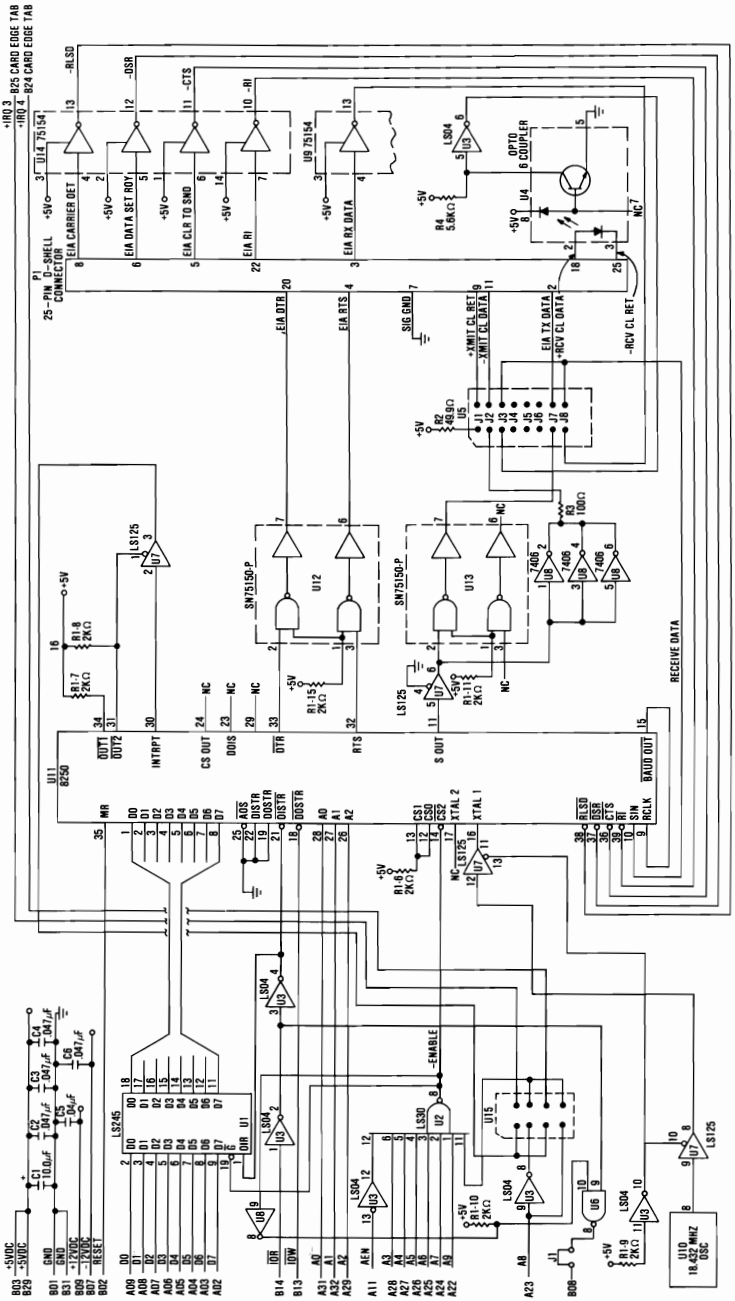


	Description	Pin	
	NC	1	
←	Transmitted Data	2	
→	Received Data	3	
←	Request to Send	4	
→	Clear to Send	5	
→	Data Set Ready	6	
	Signal Ground	7	
→	Received Line Signal Detector	8	
←	+ Transmit Current Loop Data	9	
	NC	10	
←	– Transmit Current Loop Data	11	
	NC	12	Asynchronous Communications Adapter (RS-232C)
External Device	NC	13	
	NC	14	
	NC	15	
	NC	16	
	NC	17	
→	+ Receive Current Loop Data	18	
	NC	19	
←	Data Terminal Ready	20	
	NC	21	
→	Ring Indicator	22	
	NC	23	
	NC	24	
→	– Receive Current Loop Return	25	

Note: To avoid inducing voltage surges on interchange circuits, signals from interchange circuits shall not be used to drive inductive devices, such as relay coils.

Connector Specifications

Logic Diagrams



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