# ROM POST™

## Advanced ROM-Based PC Diagnostics

# User's Manual

Document # MAN-RP-110191-JDR


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### Congratulations!

You are now among the ranks of thousands of successful technicians that rely on the solid performance of ROM POST. Large manufacturers, OEMs, distributors, and dealers around the world agree that ROM POST is a power-packed product that repeatedly delivers an accurate diagnosis!

### A Short History Lesson

The roots of ROM POST can be traced to the days when CP/M dinosaurs walked the earth. As you know, the dinosaurs died out long ago, but ROM POST has evolved to take on the special needs of today's IBM compatible machines, regardless of the operating system. For over 10 years, our engineering team has been working hard to tweak compatibility and add exciting new features to ensure that ROM POST will continue to reliably meet your exacting specifications.

### System Requirements

ROM POST is not demanding of your system resources, however, these are a few fundamental requirements:

- IBM PC, XT, AT-286, AT-386, AT-486, or 100% compatible
- Not operating-system dependent

## Who Can Benefit?

**Everyone!** - ROM POST was designed from the ground up to handle the needs of sophisticated service technicians. System testing and burn-in has never been easier. However, manufacturers, distributors, dealers, and educators have needs for which ROM POST is the ideal tool.

• **Service Technicians** - It's no fun to stare at a blank screen when you arrive onsite to service a system! Software-based diagnostics are useless at that point! Most technicians swap boards in order to isolate the fault, while advanced technicians rely upon bulky and expensive test equipment. Now you can look forward to these encounters, because ROM POST will diagnose problems even if major motherboard components are defective. Just pop ROM POST into the BIOS socket(s). The screen will let you know which component is under test, in addition to a simple **PASS** or **FAIL** indication. ROM POST helps service technicians to quickly and accurately diagnose "dead" systems that normally have to be taken back to the shop for repair. ROM POST can even be used to burn-in a newly repaired system to ensure that a quality repair has been made.

• **Manufacturers** - ROM POST is the ideal tool for a burn-in procedure as new systems or devices come off the line. When units are repaired under manufacturer warranty, ROM POST will help to efficiently complete the repair.

• **Distributors** - When evaluating new products to distribute, Landmark's ROM POST can provide a picture as to the extent of "IBM-compatibility."

• **Dealers** - Nothing upsets a client more than getting a new or newly-repaired unit home and having it fail shortly thereafter. By using ROM POST to burn-in units before they go out the door, dealers can reduce returns.

• **Educators** - Boards can be fault-injected by the instructor, later to be found by ROM POST. Students can be taught to find faulty components without actually having the electronics theory needed to test individual gates on ICs. Advanced courses in troubleshooting are supported by ROM POST's ability to test memory, DMA and Interrupt Controllers, timers, CMOS RAM, RTC, and other board-level components.



## First Things To Do

• **Inspect the package** - Although Landmark makes every attempt to provide complete packages, from time to time an item might be overlooked. If you find that an item is missing, a quick call to our Customer Service Department will rectify the situation.

**The ROM POST package includes:**

- This manual,
- Registration card,

**One or more of the following:**

- One 64KB PC ROM POST,
- One 64KB XT ROM POST,
- One combined 64KB PC/XT ROM POST (switch selectable),
- Even and Odd 128KB or 256KB AT ROM POST,
- One 512KB AT ROM POST (for single-BIOS AT-class systems).

**Note:** Any other variance previously agreed upon with your Product Consultant will be reflected on the invoice.

• **Register Your Product** - As noted above, you should have received a registration card. In order to ensure continued support from Landmark, please complete and mail the registration card. Your warranty, of course, is still valid without the registration card.

### If the Unexpected Happens...

• **Customer Service** - If your package is missing a component, a component is found to be defective, or a component fails within the warranty period, and the product was purchased directly from Landmark, please contact our Customer Service Department. They will be happy to service your needs. If the product was obtained through a distributor or dealer, please contact the distributor or dealer for support.

• **Technical Support** - Sometimes additional information is required to better apply Landmark's ROM POST to a particular case. If you are in need of information beyond that which is presented here, please feel free to contact your supplier's Technical Support Department. If the product was purchased directly from Landmark, you will find that our Technical Support is unsurpassed.

• **RMA Procedures** - If it is necessary to return your product for any reason (ie. exchange, replacement, repair), first contact your supplier's Technical Support Department. A Technical Support Agent will provide instructions for packaging, marking, and shipping your product to a factory-authorized repair facility. Additionally, an RMA number will be provided to ensure proper handling of your package. If Landmark is your direct supplier, please contact Landmark's Technical Support Department directly at:

- (800) 683-0854 (continental U.S.)
- (813) 443-1331 (outside U.S.)
- Hours: 9AM - 6PM EST



### What is ROM POST?

Landmark's ROM POST (ROM-based Power On Self Test) diagnostic module is a set of comprehensive tests that initialize and test the system board and components required to boot a personal computer from a floppy drive. The tests are actually programs that reside in one or two ROM chips. The ROM POST is used by replacing the system BIOS chip(s) with the ROM POST chip(s). Once the system is powered on, system tests are performed automatically by the ROM POST module. Test progress and results can be displayed on any Monochrome Display Adapter (MDA), Color Display Adapter (CGA), Enhanced Display Adapter (EGA), or self-initializing Video Graphics Array (VGA).

### What if my display is not working?

The ROM POST module also generates a unique series of beep codes for each failing test. The beep codes are in the form of a group of at least one high-low tone followed by at least one short tone. The resulting string of beeps can be heard over the system's speaker, then looked up in this manual for interpretation of the error.

### When do I use ROM POST?

A computer that seems to be "dead" usually is not totally dysfunctional, so the ROM POST module can be effectively used for testing it; a failure in the first 16KB of memory, or other system board component, or a failure of the video display adapter can cause a system to appear to be "dead." Part of the reason for this is that the Power On Self Test (POST) contained in most of the standard system BIOSes performs a number of basic tests (such as testing the first 16KB of RAM). If a failure is detected, the BIOS halts the system, sometimes without any error indication. Landmark's ROM POST is able to pick up where the system BIOS left off in determining and reporting the cause of such a failure. Because a RAM error or faulty timer channel does not prevent the CPU from initializing the video display, ROM POST is able to report the failing component. As mentioned earlier, if the problem is related to the video display, ROM POST will generate a unique set of beep codes for each test using the system speaker. This aids in identifying the failing component even if the display does not work.

Technicians may also find that Landmark's ROM POST is useful in performing tests on the system board and system memory in computers that cannot boot from a floppy drive. Because ROM POST's program is on a chip, testing cannot "crash" like software-based diagnostics when memory is faulty or memory refresh is erratic or missing. For example, ROM POST includes a slow refresh memory test which can be used to find the weaker chips in system memory. Borderline memory is usually the cause of intermittent Parity Check errors.

> **Notice:** Landmark cannot be held responsible for any type of damage or injury resulting to either the system under test or the user of the product, without regard to the correct use or function of this product. To avoid potential system damage from static discharge, assure adequate grounding when working with components or when touching the system.

### What if ROM POST does not run?

Of course, your system must be operating to a certain level in order to execute code located in ROM POST. Sometimes, even ROM POST will not execute.

#### • Power Problems

When a system appears to be dead, first suspect power problems (to simplify power testing, try Landmark's KickStart 1 diagnostic card). First, check to see that 110 VAC is being supplied to the power supply. If this is so, check the DC voltage present at each power connector (these connectors are usually white, four-prong female connectors). If the voltage is ok, firmly reconnect all power connectors to drives and accessories. If the power supply's fan (usually located on the back of the system) is not rotating, you can assume that the power supply is not good. Because PC power supplies monitor their own power, and shut themselves down automatically when either voltage or current drain stray from a preset range, it is possible that a device is drawing too much power. In addition, the Power Good Signal must be supplied to the system board. To test for a short, unplug all devices that use a power connector. Turn the power supply off and then on. If the power supply now works, there is a short in one of the devices normally connected to the power supply.



With a voltmeter, check the power supply output voltages to the system board power connector and any expansion connector. The four-pin power connector can be diagrammed like this:

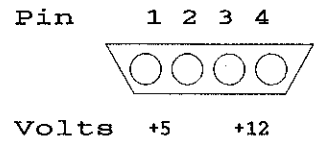


**Figure 1**: 4-Pin Power Connector

There are usually two connectors for the system board power, sometimes labeled P8 and P9. They can be diagrammed like this:

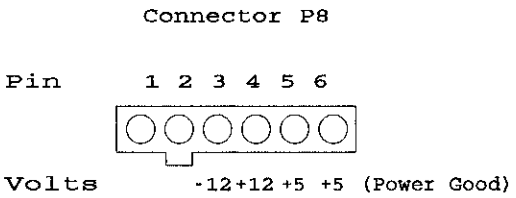


**Figure 2**: Power Connector P8

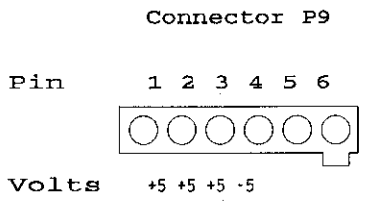


**Figure 3**: Power Connector P9

The wires from the power supply are usually color coded as follows:

| Color | Volts |
|---|---|
| Red | +5 |
| Yellow | +12 |
| Blue | -12 |
| White | -5 |
| Black | 0 (Ground) |
| Orange | +5 (Power Good Signal) |

### • No Video Display

Remove any adapters from the bus that are not essential to the operation of the system. This includes expanded memory adapters, and any adapters that are not tested by Landmark's ROM POST. If there is no cursor on the monitor when power is on, then the system BIOS has not been able to initialize the video adapter, the display adapter or monitor may be defective, or the system BIOS cannot recognize the video card (check the setup of the machine; the machine should be configured for this video adapter). Since the system BIOS attempts to initialize the monitor very early in the POST sequence, a critical element might be broken such as the CPU clock or the CPU itself. A bad monitor or video adapter card will mimic a totally dead state, although the system may be operable with the exception of video output (you just can't see what you type).

When experiencing difficulties with video, first check the motherboard for proper configuration (refer to motherboard user's guide). If the motherboard has a built-in video adapter, it is recommended that this be disabled, and that a separate video adapter be installed. Next, check the video adapter for proper configuration (refer to video adapter user's guide). Because certain VGA adapters are not self-initializing (they rely upon certain BIOS routines to be present), they are not appropriate for testing purposes and may be incompatible with ROM POST (use of a monochrome adapter is recommended). After checking the motherboard and video adapter, ensure that the monitor is adjusted properly (refer to the monitor user's guide). If video problems persist, it may be necessary to troubleshoot the system by listening to ROM POST's beep codes (explained later in this manual).



Check to see if the processor is issuing memory requests. If not, check whether or not the processor clock is running. If a clock signal is being applied to the CPU, replace the processor. Finally, you should ensure that the correct voltage is available to the CPU.

**Note:** If the system still does not appear to be operational, you will need to troubleshoot on a gate level using a logic probe and an oscilloscope. This should only apply to the most severely impaired systems.

### What Computers can be Tested by ROM POST?

ROM POST can diagnose any IBM PC/XT or 100% compatible, AT-286, AT-386, or AT-486 computers. For 80386 and 80486 machines that use a single BIOS, Landmark has a single 512KB ROM POST available (contact your Product Consultant if you require this single ROM POST).

In order for ROM POST to function, a small amount of circuitry must be operating (power must be available, the processor must be running, and the processor must be able to access the ROM POST via the local address and data bus). A working speaker should be attached to the system board, but its absence will not prevent ROM POST from displaying results on the monitor. Note that no adapter cards need be in the system, however it is preferable to have a Monochrome or Graphics monitor adapter in the system.

## Installation

### • PC/XT-Compatible Systems

Landmark provides a PC-compatible ROM POST, an XT-compatible ROM POST, and a combined ROM POST that can be set via a switch to perform with a PC or an XT. Each is designed to replace the system BIOS EPROM or ROM chip located on the system board. This chip is labelled **U33** on an actual IBM PC motherboard, and **U18** on a genuine IBM XT. For compatible computers, before removing any chips or inserting ROM POST, please check with the manufacturer or consult the technical manual for that computer to determine into which socket ROM POST should be installed, since your motherboard probably does not label components the same as IBM.

> **Warning!!!** When using the combined PC/XT ROM POST, be sure to position the slide switch according to the system under test. The "PC" position is used for PCs with a 24-pin socket. The pair of pins nearest the switch will hang over the end of the BIOS socket. The "XT" position is used for XTs and compatibles that have 28-pin sockets. Make sure that the slide switch is all the way to one direction or the other. If it is stuck in the middle, ROM POST will not function.

Note the proper orientation of ROM POST:

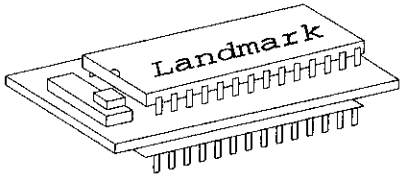


**Figure 4**: Combined PC/XT ROM POST

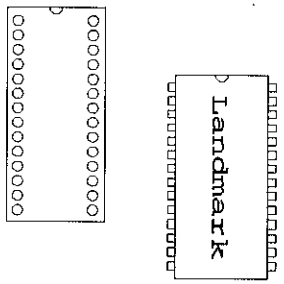


**Figure 5**: Proper orientation



Landmark provides three versions of ROM POST for 8088-based systems. The PC ROM POST is designed for PC compatibles, the XT ROM POST is for use in XT compatibles, and the combined PC/XT ROM POST will work in either a PC or an XT system. Before installing ROM POST, ensure that the notch is aligned with the notch in the mother-board's socket. Because the BIOS sockets in PC-compatible systems have only 24 pins, when using the combined PC/XT ROM POST in a PC compatible, align the notch as usual, however two pins on each side at the end closest to the switch will hang over the edge. This is normal and will not affect the operation of the combined PC/XT ROM POST.

Remove the original BIOS chip with a chip-pulling tool or a long, flat-blade screwdriver. The screwdriver is actually the preferred tool if you are careful. Simply insert the blade under one end of the chip about ¼ of an inch. Do not insert the screwdriver any further, otherwise you might break components located under the socket. Then, rotate the screwdriver shaft so that the blade of the screwdriver wiggles the chip's pins from the socket. Repeat at the other end of the BIOS chip. Make sure to orient the chip so that the notch in the chip is aligned with the notch in the socket. Please ensure that the chip is properly inserted before applying power to the computer to avoid possible damage to the ROM POST chip or to the computer under test.

> **Note:** To make first-time insertion of ROM POST easier, it might be necessary to place ROM POST on its side and gently roll the chip so that all the pins are slightly bent inward at once. Repeat on the other side.

**• AT-Compatible Systems**

ROM POST for AT compatibles replaces both the odd and even (or high and low, respectively) BIOS ROMs on the system board. Before removing the system BIOS chips, take note as to which socket each BIOS ROM is assigned; this will allow you to correctly replace the system BIOS ROMs after testing is complete.

The BIOS ROMs are in U27 and U47 on a genuine IBM AT system motherboard. The chip marked "EVEN" should be placed in the socket U27, while the chip marked "ODD" should be placed in the socket marked U47. On non-IBM system boards, examine the chips that you are removing. They should each have a unique number. One number may be odd the other even, or one chip may be labeled "HIGH" and another "LOW". Replace these chips with the "ODD" and "EVEN" chips respectively. Don't worry if you insert the "ODD" ROM where the "EVEN" should go. As long as the notch on the ROM is aligned with the notch on the socket, the only result will be that ROM POST will not run.

Remove each BIOS chip with a chip-pulling tool or a long, flat-blade screwdriver. The screwdriver is actually the preferred tool if you are careful. Simply insert the blade under one end of the chip about ¼ of an inch. Do not insert the screwdriver any further, otherwise you might break components located under the socket. Then, rotate the screwdriver shaft so that the blade of the screwdriver wiggles the chip's pins from the socket. Repeat at the other end of the BIOS chip. Make sure to orient the chip so that the notch in the chip is aligned with the notch in the socket (see Figures 4 and 5). Please ensure that the chip is properly inserted before applying power to the computer to avoid possible damage to ROM POST or to the computer under test.

> **Note:** To make first-time insertion of ROM POST easier, it might be necessary to place ROM POST on its side and gently roll the chip so that all the pins are slightly bent at once. Repeat on the other side.



**General Information**

All of the ROM POST tests are performed in sequence. No user input is required. Tests will loop continuously until the system halts or power is turned off. Throughout the test suite, the currently active test is highlighted in reverse video on the display. The most recent results from each test, as well as a summary of failures, is maintained on the screen for each test. The summary box on the screen contains information such as the total number of errors that have occurred, the total number of passes that have completed, and the physical address and bit of the most recent memory failure.

If no video display is detected in the system, a beep code will be issued. If the system has an EGA or VGA adapter, and the switches on the adapter are in invalid positions, a beep code will also be issued. If there are no beep codes and no video, try swapping the "EVEN" and "ODD" chips in the BIOS sockets, perhaps they were inserted wrong. Another possibility is that the motherboard is expecting a 128KB ROM, but the ROM POST inserted is 256K. The motherboard is usually configured via jumpers located in close proximity to the BIOS socket(s). Ensure that this setting matches the actual size of the ROM POST in use.

The video display should look like this on a PC/XT:

```
                SUPERSOFT ROMPOST DIAGNOSTICS VERSION 1.2
U3 CPU REGISTERS AND LOGIC          PASSED | U28 SYSTEM BIOS 1          PASSED
U33 SUPERSOFT ROM CHECKSUM          PASSED | U29 BASIC ROM 1            PASSED
U34 8253 TIMER CHANNEL 0            PASSED | U30 BASIC ROM 2            PASSED
U34 8253 TIMER CHANNEL 1            PASSED | U31 BASIC ROM 3            PASSED
U34 8253 TIMER CHANNEL 2            PASSED | U32 BASIC ROM 4            PASSED
U35 8237A DMA CONTROLLER            PASSED |       SYSTEM SWITCH SETTINGS
U36 8255 PARITY DETECTED            PASSED |         -PC SW1-   -PC SW2-
16K CRITICAL MEMORY REGION          PASSED |         |12345678| |12345NNN|
MEMORY REFRESH                      PASSED |         | X X XX | |X XX    |
U2 8259 INTERRUPT CONTROLLER        PASSED |         |X XX X  | | XX     |
HOT INTERRUPT                       PASSED |         ---------- ----------
INTERRUPT LEVEL 0                   PASSED |              -XT SW1-
NONMASKABLE INTERRUPT               PASSED |              |12345678|
MDA MEMORY                          PASSED |              |X  XX  X|
CGA MEMORY                          PASSED |              | XX  XX |
EGA/VGA MEMORY                      PASSED |              ----------
U4 8087 NUMERIC CO-PROCESSOR        PASSED |       DIAGNOSTIC SUMMARY
KEYBOARD CONTROLLER                 PASSED | TOTAL PASSES COMPLETED 00008
KEYBOARD SCAN LINES                 PASSED | TOTAL ERRORS 00055
FLOPPY CONTROLLER                   PASSED | MEMORY ERROR AT ADDRESS 98000
FLOPPY DRIVE READ                   PASSED |                 7 6 5 4 3 2 1 0
SYSTEM MEMORY TO A0000              PASSED | FAILING BITS  X X     X   X
SLOW REFRESH TO  A0000              PASSED | NO FALSE PARITY ERRORS
                COPYRIGHT 1988 SUPERSOFT INC
```



**PC/XT Test Suite:**

- U3 CPU Registers and Logic
- U33 ROM POST Checksum
- U34 8253 Timer Channel 0
- U34 8253 Timer Channel 1
- U34 8253 Timer Channel 2
- U35 8237A DMA Controller
- U36 8255 Parity Detected
- 16KB Critical Memory Region
- Memory Refresh
- U2 8259 Interrupt Controller
- Hot interrupt
- Interrupt level 0
- Nonmaskable interrupt
- MDA Memory
- CGA Memory
- EGA/VGA Memory
- U4 8087 Numeric Co-Processor
- Keyboard Controller
- Keyboard Scan Lines
- Floppy Controller
- Floppy Drive Read
- System Memory to XXXXXX
- Slow Refresh to XXXXXX
- U28 System BIOS
- U29 Basic ROM 1
- U30 Basic ROM 2
- U31 Basic ROM 3
- U32 Basic ROM 4
- System Switch Settings

**AT Test Suite:**

- U74 CPU Registers and Logic
- U27 Landmark/SuperSoft ROM A Checksum
- U47 Landmark/SuperSoft ROM B Checksum
- U103 8254 Timer Channel 0
- U103 8254 Timer Channel 1
- U103 8254 Timer Channel 2
- U111 8237A DMA Controller 1
- U122 8237A DMA Controller 2
- U124 74LS612 DMA Page Registers
- U126 8042 Parity Detected
- 16KB Critical Memory Region
- Memory Refresh
- Protected Mode CPU
- U114 8259 Interrupt Controller 1
- U125 8259 Interrupt Controller 2
- Hot Interrupt
- Interrupt Level 0
- Real Time Clock Interrupt
- Nonmaskable Interrupt
- U76 Numeric Co-Processor
- U126 Keyboard Controller
- Keyboard Scan Lines
- CMOS RAM Test
- Floppy Controller
- Floppy Drive Read
- MDA Memory
- CGA Memory
- EGA/VGA Memory
- System Memory to XXXXXX
- Slow Refresh to XXXXXX
- System BIOS
- CMOS RAM Configuration



## CPU Register and Logic Tests

The CPU Register and Logic Tests perform a basic assurance test of the CPU's function. The fact that ROM POST is running is the initial indication that the CPU is working. These tests check most of the operations that the CPU will need to perform in order to successfully boot the computer. Failure of the CPU test to complete should be considered exactly as if the test returned an actual failure message. ROM POST tests the CPU by feeding instructions to the CPU and examining the results. First, the CPU is instructed to execute the basic combinations of conditional and direct jump instructions, the results of which are verified to ensure that the instructions were correctly performed. Next, the general purpose, index, and segment registers are checked to verify that they can hold several different bit combinations correctly. Finally, the CPU's basic integer mathematics instructions (add, subtract, multiply, and divide) and the string instructions are tested for correct operation. Failure of the CPU test will generate a beep code. Replace the CPU and re-run the CPU tests. If the CPU still fails, suspect support circuitry to be at fault. Closely monitor the results of the remainder of ROM POST's test suite (failure of other components in the system are usually related to failure of the CPU test).

## ROM POST Checksum Test

This test performs a checksum of the ROM POST module itself. The sum of all of the bytes in the ROM POST module should always be zero. If there is a failure in either the ROM POST module or the data and address lines to the socket containing the ROM POST module, this test will fail. A damaged ROM POST module may also fail to initialize the system at all, so that neither this test nor the CPU test can be performed. Careful handling should prevent any damage from occurring to the module. Failure of the checksum will generate a beep code. To correct this situation, first remove ROM POST and check for bent pins. Then, re-insert ROM POST and observe the results of this test once again. Before calling Technical Support to report a second failure, verify the results of this test in another system. If your ROM POST passes this test in the second system, suspect a broken trace leading to the BIOS socket(s), or possibly a bad solder joint.

**Note:** The AT version of ROM POST is a two-chip set, and each chip is tested for a good checksum. If either chip fails the checksum test, a beep code is issued.

## A Note About Chipsets

The following pages discuss the various functions that take place within a system. This manual will refer to these functions by their discreet component names (ie. 8254 Timer, 8237 DMA Controller, 8259 Interrupt Controller, etc.). It is imperative that you understand that early motherboards contained many discreet components, each performing a specific function. These discreet components are actually labelled according to their function within the system (ie. 8254, 8237, 8259, etc.). Due to technological advances in semiconductor implementations, it is now common practice for chip designers to place several of these discreet components into a single package. A couple of these hybrid packages can replace an entire motherboard of discreet components. A collection of these hybrid packages that is capable of performing the majority of the support functions needed by a system is referred to as a "chipset." This has several implications:

- Most newer motherboards have a low chip-count (few components)
- Members of a chipset are not labelled 8253, 8237, 8259, etc.
- The repair technician must know which hybrid package performs the function of the component to be replaced.

For example, the system that you are troubleshooting has failed the 8237A DMA Controller test. When you attempt to replace the 8237 DMA Controller, you are unable to find a chip labelled "8237." Upon closer inspection of the motherboard, you find that three large chips are labelled "Super-Mega Chips" (or something to that effect). At this point, you should contact the manufacturer of the Super-Mega Chips chipset to obtain more detailed information. They will be able to tell you which chip in their chipset performs the function of an 8237 DMA Controller. This is precisely the chip that you should replace.



## 8253/8254 Timer Test

The 8253 Timer can be found on PCs and XTs, while the 8254 Timer is present in AT-class systems. For diagnostic purposes, these two chips are identical (each involved in the time-of-day interrupt, dynamic memory refresh, and the generation of audio signals). Each channel of the Timer is tested to ensure that each bit in the counter register for that channel can assume either a one or a zero value. Additionally, each channel is tested to ensure that it is counting within an acceptable range of accuracy. Look for this Timer to be included in a chipset.

The Timer is a very important device and is used for controlling necessary system functions. Channel 0 of the timer is tied directly to channel 0 of the 8259 Interrupt Controller, and is used to provide a time-of-day interrupt 18.2 times every second. Timer channel 1 cycles once every 15.12 microseconds, ensuring that a memory refresh cycle is initiated at least once every 2 milliseconds. Without this channel's correct operation, system memory refresh will not occur, and thus the system will fail to boot (dynamic memory must be refreshed periodically to maintain their correct values). In a PC or XT, channel 1 is tied directly to channel 0 of the DMA Controller. Failure of the timer channels will generate a beep code. Timer channel 2 is not critical to the operation of the system. This channel is responsible for generating sine waves that produce sound from the system's speaker.

## 8237 DMA Controller Test

The 8237 DMA contains four channels that enable I/O devices to access the system's RAM without assistance from the CPU; the DMA Controller actually instructs the CPU to leave the bus while a DMA transfer is in progress. ROM POST checks the 6-bit mode word, in addition to its four 16-bit registers. In a PC or XT, channel 0 is tied directly to channel 1 of the 8253 Timer to aid in memory refresh; the 8254 Timer actually performs the refresh cycle in AT-class systems. Channel 1 is typically reserved for networks. Channel 2 is used by the floppy drive controller for DMA transfers between the floppy drive and the system's RAM. Channel 3 is unused.

This test writes, reads, and verifies that the DMA controller registers can hold all possible bit combinations, providing a basic functional test of the DMA controller. Further verification of the DMA controller is done by the Memory Refresh test and the Floppy Read test. DMA channel 2 is used to transfer data to and from system memory and the floppy disk controller. The AT has a second 8237 DMA controller which is tested in the same manner. A failure of either controller will generate a beep code. The function of the 8237 DMA Controller(s) is often included in a chipset.

Both the PC/XT and the AT have page registers that provide the DMA controller(s) with additional address lines, permitting access to more than 64KB of memory. The page registers on the PC/XT were not designed to be directly tested, however the page registers in the AT's 74LS612 can be directly tested by ROM POST. 80386 and 80486 systems are equipped with a second 74LS612 to accommodate their capabilities to access gigabytes of RAM. The page registers are tested by writing, reading, and verifying all possible bit patterns. If an error is detected, a beep code is generated. This particular chip is relatively small, and should be easy to find at your local electronics house. If the 74LS612 cannot be located, suspect that its function is included in a chipset on the motherboard.

### 8255 Parallel Peripheral Interface Test

This test exercises a portion of the 8255 PPI. The 8255 has two of its input ports connected, thus permitting the 8255 to monitor system and I/O channel memory parity errors. When the system is first initialized, no RAM accesses have been made, therefore, no parity errors should exist or be indicated by the 8255. If a parity error is being indicated by the 8255, this test will fail. Failure of this test will generate a beep code.

> **Note:** The 8255 is also responsible for reading the configuration DIP switches located on the motherboards of PCs and XTs. If a video card, portion of memory, floppy drive, or math coprocessor is not being recognized, try replacing the 8255.



### 16KB Critical Memory Region Test

This is a test of the first 16KB of memory. The memory is tested for its ability to maintain several patterns. This is the same memory test that is performed in a later test for all system memory. Functional memory in the first 16KB is a requirement to be able to boot your system. A failure in this region of memory is one possible source of a seemingly dead computer. If any failures are detected in this region of memory, a failure will be reported for this test. In the event of a failure, testing will resume at the system memory test; the other tests are bypassed because they require some functional memory in order to be performed. Failure of this memory test will generate a beep code.

In most systems, the first 16KB of memory is located in Bank 0. Replace the RAM in this bank to correct a failure. The only exception to this is when the motherboard's RAM is interleaved. Some motherboards support 2-way and 4-way interleaving of memory. The 2-way scheme separates even addresses from odd addresses. 4-way interleaving further separates the odd addresses into two sections, and the even addresses into two sections. This provides quicker access to memory in some layouts. Either disable memory interleaving and try ROM POST again, or replace the appropriate banks of memory if you are certain which banks contain the first 16KB of memory.

### Memory Refresh Test

The Memory Refresh Test verifies that all of the logic associated with memory refresh on the system board is functioning correctly. This is done by filling the first 16KB of memory with known values. The system then waits approximately 10 seconds so that no RAM memory accesses are made. Then the pattern written to memory is read and verified. If data read does not match the data written, then the test fails. A failure of this test could indicate a problem with the refresh circuitry, the 8253/8254 timer channel one (which should be initiating a refresh cycle every 15.12 microseconds), or a problem with the 8237 DMA controller channel 0 (which performs the dummy read cycle that allows refresh to occur). Failure of the refresh test will generate a beep code. Replace the Timer and observe the results. If this test still fails, try replacing the system's RAM.

### Protected Mode CPU Test (AT ROM POST only!)

This test checks the CPU's descriptor register caches, the global descriptor table register, the interrupt descriptor table register, the local descriptor table register, the task register, and the computer status register. It checks the CPU's ability to enter and run in protected mode, generate exceptions when an exception condition exists, and to perform task switching. If any errors are detected, a beep code is issued. If a failure occurs in this test, try replacing the CPU and observe results.



### 8259 Interrupt Controller Test

This is a test of the 8259 Interrupt Controller registers, performed to ensure that the 8259 can be properly initialized and that data can be correctly written to and read from its registers. The function of the 8259 Interrupt Controller is to prioritize hardware interrupts, providing arbitration between external interrupt requests from devices on the bus and the CPU. Channel 0 is used for a real-time-clock update, channel 1 is used to indicate a keypress, and channel 6 is reserved for the floppy drive controller.

PCs and XTs have one 8259 Interrupt Controller, allowing up to eight hardware interrupts to be handled. The eight channels are designated 0-7.

AT-class systems contain a second 8259 Interrupt Controller cascaded through the first controller. This allows AT-class systems to prioritize and arbitrate up to 16 hardware interrupts. The first eight channels are 0-7, while the second eight channels are designated 8-15. The AT ROM POST tests this controller in the same manner as the first Interrupt Controller.

This is the first of several tests which involves testing of the Interrupt Controller. Failure of this test will generate a beep code, and indicates a problem with the Interrupt Controller. Replacement of the 8259 is recommended.

### Hot Interrupt Test

This test disables all interrupts on the system at the 8259, it then enables interrupts to the CPU and waits approximately 1 second. During this time, the CPU will record any interrupts that may occur. Because all interrupts were disabled, none should registered by the CPU. The test fails if any interrupts occur. Failure of this test is an indication of a problem with either the 8259 Interrupt Controller, the 8288 Bus Controller, or the CPU. Detection of a hot interrupt will cause a beep code. Replace the 8259, 8288, or CPU and try again.

### Interrupt Level 0 Test

This test checks to see that time-of-day interrupt from channel 0 of the 8253/8254 Timer (which is connected to interrupt request 0 of the 8259 interrupt controller) is able to interrupt the CPU. Furthermore, the test ensures that the CPU was interrupted at the correct rate. Failure of this test can indicate a problem with either the 8253/8254 Timer, the 8259 Interrupt Controller, the 8288 Bus Controller, or the CPU; replace these components in order one at a time and observe results. Failure of this test is reported by a beep code.



### Real-Time Clock Interrupt Test (AT ROM POST Only!)

The Real-Time Clock (RTC) Interrupt Test checks the RTC to ensure that it can interrupt the CPU at the correct rate when programmed to generate interrupts, and that it does not generate interrupts when it is disabled. A failure of this test indicates a problem with the RTC, the 8259 Interrupt Controller(s), the CPU, or 8253/8254 Timer channel 0 (which is used as a basis of comparison for counting the Real-Time Clock interrupts). Replace these components in order and observe results. A failure generates a beep code.

### Nonmaskable Interrupt Test

The Nonmaskable Interrupt, or NMI, is a separate source of interrupts to the CPU and, unlike the interrupts from the 8259, NMIs cannot be inhibited (or "masked") from the CPU. The source of Nonmaskable Interrupts in PCs is the Numeric Co-Processor's Interrupt Request Line. Neither the Co-Processor nor memory parity detection logic should be generating an NMI at this point in testing. If an NMI occurs at this time, the test fails and a beep code is sounded. If a Numeric Co-processor is present, try removing it. If this test now passes, the Numeric Co-processor was at fault.

### MDA/CGA/EGA/VGA Memory Test

If an MDA, CGA, EGA, or VGA adapter is detected, a memory test is performed on the video adapter's memory. This test is similar to the system memory test, reporting a failure if any memory on the adapter should fail the test. When testing an EGA or VGA adapter, memory is tested in 64KB banks up to a total of 256KB of RAM (depending upon the amount of memory that can be detected). If a particular adapter is not detected in the system, then the result of the test for that adapter will be "NOT PRESENT." Failure of any of these tests will cause a beep code to be issued. Upon failure, ensure that the video adapter is installed properly, or try another adapter.

> **Note:** Memory above 256KB will not be tested, as this will not prevent your system from booting to DOS. Software diagnostics (such as Landmark's Service Diagnostics) can more thoroughly test the graphics memory and extended capabilities of your video adapter.

### Numeric Co-Processor Test

The Numeric Co-Processor Test first identifies whether or not a co-processor is installed. If there is no co-processor, the test concludes by reporting that the co-processor is "NOT PRESENT." If the co-processor is installed in the system, then a register test of the Numeric Co-Processor is performed to verify that it can properly obtain the system bus and perform data read and write operations. Failure of the Co-Processor will generate a beep code. This test performs basic logic testing of the co-processor instruction set. To do further testing of the Numeric Co-Processor, use the Co-Processor test of Service Diagnostics (check with your Product Consultant for further information concerning Service Diagnostics).

### Keyboard Controller Test

This test initializes the keyboard and Keyboard Controller subsystem in the computer. The test fails if the controller does not complete the reset and initialization properly, or if either too many or too few interrupts from the Keyboard Controller are received by the CPU.

> **Note:** Just as in the level 0 interrupt test, passing this test also requires the proper operation of other system board devices such as the 8259 Interrupt Controller, the 8288 Bus Controller (to process interrupts), and the 8255 Parallel Peripheral Interface controller (to receive scan codes from the Keyboard Controller).

The Keyboard Controller Test will generate a beep code upon failure. If using an extended keyboard, ensure that the "XT/AT" switch is properly positioned. This can be located on the back of the keyboard, or possibly under a cover or in a recess. The Keyboard Controller has the physical appearance of a system BIOS, although having several more pins than the system BIOS. Most motherboards have the Keyboard Controller positioned next to the keyboard connector, toward the rear by the power supply connectors. Most supplier's of system BIOSes also carry Keyboard Controllers. The biggest cause of failure of this component is static discharge from your fingertips when plugging or unplugging the keyboard. Always touch a metal portion of the case before attempting to disconnect or reconnect the keyboard.



### Keyboard Scan Line Test

This test verifies that no keys on the keyboard are stuck. During this test, the system waits for scan codes from the Keyboard Controller. If any scan codes are generated, it is an indication of a scan line problem or a stuck key, so the test fails. The test will fail if you are typing on the keyboard during this part of the test, or if the test is entered while one of the shift keys is depressed (Control, Alt, Shift, Caps Lock, Num Lock, or Scroll Lock will also cause a failure if active when the test is executing). This test may also fail if the previous test of the Keyboard Controller failed. This test will cause a beep code if the test fails. Stuck keys can easily be remedied by disassembling the keyboard, cleaning the post of the troublesome key with soap and water, allowing to air dry, and reassembling the keyboard.

### CMOS RAM Test (AT ROM POST Only!)

The CMOS RAM Test reads the contents of the CMOS RAM and stores the information in system RAM. Next, the test writes, reads, and verifies several patterns to the CMOS RAM. Any errors in verifying the contents of the RAM is a failure and generates a beep code. After the test is completed, the contents of the CMOS RAM before the test started are restored.

> **Warning!!!** If ROM POST is aborted (by turning the computer off) during this test, the contents of the CMOS RAM may be corrupted which will require that the system be reconfigured. If the CMOS RAM becomes badly corrupted, you may have to remove the CMOS battery (check the system board, or the sides of the case for this battery). Most batteries have a connector that can be unplugged from the motherboard. For batteries that are wedged between two metal clips, simply pull the battery free. Batteries can even be soldered in place, in which case you will need to desolder one side of the battery. With the battery removed, connect the exposed terminals by placing a screwdriver or short piece of wire between them for a short period of time (about a second or two). This will re-initialize the CMOS RAM.

### Floppy Controller Test

This test initializes the Floppy Controller subsystem. The test then performs read/write tests on the Floppy Controller registers, verifying that the controller was properly initialized for operation. The Floppy Controller can be a single card on the I/O bus, it can be built into the Hard Drive Controller, or it can be built into the motherboard itself. If two Floppy Controllers are present, only the primary controller will be tested. Failure of this test will cause a beep code. Probable causes of failure include a loose/broken data or power cable, or incorrect configuration of the floppy drives. In AT-class systems, verify the CMOS setup. If problems persist, verify the switch settings on the Floppy Controller, or replace.

### Floppy Read Test

This test causes the Floppy Controller to turn on the motor of the A: drive, recalibrate the drive to track 0, and read the first sector on head zero track zero of the floppy in drive A:. Any diskette errors will cause the test to fail. The test performs the same type of operation that is performed by the system BIOS when it is booting the system from a floppy disk. In order to pass this test, the floppy drive will need to contain a formatted floppy disk. ROM POST can test a 1.2MB floppy in a 1.2MB drive, a 360KB floppy in a 1.2MB drive, a 360KB floppy in a 360KB drive, a 1.44MB floppy in a 1.44MB drive, a 720KB floppy in a 1.44MB drive, and a 720KB floppy in a 720KB drive. If a read error occurs during the test, the drive is recalibrated and the test repeated five times before a failure is reported. Failure of the floppy read test will generate a beep code.

> **Note:** The floppy tests in ROM POST will not work with floppy drives that require any form of driver software. This includes drivers that allow high-density drives to work with older PCs, in addition to external floppy drives that connect to the system via the serial or parallel ports.



### System Memory Test

This test verifies the integrity of the system memory. The PC/XT test will test up to 640KB of RAM. For the AT, the test will check conventional memory up to 640KB and then extended memory starting at 1MB (up to a maximum of 64MB). ROM POST, however, will neither identify nor test expanded (EMS/EEMS/LIM/bank switched) memory adapters. This should not be problem, however, since faulty expanded memory will not keep your system from booting to DOS. The test stores a number of patterns to memory, then reads back and verifies the pattern. The test writes patterns of all zero bits, all one bits, a pattern which produces odd parity, and a pattern of bits that alternate as zero's and one's. In addition to the test being reported as failing when an error occurs, each failing address is reported in the diagnostic summary as the physical address that failed and the bit or bits that were incorrect. After each byte is read and determined to be correct, a test is made to determine whether a parity error has occurred with that particular read operation. The address of any parity error is reported in the diagnostic summary. A parity error without a data error would be an indication of a failure of the parity chip at that address. A failure of this memory test will generate a beep code.

- **Static RAM**

Static RAM, or cache RAM, cannot be tested due to the fact that this region of RAM is not mapped into the address space of the CPU. The CPU is not aware of the presence of the cache, and goes about addressing memory exactly the same as an un-cached system. Though there are several different caching schemes in use, the concept is similar across the board; CPU memory fetches are filled with values from fast (sub-10 nanosecond) static RAM whenever the contents of the desired memory location is present in the cache. Otherwise, the data is actually fetched from the dynamic RAM location, and held in the cache in case the CPU wants that information again. If this cache is defective, the system will probably give the appearance of a dead CPU. Replace the static RAM cache only under the instruction of the motherboard manufacturer.

**• Interpretation of Memory Tests**

The failure information can be used to determine the cause of the failure, although this is more of an art than science. Memory is said to fail when it cannot read the same data written, or is reading/writing data from/to the wrong location. The first errors are called data errors and the latter are called addressing errors. All failures are identified down to the bit level. This is useful, since many RAM chips are organized by bit. That is, each chip holds one bit within a particular region (1KB, 4KB, 16KB, 256KB, 1024KB, or 4096KB regions are typical). Since chips tend to fail individually, this will locate the particular chip that has failed. Memory chips are often socketed and can be replaced easily. If you do not have spare memory chips and do not have chip locating information, you can still debug the memory by swapping chips until the problem moves.

To determine which chip or chips has failed based on the addresses reported, a few simple calculations must be made. To begin, determine the type of each bank of chips in the computer. The chips will be 16K, 64K, 128K, 256K, 1024K, or 4096K in size.

> **Note:** Only the oldest computers will use 16K, such as the original IBM PC. This computer had four banks of 16K chips on the system board to comprise the lowest 64K of RAM. Only the original IBM AT will have 128K chips. These chips can be found easily, because they are actually two chips piggy-backed (soldered) together.

Unless the computer has 16K chips, the first two digits of the memory address starting at the left are the significant digits in locating a failing chip; the other digits are provided for determination of addressing problems.

The first digit will be 0 for all memory that makes up the 640K of conventional RAM in the computer. If the first digit is non-zero, then the failing memory is located in extended memory on 80286, 80386, and 80486 systems (starting at 1MB).



The second digit will identify which bank contains the failing chip for the region under test. The value of the second digit of the number is equivalent to a 64K segment of memory, with the first segment starting at 0. The determination of this address is going to vary according to the arrangement of the banks of memory.

8088 CPU's typically have memory arranged in byte banks. For example, if the address of the error is 009000h, then the error occurred in the first bank. If the address of the failing memory is 030101h, then some calculations must be performed. The **'3'** indicates that the error is in the fourth 64K of memory in the computer (remember that **'0'** was the first 64K in the computer). If 64K chips comprise the first four banks, then the error is in the fourth bank. However, if the system board is filled with 128K chips, then the error would be found in the second bank, since the first bank of chips would be the first and second 64K segments in the computer and the second bank would be the third and fourth 64K segments in the computer.

If the computer is populated with 256K chips, the error would be in the first bank, since this would comprise the first four 64K segments of memory.

If the computer is populated with 1024K chips, the error would be in the first bank, since this would comprise the first sixteen 64K segments of memory.

If the computer is populated with 4096K chips, the error would be in the first bank, since this would comprise the first sixty-four 64K segments of memory.

The failing chip can then be found be counting from the first chip in the bank which would be bit **'0'**, the second chip being bit **'1'**, and so on, until the failing bit is reached.

All computer with 80386SX, 80286, 80186, V30, and 8086 processors have 16 data lines. The banks of memory are arranged in words. For PC compatibles, this arrangement may be true only for the system board.

Memory boards on the I/O bus with two edge connectors (16-bit) use word arrangement, while those with only one edge connector are byte banked (8-bit).

> **Note:** Memory on the IBM PC bus (add-on memory) is always byte banked, since the PC only has an 8-bit bus.

Machines with 80386 CPU's (except the 80386SX) and 80486 CPU's use 32 data lines for memory on the system board or memory that plugs into special connectors on the system board (memory bus). These CPU's are likely to have memory arranged in double word (32-bit, or 4-byte) banks. The memory size of each bank would be four times the size of the chips in that bank.

To determine the failing chip in systems with memory addressed as (16-bit) words, the banks may comprise one or two physical rows of chips containing 18 chips if parity is being checked, or 16 chips if parity checking is not provided. The size of each of these banks is double the size of the chips. In other words, a bank containing 64K chips will represent 128K of memory in the system and a bank of 256K chips will represent 512K of system memory. For example, an error at address 090105 in a computer with 64K chips would be in the fifth 128K bank of memory. (The **'9'** tells us that the error is in the tenth 64K segment, which would be the fifth 128K bank). To determine the failing chip the last digit of the number must be examined. If the last digit is even, then the failing chip is in the first physical row or half of the bank, if the last digit is odd, then the failing chip is in the second physical row or half of the bank.

Having determined which half of the bank contained the error, the chip can be determined by counting from the first chip as bit **'0'** and so on until the failing chip is located.



To determine the failing chip in systems with memory addressed as long (32-bit) words, the banks may comprise one, two, or four physical rows of chips containing 34 chips if parity is being checked, or 18 chips if parity checking is not provided. The size of each of these banks is four times the size of the chips. In other words, a bank containing 64K chips will represent 256K of memory in the system, a bank of 256K chips will represent 1024K of system memory, a bank of 1024K chips will represent 4096K of system memory, and a bank of 4096K chips will represent 16384K. For example, an error at address 090105 in a computer with 64K chips would be in the fifth 128K bank of memory. (The **'9'** tells us that the error is in the tenth 64K segment, which would be the fifth 128K bank). To determine the failing chip the last digit of the number must be examined. If the last digit is even, then the failing chip is in the first physical row or half of the bank, if the last digit is odd, then the failing chip is in the second physical row or half of the bank.

Having determined which half of the bank contained the error, the chip can be determined by counting from the first chip as bit **'0'** and so on until the failing chip is located.

One final word on determining the location of a failing chip. Some computers may not use 1-bit chips, they may use 4-bit chips, or some other configuration. In these cases, locating the correct bank will be the same as before, but locating the chip within the bank will depend on size of chip. As an example, if the error is in bit **'5'**, and the computer uses 4-bit chips, then the second chip is the source of the failure.

> **Note:** Consult your memory board hardware manual for further information concerning the arrangement of memory.

### Slow-Refresh Memory Test

The Slow-Refresh Test is similar to the System Memory Test with two important differences. The System Memory Test detects hard (persistent) memory errors. The Slow-Refresh Memory Test is a tool to help pinpoint which chip is the source of the intermittent memory errors such as "PARITY CHECK." The test works by slowing the refresh interval for memory from 15 microsecond intervals to a 2 millisecond interval. This test is only usefully for dynamic memory that must be refreshed.

Each bit in a dynamic memory chip consists of a single transistor used as a capacitor. The image written to memory must be refreshed periodically to recharge the capacitor, and thus restore the data. The test works by slowing the refresh rate, writing a pattern to memory, and reading back the data after a ten second delay. Any weak cells in the chips will fail. A chip that fails the slow memory refresh test does not necessarily need to be replaced unless it was also failed the System Memory Test. On the other hand, if the system is being plagued by intermittent memory errors, the first chips to be replaced should be the chips that fail the Slow-Refresh Memory Test. A failure of this test will cause a beep code.

> **Note:** The type of memory package (DIP, SIP, or SIMM) and the speed (persistence rating in nanoseconds) does not have any bearing upon the results of this test.

### System BIOS Test

The System BIOS Test is a checksum test of the system BIOS(es). This test is only applicable to original IBM PC/XTs and IBM ATs. IBM motherboards have sockets adjacent to the BIOS sockets, into which ROM BASIC is usually inserted. If the system BIOS(es) are placed into these adjacent sockets, ROM POST will perform a test of the system BIOS(es). The socket is labelled U28 on a PC/XT, while an AT's sockets are labelled U17 and U37. A failure of this test should be ignored unless you have installed the system BIOS(es) as previously mentioned. Failure of this test will cause a beep code to sound. Upon failure, ensure that each BIOS was installed correctly and observe results. Failure at this point indicates a faulty BIOS, and the failing chip should be replaced.



### BASIC ROM Module Test (PC/XT ROM POST Only!)

This test performs a checksum of the ROM modules in U29, U30, U31, and U32 of the IBM PC or XT system board. This test may fail on IBM XT-compatible computers. A failure of this test on any other computer should be ignored. A failure of the test on an IBM PC or XT is an indication of a fault in the ROM BASIC installed in the computer. Such a failure is not critical to computer operation unless the user of the system uses cassette basic or the BASIC interpreter supplied with the IBM PC or XT. If any one of the BASIC ROM tests fails, a beep code will be issued. As with the system BIOS, make sure that the BASIC ROM modules are correctly installed, and attempt this test once again. Continued failure indicates the need to replace the BASIC ROM module.

### System Switch Settings (PC/XT ROM POST Only!)

The system switch settings are both an informational display and a test of the switches and the 8255 Parallel Peripheral Interface (PPI) which reads the switch settings when requested by the CPU. The settings should be verified against what is actually set in the system. Although the switches would not cause the system to fail to boot properly in most cases, a discrepancy between the setting of a switch and what is displayed on the screen is either a failure of the switch or a failure of the 8255 PPI.

If your computer initializes and goes through the POST without any errors, but begins the POST again instead of booting, that may be an indication of a failure of either the 8255 or switch position 1 on switch bank 1. When this position is set to ON, the POST is instructed to loop rather then continue with the boot up process, even after completing an otherwise successful initialization.

There are two switch blocks to locate on the system board. They are usually labeled switch block 1 (S1 or SW1) and switch block 2 (S2 or SW2). Switch block 1 is interpreted as follows:

- Positions 1, 7, and 8 indicate the number of diskette drives installed in the system.
- Position 2, when ON, indicates the presence of a Numeric Co-Processor.
- Positions 5 and 6, when OFF, indicate a Monochrome display is installed. When 5 is OFF and 6 is ON, this indicates that a Graphics display capable of 40 by 25 characters is installed. 5 OFF and 6 ON indicates that the display is capable of 80 by 25 characters.
- Positions 3 and 4 indicate the amount of low memory in 16K increments. These positions are interpreted as the complement of a binary number (that is, {3:ON, 4:ON} is 16K; {3:OFF, 4:ON} is 32K; {3:ON, 4:OFF} is 48K; and {3:OFF, 4:OFF} is 64K). These positions are usually both OFF indicating at least 64K of memory.
- Switch block 2 positions 1, 2, 3, 4, and 5 indicate the amount of memory above 64K in increments of 32K. These positions are interpreted as the complement of a binary number. Switch block 2 positions 6, 7, and 8 should always be OFF.

### CMOS RAM Configuration (AT ROM POST Only!)

The contents of the CMOS configuration RAM are read and displayed on the screen. If the configuration is incorrect, the computer should be re-initialized. A sample format of the configuration display is as follows:

```
FLOPPY TYPES    A:1.2M  B:360K
HARD DISK TYPES     0:02    1:00
MATH CO-PROCESSOR:  NOT PRESENT
BASE: 640K      EXPANSION 00000K
CMOS RAM CHECKSUM:  VALID
DATE 12/30/91   TIME 11:23:33
```



If these setting are invalid, they must be corrected. This is accomplished by running a program such as IBM's SETUP.COM, however, most BIOSes have a setup program in ROM that is accessible from a keyboard sequence. Consult your computer's manual for further information on setup.

An incorrect CMOS setting may cause your system to be unable to boot. This requires the use of the ROM setup if available. If your system does not have a ROM setup or you do not know how to access it, there are several techniques to try. One technique is to alter your system's configuration (remove floppy drives or remove memory, for instance). This will sometimes cause the ROM setup to come up. Another technique is to remove the CMOS battery connection from your system board and to wait for the CMOS to discharge, causing it to "forget" its configuration. Shorting the motherboard connections after removing the battery may help speed up the discharging. This discharging may take a while (try leaving the battery disconnected overnight). Sometimes a key sequence will force the system BIOS to take you to the CMOS setup utility. Try <Ctl><Alt><S> or <Ctl><Alt><Esc>.

## Beep Codes by Hi/Lo-Short Count

| PC/XT Beep Codes | | | |
|---|---|---|---|
| **Hi/Lo** | **Short** | **Chip** | **Error** |
| 1 | 1 | U3 | 8088/8086 CPU registers and logic |
| 1 | 2 | U33 | ROM POST checksum |
| 1 | 3 | U34 | 8253 Timer channel 0 |
| 1 | 4 | U34 | 8253 Timer channel 1 |
| 1 | 5 | U34 | 8253 Timer channel 2 |
| 1 | 6 | U35 | 8237A DMA controller |
| 1 | 7 | U36 | 8255 Parity detected |
| 1 | 8 | | 16K critical memory region |
| 1 | 9 | | Memory refresh |
| 2 | 1 | U2 | 8259 Interrupt controller |
| 2 | 2 | | Hot interrupt |
| 2 | 3 | | Interrupt level 0 |
| 2 | 4 | | Nonmaskable interrupt (NMI) |
| 2 | 5 | | MDA memory |
| 2 | 6 | | CGA memory |
| 2 | 7 | | EGA/VGA memory |
| 2 | 8 | U4 | Numeric Co-Processor |
| 2 | 9 | | Keyboard controller |
| 3 | 1 | | Keyboard scan lines |
| 3 | 2 | | Floppy controller |
| 3 | 3 | | Floppy disk read |
| 3 | 4 | | System memory at address 00000 |
| 3 | 5 | | Slow refresh at address 00000 |



| PC/XT Beep Codes (cont.) | | | |
|---|---|---|---|
| **Hi/Lo** | **Short** | **Chip** | **Error** |
| 4 | 1 | U28 | System BIOS |
| 4 | 2 | U29 | BASIC ROM 1 |
| 4 | 3 | U30 | BASIC ROM 2 |
| 4 | 4 | U31 | BASIC ROM 3 |
| 4 | 5 | U32 | BASIC ROM 4 |
| 4 | 6 | | Total passes completed 00000 |
| 4 | 7 | | Total errors 00000 |
| 5 | 8 | | Cannot initialize monitor |
| 5 | 9 | | Cannot initialize monitor |
| 6 | 1 | | Cannot initialize monitor |

| AT Beep Codes | | | |
|---|---|---|---|
| **Hi/Lo** | **Short** | **Chip** | **Error** |
| 1 | 1 | U74 | 80286/80386/80486 CPU registers and logic |
| 1 | 2 | U27 | ROM POST A checksum |
| 1 | 3 | U47 | ROM POST B checksum |
| 1 | 4 | U103 | 8254 Timer channel 0 |
| 1 | 5 | U103 | 8254 Timer channel 1 |
| 1 | 6 | U103 | 8254 Timer channel 2 |
| 1 | 7 | U111 | 8237A DMA controller 1 |
| 1 | 8 | U122 | 8237A DMA controller 2 |
| 1 | 9 | U124 | 74LS612 DMA page register |
| 1 | 10 | U126 | 8042 parity detected |
| 2 | 1 | | 16K critical memory region |
| 2 | 2 | | Memory refresh |
| 2 | 3 | | Protected mode CPU |
| 2 | 4 | U114 | 8259 interrupt controller 1 |
| 2 | 5 | U125 | 8259 interrupt controller 2 |
| 2 | 6 | | Hot interrupt |
| 2 | 7 | | Interrupt level 0 |
| 2 | 8 | | Real time clock interrupt |
| 2 | 9 | | Nonmaskable interrupt (NMI) |
| 2 | 10 | U76 | 80x87 Numeric Co-Processor |



| AT Beep Codes (cont.) | | | |
|---|---|---|---|
| **Hi/Lo** | **Short** | **Chip** | **Error** |
| 3 | 1 | U126 | Keyboard controller |
| 3 | 2 | | Keyboard scan lines |
| 3 | 3 | | CMOS RAM |
| 3 | 4 | | Floppy adapter |
| 3 | 5 | | Floppy read |
| 3 | 6 | | MDA memory |
| 3 | 7 | | CGA memory |
| 3 | 8 | | EGA/VGA memory |
| 3 | 9 | | System BIOS |
| 4 | 1 | | System memory at address 00000 |
| 4 | 2 | | Slow refresh at address 00000 |
| 4 | 5 | | Total passes completed 00000 |
| 5 | 8 | | Cannot initialize monitor |
| 5 | 9 | | Cannot initialize monitor |
| 6 | 1 | | Cannot initialize monitor |