RTL8111B
RTL8168B

INTEGRATED GIGABIT ETHERNET CONTROLLER FOR PCI EXPRESS™ APPLICATIONS

REGISTERS DATASHEET

Rev. 1.0
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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's register information on the Realtek RTL8111B and RTL8168B chips.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2006/01/26	First release.

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1. General Description

The Realtek RTL8111B/RTL8168B Gigabit Ethernet controllers combine a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111B/RTL8168B offer high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The devices support the PCI Express 1.0a bus interface for host communications with power management and comply with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. They also support an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet™, Re-LinkOK, and Microsoft® Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e. main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111B/RTL8168B.

The RTL8111B/RTL8168B fully comply with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and support IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The devices also features next-generation interconnect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial interconnect technology that offers significant improvements in performance over conventional PCI, and also maintains software compatibility with existing PCI infrastructure.

The RTL8168B supports the attachment of a 64Kbyte external Serial Peripheral Interface (SPI) Flash. The AT25F512 interface permits the RTL8168B to read from, and write data to, an external SPI Flash device, and provides 64Kbytes of serial re-programmable Flash memory.

Note: The RTL8111B does not support SPI.

The RTL8111B/RTL8168B is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Register Descriptions

The RTL8111B/RTL8168B provide the following set of operational registers mapped into PCI memory space and I/O space.

2.1. MAC Registers

Table 1. MAC Registers

Offset	Tag	RW	Description
0000h	IDR0	RW	ID Register 0. ID registers 0-5 are only permitted to read/write via 4-byte access. Read access can be byte, word, or double word access. The initial value is autoloaded from the EEPROM EthernetID field.
0001h	IDR1	RW	ID Register 1
0002h	IDR2	RW	ID Register 2
0003h	IDR3	RW	ID Register 3
0004h	IDR4	RW	ID Register 4
0005h	IDR5	RW	ID Register 5
0006h-0007h	-	-	Reserved
0008h	MAR7	RW	Multicast Address Register 7. The MAR register 0-7 are only permitted to read/write via 4-byte access. Read access can be byte, word, or double word access. The driver is responsible for initializing these registers.
0009h	MAR6	RW	Multicast Register 6
000Ah	MAR5	RW	Multicast Register 5
000Bh	MAR4	RW	Multicast Register 4
000Ch	MAR3	RW	Multicast Register 3
000Dh	MAR2	RW	Multicast Register 2
000Eh	MAR1	RW	Multicast Register 1
000Fh	MAR0	RW	Multicast Register 0
0010h-0017h	DTCCR	RW	Dump Tally Counter Command Register (64-byte alignment)
0018h-001Fh	-	-	Reserved
0020h-0027h	TNPDS	RW	Transmit Normal Priority Descriptors: Start address (64-bit). (256-byte alignment)
0028h-002Fh	THPDS	RW	Transmit High Priority Descriptors: Start address (64-bit). (256-byte alignment)
0030h-0036h	-	-	Reserved
0037h	CR	RW	Command Register
0038h	TPPoll	W	Transmit Priority Polling register
0039h-003Bh	-	-	Reserved
003Ch-003Dh	IMR	RW	Interrupt Mask Register
003Eh-003Fh	ISR	RW	Interrupt Status Register
0040h-0043h	TCR	RW	Transmit (Tx) Configuration Register
0044h-0047h	RCR	RW	Receive (Rx) Configuration Register

Offset	Tag	RW	Description
0048h-004Bh	TCTR	RW	Timer CounT Register: This register contains a 32-bit general-purpose timer. Writing any value to this 32-bit register will reset the original timer and begin the count from zero. This counter is based on the PCI clock connected. For PCI-E NICs, the internal PCI clock is 125MHz. Therefore, the unit of TCTR of the RTL8111B/RTL8168B is 8ns.
004Ch-004Fh	-	-	Reserved
0050h	9346CR	RW	93C46 Command Register
0051h	CONFIG0	RW	Configuration Register 0
0052h	CONFIG1	RW	Configuration Register 1
0053h	CONFIG2	RW	Configuration Register 2
0054h	CONFIG3	RW	Configuration Register 3
0055h	CONFIG4	RW	Configuration Register 4
0056h	CONFIG5	RW	Configuration Register 5
0057h	-	-	Reserved
0058h-005Bh	TimerInt	R /W	Timer Interrupt Register. Once having written a non-zero value to this register, the Timeout bit of the ISR register will be set whenever the TCTR reaches that value. The Timeout bit will never be set whilst the TimerInt register is zero.
005Ch-005Fh	-	-	Reserved
0060h-0063h	PHYAR	RW	PHY Access Register
0064h-006Bh	-	-	Reserved
006Ch	PHYStatus	R	PHY Status Register
006Dh~0083h	-	-	Reserved
0084h–008Bh	Wakeup0	RW	Power Management wakeup frame0 (64bit)
008Ch–0093h	Wakeup1	RW	Power Management wakeup frame1 (64bit)
0094h–009Bh	Wakeup2LD	RW	Power Management wakeup frame2 (128bit), Low DWord
009Ch–00A3h	Wakeup2HD	RW	Power Management wakeup frame2, High DWord
00A4h–00ABh	Wakeup3LD	RW	Power Management wakeup frame3 (128bit), Low DWord
00ACh–00B3h	Wakeup3HD	RW	Power Management wakeup frame3, High DWord
00B4h–00BBh	Wakeup4LD	RW	Power Management wakeup frame4 (128bit), Low DWord
00BCh–00C3h	Wakeup4HD	RW	Power Management wakeup frame4, High DWord
00C4h-00C5h	CRC0	RW	16-bit CRC of wakeup frame 0
00C6h-00C7h	CRC1	RW	16-bit CRC of wakeup frame 1
00C8h-00C9h	CRC2	RW	16-bit CRC of wakeup frame 2
00CAh-00CBh	CRC3	RW	16-bit CRC of wakeup frame 3
00CCh-00CDh	CRC4	RW	16-bit CRC of wakeup frame 4
00CEh-00D9h	-	-	Reserved
00DAh-00DBh	RMS	RW	Rx packet Maximum Size
00DCh-00DFh	-	-	Reserved
00E0h-00E1h	C+CR	RW	C+ Command Register
00E2h-00E3h	-	-	Reserved
00E4h-00EBh	RDSAR	RW	Receive Descriptor Start Address Register (256-byte alignment)
00ECh	MTPS	RW	Max Transmit Packet Size Register
00EDh-00FFh	-	-	Reserved

2.2. DTCCR: Dump Tally Counter Command (Offset 0010h-0017h, RW)

Table 2. DTCCR: Dump Tally Counter Command (Offset 0010h-0017h, RW)

<table>
<tr><th>Bit</th><th>Symbol</th><th>RW</th><th>Description</th></tr>
<tr><td>63-6</td><td>CntrAddr</td><td>RW</td><td>Starting address of the 12 Tally Counters being dumped to. (64-byte alignment address, 64 bytes long)
<table>
<tr><th>Offset of Starting Address</th><th>Counter</th><th>Description</th></tr>
<tr><td>0</td><td>TxOk</td><td>64-bit counter of Tx Ok packets.</td></tr>
<tr><td>8</td><td>RxOk</td><td>64-bit counter of Rx Ok packets.</td></tr>
<tr><td>16</td><td>TxER</td><td>64-bit packet counter of Tx errors including Tx abort, carrier lost, Tx underrun, and out of window collision.</td></tr>
<tr><td>24</td><td>RxEr</td><td>32-bit packet counter of Rx errors including CRC error packets (should be larger than 8 bytes)</td></tr>
<tr><td>28</td><td>MissPkt</td><td>16-bit counter of missed packets (CRC Ok) resulted from Rx FIFO full.</td></tr>
<tr><td>30</td><td>FAE</td><td>16-bit counter of Frame Alignment Error packets (MII mode only)</td></tr>
<tr><td>32</td><td>Tx1Col</td><td>32-bit counter of Tx Ok packets with only 1 collision before Tx Ok.</td></tr>
<tr><td>36</td><td>TxMCol</td><td>32-bit counter of Tx Ok packets with more than 1, and less than 16 collisions before Tx Ok.</td></tr>
<tr><td>40</td><td>RxOkPhy</td><td>64-bit counter of Rx Ok packets with physical address matching destination ID.</td></tr>
<tr><td>48</td><td>RxOkBrd</td><td>64-bit counter of Rx Ok packets with broadcast destination ID.</td></tr>
<tr><td>56</td><td>RxOkMul</td><td>32-bit counter of Rx Ok packets with multicast destination ID.</td></tr>
<tr><td>60</td><td>TxAbt</td><td>16-bit counter of Tx abort packets.</td></tr>
<tr><td>62</td><td>TxUndrn</td><td>16-bit counter of Tx underrun and discard packets (only possible on jumbo frames).</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>Cmd</td><td>RW</td><td>Command: When set, the RTL8111B/RTL8168B begins dumping 13 Tally counters to the address specified above.
When this bit is reset by the RTL8111B/RTL8168B, the dumping has been completed.</td></tr>
<tr><td>2-0</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

2.3. Command (Offset 0037h, RW)

Table 3. Command (Offset 0037h, RW)

Bit	Symbol	RW	Description
7-5	-	-	Reserved
4	RST	RW	Reset: Set this bit to 1 to force the RTL8111B/RTL8168B into a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, and resets the system buffer pointer to the initial value (the start address of each descriptor group set in TNPDS, THPDS, and RDSAR registers). The values of IDR0-5, MAR0-7 and PCI configuration space will have no changes. This bit is 1 during the reset operation, and is self-cleared to 0 when the reset operation is complete.
3	RE	RW	Receiver Enable
2	TE	RW	Transmitter Enable
1-0	-	-	Reserved

2.4. TPPoll: Transmit Priority Polling (Offset 0038h, RW)

Table 4. TPPoll: Transmit Priority Polling (Offset 0038h, RW)

Bit	Symbol	RW	Description
7	HPQ	W	High Priority Queue polling: Writing a '1' to this bit will notify the RTL8111B/RTL8168B that there is a high priority packet(s) waiting to be transmitted. The RTL8111B/RTL8168B will clear this bit automatically after all high priority packets have been transmitted. Writing a '0' to this bit has no effect.
6	NPQ	W	Normal Priority Queue polling: Writing a '1' to this bit will notify the RTL8111B/RTL8168B that there is a normal priority packet(s) waiting to be transmitted. The RTL8111B/RTL8168B will clear this bit automatically after all normal priority packets have been transmitted. Writing a '0' to this bit has no effect.
5-1	-	-	Reserved
0	FSWInt	W	Forced Software Interrupt: Writing a '1' to this bit will trigger an interrupt, and the SWInt bit (bit8, ISR, offset3Eh-3Fh) will set. The RTL8111B/RTL8168B will clear this bit automatically after the SWInt bit (bit8, ISR) is cleared. Writing a '0' to this bit has no effect.

2.5. Interrupt Mask (Offset 003Ch-003Dh, RW)

Table 5. Interrupt Mask (Offset 003Ch-003Dh, RW)

Bit	Symbol	RW	Description
15	-	-	Reserved
14	TimeOut	RW	Time Out Interrupt: 1: Enable, 0: Disable.

Bit	Symbol	RW	Description
13-10	-	-	Reserved
9	FEmp	RW	Rx FIFO empty under FIFO full Status Interrupt: 1: Enable, 0: Disable.
8	SWInt	RW	Software Interrupt: 1: Enable, 0: Disable.
7	TDU	RW	Tx Descriptor Unavailable Interrupt: 1: Enable, 0: Disable.
6	FOVW	RW	Rx FIFO Overflow Interrupt: 1: Enable: Software must read FEmp to confirm the FIFO is empty, then write one to FOVW of ISR to clear this bit. 0: Disable: Hardware automatically clears Rx FIFO full in ISR when the Rx FIFO empty..
5	LinkChg	RW	Link Change Interrupt: 1: Enable, 0: Disable.
4	RDU	RW	Rx Descriptor Unavailable Interrupt: 1: Enable, 0: Disable.
3	TER	RW	Tx Error Interrupt: 1: Enable, 0: Disable.
2	TOK	RW	Tx OK: Transmit (Tx) OK: Indicates that a packet transmission has completed successfully. 1: Enable, 0: Disable.
1	RER	RW	Rx Error Interrupt: 1: Enable, 0: Disable.
0	ROK	RW	Rx OK Interrupt: 1: Enable, 0: Disable.

2.6. Interrupt Status (Offset 003Eh-003Fh, RW)

Table 6. Interrupt Status (Offset 003Eh-003Fh, RW)

Bit	Symbol	RW	Description
15	-	-	Reserved
14	TimeOut	RW	Time Out: This bit is set to 1 when the TCTR register reaches the value of the TimerInt register.
13-10	-	-	Reserved
9	FEmp	RW	Rx FIFO empty under FIFO full Status Interrupt: When set, this bit indicates that the Rx FIFO is empty after an Rx FIFO full indication.
8	SWInt	RW	Software Interrupt: This bit is set to 1 whenever a '1' is written by software to FSWInt (bit0, offset D9h, TPPoll register).
7	TDU	RW	Tx Descriptor Unavailable: When set, this bit indicates that the Tx descriptor is unavailable.
6	FOVW	RW	Rx FIFO Overflow: This bit set to 1 is caused by RDU, poor PCI performance, or overloaded PCI traffic.

Bit	Symbol	RW	Description
5	LinkChg	RW	Link Change: This bit is set to 1 when link status is changed.
4	RDU	RW	Rx Descriptor Unavailable: When set to 1, this bit indicates that the Rx descriptor is unavailable.
3	TER	RW	Transmit (Tx) Error: This bit set to 1 indicates that a packet transmission was aborted, due to excessive collisions.
2	TOK	RW	Transmit (Tx) OK: When set to 1, this bit indicates that a packet transmission has been completed successfully.
1	RER	RW	Receive (Rx) Error: When set to 1, this bit indicates that a packet has either a CRC error or a frame alignment error (FAE). An Rx CRC error packet is determined according to the settings of RER8, AER, and AR bits in the RCR register (offset 44h-47h).
0	ROK	RW	Receive (Rx) OK: In normal mode, this bit set to 1 indicates the successful completion of a packet reception.

Note: Writing 1 to any bit in the ISR will reset that bit.

2.7. Transmit Configuration (Offset 0040h-0043h, RW)

Table 7. Transmit Configuration (Offset 0040h-0043h, RW)

<table>
<tr><th>Bit</th><th>Symbol</th><th>RW</th><th>Description</th></tr>
<tr><td>31-30</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>29-28</td><td>HWVERID0</td><td>R</td><td>Hardware Version ID0:
<table>
<tr><th></th><th>Bit29</th><th>Bit28</th><th>Bit26</th><th>Bit23</th></tr>
<tr><td>RTL8111B/RTL8168B</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>RTL8100E</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>RTL8101E</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>27</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>26</td><td>HWVERID1</td><td>R</td><td>Hardware Version ID1: Please refer to HWVERID0 (above).</td></tr>
<tr><td>25-24</td><td>IFG1, 0</td><td>RW</td><td>InterFrame Gap Time: This field allows the InterFrame gap time to be longer than the standards of 9.6µs for 10Mbps, 960ns for 100Mbps, and 96ns for 1000Mbps. The time can be programmed from 9.6µs to 14.4µs (10Mbps), 960ns to 1440ns (100Mbps), and 96ns to 144ns (1000Mbps).
The setting of the InterFrame gap is:
<table>
<tr><th colspan="3">IFG[2:0]</th><th>IFG@1000MHz (ns)</th><th>IFG@100MHz (ns)</th><th>IFG@10MHz (us)</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>96</td><td>960</td><td>9.6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>96 + 8</td><td>960 + 8 * 10</td><td>9.6 + 8 * 0.1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>96 + 16</td><td>960 + 16 * 10</td><td>9.6 + 16 * 0.1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>96 + 24</td><td>960 + 24 * 10</td><td>9.6 + 24 * 0.1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>96 + 48</td><td>960 + 48 * 10</td><td>9.6 + 48 * 0.1</td></tr>
<tr><td colspan="6">Other values are reserved.</td></tr>
</table></td></tr>
<tr><td>23</td><td>HWVERID2</td><td>R</td><td>Hardware Version ID2: Please refer to HWVERID0 (bits 29-28 above).</td></tr>
<tr><td>22-20</td><td>-</td><td></td><td>Reserved</td></tr>
<tr><td>19</td><td>IFG2</td><td>RW</td><td>InterFrameGap2</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Symbol</th><th>RW</th><th>Description</th></tr>
<tr><td>31-30</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>29-28</td><td>HWVERID0</td><td>R</td><td>Hardware Version ID0:
<table>
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<tr><td>RTL8111B/RTL8168B</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>RTL8100E</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>RTL8101E</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>27</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>26</td><td>HWVERID1</td><td>R</td><td>Hardware Version ID1: Please refer to HWVERID0 (above).</td></tr>
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<tr><td>0</td><td>1</td><td>0</td><td>96 + 48</td><td>960 + 48 * 10</td><td>9.6 + 48 * 0.1</td></tr>
<tr><td colspan="6">Other values are reserved.</td></tr>
</table></td></tr>
<tr><td>18, 17</td><td>LBK1, LBK0</td><td>RW</td><td>Digital Loopback test: The digital loopback function is independent of the current link status.
For analog loopback tests, software must force the phyceiver into loopback mode through PHYAR register while the RTL8111B/RTL8168B operates normally.
00 : Normal operation
01 : MAC loopback mode
10 : Reserved
11 : Reserved</td></tr>
<tr><td>16</td><td>TX_NOCRC</td><td>RW</td><td>NO CRC: Setting this bit to 1 means that there is no CRC appended at the end of a packet. Setting to 0 means that there is a CRC appended at the end of a packet.</td></tr>
<tr><td>15-11</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>10-8</td><td>MXDMA2, 1, 0</td><td>RW</td><td>Max DMA Burst Size per Tx DMA Burst: This field sets the maximum size of transmit DMA data bursts according to the following table:
000: 16 bytes
001: 32 bytes
010: 64 bytes
011: 128 bytes
100: 256 bytes
101: 512 bytes
110: 1024 bytes
111: Unlimited</td></tr>
<tr><td>7-0</td><td>-</td><td>-</td><td>Reserved</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Symbol</th><th>RW</th><th>Description</th></tr>
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<tr><td>0</td><td>1</td><td>0</td><td>96 + 48</td><td>960 + 48 * 10</td><td>9.6 + 48 * 0.1</td></tr>
<tr><td colspan="6">Other values are reserved.</td></tr>
</table></td></tr>
</table>

Note: The Transmit Configuration register can only be changed after having set TE (bit2, Command register, offset 0037h).

2.8. Receive Configuration (Offset 0044h-0047h, RW)

Table 8. Receive Configuration (Offset 0044h-0047h, RW)

Bit	Symbol	RW	Description
31-16	-	-	Reserved
15-13	RXFTH2, 1, 0	RW	Rx FIFO Threshold: Specifies the Rx FIFO Threshold level. When the number of the received data bytes from a packet, which is being received into the RTL8111B/RTL8168B's Rx FIFO, has reached this level (or the FIFO contains a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following list: 000: Reserved 001: Reserved 010: 64 bytes 011: 128 bytes 100: 256 bytes 101: 512 bytes 110: 1024 bytes 111: No Rx threshold. The RTL8111B/RTL8168B begins the transfer of data after having received a whole packet in the FIFO.
12-11	-	-	Reserved

Bit	Symbol	RW	Description
10-8	MXDMA2, 1, 0	RW	Max DMA Burst Size per Rx DMA Burst: This field sets the maximum size of the receive DMA data bursts according to the following list: 000: Reserved 001: Reserved 010: 64 bytes 011: 128 bytes 100: 256 bytes 101: 512 bytes 110: 1024 bytes 111: Unlimited
7	-	-	Reserved
6	9356SEL	R	This bit reflects what type of EEPROM is used. 1: The EEPROM used is 9356. 0: The EEPROM used is 9346.
5	AER	RW	Accept Error Packet: When set to 1, all packets with CRC error, alignment error, and/or collided fragments will be accepted. When set to 0, all packets with CRC error, alignment error, and/or collided fragments will be rejected.
4	AR	RW	Accept Runt: This bit set to 1 allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt.
3	AB	RW	Accept Broadcast Packets: 1: Accept, 0: Reject
2	AM	RW	Accept Multicast Packets: 1: Accept, 0: Reject
1	APM	RW	Accept Physical Match Packets: 1: Accept, 0: Reject
0	AAP	RW	Accept All Packets with Destination Address: 1: Accept, 0: Reject

2.9. 9346CR: 93C46 (93C56) Command (Offset 0050h, RW)

Table 9. 9346CR: 93C46 (93C56) Command (Offset 0050h, RW)

<table>
<tr><th>Bit</th><th>Symbol</th><th>RW</th><th>Description</th></tr>
<tr><td>7-6</td><td>EEM1-0</td><td>RW</td><td>Operating Mode: These 2 bits select the RTL8111B/RTL8168B operating mode.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (RTL8111B/RTL8168B network/host communication mode)</td></tr>
<tr><td>0</td><td>1</td><td>Auto-load: Entering this mode will make the RTL8111B/RTL8168B load the contents of the 93C46 (93C56) as when the PCI RSTB signal is asserted. This auto-load operation will take about 2ms.</td></tr>
<tr><td>1</td><td>0</td><td>93C46 (93C56) programming: In this mode, both network and host bus master operations are disabled. The 93C46 (93C56) can be directly accessed via bit3-0 which now reflect the states of EECS, EESK, EEDI, & EEDO pins respectively.</td></tr>
<tr><td>1</td><td>1</td><td>Config register write enable: Before writing to CONFIGx registers, the RTL8111B/RTL8168B must be placed in this mode. This will prevent RTL8111B/RTL8168B configurations from accidental change.</td></tr>
<tr><td></td><td></td><td></td></tr>
</table></td></tr>
<tr><td>4-5</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3</td><td>EECS</td><td>RW</td><td rowspan="4">These bits reflect the state of the EECS, EESK, EEDI, and EEDO pins in auto-load or 93C46 (93C56) programming mode, and are valid only when the Flash bit is cleared.
Note: EESK, EEDI and EEDO are valid after boot ROM complete.</td></tr>
<tr><td>2</td><td>EESK</td><td>RW</td></tr>
<tr><td>1</td><td>EEDI</td><td>RW</td></tr>
<tr><td>0</td><td>EEDO</td><td>R</td></tr>
</table>

2.10. CONFIG 0 (Offset 0051h, RW)

Table 10. CONFIG 0 (Offset 0051h, RW)

Bit	Symbol	RW	Description
7-3	-	-	Reserved
2-0	BS2, BS1, BS0	R	Select Boot ROM Size

BS2	BS1	BS0	Description
0	0	0	No Boot ROM
0	0	1	8K Boot ROM
0	1	0	16K Boot ROM
0	1	1	32K Boot ROM
1	0	0	64K Boot ROM
1	0	1	128K Boot ROM
1	1	0	Reserved
1	1	1	Reserved

2.11. CONFIG 1 (Offset 0052h, RW)

Table 11. CONFIG 1 (Offset 0052h, RW)

Bit	Symbol	RW	Description
7-6	LEDS1-0	RW	Refer to the LED PIN definition. The initial value of the 2 bits com from 93C46/93C56. Refer to section 6.3 LED Functions, page 63, for a detailed LED pin description. The initial value of these bits comes from the 93C46/93C56.
5-4	-	-	Reserved.
3	MEMMAP	R	Memory Mapping: The operational registers are mapped into PCI memory space. Always 1.
2	IOMAP	R	I/O Mapping: The operational registers are mapped into PCI I/O space. Always 1.
1	VPD	R	Vital Product Data: Set to enable Vital Product Data. Always 1.
0	PMEn	R	Power Management Enable: Always 1.

2.12. CONFIG 2 (Offset 0053h, RW)

Table 12. CONFIG 2 (Offset 0053h, RW)

Bit	Symbol	RW	Description
7-5	-	-	Reserved
4	Aux_Status	R	Auxiliary Power Present Status: 1: Aux. Power is present. 0: Aux. Power is absent. The value of this bit is fixed after each PCI reset.
3-0	-	-	Reserved.

2.13. CONFIG 3 (Offset 0054h, RW)

Table 13. CONFIG 3 (Offset 0054h, RW)

Bit	Symbol	RW	Description
7	-	-	Reserved
6	VPDSel	RW	VPD Offset Select: 1'b0 (default) : VPD address start point = 40h 1'b1 : VPD address start point = 00h
5	Magic	RW	Magic Packet. This bit is valid when the PWEn bit of the CONFIG1 register is set. The RTL8111B/RTL8168B will assert the PMEB signal to wakeup the operating system when a Magic Packet is received. Once the RTL8111B/RTL8168B has been enabled for Magic Packet wakeup, it scans all incoming packets addressed to the node for a specific data sequence that indicates to the controller that this is a Magic Packet. A Magic Packet must also meet the basic requirements of: Destination address + Source address + data + CRC. The destination address may be the node ID of the receiving station or a multicast address, which includes the broadcast address. The specific sequence consists of 16 duplications of a 6-byte ID register, with no breaks nor interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE MAC address match the address of the ID register. If the Node ID is 11h 22h 33h 44h 55h 66h, then the format of the Magic frame looks like the following: Destination address + source address + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC
4-0	-	-	Reserved

2.14. CONFIG 4 (Offset 0055h, RW)

Table 14. CONFIG 4 (Offset 0055h, RW)

Bit	Symbol	RW	Description
7-0	-	-	Reserved

2.15. CONFIG 5 (Offset 0056h, RW)

Table 15. CONFIG 5 (Offset 0056h, RW)

Bit	Symbol	RW	Description
7	-	-	Reserved
6	BWF	RW	Broadcast Wakeup Frame: 1: Enable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF. 0: Default value. Disable Broadcast Wakeup Frame with mask bytes of only DID field = FF FF FF FF FF FF. The power-on default value of this bit is 0.
5	MWF	RW	Multicast Wakeup Frame: 1: Enable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address. 0: Default value. Disable Multicast Wakeup Frame with mask bytes of only DID field, which is a multicast address. The power-on default value of this bit is 0.
4	UWF	RW	Unicast Wakeup Frame: 1: Enable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address. 0: Default value. Disable Unicast Wakeup Frame with mask bytes of only DID field, which is its own physical address. The power-on default value of this bit is 0.
3-0	-	-	Reserved

2.16. PHYAR: PHY Access (Offset 0060h-0063h, RW)

Table 16. PHYAR: PHY Access (Offset 0060h-0063h, RW)

Bit	Symbol	RW	Description
31	Flag	RW	Flag bit, used as PCI VPD access method: 1: Write data to MII register, and indicate 0 automatically whenever the RTL8111B/RTL8168B has completed writing to the specified MII register. 0: Read data from MII register, and indicate 1 automatically whenever the RTL8111B/RTL8168B has completed retrieving data from the specified MII register.
30-21	-	-	Reserved
20-16	RegAddr 4-0	RW	5-bit GMII/MII register address.
15-0	Data15-0	RW	16-bit GMII/MII register data.

2.17. PHYStatus: PHY Status (Offset 006Ch, R)

Table 17. PHYStatus: PHY Status (Offset 006Ch, R)

Bit	Symbol	RW	Description
7	-	-	Reserved
6	TxFlow	R	Transmit Flow Control: 1: Enabled, 0: Disabled.
5	RxFlow	R	Receive Flow Control: 1: Enabled, 0: Disabled.
4	1000MF	R	Link speed is 1000Mbps and in full-duplex (GMII mode only).
3	100M	R	Link speed is 100Mbps (GMII or MII mode only).
2	10M	R	Link speed is 10Mbps (GMII or MII mode only).
1	LinkSts	R	Link Status. 1: Link Ok, 0: No Link.
0	FullDup	R	Full-Duplex Status: 1: Full-duplex mode, 0: Half-duplex mode.

Note1: This register is updated continuously at maximum periods of 300μs.
*Note2: MII registers polling cycle: 320ns * (32 MDC clock + 32 MDC clock) * 6 registers.*

2.18. RMS: Receive (Rx) Packet Maximum Size (Offset 00DAh-00DBh, R)

Table 18. RMS: Receive (Rx) Packet Maximum Size (Offset 00DAh-00DBh, R)

Bit	Symbol	RW	Description
15-14	-	-	Reserved
13-0	RMS	RW	Rx packet Maximum Size: This register should be always be set to a value other than 0, in order to receive packets. The maximum Rx packet size supported is 16000 bytes. If a received packet of packet length larger than the value set here, then it will set both RWT and RES bits in the corresponding Rx Status Descriptor. If the packet, which is larger than the RMS value, is received without CRC error, it is still a good packet, although both RWT and RES bits are set in the corresponding Rx Status Descriptor.

2.19. C+CR: C+ Command (Offset 00E0h-00E1h, RW)

Table 19. C+CR: C+ Command (Offset 00E0h-00E1h, RW)

Bit	Symbol	RW	Description
15-7	-	-	Reserved
6	RxVLAN	RW	Receive VLAN De-tagging Enable: 1: Enable. 0: Disable.
5	RxChkSum	RW	Receive Checksum Offload Enable: 1: Enable. 0: Disable.
4:0	-	-	Reserved

Note1: This register is the key before configuring other registers and descriptors.
Note2: This register is word access only. Byte access to this register has no effect.

2.20. RDSAR: Receive Descriptor Start Address (Offset 00E4h-00EBh, RW)

Table 20. RDSAR: Receive Descriptor Start Address (Offset 00E4h-00EBh, RW)

Bit	Symbol	RW	Description
63-0	RDSA	RW	Receive Descriptor Start Address: 64-bit address, 256-byte alignment address. Bit[31:0]: Offset E7h-E4h, low 32-bit address. Bit[63:32]: Offset EBh-E8h, high 32-bit address.

2.21. MTPS: Max Transmit Packet Size (Offset 00ECh, RW)

Table 21. MTPS: Max Transmit Packet Size (Offset 00ECh, RW)

Bit	Symbol	RW	Description
7-6	-	-	Reserved
5-0	MTPS	RW	Max Tx Packet Size: Specifies the maximum packet size that the RTL8111B/RTL8168B is to transmit. These fields count from 000001 to 111111 in unit of 128 bytes. For regular LAN applications, i.e., the max packet size is either 1518 or 1522(VLAN) bytes, this field must be larger than the max packet size. E.g., 0x0C. 000000 is reserved. This is the default value after power-on. The driver must set to a value other than 0 for correct operation. Do not set to this value. To support Jumbo Frame without possible Tx underruns, this field is suggested to be larger than the maximum packet transmitted. The maximum Jumbo Frame (without possible Tx underruns) that the RTL8111B/RTL8168B is able to transmit is 7440 (7436 + 4-byte CRC) bytes, therefore, this field has to be set to values larger than that to transmit a Jumbo Frame packet of size up to 7440 bytes. Ex., 0x3B (7552) bytes. If the MTPS is set to a value larger than 0x3B, the maximum length of packets transmitted can not exceed 7440 (7436 + CRC) bytes. If the MTPS is set to a value less than 0x3B, ex. 0x1F, then, as long as the PCI performance is good enough such that there's no Tx underruns, the length of the transmitted packet might be larger than 7440 bytes. Drivers should have to take good care of this configuration to transmit packets larger than 7440 bytes on different PC platforms to prevent from Tx underruns.

3. PHY Register Description

3.1. PHY Register Definitions

Register maps and address definitions are given in Table 22:

Table 22. PHY Register Definitions

Offset	Access	Tag	Description
0	RW	BMCR	Basic mode control register
1	RO	BMSR	Basic mode status register
2	RO	PHYAD1	PHY identifier register 1
3	RO	PHYAD2	PHY identifier register 2
4	RW	ANAR	Auto-negotiation advertising register
5	RW	ANLPAR	Auto-negotiation link partner ability register
6	RW	ANER	Auto-negotiation expansion register
7	RW	ANNPTR	Auto-negotiation next page transmit register
8	RW	ANNRPR	Auto-negotiation next page receive register
9	RW	GBCR	1000Base-T control register
10	RO	GBSR	1000Base-T status register
11-14	RO	Reserved	
15	RO	GBESR	1000Base-T extended status register
25-31	RO	Reserved	

3.2. PHY Register

3.2.1. BMCR (Address 0x00)

Table 23. BMCR (Address 0x00)

Bit	Name	RW	Default	Description
15	Reset	RW	0	Reset: 1: Initiate software Reset / Reset in Process. 0: Normal operation. This bit sets the status and control registers of the PHY to their default states. This bit, which is self-clearing, returns a value of one until the reset process is complete. Reset is finished once the Auto-Negotiation process has begun or the device has entered its forced mode.
14	Loopback	RW	0	Loopback: 1: Loopback enabled. 0: Normal operation. The loopback function enables MII/GMII transmit data to be routed to the MII/GMII receive data path.

Bit	Name	RW	Default	Description
13	Speed[0]	RW	0	Speed Select: When Auto-Negotiation is disabled, bits 6 and 13 select device speed selection per table below: Speed[1] Speed[0] Speed Enabled 11: Reserved 10: 1000 Mb/s 01: 100 Mb/s 00: 10 Mb/s
12	ANE	RW	1	Auto-Negotiation Enable: 1: Auto-Negotiation Enabled - bits 6, 8 and 13 of this register are ignored when this bit is set. 0: Auto-Negotiation Disabled - bits 6, 8 and 13 determine the link speed and mode.
11	PWD	RW	0	Power Down: 1: Power down (only Management Interface and logic active.) 0: Normal operation.
10	Isolate	RW	0	Isolate: 1: Isolates the Port from the MII with the exception of the serial management. 0: Normal operation.
9	Restart_AN	RW	0	Restart Auto-Negotiation: 1: Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0: Normal operation.
8	Duplex	RW	1	Duplex Mode: 1: Full Duplex operation. Duplex selection is allowed only when Auto-Negotiation is disabled (bit 12 = 0). 0: Half Duplex operation.
7	Reserved	RW	0	
6	Speed[1]	RW	1	Speed Select: See description for bit 13.
5:0	Reserved	RO	000000	Reserved by IEEE

3.2.2. BMSR (Address 0x01)

Table 24. BMSR (Address 0x01)

Bit	Name	RW	Default	Description
15	100Base-T4	RO	0	100Base-T4 Capable: 1: Device able to perform 100Base-T4 mode. 0: Device not able to perform 100Base-T4 mode. RTL8111B/RTL8168B does not support 100Base-T4 mode and bit should always be read back as '0'.
14	100Base-TX(full)	RO	1	100Base-TX Full Duplex Capable: 1: Device able to perform 100Base-TX in full duplex mode. 0: Device unable to perform 100Base-TX in full duplex mode.
13	100Base-TX(half)	RO	1	100Base-TX Half Duplex Capable: 1: Device able to perform 100Base-TX in half duplex mode. 0: Device unable to perform 100Base-TX in half duplex mode.
12	10Base-T(full)	RO	1	10Base-T Full Duplex Capable: 1: Device able to perform 10Base-T in full duplex mode. 0: Device unable to perform 10Base-T in full duplex mode.
11	10Base-T(half)	RO	1	10Base-T Half Duplex Capable: 1: Device able to perform 10Base-T in half duplex mode. 0: Device unable to perform 10Base-T in half duplex mode.
10	100Base-T2(full)	RO	0	100Base-T2 Full Duplex Capable: 1: Device able to perform 100Base-T2 Full Duplex mode. 0: Device unable to perform 100Base-T2 Full Duplex mode. RTL8111B/RTL8168B does not support 100Base-T2 mode and bit should always be read back as '0'.
9	100Base-T2(half)	RO	0	100Base-T2 Half Duplex Capable: 1: Device able to perform 100Base-T2 Half Duplex mode. 0: Device unable to perform 100Base-T2 Full Duplex mode. RTL8111B/RTL8168B does not support 100Base-T2 mode and bit should always be read back as '0'.
8	1000Base-T Extended status	RO	1	1000Base-T Extended Status Register: 1: Device supports Extended Status Register 0x0F (15). 0: Device does not supports Extended Status Register 0x0F
7	Reserved	RO	0	Reserved
6	Preamble Suppression	RO	1	Preamble suppression Capable: 1: Device is able to perform management transaction with preamble suppressed, 32-bits of preamble is needed only once after reset, invalid opcode or invalid turnaround.
5	Auto-Negotiation Complete	RO	0	Auto-Negotiation Complete: 1: Auto-Negotiation process complete, and contents of registers 5, 6, 7, & 8 are valid. 0: Auto-Negotiation process not complete.

Bit	Name	RW	Default	Description
4	Remote Fault	RO	0	Remote Fault: 1: Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from Link Partner of Remote Fault. 0: No remote fault condition detected.
3	Auto-Negotiation Ability	RO	1	Auto Configuration Ability: 1: Device is able to perform Auto-Negotiation. 0: Device is not able to perform Auto-Negotiation.
2	Link Status	RO	0	1: Link is up 0: Link is down This bit indicates if link was lost since the last read.
1	Jabber detect	RO	0	1: Jabber condition detected 0: Jabber condition not detected
0	Extended Capability	RO	1	1: Extended register capability is enabled 0: Extended register capability is disabled

3.2.3. PHY Identifier Register 1 (Address 0x02)

Table 25. PHY Identifier Register 1 (Address 0x02)

Bit	Name	RW	Default	Description
15:0	OUI_MSB	RO	001C	Organization unique identifier

3.2.4. PHY Identifier Register 2 (Address 0x03)

Table 26. PHY Identifier Register 2 (Address 0x03)

Bit	Name	RW	Default	Description
15:0	OUI_LSB	RO	C910	Organization unique identifier

3.2.5. ANAR (Address 0x04)

Table 27. ANAR (Address 0x04)

Bit	Name	RW	Default	Description
15	NextPage	RW	0	1: Advertise 0: Not advertised
14	Resv	RO	0	
13	Remote fault	RW	0	1: Set Remote Fault bit 0: Do not set Remote Fault bit
12	Resv	RW	0	
11	Asymmetric PAUSE	RW	0	1: Asymmetric Pause 0: No asymmetric Pause
10	PAUSE	RW	0	1: MAC PAUSE implemented 0: MAC PAUSE not implemented
9	100Base-T4	RO	0	0: Not capable of 100Base-T4
8	100Base-TX(full)	RW	1	1: Advertise 0: Not advertised
7	100Base-TX(half)	RW	1	1: Advertise 0: Not advertised
6	10Base-T(full)	RW	1	1: Advertise 0: Not advertised
5	10Base-T(half)	RW	1	1: Advertise 0: Not advertised
4:0	Selector field	RO	00001	For 802.3

3.2.6. ANLPAR (Address 0x05)

Table 28. ANLPAR (Address 0x05)

Bit	Name	RW	Default	Description
15	Next Page	RO	0	Received Code Word Bit 15
14	ACK	RO	0	Received Code Word Bit 14
13	Remote Fault	RO	0	Received Code Word Bit 13
12:5	Technology Ability Field	RO	0	Received Code Word Bit 12:5
4:0	Selector Field	RO	0	Received Code Word Bit 4:0

3.2.7. ANER (Address 0x06)

Table 29. ANER (Address 0x06)

Bit	Name	RW	Default	Description
15:5	resv	RO	0	Resv
4	Parallel Detection Fault	RO	0	1: A fault has been detected via the Parallel Detection function 0: A fault has not been detected via the Parallel Detection function
3	Link Partner Next Pageable	RO	0	1: Link Partner is Next Page capable 0: Link Partner is not Next Page capable
2	Local Next Pageable	RO	1	1: Local Device is Next Page able
1	Page Received	RO	0	1: A New Page has been received 0: A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0	1: Link Partner is Auto-Negotiation capable 0: Link Partner is not Auto-Negotiation capable

3.2.8. ANNPTR (Address 0x07)

Table 30. ANNPTR (Address 0x07)

Bit	Name	RW	Default	Description
15	Next Page	RW	0	Transmit Code Word Bit 15
14	Resv	RO	0	Transmit Code Word Bit 14
13	Message Page	RW	1	Transmit Code Word Bit 13
12	Acknowledge 2	RO	0	Transmit Code Word Bit 12
11	Toggle	RO	0	Transmit Code Word Bit 11
10:0	Message/Unformatted Field	RW	0x001	Transmit Code Word Bit 10:0

3.2.9. ANNPRR(Address 0x08)

Table 31. ANNPRR(Address 0x08)

Bit	Name	RW	Default	Description
15	Reserved	RO	0	Received Code Word Bit 15
14	Acknowledge	RO	0	Received Code Word Bit 14
13	Message Page	RO	0	Received Code Word Bit 13
12	Acknowledge 2	RO	0	Received Code Word Bit 12
11	Toggle	RO	0	Received Code Word Bit 11
10:0	Message/Unformatted Field	RO	0x00	Received Code Word Bit 10:0

3.2.10. GBCR (Address 0x09)

Table 32. GBCR (Address 0x09)

Bit	Name	RW	Default	Description
15:13	Test Mode	RW	0	000: Normal Mode 001: Test Mode 1 - Transmit Jitter Test 010: Test Mode 2 - Transmit Jitter Test (MASTER mode) 011: Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100: Test Mode 4 - Transmit Distortion Test 101, 110, 111: Reserved
12	MASTER/SLAVE Manual Configuration Enable	RW	0	1: Manual MASTER/SLAVE configuration 0: Automatic MASTER/SLAVE
11	MASTER/SLAVE Configuration Value	RW	0	1: Manual configure as MASTER 0: Manual configure as SLAVE
10	Port Type	RW	0	1: Prefer multi-port device (MASTER) 0: Prefer single port device (SLAVE)
9	1000Base-T Full Duplex	RW	0	1: Advertise 0: Not advertised
8	1000Base-T Half Duplex	RW	0	1: Advertise 0: Not advertised
7:0	Resv	RW	0	Reserved

3.2.11. GBSR (Address 0x0A)

Table 33. GBSR (Address 0x0A)

Bit	Name	RW	Default	Description
15	MASTER/SLAVE Configuration Fault	RO	0	1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected
14	MASTER/SLAVE Configuration Resolution	RO	0	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
13	Local Receiver Status	RO	0	1: Local Receiver OK 0: Local Receiver Not OK
12	Remote Receiver Status	RO	0	1: Remote Receiver OK 0: Remote Receiver Not OK
11	Link Partner 1000Base-T Full Duplex Capability	RO	0	1: Link Partner is capable of 1000BASET full duplex 0: Link Partner is not capable of 1000Base-T full duplex
10	Link Partner 1000Base-T Half Duplex Capability	RO	0	1: Link Partner is capable of 1000BASET half duplex 0: Link Partner is not capable of 1000Base-T half duplex
9:8	Reserved	RO	00	Reserved
7:0	Idle Error Count	RO	0x00	MSB of Idle Error Counter

3.2.12. GBESR (Address 0x0F)

Table 34. GBESR (Address 0x0F)

Bit	Name	RW	Default	Description
15	1000BASE-X FD	RO	0	0: not 1000BASE-X full duplex capable
14	1000BASE-X HD	RO	0	0: not 1000BASE-X half duplex capable
13	1000Base-T FD	RO	1	1: 1000Base-T full duplex capable
12	1000Base-T HD	RO	1	1: 1000Base-T half duplex capable
11:0	Reserved	RO	0	Reserved

4. EEPROM (93C46/93C56) Contents

The RTL8111B/RTL8168B requires the attachment of an external EEPROM. The 93C46 is a 1K-bit EEPROM (the 93C56 is a 2K-bit EEPROM). The EEPROM interface provides the ability for the RTL8111B/RTL8168B to read from and write data to an external serial EEPROM device. Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following internal power on reset or software EEPROM autoload command. The RTL8111B/RTL8168B autoloads values from the EEPROM to these fields in configuration space and I/O space. If the EEPROM is not present, the RTL8111B/RTL8168B initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using “bit-bang” accesses via the 9346CR Register, or using PCI VPD.

Although it is actually addressed by words, its contents are listed below by bytes for convenience. After the initial power on or auto-load command in 9346CR, the RTL8111B/RTL8168B performs a series of EEPROM read operations from the 93C46 (93C56) Address 00h to 3Fh.

We recommend you obtain Realtek approval before changing the default settings of the EEPROM.

Table 35. EEPROM Contents

Bytes	Contents	Description
00h	29h	These 2 bytes contain ID code words for the RTL8111B/RTL8168B. The RTL8111B/RTL8168B will load the contents of the EEPROM into the corresponding location if the ID word (8129h) is correct. Otherwise, the Vendor ID and Device ID of the PCI configuration space are "10ECh" and "8129h".
01h	81h	
02h-03h	VID	PCI Vendor ID: PCI configuration space offset 00h-01h.
04h-05h	DID	PCI Device ID: PCI configuration space offset 02h-03h.
06h-07h	SVID	PCI Subsystem Vendor ID: PCI configuration space offset 2Ch-2Dh.
08h-09h	SMID	PCI Subsystem ID: PCI configuration space offset 2Eh-2Fh.
0Ah	BAR2	PCI BAR2[7:0] : 04h for 64-bit MEM, 00h for 32-bit MEM.
0Bh	BAR0	PCI BAR0[7:0] : 01h for IO.
0Ch	CONFIGx	Reserved.
0Dh	CONFIG3	RTL8111B/RTL8168B Configuration register 3: Operational register offset 54h.
0Eh-13h	Ethernet ID	Ethernet ID: After auto-load command or hardware reset, the RTL8111B/RTL8168B loads Ethernet ID to IDR0-IDR5 of the RTL8111B/RTL8168B's I/O registers.
14h	CONFIG0	RTL8111B/RTL8168B Configuration register 0: Operational registers offset 51h.

Bytes	Contents	Description
15h	CONFIG1	RTL8111B/RTL8168B Configuration register 1: Operational registers offset 52h.
16h-17h	PMC	Reserved: Do not change this field without Realtek approval. Power Management Capabilities. PCI configuration space addresses 42h and 43h.
18h	Express Cap	[7] => memory space offset 6D bit [7] [6:5] =>Reserved. [4] => configuration space offset 62h bit[4] [3:0] => memory space offset 6D bit [3:0]
19h	CONFIG4	Reserved: Do not change this field without Realtek approval. RTL8111B/RTL8168B Configuration register 4, operational registers offset 55h.
1Ah	Express Device Capability	PCIE configuration space offset 64h
1Bh		PCIE configuration space offset 65h
1Ch	Link Control / Status	PCIE configuration space offset 70h
1Dh		PCIE configuration space offset 73h
1Eh	PCIE Link Cap	[3:2] => PCIE configuration space offset 6Dh bit[3:2]
1Fh	CONFIG_5	Do not change this field without Realtek approval.
20h-27h	Serial Number	PCIE configuration space offset 14Ch-153h
28h	PM Exit Control	PCIE configuration space offset B4h
29h		PCIE configuration space offset B5h
2Ah		PCIE configuration space offset B6h
2Bh		PCIE configuration space offset B7h
2Ch	Active PM Timer	PCIE configuration space offset B8h
2Dh		PCIE configuration space offset B9h
2Eh	EPHY2	[7:3] => EPHY Register Offset 0x01 bit[15:11] [2:0] => EPHY Register Offset 0x00 bit[5:3]
2Fh	ROMBAR	PCI Expansion ROM BAR Offset 30h
30h	VSR P Credit	PCIE configuration space offset 96h
31h	EPHY0	[7:4] => EPHY Register Offset 0x07 bit[15,14,10,9] [3:2] => EPHY Register Offset 0x00 bit[7:6] [1] => EPHY Register Offset 0x01 bit[4] [0] => EPHY Register Offset 0x07 bit[11]
32h-33h	CheckSum	Reserved: Do not change this field without Realtek approval. Checksum of the EEPROM content.
34h	VSR P Credit	PCIE configuration space offset 94h
35h		PCIE configuration space offset 95h
36h	VSR NP Credit	PCIE configuration space offset 99h
37h		PCIE configuration space offset 9Ah
38h	VSR CPL Credit	PCIE configuration space offset 9Ch
39h		PCIE configuration space offset 9Dh
3Ah	VSR Link Timer	PCIE configuration space offset B2h
3Bh		PCIE configuration space offset B3h
3Ch	EPHY1	[7:3] => EPHY Register Offset 0x06 bit[14:12,8:7]
3Dh	VSR Link Timer	PCIE configuration space offset B1h
3Eh		PCIE configuration space offset B0h

Bytes	Contents	Description
3Fh	PXE_Para	Reserved: Do not change this field without Realtek approval. PXE ROM code parameter.
40h-7Fh	VPD_Data	VPD data field: Offset 40h is the start address of the VPD data.
80h-FFh	CIS_Data	CIS data field: Offset 80h is the start address of the CIS data.(Not for 93C46)

4.1. EEPROM Related Ethernet MAC Registers

Table 36. EEPROM Related MAC Registers

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h-05h	IDR0 – IDR5	RW*								
51h	CONFIG0	R		-	-	-	-	BS2	BS1	BS0
		W*	-	-	-	-	-	-	-	-
52h	CONFIG1	R	LEDS1	LEDS0	DVRLOAD	LWACT	-	-	-	-
		W*	LEDS1	LEDS0	DVRLOAD	LWACT				
53h	CONFIG2	R	-	-	-	-	-	-	-	-
		W*	-	-	-	-	-	-	-	-
54h	CONFIG3	R	-	-	Magic	LinkUp	-	-	-	-
		W*	-	-	Magic	LinkUp	-	-	-	-
55h	CONFIG4	RW*	-	-	-	LWPME	-	LWPTN	-	-
56h	CONFIG5	RW*	-	-	-	-	-	-	-	-

Note: Registers marked with type = 'W' can be written only if bits EEM1=EEM0=1.*

4.2. EEPROM Related Power Management Registers

Table 37. EEPROM Related Power Management Registers

Configuration Space offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
43h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2

5. PCI EXPRESS™

5.1. PCI EXPRESS™ Bus Interface

The RTL8111B/RTL8168B is compliant with PCI Express™ Base Specification Revision 1.0a, and is running at 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pairs. The RTL8111B/RTL8168B supports 4 kinds of PCI Express™ messages, interrupt messages, error messages, power management messages, and hot-plug messages. The PCI Express™ lane polarity reversal and link reversal are also supported to ease PCB layout constraints.

5.1.1. PCI Express™ Transmitter

The RTL8111B/RTL8168B's PCI Express™ block receives digital data recovered from Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. The data scrambling is used for reducing the possibility of electrical resonance on the link, and the 8B/10B coding technology is used for the benefits of embedded clocking, error detection, and DC balance by sacrificing the 25 percent overhead to the system through the addition of 2 extra bits. Then, the data code groups are passed through its serializer for packet framing to generate 2.5 Gbps serial data and transmitted onto PCB trace to its upstream device via differential driver.

5.1.2. PCI Express™ Receiver

The RTL8111B/RTL8168B's PCI Express™ block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are resynchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data descrambling, the original digital data is able to be recovered and then the data is passed to the RTL8111B/RTL8168B's internal Ethernet MAC to be transmitted on to Ethernet.

5.2. PCI Configuration Space Table

Table 38. PCI Configuration Space Table

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	PERRSP	0	0	0	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	IntDisable	0	SERREN
		W	-	-	-	-	-	IntDisable	-	SERREN

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	Status	R	0	0	0	1	IntSt	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	0	0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	0	1
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	RW	CLS7	CLS6	CLS5	CLS4	CLS3	CLS2	CLS1	CLS0
0Dh	LTR	R	0	0	0	0	0	0	0	0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		RW	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		RW	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		RW	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h-17h	Reserved									
18h	MEM 64 BAR	R	0	0	0	0	MEM64	0	0	0
19h		RW	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
1Ah		RW	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
1Bh		RW	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
1Ch		RW	MEM39	MEM38	MEM37	MEM36	MEM35	MEM34	MEM33	MEM32
1Dh		RW	MEM47	MEM46	MEM45	MEM44	MEM43	MEM42	MEM41	MEM40
1Eh		RW	MEM55	MEM54	MEM53	MEM52	MEM51	MEM50	MEM49	MEM48
1Fh		RW	MEM63	MEM62	MEM61	MEM60	MEM59	MEM58	MEM57	MEM56
20h-27h	RESERVED									
28h-2Bh	CISPtr	CardBus CIS Pointer								
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		RW	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		RW	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap_Ptr	R	0	1	0	0	0	0	0	0
35h-3Bh	RESERVED									
3Ch	ILR	RW	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	0	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Fh	MXLAT	R	0	0	0	0	0	0	0	0
40h	PMID	R	0	0	0	0	0	0	0	1
41h	NextPtr	R	0	1	0	0	1	0	0	0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
43h		R	PME_D3_{cold}	PME_D3_{hot}	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
44h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
45h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
46-47h	Reserved									
48h	VPDID	R	0	0	0	0	0	0	1	1
49h	NextPtr	R	0	1	0	1	0	0	0	0
4Ah	Flag VPD Address	RW	VPDADDR7	VPDADDR6	VPDADDR5	VPDADDR4	VPDADDR3	VPDADDR2	VPDADDR1	VPDADDR0
4Bh		RW	Flag	VPDADDR14	VPDADDR13	VPDADDR12	VPDADDR11	VPDADDR10	VPDADDR9	VPDADDR8
4Ch	VPD Data	RW	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
4Dh		RW	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
4Eh		RW	Data23	Data22	Data21	Data20	Data19	Data18	Data17	Data16
4Fh		RW	Data31	Data30	Data29	Data28	Data27	Data26	Data25	Data24
50h	MSIID	R	0	0	0	0	0	1	0	1
51h	NextPtr	R	0	1	1	0	0	0	0	0
52h	Message Control	R	64-bit Address Capable	Multiple Message Enable			0	0	1	MSI Enable
		W	-	Multiple Message Enable			-	-	1	MSI Enable
53h		Reserved. Always return 0								
54h-57h	Message Address Low	RW	64-bit Interrupt Message Address Low							
58h-5Bh	Message Address High	RW	64-bit Interrupt Message Address High							
5Ch-5Dh	Message Data	RW	16-bit Message Data							
5E-5Fh	RESERVED									
60h	PCIEID	R	0	0	0	1	0	0	0	0
61h	NextPtr	R	1	0	0	0	0	1	0	0
62h-63h	PCIE Cap.	R	0	0	0	Legacy	0	0	0	1
		R	0	0	0	0	0	0	0	0
64h-67h	Device Capability Register	R	L0s_acpt_latency[1]	L0s_acpt_latency[0]	Entend_tag_support	0	0	Max_payload_size_support		
		R	0	Pwr_ind_present	Attn_ind_present	Attn_button_present	L1s_acpt_latency[2]	L1s_acpt_latency[1]	L1s_acpt_latency[0]	L0s_acpt_latency[2]

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		R	0	0	0	0	0	0	0	0
		R	0	0	0	0	0	0	0	0
68h-69h	Device Control Register	RW	Max_payload_size			Relaxed_ ordering_ en	Unsupport _rqst_rpt_ en	Fatal_err_ rpt_en	Non_fatal _err_rpt_ en	Correct-able_err_ rpt_en
		RW	0	Max_read_request_size			No_snoop _en	Auxpwr_ PM_en	0	Entend_ tag_en
6Ah	Device Status Register	R	0	0	Transact_ ion_ pending	AuxPwr_ det	Upsupport _rqst_det	Fatal_err_ det	Non_fatal _err_det	Correct-able_err_ det
		W	0	0	-	-	Upsupport _rqst_det	Fatal_err_ det	Non_fatal _err_det	Correcta-ble_err_ det
6Bh		R	0	0	0	0	0	0	0	0
6Ch	Link Capability Register	R	0	0	0	1	0	0	0	1
6Dh		R	L1_exit_ lat[0]	L0s_exit_ lat[2]	L0s_exit_ lat[1]	L0s_exit_ lat[0]	ASPM_support		0	0
6Eh		R	0	0	0	0	0	0	L1_exit_ lat[2]	L1_exit_ lat[1]0
6Fh		R	0	0	0	0	0	0	0	0
70h	Link Control Register	R	Extended_ sync	Common_ clock	0	0	0	0	ASPM_control	
		W	Extended_ sync	Common_ clock	0	0	0	0	ASPM_control	
71h		R	0	0	0	0	0	0	0	0
72h	Link Status Register	R	0	0	0	1	0	0	0	1
73h		R	0	0	0	Slot_clock _cfg	0	0	0	0
74h-83h	Reserved									
84h	SpecificID	R	0	0	0	0	1	0	0	1
85h	NextPtr	R	0	0	0	0	0	0	0	0
86h	Byte_Len	R	0	1	0	0	1	1	0	0
87h	Version	R	0	0	0	0	0	0	0	1
88h	Receive Capability	R	0	0	0	0	0	0	0	1
89h		R	0	0	0	1	1	1	0	0
8Ah	Receive Control	R	0	0	0	0	0	0	0	0
8Bh		R	0	0	0	0	0	0	0	0
8Ch-8Eh	Error Mask register	RW	RX_Error_mask							
8Fh	ROM BAR Mask	R	0	0	ROM_BAR_MASK					
90h	BAR MASK Register	R	0	0	0	0	1	0	0	0
91h		R	0	0	1	0	0	0	0	0
92h		R	1	0	0	0	0	0	0	0
93h		R	0	0	0	0	0	0	0	0
94h	Allocated Posted	R	PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
95h		R	PH[3]	PH[2]	PH[1]	PH[0]	PD[11]	PD[10]	PD[9]	PD[8]

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
96h	Credit	R	0	0	0	0	PH[7]	PH[6]	PH[5]	PH[4]
97h		R	0	0	0	0	0	0	0	0
98h	Allocated Nonposted Credit	R	ND[7]	ND[6]	ND[5]	ND[4]	ND[3]	ND[2]	ND[1]	ND[0]
99h		R	NH[3]	NH[2]	NH[1]	NH[0]	ND[11]	ND[10]	ND[9]	ND[8]
9Ah		R	0	0	0	0	NH[7]	NH[6]	NH[5]	NH[4]
9Bh		R	0	0	0	0	0	0	0	0
9Ch		R	CPLD[7]	CPLD[6]	CPLD[5]	CPLD[4]	CPLD[3]	CPLD[2]	CPLD[1]	CPLD[0]
9Dh		R	0	0	0	0	CPLD[11]	CPLD[10]	CPLD[9]	CPLD[8]
9Eh		R	0	0	0	0	0	0	0	0
9Fh		R	0	0	0	0	0	0	0	0
A0h-A1h	Transmit Capability	R	0	0	0	0	0	0	1	0
		R	0	0	1	0	1	0	0	0
A2h-A3h	Transmit Control	R	1	1	1	1	1	1	1	1
		R	0	0	0	0	0	0	0	1
A4h	Transmit First Error Report	R	Tag[7]	Tag[6]	Tag[5]	Tag[4]	Tag[3]	Tag[2]	Tag[1]	Tag[0]
A5h		R	0	0	Class[2]	Class[1]	Class[0]	Tag[10]	Tag[9]	Tag[8]
A6h		R	0	0	0	0	0	0	0	0
A7h		R	Txer_flag	Txer[4]	Txer[3]	Txer[2]	Txer[1]	Txer[0]	0	0
		W	Txer_flag	Txer[4]	Txer[3]	Txer[2]	Txer[1]	Txer[0]	0	0
A8h-A9h	Transmit Buffer Top	R	TX_buffer_address							
AAh-ABh	Reserved									
ACh	Aux Capability	R	0	0	0	0	0	0	1	1
ADh		R	0	0	0	0	0	0	0	0
AEh	Aux Control	R	0	0	0	0	0	0	1	1
AFh		R	0	0	0	0	0	0	0	0
B0h	Link Timer	RW	Replay[7]	Replay[6]	Replay[5]	Replay[4]	Replay[3]	Replay[2]	Replay[1]	Replay[0]
B1h		RW	Ack_Nack [5]	Ack_Nack [4]	Ack_Nack [3]	Ack_Nack [2]	Ack_Nack [1]	Ack_Nack [0]	Repaly[9]	Replay[8]
B2h		RW	Flow_ctrl [3]	Flow_ctrl [2]	Flow_ctrl [1]	Flow_ctrl [0]	Ack_Nack [9]	Ack_Nack [8]	Ack_Nack [7]	Ack_Nack [6]
B3h		RW	Receive_ flow_ctrl[1]	Receive_ flow_ctrl[0]	Flow_ctrl [9]	Flow_ctrl [8]	Flow_ctrl [7]	Flow_ctrl [6]	Flow_ctrl [5]	Flow_ctrl [4]
B4h	PM Exit Control	R	Common_N_FTS							
B5h		R	0	0	Common_L1_exit			Common_L0s_exit		
B6h		R	Non_common_N_FTS							
B7h		R	0	0	Non_common_L1_exit			Non_common_L0s_exit		
B8h	Active PM Timer	RW	L1_idle_time_required							
B9h		RW	L0s_idle_time_required							
BAh		RW	0	0	0	0	0	0	L1_scale	L0s_scale
BBh		R	Attn_ind_state		Power_ind_state		0	0	0	0
BCh-BFh	Aux Header Log	R	Aux Header Log 1							
C0h-C3h		R	Aux Header Log 2							

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C4h-C7h		R	Aux Header Log 3							
C8h-CBh		R	Aux Header Log 4							
CCh	Aux Error Type/ Report	R	Error type Indicator							
CDh CFh		R	Reserved							
D0h-FFh	Reserved									
100h	Adv Error Report ID	R	0	0	0	0	0	0	0	1
101h		R	0	0	0	0	0	0	0	0
102h	Offset / Version	R	1	1	0	0	0	0	0	1
103h		R	0	0	0	1	0	0	1	0
104h	Uncorrect-able Error Status	RW	0	0	0	Data_Link _err_st	0	0	0	0
105h		RW	CPL_abort_ st	CPL_ timeout_st	FlowCtrl_ err_st	Poisoned_ TLP_st	0	0	0	0
106h		RW	0	0	0	Unsupport _rqst_st	0	Malform_ TLP_st	Rx_over-flow_st	Unexpect_ CPL_st
107h		R	0	0	0	0	0	0	0	0
108h	Uncorrect-able Error Mask	RW	0	0	0	Data_Link _err_msk	0	0	0	0
109h		RW	CPL_abort_ msk	CPL_time-out_msk	FlowCtrl_ err_msk	Poisoned_ TLP_msk	0	0	0	0
10A h		RW	0	0	0	Unsupport _rqst_msk	0	Malform_ TLP_msk	Rx_over-flow_msk	Unexpect_ CPL_msk
10Bh		R	0	0	0	0	0	0	0	0
10Ch	Uncorrect-able Error Severity	RW	0	0	0	Data_Link _err_sev	0	0	0	1
10D h		RW	CPL_abort_ sev	CPL_time-out _sev	FlowCtrl_ err_sev	Poisoned_ TLP_sev	0	0	0	0
10Eh		RW	0	0	0	Unsupport _rqst_sev	0	Malform_ TLP_sev	Rx_overfl ow_sev	Unexpect_ CPL_sev
10Fh		R	0	0	0	0	0	0	0	0
110h	Correct-able Error Status	RW	Bad_DLLP _st	Bad_TLP_ st	0	0	0	0	0	Receive_ err_st
111h		RW	0	0	0	Replay_ti meout_st	0	0	0	Replay_ro llover_st
112h -113 h		R	Reserved							
114h	Correct-able Error Mask	RW	Bad_DLLP _msk	Bad_TLP_ msk	0	0	0	0	0	Receive_ err_msk
115h		RW	0	0	0	Replay_ timeout_ msk	0	0	0	Replay_ rollover_ msk
116h -117 h		R	Reserved							
118h	Capability	R	0	0	0	First_error_pointer				

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
119h-11Bh	/ Control	Reserved								
11Ch-12Bh	Header Log	R	Header Log Register							
12Ch	VC ID	R	0	0	0	0	0	0	1	0
12Dh		R	0	0	0	0	0	0	0	0
12Eh	Offset / Version	R	1	0	0	0	0	0	0	1
12Fh		R	0	0	0	1	0	1	0	0
130h	Port VC capability Reg1	R	0	0	0	0	0	0	0	0
131h		R	0	0	0	0	0	0	0	0
132h-133h		R	Reserved							
134h-13FH	Reserved									
140h	VC Resource Control Reg0	RW	TC_VC [7]	TC_VC [6]	TC_VC [5]	TC_VC [4]	TC_VC [3]	TC_VC [2]	TC_VC [1]	1
141h		R	0	0	0	0	0	0	0	0
142h		R	0	0	0	0	0	0	0	0
143h		R	1	0	0	0	0	0	0	0
144h-145h	VC Resource Status Reg0	R	Reserved							
146h		R	0	0	0	0	0	0	Nego_ pending	0
147h		R	0	0	0	0	0	0	0	0
148h	Serial No ID	R	0	0	0	0	0	0	1	1
149h		R	0	0	0	0	0	0	0	0
14Ah-14Bh	Offset / Version	R	0	1	0	0	0	0	0	1
		R	0	0	0	1	0	1	0	1
14Ch-153h	Serial number	R	Serial Number[63:0]							
154h	Power Budget ID	R	0	0	0	0	0	1	0	0
155h		R	0	0	0	0	0	0	0	0
156h-157h	Offset / Version	R	0	0	0	0	0	0	0	1
		R	0	0	0	0	0	0	0	0
158h	Data select	RW	Data Select							
159h-15Bh		Reserved								
15Ch	Data	R	Base power							
15Dh		R	Type[0]	PM_state		PM_substate			Data_scale	
15Eh		R	0	0	0	Power_rail			Type[2]	Type[1]

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
15Fh		R	0	0	0	0	0	0	0	0
160h	Capability	R	0	0	0	0	0	0	0	System_ allocated
161h -163 h		Reserved								
164h -FFF h	Reserved									

5.3. PCI Configuration Space Functions

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of the RTL8111B/RTL8168B's configuration space are described below.

VID: Vendor ID. This field will be set to a value corresponding to PCI Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh which is Realtek Semiconductor's PCI Vendor ID.

DID: Device ID. This field will be set to a value corresponding to PCI Device ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

Command: The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Table 39. Command Register in PCI Configuration Space

Bit	Symbol	Description
15-11	-	Reserved
10	IntDisable	Interrupt Disable: This Bit enables/disables the RTL8111B/RTL8168B to assert Int# signal. 1: Force RTL8111B/RTL8168B not to assert Int# signal. 0: Enable RTL8111B/RTL8168B to assert Int# signal. It's also the default value after PCI reset.
9	FBTBEN	Fast Back-To-Back Enable: Does not apply to PCI Express. Must be hardwired to 0.
8	SERREN	System Error Enable: This bit, when set, enables reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI-Express specific bits in the Device Control register.
7	ADSTEP	Address/Data Stepping: Does not apply to PCI Express. Must be hardwired to 0.
6	PERRSP	Parity Error Response: In the Status register, the Master Data Parity Error bit is set by a Requester if its Parity Error Response bit is set and either of the following two conditions occurs: - If the Requester receives a poisoned Completion. - If the Requester poisons a write request. If the Parity Error Response bit is cleared, the Master Data Parity Error status bit is never set.
5	VGASNOOP	VGA palette SNOOP: Does not apply to PCI Express. Must be hardwired to 0.

Bit	Symbol	Description
4	MWIEN	Memory Write and Invalidate cycle Enable: Does not apply to PCI Express. Must be hardwired to 0.
3	SCYCEN	Special Cycle Enable: Does not apply to PCI Express. Must be hardwired to 0.
2	BMEN	Bus Master Enable: When set to 1, the RTL8111B/RTL8168B is capable of acting as a PCI bus master. When set to 0, it is prohibited from acting as a bus master. For normal operations, this bit must be set by the system BIOS.
1	MEMEN	Memory Space Access: When set to 1, the RTL8111B/RTL8168B responds to memory space accesses. When set to 0, the RTL8111B/RTL8168B ignores memory space accesses.
0	IOEN	I/O Space Access: When set to 1, the RTL8111B/RTL8168B responds to IO space accesses. When set to 0, the RTL8111B/RTL8168B ignores I/O space accesses.

Status: The status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Table 40. Status Register in PCI Config Space

Bit	Symbol	Description
15	DPERR	Detected Parity Error: This bit is set by the RTL8111B/RTL8168B whenever it receives a Poisoned TLP, regardless of the state the Parity Error Enable bit. Default value of this field is 0.
14	SSERR	Signaled System Error: This bit is set when the RTL8111B/RTL8168B sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. Default value of this field is 0.
13	RMABT	Received Master Abort: This bit is set when the RTL8111B/RTL8168B receives a Completion with Unsupported Request Completion Status. Default value of this field is 0.
12	RTABT	Received Target Abort: This bit is set when the RTL8111B/RTL8168B receives a Completion with Completer Abort Completion Status. Default value of this field is 0.
11	STABT	Signaled Target Abort: This bit is set when the RTL8111B/RTL8168B completes a Request using Completer Abort Completion Status. Default value of this field is 0.
10-9	DST1-0	Device Select Timing: Does not apply to PCI Express. Must be hardwired to 0.
8	DPD	Data Parity error Detected: This bit is set by the RTL8111B/RTL8168B if its Parity Error Enable bit is set and either of the following two conditions occurs: - Requestor receives a Completion marked poisoned - Requestor poisons a write Request If the Parity Error Enable bit is cleared, this bit is never set. Default value of this field is 0.
7	FBBC	Fast Back-To-Back Capable: Does not apply to PCI Express. Must be hardwired to 0.
6	-	Reserved.
5	66MHz	66MHz Capable: Does not apply to PCI Express. Must be hardwired to 0.
4	CapList	Capability List: Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.

Bit	Symbol	Description
3	IntSt	Interrupt Status: This bit reflects the interrupt status of RTL8111B/RTL8168B. Unlike ISR bits, this bit is a read-only bit and can't be reset by writing a 1 to this bit. The only way to reset this bit is to reset ISR register. The setting of the 'Interrupt Disable' bit in Command Register has no effect on the state of the 'Interrupt Status' bit. Only when the 'Interrupt Disable' bit is a 0 and the 'Interrupt Status' bit is a 1, will the RTL8111B/RTL8168B's Int# signal be asserted.
0	-	Reserved

RID: Revision ID Register

The Revision ID register is an 8-bit register that specifies the RTL8111B/RTL8168B controller revision number.

PIFR: Programming Interface Register

The programming interface register is an 8-bit register that identifies the programming interface of the RTL8111B/RTL8168B controller. The PCI specification reversion 2.1 doesn't define any other specific value for network devices. So PIFR = 00h.

SCR: Sub-Class Register

The Sub-class register is an 8-bit register that identifies the function of the RTL8111B/RTL8168B. SCR=00h indicates that the RTL8111B/RTL8168B is an Ethernet controller.

BCR: Base-Class Register

The Base-class register is an 8-bit register that broadly classifies the function of the RTL8111B/RTL8168B. BCR = 02h indicates that the RTL8111B/RTL8168B is a network controller.

CLS: Cache Line Size

This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

LTR: Latency Timer Register

This register is also referred to as primary latency timer for Type 1 Configuration Space header devices. The primary/master latency timer does not apply to PCI Express. This register must be hardwired to 0.

HTR: Header Type Register

Reads will return a 0, writes are ignored.

BIST: Built-in Self Test

Reads will return a 0, writes are ignored.

IOAR: This register specifies the BASE IO address which is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into IO space.

Table 41. IOAR Register in PCI Config Space

Bit	Symbol	Description
31-8	IOAR31-8	BASE IO Address: This is set by software to the Base IO address for the operational register map.
7-2	IOSIZE	Size Indication: Read back as 0. This allows the PCI bridge to determine that the RTL8111B/RTL8168B requires 256 bytes of IO space.
1	-	Reserved
0	IOIN	IO Space Indicator: Read only. Set to 1 by the RTL8111B/RTL8168B to indicate that it is capable of being mapped into IO space.

MEMAR: This register specifies the base memory address for memory accesses to the RTL8111B/RTL8168B operational registers. This register must be initialized prior to accessing any RTL8111B/RTL8168B's register with memory access.

Table 42. MEMAR Register in PCI Config Space

Bit	Symbol	Description
31-7	MEMAR	Base Memory Address: This is set by software to the base address for the operational register map.
6-4	-	Reserved
3	MEMPF	Memory Prefetchable: Read only. Set to 0 by the RTL8111B/RTL8168B.
2-1	MEMLOC	Memory Location Select: Read only. Set to 10b by the RTL8111B/RTL8168B. This indicates that the base register is 64-bits wide and can be located anywhere in 2^{64} memory space.
0	MEMIN	Memory Space Indicator: Read only. Set to 0 by the RTL8111B/RTL8168B to indicate that it is capable of being mapped into memory space.

CISPtr: CardBus CIS Pointer. This register does not apply to PCI Express. It must be read-only and must be hardwired to 0.

SVID: Subsystem Vendor ID. This field will be set to a value corresponding to PCI Subsystem Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh which is Realtek Semiconductor's PCI Subsystem Vendor ID.

SMID: Subsystem ID. This field will be set to value corresponding to the PCI Subsystem ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8129h.

BMAR: This register specifies the base memory address for memory accesses to the RTL8111B/RTL8168B operational registers. This register must be initialized prior to accessing any of the RTL8111B/RTL8168B's registers with memory access.

Table 43. BMAR Register in PCI Configuration Space

Bit	Symbol	Description
31-18	BMAR31-18	Boot ROM Base Address
17-11	ROMSIZE	Boot ROM Size: These bits indicate how many Boot ROM spaces are to be supported. The Relationship between Config 0 <BS2:0> and BMAR17-11 is as follows: BS2 BS1 BS0 Description 0 0 0 No Boot ROM 0 0 1 8K Boot ROM, BROMEN (RW), BMAR12-11: 0 (R), BMAR17-13 (RW) 0 1 0 16K Boot ROM, BROMEN (RW), BMAR13-11: 0 (R), BMAR17-14 (RW) 0 1 1 32K Boot ROM, BROMEN (RW), BMAR14-11: 0 (R), BMAR17-15 (RW) 1 0 0 64K Boot ROM, BROMEN (RW), BMAR15-11: 0 (R), BMAR17-16 (RW) 1 0 1 128K Boot ROM, BROMEN(RW), BMAR16-11=0 (R), BMAR17 (RW) 1 1 0 unused 1 1 1 unused
10-1	-	Reserved (read back 0)
0	BROMEN	Boot ROM Enable: This is used by the PCI BIOS to enable accesses to Boot ROM.

ILR: Interrupt Line Register. The Interrupt Line Register is an 8-bit register used to communicate with the routing of the interrupt. It is written by the POST software to set interrupt line for the RTL8111B/RTL8168B.

IPR: Interrupt Pin Register. The Interrupt Pin register is an 8-bit register indicating the interrupt pin used by the RTL8111B/RTL8168B. The RTL8111B/RTL8168B uses INTA interrupt pin. Read only. IPR = 01h.

MNGNT: Minimum Grant Timer: Read only. This register does not apply to PCI Express. It must be read-only and must be hardwired to 0.

MXLAT: Maximum Latency Timer. This register does not apply to PCI Express. It must be read-only and must be hardwired to 0.

5.4. Default Values After EEPROM Autoload

Table 44. Default Values After EEPROM Autoload

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01h		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02h	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03h		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04h	Command	R	0	0	0	0	0	0	0	0
05h		R	0	0	0	0	0	0	0	0
06h	Status	R	0	0	0	1	0	0	0	0
07h		R	0	0	0	0	0	0	0	0
08h	Revision ID	R	0	0	0	0	0	0	0	1
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R	0	0	0	0	0	0	0	0
0Dh	LTR	R	0	0	0	0	0	0	0	0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
11h		R	0	0	0	0	0	0	0	0
12h		R	0	0	0	0	0	0	0	0
13h		R	0	0	0	0	0	0	0	0
14h-17h	Reserved									
18h	MEM 64 BAR	R	0	0	0	0	MEM64	0	0	0
19h		R	0	0	0	0	0	0	0	0
1Ah		R	0	0	0	0	0	0	0	0
1Bh		R	0	0	0	0	0	0	0	0
1Ch		R	0	0	0	0	0	0	0	0
1Dh		R	0	0	0	0	0	0	0	0
1Eh		R	0	0	0	0	0	0	0	0
1Fh		R	0	0	0	0	0	0	0	0
20h-27h	RESERVED									
28h-2Bh	CISPtr	32'h0000_0000								
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
31h		R	0	0	0	0	0	0	0	0
32h		R	0	0	0	0	0	0	0	0
33h		R	0	0	0	0	0	0	0	0
34h	Cap_Ptr	R	0	1	0	0	0	0	0	0
35h-3Bh	RESERVED									
3Ch	ILR	R	0	0	0	0	0	0	0	0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	0	0	0	0	0	0
3Fh	MXLAT	R	0	0	0	0	0	0	0	0
40h	PMID	R	0	0	0	0	0	0	0	1
41h	NextPtr	R	0	1	0	0	1	0	0	0
42h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43h		R	PME_ $D3_{cold}$	PME_ $D3_{hot}$	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
44h	PMCSR	R	0	0	0	0	0	0	2'h0	
45h		R	0	0	0	0	0	0	0	0
46-47h	Reserved									
48h	VPDID	R	0	0	0	0	0	0	1	1
49h	NextPtr	R	0	1	0	1	0	0	0	0
4Ah	Flag VPD Address	R	0	0	0	0	0	0	0	0
4Bh		R	0	0	0	0	0	0	0	0
4Ch	VPD Data	R	0	0	0	0	0	0	0	0
4Dh		R	0	0	0	0	0	0	0	0
4Eh		R	0	0	0	0	0	0	0	0
4Fh		R	0	0	0	0	0	0	0	0
50h	MSIID	R	0	0	0	0	0	1	0	1
51h	NextPtr	R	0	1	1	0	0	0	0	0
52h	Message Control	R	1	3'h0			0	0	1	0
53h		Reserved. Always return 0								
54h-57h	Message Address Low	R	32'h0							
58h-5Bh	Message Address High	R	32'h0							
5Ch-5Dh	Message Data	R	16'0							
5E-5Fh	RESERVED									
60h	PCIEID	R	0	0	0	1	0	0	0	0
61h	NextPtr	R	1	0	0	0	0	1	0	0
62h-63h	PCIE Cap.	R	0	0	0	Legacy	0	0	0	1
		R	0	0	0	0	0	0	0	0
64h-67h	Device Capability Register	R	L0s_acpt_ latency[1]	L0s_acpt_ latency[0]	Entend_ tag_ support	0	0	Max_payload_size_support		
		R	0	Pwr_ind_ present	Attn_ind _present	Attn_ button_ present	L1s_ acpt_ latency [2]	L1s_ acpt_ latency [1]	L1s_ acpt_ latency [0]	L0s_ acpt_ latency [2]
		R	0	0	0	0	0	0	0	0
		R	0	0	0	0	0	0	0	0
68h-69h	Device Control Register	R	3'h0			1	0	0	0	0
		R	0	3'h2			1	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Ah	Device Status Register	R	0	0		AuxPwr_det	0	0	0	0
6Bh		R	0	0	0	0	0	0	0	0
6Ch	Link Capability Register	R	0	0	0	1	0	0	0	1
6Dh		R	L1_exit_lat[0]	L0s_exit_lat[2]	L0s_exit_lat[1]	L0s_exit_lat[0]	ASPM_support		0	0
6Eh		R	0	0	0	0	0	0	L1_exit_lat[2]	L1_exit_lat[1]0
6Fh		R	0	0	0	0	0	0	0	0
70h	Link Control Register	R	Extended_sync	Common_clock	0	0	0	0	ASPM_control	
71h		R	0	0	0	0	0	0	0	0
72h	Link Status Register	R	0	0	0	1	0	0	0	1
73h		R	0	0	0	Slot_clock_cfg	0	0	0	0
74h-83h	Reserved									
84h	SpecificID	R	0	0	0	0	1	0	0	1
85h	NextPtr	R	0	0	0	0	0	0	0	0
86h	Byte_Len	R	0	1	0	0	1	1	0	0
87h	Version	R	0	0	0	0	0	0	0	1
88h	Receive Capability	R	0	0	0	0	0	0	0	1
89h		R	0	0	0	1	1	1	0	0
8Ah	Receive Control	R	0	0	0	0	0	0	0	0
8Bh		R	0	0	0	0	0	0	0	0
8Ch-8Eh	Error Mask Register	R	24'hFF_FFFB							
8Fh	ROM BAR Mask	R	0	0	8'hE					
90h	BAR MASK Register	R	0	0	0	0	1	0	0	0
91h		R	0	0	1	0	0	0	0	0
92h		R	1	0	0	0	0	0	0	0
93h		R	0	0	0	0	0	0	0	0
94h	Allocated Posted Credit	R	PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
95h		R	PH[3]	PH[2]	PH[1]	PH[0]	PD[11]	PD[10]	PD[9]	PD[8]
96h		R	0	0	0	0	PH[7]	PH[6]	PH[5]	PH[4]
97h		R	0	0	0	0	0	0	0	0
98h	Allocated Non-posted Credit	R	ND[7]	ND[6]	ND[5]	ND[4]	ND[3]	ND[2]	ND[1]	ND[0]
99h		R	NH[3]	NH[2]	NH[1]	NH[0]	ND[11]	ND[10]	ND[9]	ND[8]
9Ah		R	0	0	0	0	NH[7]	NH[6]	NH[5]	NH[4]
9Bh		R	0	0	0	0	0	0	0	0
9Ch		R	CPLD [7]	CPLD [6]	CPLD [5]	CPLD [4]	CPLD [3]	CPLD [2]	CPLD [1]	CPLD [0]

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Dh		R	0	0	0	0	CPLD [11]	CPLD [10]	CPLD [9]	CPLD[8]
9Eh		R	0	0	0	0	0	0	0	0
9Fh		R	0	0	0	0	0	0	0	0
A0h -A1h	Transmit Capability	R	0	0	0	0	0	0	1	0
		R	0	0	1	0	1	0	0	0
A2h -A3h	Transmit Control	R	1	1	1	1	1	1	1	1
		R	0	0	0	0	0	0	0	1
A4h	Transmit First Error Report	R	0	0	0	0	0	0	0	0
A5h		R	0	0	0	0	0	0	0	0
A6h		R	0	0	0	0	0	0	0	0
A7h		R	0	0	0	0	0	0	0	0
A8h -A9h	Transmit Buffer Top	R	16’h0800							
AAh -ABh	Reserved									
ACh	Aux Capability	R	0	0	0	0	0	0	1	1
ADh		R	0	0	0	0	0	0	0	0
AEh	Aux Control	R	0	0	0	0	0	0	1	1
AFh		R	0	0	0	0	0	0	0	0
B0h	Link Timer	R	0	0	0	0	0	0	0	0
B1h		R	0	0	0	0	0	0	0	0
B2h		R	0	0	0	0	0	0	0	0
B3h		R	0	0	0	0	0	0	0	0
B4h	PM Exit Control	R	Common_N_FTS							
B5h		R	0	0	Common_L1_exit			Common_L0s_exit		
B6h		R	Non_common_N_FTS							
B7h		R	0	0	Non_common_L1_exit			Non_common_L0s_exit		
B8h	Active PM Timer	RW	L1_idle_time_required							
B9h		RW	L0s_idle_time_required							
BAh		R	0	0	0	0	0	0	L1_scale	L0s_scale
BBh		R	2’h0		2’h0		0	0	0	0
BCh -BFh	Aux Header Log	R	32’h0							
C0h -C3h		R	32’h0							
C4h -C7h		R	32’h0							

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C8h -CBh		R	32'h0							
CCh	Aux Error Type/ Report	R	8'h0							
CDh CFh		R	Reserved							
D0h -FFh	Reserved									
100h	Adv Error Report ID	R	0	0	0	0	0	0	0	1
101h		R	0	0	0	0	0	0	0	0
102h	Offset / Version	R	1	1	0	0	0	0	0	1
103h		R	0	0	0	1	0	0	1	0
104h	Uncorrect -able Error Status	R	0	0	0	0	0	0	0	0
105h		R	0	0	0	0	0	0	0	0
106h		R	0	0	0	0	0	0	0	0
107h		R	0	0	0	0	0	0	0	0
108h	Uncorrect -able Error Mask	R	0	0	0	0	0	0	0	0
109h		R	0	0	0	0	0	0	0	0
10Ah		R	0	0	0	0	0	0	0	0
10Bh		R	0	0	0	0	0	0	0	0
10Ch	Uncorrect -able Error Severity	R	0	0	0	1	0	0	0	1
10Dh		R	0	0	1	0	0	0	0	0
10Eh		R	0	0	0	0	0	1	1	0
10Fh		R	0	0	0	0	0	0	0	0
110h	Correct- able Error Status	R	0	0	0	0	0	0	0	0
111h		R	0	0	0	0	0	0	0	0
112h-113h		R	Reserved							

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
114h	Correct-able Error Mask	R	0	0	0	0	0	0	0	0
115h		R	0	0	0	0	0	0	0	0
116h-117h		R	Reserved							
118h	Capability / Control	R	0	0	0	5'h0				
119h-11Bh		Reserved								
11Ch-12Bh	Header Log	R	All 0's							
12Ch	VC ID	R	0	0	0	0	0	0	1	0
12Dh		R	0	0	0	0	0	0	0	0
12Eh	Offset / Version	R	1	0	0	0	0	0	0	1
12Fh		R	0	0	0	1	0	1	0	0
130h	Port VC capability Reg1	R	0	0	0	0	0	0	0	0
131h		R	0	0	0	0	0	0	0	0
132h-133h		R	Reserved							
134h-13FH	Reserved									
140h	VC Resource Control Reg0	R	1	1	1	1	1	1	1	1
141h		R	0	0	0	0	0	0	0	0
142h		R	0	0	0	0	0	0	0	0
143h		R	1	0	0	0	0	0	0	0
144h-145h	VC Resource Status Reg0	R	Reserved							
146h		R	0	0	0	0	0	0	0	0
147h		R	0	0	0	0	0	0	0	0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
148h	Serial No ID	R	0	0	0	0	0	0	1	1
149h		R	0	0	0	0	0	0	0	0
14Ah-14Bh	Offset / Version	R	0	1	0	0	0	0	0	1
		R	0	0	0	1	0	1	0	1
14Ch-153h	Serial number	R	Serial Number[63:0]							
154h	Power Budget ID	R	0	0	0	0	0	1	0	0
155h		R	0	0	0	0	0	0	0	0
156h-157h	Offset / Version	R	0	0	0	0	0	0	0	1
		R	0	0	0	0	0	0	0	0
158h	Data select	RW	8'h0							
159h-15Bh		Reserved								
15Ch	Data	R	8'h0							
15Dh		R	0	2'h0		3'h0			2'h0	
15Eh		R	0	0	0	3'h0			0	0
15Fh		R	0	0	0	0	0	0	0	0
160h	Capability	R	0	0	0	0	0	0	0	0
161h-163h		Reserved								
164h-FFFh	Reserved									

5.5. Power Management Function

The RTL8111B/RTL8168B complies with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8111B/RTL8168B can monitor the network for a Wakeup Frame, a Magic Packet, or a Re-LinkOk, and notify the system via a PCI Express Power Management Event (PME) Message, Beacon, or LANWAKEB pin when such a packet or event occurs. Then the system can be restored to a normal state to process incoming jobs.

When the RTL8111B/RTL8168B is in power down mode (D1 ~ D3):

- The Rx state machine is stopped. The RTL8111B/RTL8168B monitors the network for wakeup events such as a Magic Packet, Wakeup Frame, and/or Re-LinkOk, in order to wake up the system. When in power down mode, the RTL8111B/RTL8168B will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx on-chip buffer.
- The on-chip buffer status and packets that have already been received into the Rx on-chip buffer before entering power down mode are held by the RTL8111B/RTL8168B.
- Transmission is stopped. PCI Express transactions are stopped. The Tx on-chip buffer is held.
- After being restored to D0 state, the RTL8111B/RTL8168B transmits data that was not moved into the Tx on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The D3cold_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power (bit15, PMC) = 1.

If EEPROM D3cold_support_PME bit (bit15, PMC) = 0, the above 4 bits are all 0 in binary.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C2 F7, then PCI PMC = C2 F7)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C2 F7, then PCI PMC = 02 76)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C2 F7 (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC (if EEPROM PMC = C2 77, then PCI PMC = C2 77)
- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C2 77, then PCI PMC = 02 76)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 02 76.

Link Wakeup occurs only when the following conditions are met:

- The LinkUp bit (CONFIG3#4) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the corresponding wake-up method (message, beacon, or LANWAKEB) can be asserted in the current power state.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8111B/RTL8168B, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8111B/RTL8168B adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the corresponding wake-up method (message, beacon, or LANWAKEB) can be asserted in the current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid (Fast) Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8111B/RTL8168B, e.g., a broadcast, multicast, or unicast address to the current RTL8111B/RTL8168B adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC[A] of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8111B/RTL8168B is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

  Note: 16-bit CRC: The RTL8111B/RTL8168B supports two normal wakeup frames (covering 64 mask bytes from offset 0 to 63 of any incoming network packet) and three long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The corresponding wake-up method (message, beacon, or LANWAKEB) is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8111B/RTL8168B may assert the corresponding wake-up method (message, beacon, or LANWAKEB) in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wakeup Frame has been received.
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8111B/RTL8168B to stop asserting the corresponding wake-up method

(message, beacon, or LANWAKEB) (if enabled).

When the device is in power down mode, e.g. D1-D3, the IO, MEM, and Boot ROM spaces are all disabled. After a PERSTB assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto loaded from EEPROM. The setting may be changed from the EEPROM, if required).

5.6. Vital Product Data (VPD)

Bit 31 of the Vital Product Data (VPD) capability structure in the RTL8111B/RTL8168B's PCI Configuration Space is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56 has completed or not.

Write VPD register: (write data to the 93C46/93C56)

Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8111B/RTL8168B, the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.

Read VPD register: (read data from the 93C46/93C56)

Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8111B/RTL8168B, the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

Note1: Refer to the PCI 2.2 Specifications for further information.

Note2: The VPD address must be a DWORD-aligned address as defined in the PCI 2.2 Specifications. VPD data is always consecutive 4-byte data starting from the VPD address specified.

Note3: Realtek reserves offset 40h to 7Fh in EEPROM, mainly for VPD data to be stored.

Note4: The VPD function of the RTL8111B/RTL8168B is designed to be able to access the full range of the 93C46/93C56 EEPROM.

5.7. Message Signaled Interrupt (MSI)

5.7.1. MSI Capability Structure in PCI Configuration Space

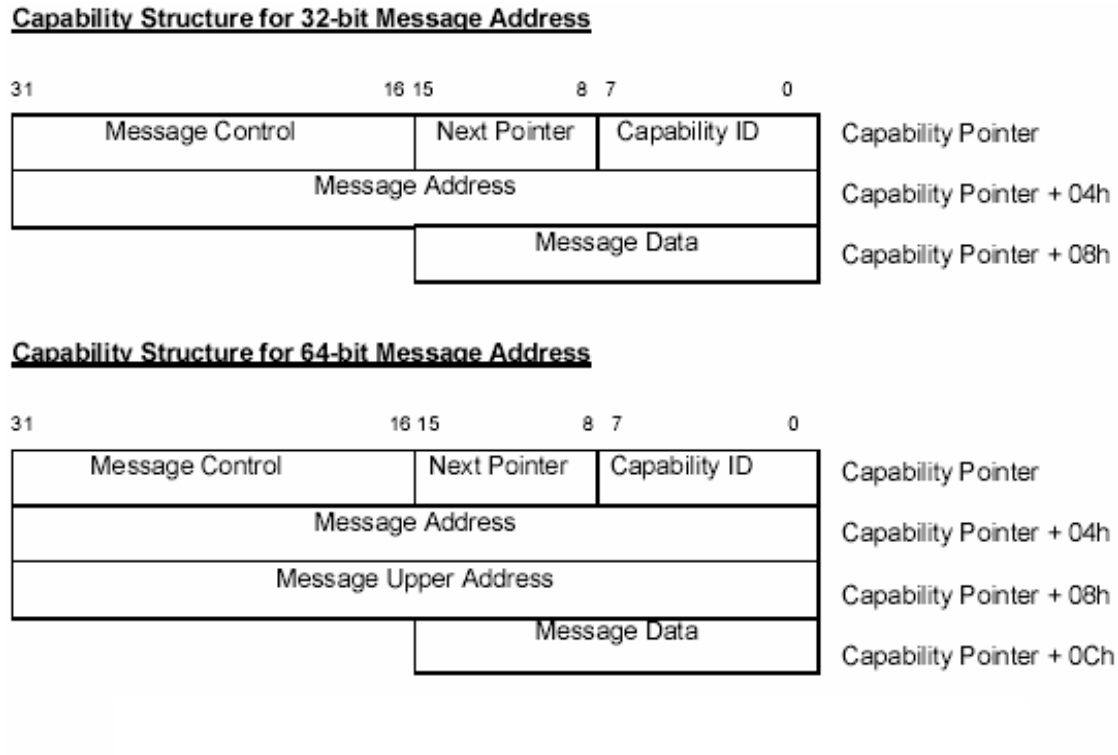

Figure 1. Message Signaled Interrupt (MSI)

5.7.2. RTL8111B/RTL8168B's MSI Function Requirement

MSI Capability ID: 05h, MSI registers start from 50h in the RTL8111B/RTL8168B's PCI configuration space.(PM Capability ID: 01h, PM registers start from 40h; VPD Capability ID: 03h, VPD registers start from 48h).

If the DAC function (64-bit addressing) is enabled, then its MSI function supports 64-bit addressing. The RTL8111B/RTL8168B's MSI capability structure turns to support 64-bit message address automatically when the DAC function is enabled.

5.7.3. Message Control

Table 45. Message Control

Bits	RW	Field	Description
15::8	RO	Reserved	Reserved. Always return 0
7	RO	64-bit address capable	1: DAC is enabled 0: No DAC The value of this bit is the same as the DAC bit (bit4 in C+CR register). The initial value of this bit comes from EEPROM auto-load to the DAC bit in the C+CR register.
6::4	RW	Multiple Message Enable	System software (e.g., BIOS, OS) indicates to the RTL8111B/RTL8168B the number of allocated messages/vectors (equal to or less than the number of requested messages/vectors). This field after PCI reset is '000'.
			Encoding / **Number of Messages/Vectors**
			000 / 1
			001 / 2
			010 / 4
			011 / 8
			100 / 16
			101 / 32
			110 / Reserved
			111 / Reserved
3::1	RO	Multiple Message Capable	Indication to system software (e.g., BIOS, OS) of the number of RTL8111B/RTL8168B requested vectors. The RTL8111B/RTL8168B supports 2 messages/vectors. Only one vector is used at a time, the other is used as a backup.
			Encoding / **Number of Messages/Vectors**
			001 / 2
			Others / Reserved
0	RW	MSI Enable	1: Enable MSI (Also the INTx pin is disabled automatically, MSI and INTx are mutually exclusive), this bit is set by system software. 0: Disable MSI (Default value after power-on or PCI reset)

5.7.4. Message Address

Table 46. Message Address

Bits	RW	Field	Description
31::02	RW	Message Address	System-specified message/vector address. Low DWORD aligned address for MSI memory write transaction. AD[1::0] are always '00' during the address phase.
01::00	RO	Reserved	Always return '00'.

5.7.5. Message Upper Address

Table 47. Message Upper Address

Bits	RW	Field	Description
31::00	RW	Message Upper Address	System-specified message/vector upper address. Upper 32 bits of a 64-bit message/vector address. This register is effective only when the DAC function is enabled, i.e., 64-bit addressing is enabled; bit7 in Message Control register is set. If the contents of this register are 0, the RTL8111B/RTL8168B only performs 32-bit addressing for the memory write of the messages/vectors.

5.7.6. Message Data

Table 48. Message Data

Bits	RW	Field	Description
15::00	RW	Message Data	If the Message Enable bit is set, the message/vector data is driven onto the lower word (AD[15::0]) of the memory write transaction's data phase. AD[31::16] are driven to zero during the memory write transaction's data phase. C/BE[3::0]# are asserted during the data phase of the memory write transaction.

6. Functional Description

6.1. Transmit & Receive Operations

The RTL8111B/RTL8168B supports a descriptor-based buffer management that significantly reduces host CPU utilization and is highly suitable for server applications. The new buffer management algorithm provides Microsoft Large-Send offload, IP checksum offload, TCP checksum offload, UDP checksum offload, and IEEE802.1P, 802.1Q VLAN tagging capabilities.

The RTL8111B/RTL8168B supports up to 1024 consecutive descriptors in memory (separated transmit and receive), which means there might be 3 descriptor rings, one high priority transmit descriptor ring, a normal priority transmit descriptor ring, and a receive descriptor ring. Each descriptor ring may consist of up to 1024 4-double-word consecutive descriptors. Each descriptor array consists of 4 consecutive double-word descriptors. The start address of each descriptor group should be 256-byte alignment. Software must pre-allocate enough buffers and configure all descriptor rings before transmitting and/or receiving packets. Descriptors can be chained to form a packet in both Tx and Rx.

Padding: The RTL8111B/RTL8168B will automatically pad any packets less than 64 bytes (including 4 bytes CRC) to 64-byte long (including 4-byte CRC) before transmitting that packet onto network medium. The padded data are all 0x00.

If a packet consists of 2 or more descriptors, then each of the descriptors in command mode should have the same configuration, except EOR, FS, LS bits.

6.1.1. Transmit

This portion implements the transmit portion of IEEE-802.3 Media Access Control. The Tx MAC retrieves packet data from the Tx Buffer Manager and sends it out through the transmit physical layer interface. Additionally, the Tx MAC provides MIB control information for transmit packets.

The Tx MAC has the capability to insert a 4-byte VLAN tag in the transmit packet. If Tx VLAN Tag insertion is enabled, the MAC will insert the 4 bytes, as specified in the VTAG register, following the source and destination addresses of the packet. The VLAN tag insertion can be enabled on a global or per-packet basis.

When operating in Gigabyte mode, the RTL8111B/RTL8168B operates in full duplex mode only.

The Tx MAC supports task offloading of IP, TCP, and UDP checksum generation. It is capable of calculating the checksums and inserting them into the packet. The checksum calculation can be enabled on a global or per-packet basis.

The following information describes the structure of the Tx descriptor, depending on different states in each Tx descriptor. The minimum Tx buffer should be at least of the size of 1 byte.

Large-Send Task Offload Tx Descriptor Format (before transmitting, OWN=1, LGSEN=1, Tx command mode 0)

Table 49. Large-Send Task Offload Tx Command Descriptor-1

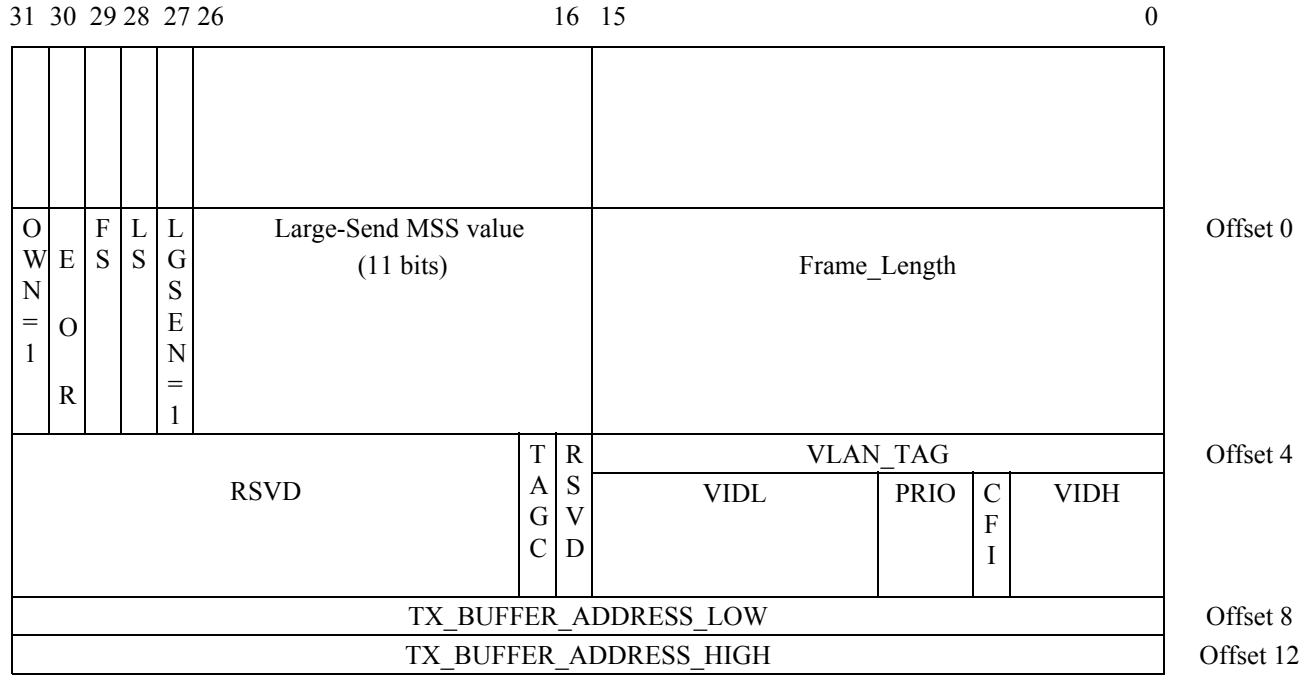

Table 50. Large-Send Task Offload Tx Command Descriptor-2

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership. When set, this bit indicates that the descriptor is owned by the NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1.
0	30	EOR	End of Descriptor Ring. This bit, when set, indicates that this is the last descriptor in descriptor ring. When the NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor.
0	29	FS	First Segment Descriptor. When set, this bit indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	Last Segment Descriptor. When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.
0	27	LGSEN	Large Send. A command bit; TCP/IP Large send operation enable. The driver sets this bit to ask the NIC to offload the Large send operation. In this case, LGSEN=1.

Offset#	Bit#	Symbol	Description
0	26-16	MSS	Maximum Segmentation Size. An 11-bit long command field, the driver passes Large-Send MSS to the NIC through this field.
0	15-0	Frame_Length	Transmit Frame Length. This field indicates the Tx frame length in the TX buffer, in bytes, to be transmitted. The maximum Large-Send frame length supported is 2^{16}-1(64KB-1).
4	31-18	RSVD	Reserved
4	17	TAGC	VLAN Tag Control Bit. 1: Enable. 0: Disable. 1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is a IEEE 802.1Q VLAN packet) is inserted after the source address, and 2 bytes are inserted after the tag protocol ID in the VLAN_TAG field of the transmit descriptor. 0: Packet remains unchanged when transmitting, i.e., the packet transmitted is the same as it was when passed down by the upper layer.
4	16	RSVD	Reserved
4	15-0	VLAN_TAG	The 2-byte VLAN_TAG contains information, from the upper layer, of user priority, canonical format indication, and VLAN ID. Please refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31-0	TxBuffL	Low 32-bit address of transmit buffer
12	31-0	TxBuffH	High 32-bit address of transmit buffer

Normal (including IP, TCP, UDP Checksum Task Offloads) Tx Descriptor Format (before transmitting, OWN=1, LGSEN=0, Tx command mode 1).

Table 51. Normal Tx Command Descriptor-1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 … 0	
OWN=1	EOR	FS	LS	LGSEN=0	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	IPCS	UDPCS	TCPCS	Frame_Length	Offset 0
RSVD														TAGC	RSVD	VLAN_TAG: VIDL / PRIO / CFI / VIDH	Offset 4
TX_BUFFER_ADDRESS_LOW																	Offset 8
TX_BUFFER_ADDRESS_HIGH																	Offset 12

Table 52. Normal Tx Command Descriptor-2

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership. When set, this bit indicates that the descriptor is owned by the NIC, and the data relative to this descriptor is ready to be transmitted. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the relative buffer data is transmitted. In this case, OWN=1.
0	30	EOR	End of Descriptor Ring. This bit, when set, indicates that this is the last descriptor in the descriptor ring. When the NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data relative to this descriptor.
0	29	FS	First Segment Descriptor. When set, this bit indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	Last Segment Descriptor. When set, indicates that this is the last descriptor of a Tx packet, and this descriptor is pointing to the last segment of the packet.
0	27	LGSEN	Large Send. A command bit; TCP/IP Large send operation enable. The driver sets this bit to ask the NIC to offload the Large send operation. In this case, LGSEN=1.
0	26-19	RSVD	Reserved
0	18	IPCS	IP Checksum Offload. A command bit. The driver sets this bit to ask the NIC to offload the IP checksum.

Offset#	Bit#	Symbol	Description
0	17	UDPCS	UDP Checksum Offload. A command bit. The driver sets this bit to ask the NIC to offload the UDP checksum.
0	16	TCPCS	TCP Checksum Offload Enable: A command bit. The driver sets this bit to ask the NIC to offload the TCP checksum.
0	15-0	Frame_Length	Transmit Frame Length: This field indicates the length of the TX buffer, in bytes, to be transmitted
4	31-18	RSVD	Reserved
4	17	TAGC	VLAN Tag Control Bit. 1: Enable. 0: Disable. 1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is a IEEE 802.1Q VLAN packet) is inserted after the source address, and 2 bytes are inserted after the tag protocol ID in the VLAN_TAG field of the transmit descriptor. 0: Packet remains unchanged when transmitting. I.e., the packet transmitted is the same as it was when passed down by the upper layer.
4	16	RSVD	Reserved
4	15-0	VLAN_TAG	VLAN Tag. The 2-byte VLAN_TAG contains information from the upper layer, of user priority, canonical format indication, and VLAN ID. Refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31-0	TxBuffL	Low 32-bit address of transmit buffer
12	31-0	TxBuffH	High 32-bit address of transmit buffer

Tx Status Descriptor (after transmitting, OWN=0, Tx status mode)

After having transmitted, the Tx descriptor turns into a Tx status descriptor.

Table 53. Tx Status Descriptor-1

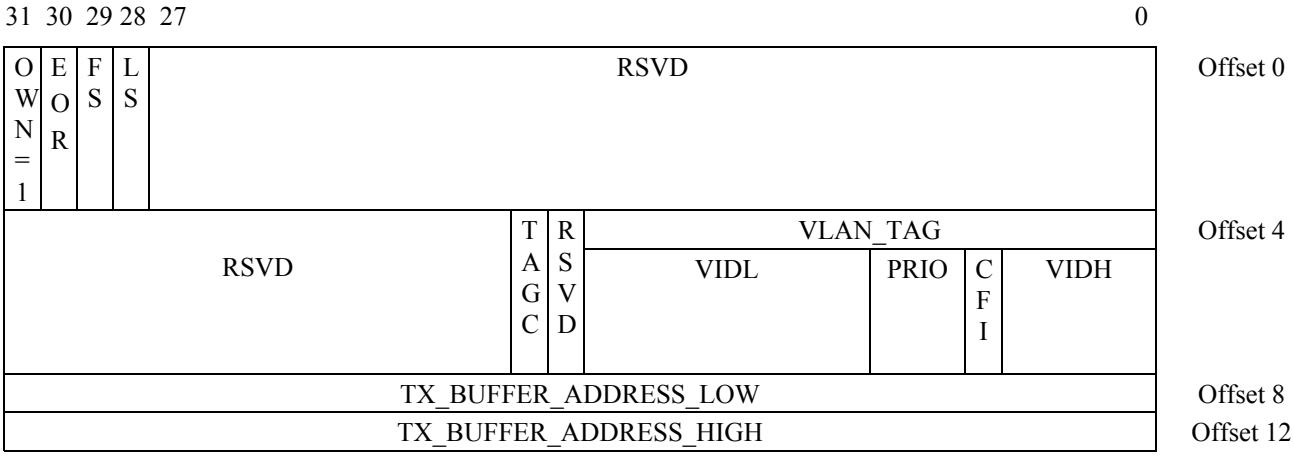

Table 54. Tx Status Descriptor-2

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership: When set, indicates that the descriptor is owned by the NIC. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the related buffer data has been transmitted. In this case, OWN=0.
0	30	EOR	End of Descriptor Ring: When set, indicates that this is the last descriptor in the descriptor ring. When the NIC's internal transmit pointer reaches here, the pointer will return to the first descriptor of the descriptor ring after transmitting the data related to this descriptor.
0	29	FS	First Segment Descriptor: This bit, when set, indicates that this is the first descriptor of a Tx packet, and that this descriptor is pointing to the first segment of the packet.
0	28	LS	Last Segment Descriptor: This bit, when set, indicates that this is the last descriptor of a Tx packet, and that this descriptor is pointing to the last segment of the packet.
0	27-0	RSVD	Reserved
4	31-18	RSVD	Reserved
4	17	TAGC	VLAN Tag Control Bit: 1: Enable. 0: Disable. 1: Add TAG. 0x8100 (Ethernet encoded tag protocol ID, indicating that this is an IEEE 802.1Q VLAN packet) is inserted after the source address, and 2 bytes are inserted after the tag protocol ID from VLAN_TAG field in transmit descriptor. 0: Packet remains unchanged when transmitting, i.e.,the packet transmitted is the same as it was passed down by the upper layer.
4	16	RSVD	Reserved

Offset#	Bit#	Symbol	Description
4	15-0	VLAN_TAG	VLAN Tag: The 2-byte VLAN_TAG contains information from the upper layer, of user priority, canonical format indicator, and VLAN ID. Refer to IEEE 802.1Q for more VLAN tag information. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31-0	TxBuffL	Low 32-bit address of transmit buffer
12	31-0	TxBuffH	High 32-bit address of transmit buffer

6.1.2. Receive

The receive portion implements the receive portion of IEEE-802.3 Media Access Control. The Rx MAC retrieves packet data from the receive portion and sends it to the Rx Buffer Manager. Additionally, the Rx MAC provides MIB control information and packet address data for the Rx Filter.

The Rx MAC can detect packets containing a 4-byte VLAN tag, and remove the VLAN tag from the received packet. If Rx VLAN Tag Removal is enabled, then the 4 bytes following the source and destination addresses will be stripped out. The VLAN status can be returned in the VLAN Tag field.

The Rx MAC supports IP checksum verification. It can validate IP checksums as well as TCP and UDP checksums. Packets can be discarded based on detecting checksum errors.

The following information describes what the Rx descriptor may look like, depending on different states in each Rx descriptor. Any Rx buffer pointed to by one of the Rx descriptors should be at least 8 bytes in length, and should be 8-byte alignment in memory. The length of each Rx buffer should be a multiple of 8 bytes.

Rx Command Descriptor (OWN=1)

The driver should pre-allocate Rx buffers and configure Rx descriptors before packet reception. Table 55 describes how Rx descriptors may look

before packet reception.

Table 55. Rx Command Descriptor-1

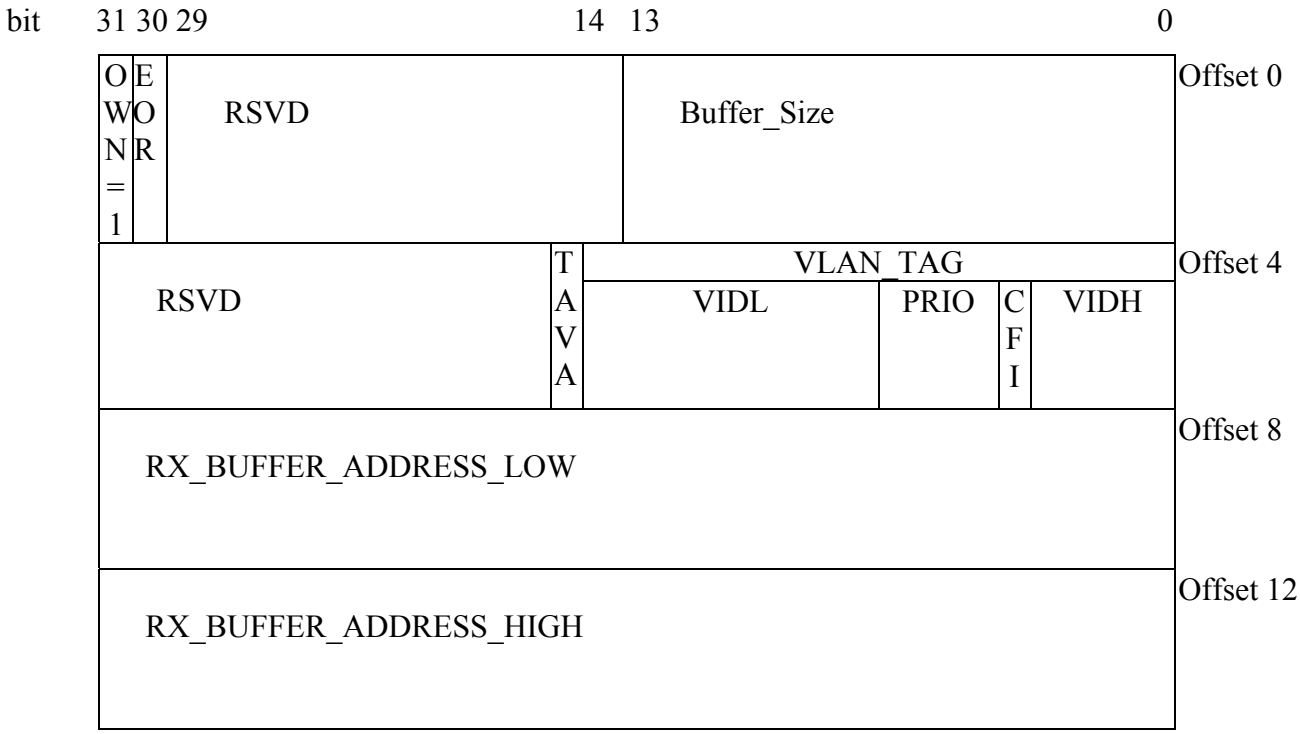

Table 56. Rx Command Descriptor-2

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership: When set, indicates that the descriptor is owned by the NIC, and is ready to receive a packet. The OWN bit is set by the driver after having pre-allocated the buffer at initialization, or the host has released the buffer to the driver. In this case, OWN=1.
0	30	EOR	End of Rx descriptor Ring: This bit, set to 1 indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29-14	RSVD	Reserved
0	13-0	Buffer_Size	Buffer Size: This field indicate the receive buffer size in bytes. The Rx buffer size should not exceed 2^{13}-1(8KB-1) and should be a multiple of 8, i.e., the maximum value of this field is 0x1FF8, and bit2-0 and bit13 should always be 0.
4	31-17	RSVD	Reserved
4	16	TAVA	Tag Available: This bit, when set, indicates that the received packet is an IEEE802.1Q VLAN TAG (0x8100) available packet.

Offset#	Bit#	Symbol	Description
4	15-0	VLAN_TAG	VLAN Tag: If the TAG of the packet is 0x8100, The RTL8111B/RTL8168B extracts four bytes from after the source ID, sets the TAVA bit to 1, and moves the TAG value of this field in the Rx descriptor. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31-0	RxBuffL	Low 32-bit Address of Receive Buffer. 8-byte alignment is required, i.e., the lowest 3 LSB bits should be 0.
12	31-0	RxBuffH	High 32-bit Address of Receive Buffer

Rx Status Descriptor (OWN=0)

When a packet is received, the Rx command descriptor becomes an Rx status descriptor.

Table 57. Rx Status Descriptor-1

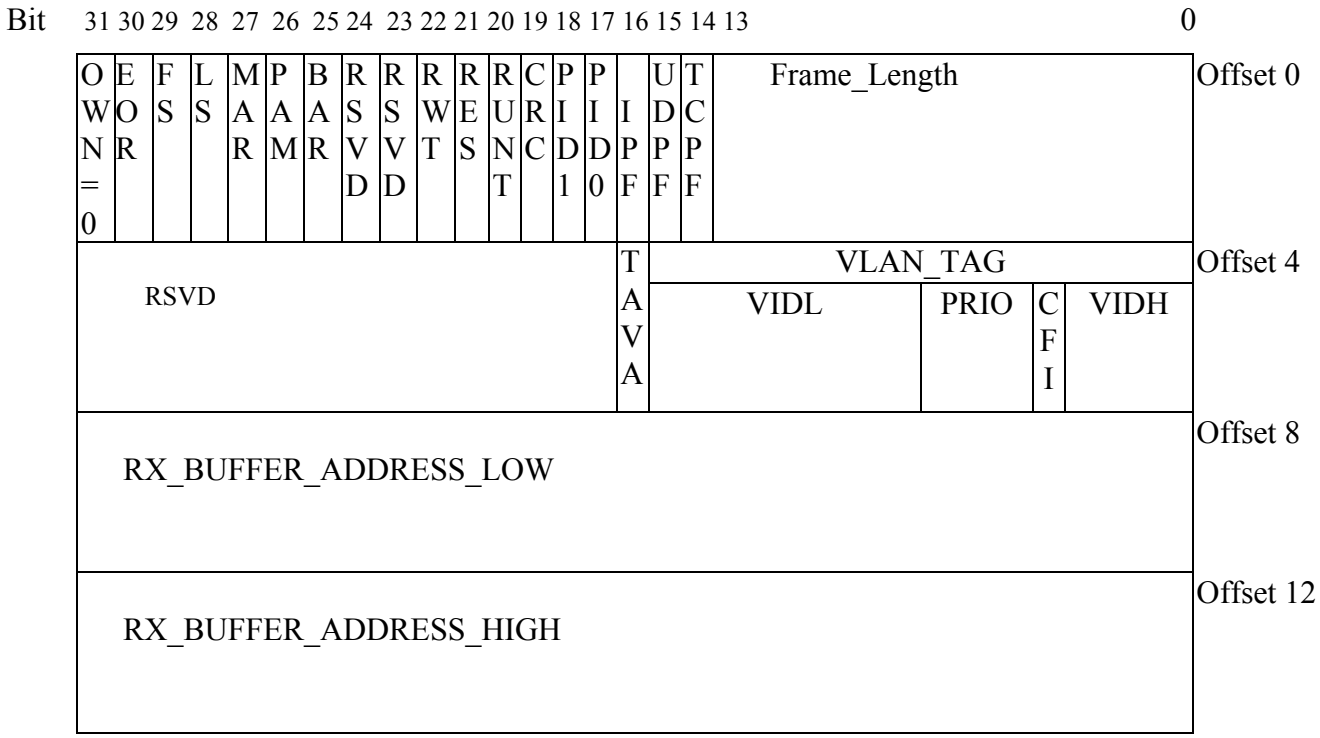

Table 58. Rx Status Descriptor-2

Offset#	Bit#	Symbol	Description
0	31	OWN	Ownership: This bit, when set, indicates that the descriptor is owned by the NIC. When cleared, it indicates that the descriptor is owned by the host system. The NIC clears this bit when the NIC has filled up this Rx buffer with a packet or part of a packet. In this case, OWN=0.

Offset#	Bit#	Symbol	Description
0	30	EOR	End of Rx Descriptor Ring: This bit, set to 1, indicates that this descriptor is the last descriptor of the Rx descriptor ring. Once the NIC's internal receive descriptor pointer reaches here, it will return to the first descriptor of the Rx descriptor ring after this descriptor is used by packet reception.
0	29	FS	First Segment descriptor: When set, indicates that this is the first descriptor of a received packet, and this descriptor is pointing to the first segment of the packet.
0	28	LS	Last Segment Descriptor: When set, indicates that this is the last descriptor of a received packet, and this descriptor is pointing to the last segment of the packet.
0	27	MAR	Multicast Address Packet Received: When set, indicates that a multicast packet has been received.
0	26	PAM	Physical Address Matched: When set, indicates that the destination address of this Rx packet matches the value in the RTL8111B/RTL8168B's ID registers.
0	25	BAR	Broadcast Address Received: When set, indicates that a broadcast packet has been received. BAR and MAR will not be set simultaneously.
0	24	RSVD	Reserved, always 0.
0	23	RSVD	Reserved, always 1.
0	22	RWT	Receive Watchdog Timer Expired: This bit is set whenever the received packet length exceeds 8192 bytes.
0	21	RES	Receive Error Summary: When set, indicates that at least one of the following errors has occurred: CRC, RUNT, RWT, FAE. This bit is valid only when LS (Last segment bit) is set
0	20	RUNT	Runt Packet: When set, indicates that the received packet length is smaller than 64 bytes. RUNT packets can only be received when RCR_AR is set.
0	19	CRC	CRC Error: When set, indicates that a CRC error has occurred on the received packet. A CRC packet can only be received when RCR_AER is set.
0	18, 17	PID1, PID0	Protocol ID1, Protocol ID0: These 2 bits indicate the protocol type of the packet received.
0	16	IPF	IP Checksum Failure: 1: Failure, 0: No failure.
0	15	UDPF	UDP Checksum Failure: 1: Failure, 0: No failure.
0	14	TCPF	TCP Checksum Failure: 1: Failure, 0: No failure.
0	13-0	Frame_Length	When OWN=0 and LS =1, these bits indicate the received packet length including CRC, in bytes.
4	31-17	RSVD	Reserved
4	16	TAVA	Tag Available: When set, the received packet is an IEEE-802.1Q VLAN TAG (0x8100) available packet.

	PID1	PID0
Non-IP	0	0
TCP/IP	0	1
UDP/IP	1	0
IP	1	1

Offset#	Bit#	Symbol	Description
4	15-0	VLAN_TAG	VLAN Tag: If the TAG of the packet is 0x8100, The RTL8111B/RTL8168B extracts four bytes from after the source ID, sets TAVA bit to 1, and moves the TAG value to this field in the Rx descriptor. VIDH: The high 4 bits of a 12-bit VLAN ID. VIDL: The low 8 bits of a 12-bit VLAN ID. PRIO: 3-bit 8-level priority. CFI: Canonical Format Indicator.
8	31-0	RxBuffL	Low 32-bit Address of Receive Buffer. 8-byte alignment is required.
12	31-0	RxBuffH	High 32-bit Address of Receive Buffer

6.2. Flow Control

The RTL8111B/RTL8168B supports IEEE 802.3X flow control, based on the results of N-Way, to improve performance in full-duplex mode. It detects and sends PAUSE packets to achieve the flow control task. Results from the N-Way process with the link partner determine if flow control is supported for the current connection.

6.2.1. Control Frame Transmission

When the RTL8111B/RTL8168B is running out of receive descriptors in full duplex mode, it sends a PAUSE packet (with pause_time=FFFFh) to inform the source station to stop transmission for the specified period of time. Once the receive descriptors are available again, the RTL8111B/RTL8168B sends another PAUSE packet (with pause_time=0000h) to wake up the source station to restart transmission.

6.2.2. Control Frame Reception

The RTL8111B/RTL8168B enters backoff state for the specified period of time when it receives a valid PAUSE packet (with pause_time=n) in full duplex mode. If the PAUSE packet is received while the RTL8111B/RTL8168B is transmitting, the RTL8111B/RTL8168B starts to backoff after the current transmission is completed. The RTL8111B/RTL8168B is free to transmit packets when it receives a valid PAUSE packet (with pause_time=0000h) or the backoff timer(=n*512 bit time) elapses.

The PAUSE operation cannot be used to inhibit transmission of MAC Control frames (e.g. a PAUSE packet). The N-way flow control capability can be disabled. Refer to Section 4, EEPROM (93C46/93C56) Contents, page 24 for further information.

6.3. LED Functions

The RTL8111B/RTL8168B supports 4 LED signals in 4 different configurable operation modes. The following sections describe the different LED actions.

6.3.1. Link Monitor

The Link Monitor senses the link integrity or if a station is down, e.g., LINK10, LINK100, LINK1000, LINK10/100/1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high indicating that no network connection exists.

6.3.2. Rx LED

In 10/100/1000Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.

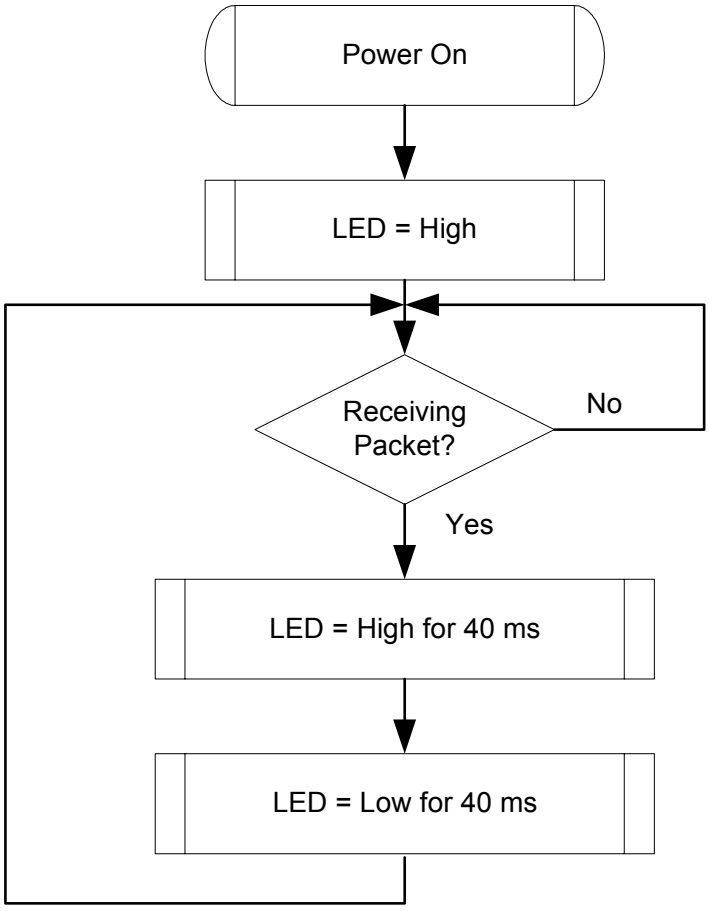

Figure 2. Rx LED

6.3.3. Tx LED

In 10/100/1000Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.

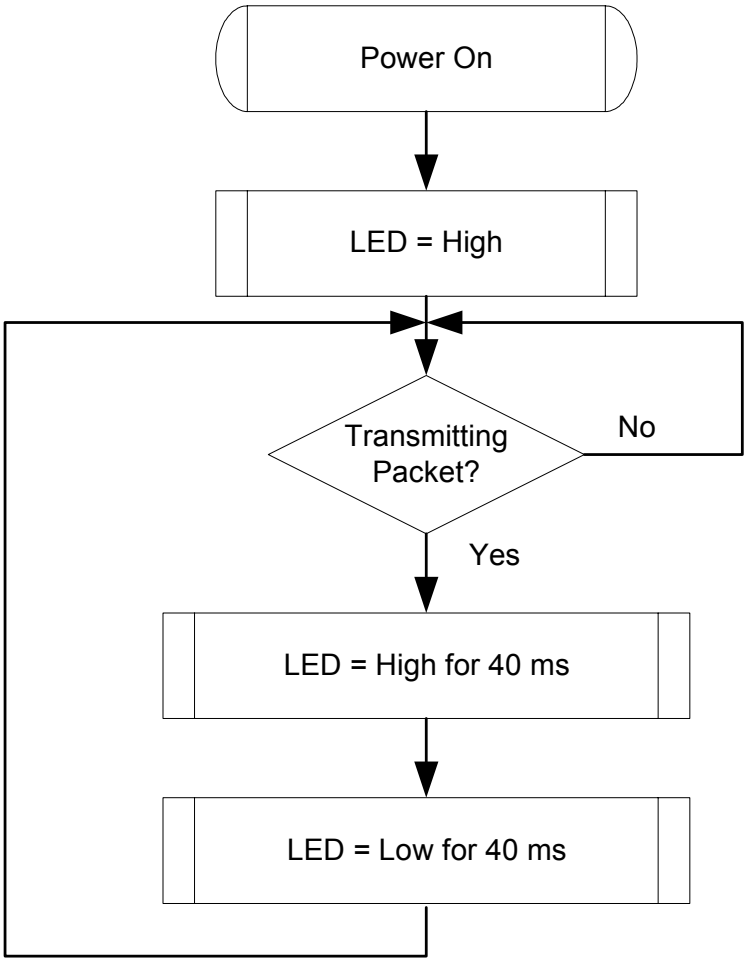

Figure 3. Tx LED

6.3.4. Tx/Rx LED

In 10/100/1000Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.

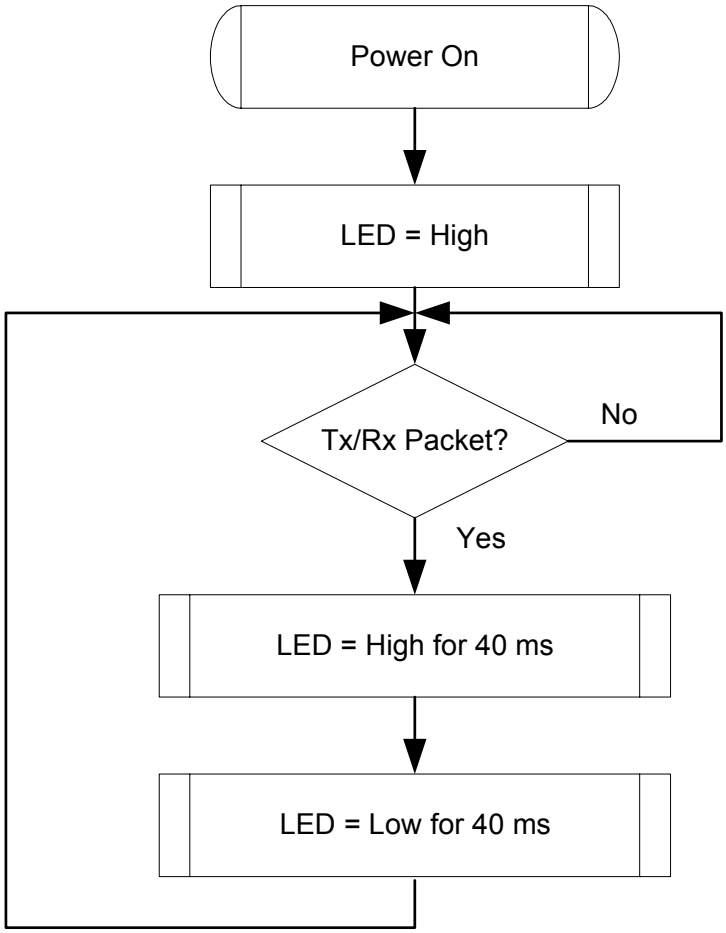

Figure 4. Tx/Rx LED

6.3.5. LINK/ACT LED

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8111B/RTL8168B is linked and operating properly. This LED high for extended periods indicates that a link problem exists.

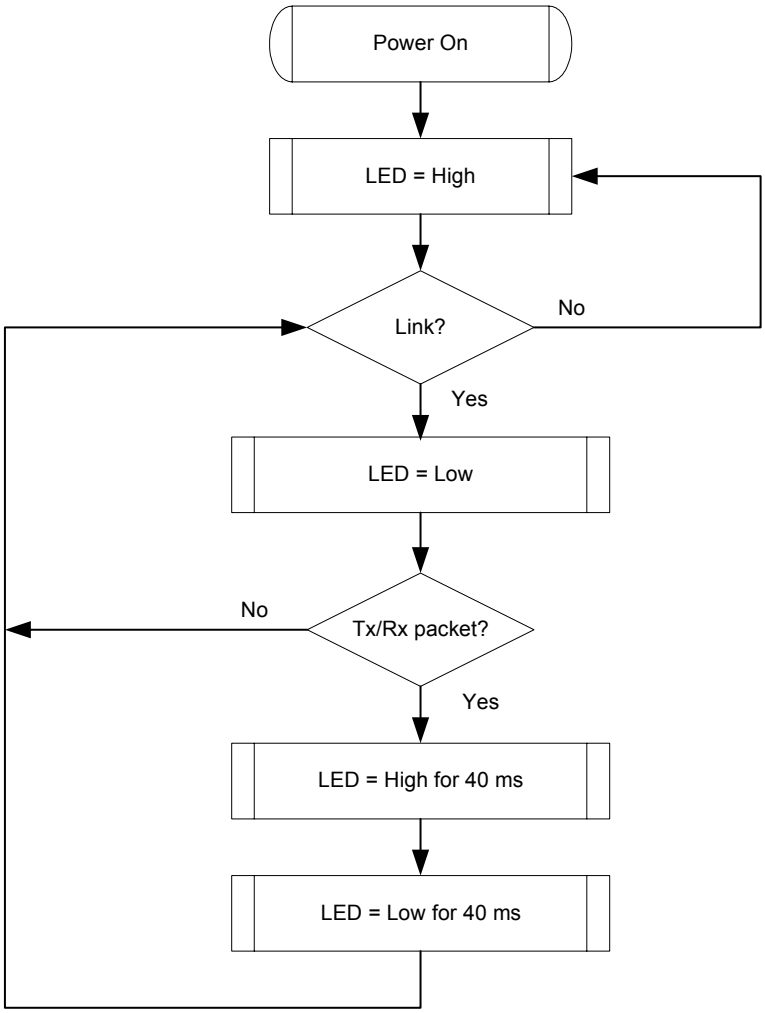

Figure 5. LINK/ACT LED

6.4. PHY Transceiver

6.4.1. PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8111B/RTL8168B operates at 10/100/1000Mbps over standard CAT.5 UTP cable (100/1000Mbps), and CAT.3 UTP cable (10Mbps).

GMII (1000Mbps) Mode

The RTL8111B/RTL8168B's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125Mhz NRZ and NRZI signals. After that, the NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.4.2. PHY Receiver

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive MII/GMII interface and sends it to the Rx Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.5. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set Reg4.15 to 1 to exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

6.6. EEPROM Interface

The RTL8111B/RTL8168B requires the attachment of an external EEPROM. The 93C46/93C56 is a 1K-bit/2K-bit EEPROM. The EEPROM interface permits the RTL8111B/RTL8168B to read from, and write data to, an external serial EEPROM device.

Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto load command. The RTL8111B/RTL8168B will auto-load values from the EEPROM. If the EEPROM is not present, the RTL8111B/RTL8168B initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using “bit-bang” accesses via the 9346CR Register, or using PCI VPD. The interface consists of EESK, EECS, EEDO, and EEDI.

Table 59. EEPROM Interface

EEPROM	Description
EECS	93C46 (93C56) chip select
EESK	EEPROM serial data clock
EEDI/Aux	Input data bus/Input pin to detect whether Aux. Power exists on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8111B/RTL8168B assumes that no Aux. Power exists.
EEDO	Output data bus

7. Driver Programming Note

A-1 MAC Registers Configuration Sequence

The '**C+ Command**' and '**Command'** registers are the key parameters before any other registers or descriptors are configured. The MAC registers must be configured as follows:

Step1. Configure C+ Command Register (Offset 00E0h-00E1h)
Step2. Configure Command Register (Offset 0037h)
Step3. Configure Other Registers

A-2 Multicast Registers Configuration

Multicast Registers Configuration (MAR) registers configuration is the same as that of the NE2000 driver.

A-3 Checksum Offload Tx Descriptor Note

To transmit an Ethernet packet, the upper layer might split this packet to several transmit buffers. Each transmit buffer corresponds to a Tx descriptor. If it transmits a packet with the **Checksum Task Offload**, it is necessary to set the related checksum offload bits of all Tx descriptors with this packet.

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